

SLPS205A - AUGUST 2009-REVISED MAY 2010

N-Channel NexFET™ Power MOSFETs

Check for Samples: CSD16410Q5A

FEATURES

- Ultra Low Qg and Qgd
- Low Thermal Resistance
- Avalanche Rated
- · Pb Free Terminal Plating
- RoHS Compliant
- Halogen Free
- SON 5mm x 6mm Plastic Package

UMENTS

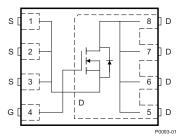
APPLICATIONS

- Point-of-Load Synchronous Buck Converter for Applications in Networking, Telecom and Computing Systems
- Optimized for Control FET Applications

DESCRIPTION

The NexFET™ power MOSFET has been designed to minimize losses in power conversion applications.





$R_{DS(ON)}$ vs V_{GS} 15 $R_{DS(on)}$ – On-State Resistance – $m\Omega$ $I_D = 17A$ 14 13 $T_C = 125^{\circ}C$ 12 11 10 9 8 7 6 T_C = 25°C 5 12 V_{GS} - Gate to Source Voltage - V G006

PRODUCT SUMMARY

V _{DS}	Drain to Source Voltage	25		V
Q_g	Gate Charge Total (4.5V)	3.9		nC
Q_{gd}	Gate Charge Gate to Drain	1.1		nC
R _{DS(on)}	Drain to Source On Resistance	$V_{GS} = 4.5V$	9.6	mΩ
		V _{GS} = 10V	6.8	mΩ
V _{GS(th)}	Threshold Voltage	1.9		V

ORDERING INFORMATION

Device	Package	Media	Qty	Ship
CSD16410Q5A	SON 5X6 Plastic Package	13-inch reel	2500	Tape and Reel

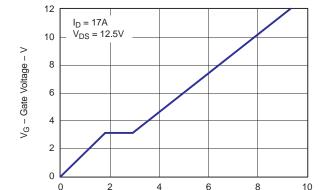
ABSOLUTE MAXIMUM RATINGS

T _A = 25°C unless otherwise stated		VALUE	UNIT
V_{DS}	Drain to Source Voltage	25	٧
V_{GS}	Gate to Source Voltage	+16 / -12	V
	Continuous Drain Current, T _C = 25°C	59	Α
I _D	Continuous Drain Current ⁽¹⁾	16	Α
I_{DM}	Pulsed Drain Current, T _A = 25°C ⁽²⁾	158	Α
P_D	Power Dissipation ⁽¹⁾	3	W
T_J , T_{STG}	Operating Junction and Storage Temperature Range	-55 to 150	°C
E _{AS}	Avalanche Energy, single pulse $I_D = 32 A, \ L = 0.1 mH, \ R_G = 25 \Omega$	51	mJ

(1) $R_{\theta,JA} = 42^{\circ}\text{C/W}$ on 1in^2 Cu (2 oz.) on 0.060" thick FR4 PCB.

Gate Charge

(2) Pulse width ≤300µs, duty cycle ≤2%



Q_q - Gate Charge - nC

G003

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These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

ELECTRICAL CHARACTERISTICS

 $(T_A = 25^{\circ}C \text{ unless otherwise stated})$

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT	
Static Ch	naracteristics	,					
BV _{DSS}	Drain to Source Voltage	$V_{GS} = 0V, I_D = 250\mu A$	25			V	
I _{DSS}	Drain to Source Leakage Current	V _{GS} = 0V, V _{DS} = 20V			1	μΑ	
I _{GSS}	Gate to Source Leakage Current	V _{DS} = 0V, V _{GS} = +16/-12V			100	nA	
V _{GS(th)}	Gate to Source Threshold Voltage	$V_{DS} = V_{GS}, I_D = 250 \mu A$	1.6	1.9	2.3	V	
D	Davis to Course On Bosistano	V _{GS} = 4.5V, I _D = 17A		9.6	12	mΩ	
R _{DS(on)}	Drain to Source On Resistance	V _{GS} = 10V, I _D = 17A		6.8	8.5	mΩ	
9 _{fs}	Transconductance	V _{DS} = 15V, I _D = 17A		38		S	
Dynamic	: Characteristics	•					
C _{ISS}	Input Capacitance			570	740	pF	
Coss	Output Capacitance	V _{GS} = 0V, V _{DS} = 12.5V, f = 1MHz		460	600	pF	
C _{RSS}	Reverse Transfer Capacitance			40	52	pF	
R _g	Series Gate Resistance			0.7	1.4	Ω	
Qg	Gate Charge Total (4.5V)			3.9	5	nC	
Q _{gd}	Gate Charge Gate to Drain	V 40.5V L 47A		1.1		nC	
Q _{gs}	Gate Charge Gate to Source	$V_{DS} = 12.5V, I_D = 17A$		1.8		nC	
Qg(th)	Gate Charge at Vth			1.1		nC	
Q _{OSS}	Output Charge	$V_{DS} = 13V, V_{GS} = 0V$		10		nC	
t _{d(on)}	Turn On Delay Time			6.2		ns	
t _r	Rise Time	$V_{DS} = 12.5V, V_{GS} = 4.5V, I_{D} = 17A$		10.7		ns	
t _{d(off)}	Turn Off Delay Time	$R_G = 2\Omega$		6.5		ns	
t _f	Fall Time			3.6		ns	
Diode Cl	haracteristics	,					
V _{SD}	Diode Forward Voltage	I _S = 17A, V _{GS} = 0V		0.85	1	V	
Q _{rr}	Reverse Recovery Charge	$V_{DD} = 13V$, $I_F = 17A$, $di/dt = 300A/\mu s$		14		nC	
t _{rr}	Reverse Recovery Time	$V_{DD} = 13V$, $I_F = 17A$, $di/dt = 300A/\mu s$		18.2		ns	

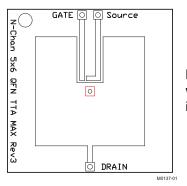
THERMAL CHARACTERISTICS

 $(T_A = 25^{\circ}C \text{ unless otherwise stated})$

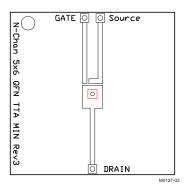
PARAMETER		MIN	TYP	MAX	UNIT
R $_{\theta JC}$	Thermal Resistance Junction to Case ⁽¹⁾			3.8	°C/W
R _{θJA}	Thermal Resistance Junction to Ambient ⁽¹⁾ (2)			52	°C/W

R_{0,UC} is determined with the device mounted on a 1 inch square 2 oz. Cu pad on a 1.5 x 1.5 in 0.060 inch thick FR4 board. R_{0,UC} is specified by design while $R_{\theta,JA}$ is determined by the user's board design. Device mounted on FR4 Material with 1 inch² of 2 oz. Cu.





Max $R_{\theta,JA} = 52^{\circ}C/W$ when mounted on 1 inch² of 2 oz. Cu.



Max $R_{\theta JA} = 121^{\circ}\text{C/W}$ when mounted on minimum pad area of 2 oz. Cu.

TYPICAL MOSFET CHARACTERISTICS

 $(T_A = 25^{\circ}C \text{ unless otherwise stated})$

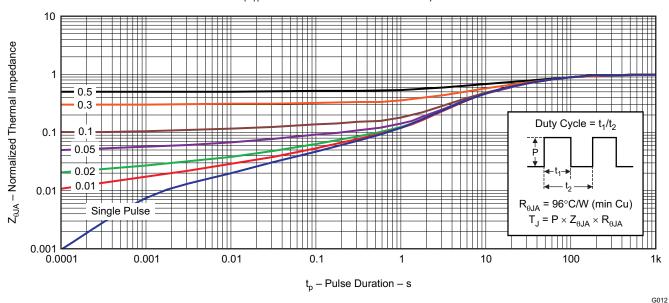


Figure 1. Transient Thermal Impedance



TYPICAL MOSFET CHARACTERISTICS (continued)

(T_A = 25°C unless otherwise stated)

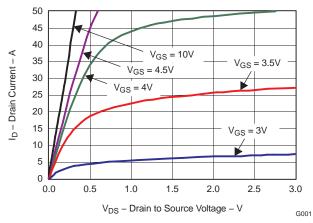


Figure 2. Saturation Characteristics

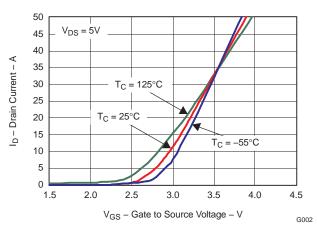


Figure 3. Transfer Characteristics

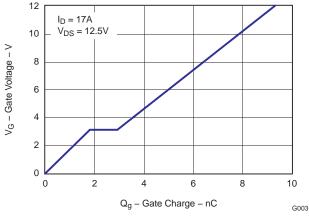


Figure 4. Gate Charge

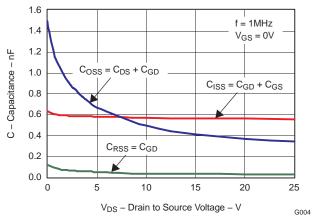


Figure 5. Capacitance

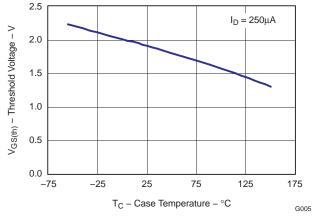


Figure 6. Threshold Voltage vs. Temperature

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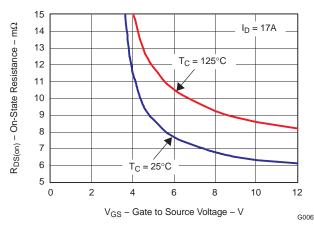


Figure 7. On Resistance vs. Gate Voltage



TYPICAL MOSFET CHARACTERISTICS (continued)

$(T_A = 25^{\circ}C \text{ unless otherwise stated})$

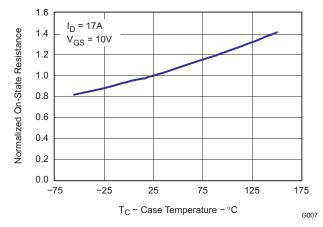


Figure 8. On Resistance vs. Temperature

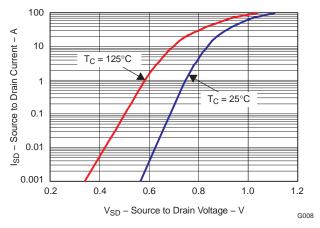


Figure 9. Typical Diode Forward Voltage

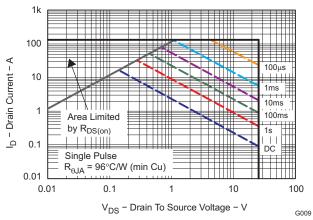


Figure 10. Maximum Safe Operating Area

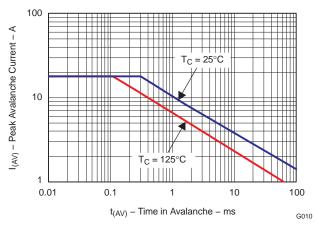


Figure 11. Single Pulse Unclamped Inductive Switching

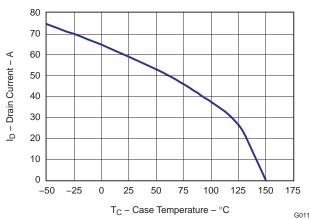
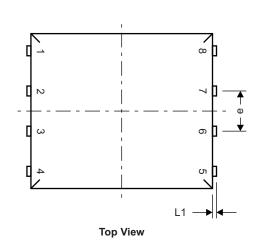


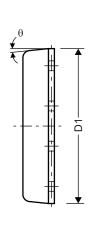
Figure 12. Maximum Drain Current vs. Temperature



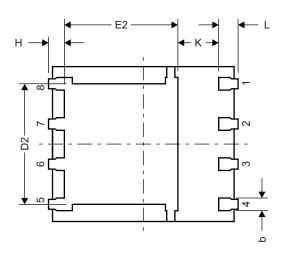
MECHANICAL DATA

Q5A Package Dimensions

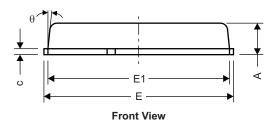




Side View



Bottom View



M0135-01

DIM	MILLIMETERS			
	MIN	NOM	MAX	
Α	0.90	1.00	1.10	
b	0.33	0.41	0.51	
С	0.20	0.25	0.30	
D1	4.80	4.90	5.00	
D2	3.61	3.81	3.96	
Е	5.90	6.00	6.10	
E1	5.70	5.75	5.80	
E2	3.38	3.58	3.78	
е	1.27 BSC			
Н	0.41	0.51	0.61	
K	1.10			
L	0.51	0.61	0.71	
L1	0.06	0.13	0.20	
θ	0°		12°	

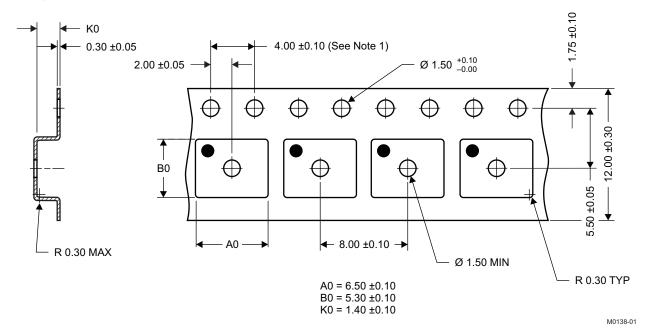


Recommended PCB Pattern						
F6 - F1	F7					
F10 F10	M0139-01 4 7 4 7 7 7 7 7 7 7 7 7 7					

DIM	MILLIMETERS		INC	HES	
	MIN	MAX	MIN	MAX	
F1	6.205	6.305	0.244	0.248	
F2	4.46	4.56	0.176	0.18	
F3	4.46	4.56	0.176	0.18	
F4	0.65	0.7	0.026	0.028	
F5	0.62	0.67	0.024	0.026	
F6	0.63	0.68	0.025	0.027	
F7	0.7	0.8	0.028	0.031	
F8	0.65	0.7	0.026	0.028	
F9	0.62	0.67	0.024	0.026	
F10	4.9	5	0.193	0.197	
F11	4.46	4.56	0.176	0.18	

For recommended circuit layout for PCB designs, see application note SLPA005 – Reducing Ringing Through PCB Layout Techniques.

Q5A Tape and Reel Information



Notes:

- 1. 10 sprocket hole pitch cumulative tolerance ±0.2
- 2. Camber not to exceed 1mm IN 100mm, noncumulative over 250mm
- 3. Material:black static dissipative polystyrene
- 4. All dimensions are in mm (unless otherwise specified)
- 5. A0 and B0 measured on a plane 0.3mm above the bottom of the pocket
- 6. MSL1 260°C (IR and Convection) PbF Reflow Compatible

SLPS205A -AUGUST 2009-REVISED MAY 2010



REVISION HISTORY

Cł	nanges from Original (August 2009) to Revision A	Page	
•	Deleted the Package Marking Information section		7

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