



CSD16411Q3

SLPS206-AUGUST 2009

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N-Channel NexFET™ Power MOSFETs

FEATURES

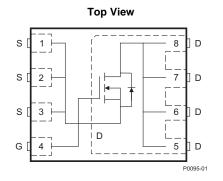
- Ultra Low Qg and Qgd
- Low Thermal Resistance
- Avalanche Rated
- Pb Free Terminal Plating
- RoHS Compliant
- Halogen Free
- SON 3.3mm x 3.3mm Plastic Package

APPLICATIONS

- Point-of-Load Synchronous Buck Converter for Applications in Networking, Telecom and Computing Systems
- Optimized for Control FET Applications

DESCRIPTION

The NexFET[™] power MOSFET has been designed to minimize losses in power conversion applications.



PRODUCT SUMMARY

V _{DS}	Drain to Source Voltage 25			
Qg	Gate Charge Total (4.5V)	2.9	nC	
Q _{gd}	Gate Charge Gate to Drain	0.7	nC	
R _{DS(op)} Drain to Source On Resistanc		$V_{GS} = 4.5V$	12	mΩ
R _{DS(on)}	Drain to Source On Resistance	V _{GS} = 10V 8		mΩ
V _{GS(th)}	Threshold Voltage	2	V	

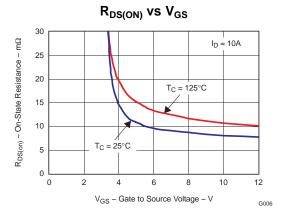
ORDERING INFORMATION

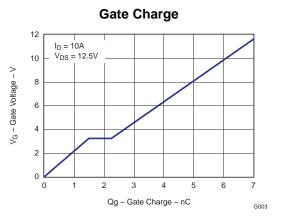
Device	Package	Media	Qty	Ship
CSD16411Q3	SON 3.3×3.3 Plastic Package	13-inch reel	2500	Tape and Reel

ABSOLUTE MAXIMUM RATINGS

$T_A = 2$	5°C unless otherwise stated	VALUE	UNIT
V_{DS}	Drain to Source Voltage	25	V
V_{GS}	Gate to Source Voltage	+16 / -12	V
	Continuous Drain Current, T _C = 25°C	56	А
ID	Continuous Drain Current ⁽¹⁾	14	А
I _{DM}	Pulsed Drain Current, $T_A = 25^{\circ}C^{(2)}$	138	А
PD	Power Dissipation ⁽¹⁾	2.7	W
T _J , T _{STG}	Operating Junction and Storage Temperature Range	-55 to 150	ů
E _{AS}	Avalanche Energy, single pulse $I_D = 18A$, L = 0.1mH, $R_G = 25\Omega$	16	mJ

(1) $R_{\theta,JA} = 47^{\circ}$ C/W on 1in² Cu (2 oz.) on 0.060" thick FR4 PCB. (2) Pulse width <300µs, duty cycle <2%





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NexFET is a trademark of Texas Instruments.



ELECTRICAL CHARACTERISTICS

 $(T_A = 25^{\circ}C \text{ unless otherwise stated})$

PARAMETER		PARAMETER TEST CONDITIONS		TYP	MAX	UNIT
Static Cl	naracteristics					
BV _{DSS}	Drain to Source Voltage	$V_{GS} = 0V, I_D = 250\mu A$	25			V
I _{DSS}	Drain to Source Leakage Current	$V_{GS} = 0V, V_{DS} = 20V$			1	μΑ
I _{GSS}	Gate to Source Leakage Current	$V_{DS} = 0V, V_{GS} = +16 / -12$			100	nA
V _{GS(th)}	Gate to Source Threshold Voltage	$V_{DS} = V_{GS}, I_D = 250 \mu A$	1.7	2	2.3	V
Р	Droin to Source On Desistance	V _{GS} = 4.5V, I _D = 10A		12	15	mΩ
R _{DS(on)}	Drain to Source On Resistance	$V_{GS} = 10V, I_{D} = 10A$		8	10	mΩ
9 _{fs}	Transconductance	V _{DS} = 15V, I _D = 10A		30		S
Dynamic	Characteristics				I	
C _{ISS}	Input Capacitance			440	570	pF
C _{OSS}	Output Capacitance	V _{GS} = 0V, V _{DS} = 12.5V, f = 1MHz		330	430	pF
C _{RSS}	Reverse Transfer Capacitance			33	43	pF
R _g	Series Gate Resistance			0.8	1.6	Ω
Qg	Gate Charge Total (4.5V)			2.9	3.8	nC
Q _{gd}	Gate Charge Gate to Drain			0.7		nC
Q _{gs}	Gate Charge Gate to Source	V _{DS} = 12.5V, I _D = 10A		1.5		nC
Qg(th)	Gate Charge at Vth			0.9		nC
Q _{OSS}	Output Charge	$V_{DS} = 12.5V, V_{GS} = 0V$		6.5		nC
t _{d(on)}	Turn On Delay Time			5.3		ns
t _r	Rise Time	V _{DS} = 12.5V, V _{GS} = 4.5V, I _D = 10A		7.8		ns
t _{d(off)}	Turn Off Delay Time	$R_{G} = 2\Omega$		6		ns
t _f	Fall Time			3.1		ns
Diode Cl	haracteristics	· · ·			1	
V _{SD}	Diode Forward Voltage	$I_{\rm S} = 10 {\rm A}, V_{\rm GS} = 0 {\rm V}$		0.85	1	V
Q _{rr}	Reverse Recovery Charge	V_{DD} = 12.5V, I _F = 10A, di/dt = 300A/µs		11.7		nC
t _{rr}	Reverse Recovery Time	V _{DD} = 12.5V, I _F = 10A, di/dt = 300A/µs		15.5		ns

THERMAL CHARACTERISTICS

($T_A = 25^{\circ}C$ unless otherwise stated)

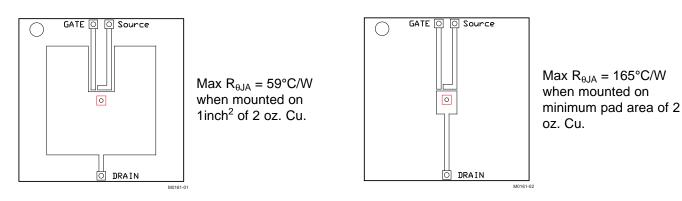
	PARAMETER	MIN	TYP	MAX	UNIT
R $_{\theta JC}$	Thermal Resistance Junction to Case ⁽¹⁾			3.5	°C/W
R $_{\theta JA}$	Thermal Resistance Junction to Ambient ⁽¹⁾⁽²⁾			59	°C/W

(1) R $_{\theta JC}$ is determined with the device mounted on a 1 inch square 2 oz. Cu pad on a 1.5 x 1.5 in .060 inch thick FR4 board. R $_{\theta JC}$ is specified by design while R $_{\theta JA}$ is determined by the user's board design.

(2) Device mounted on FR4 Material with 1 inch² of 2 oz. Cu.



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 $(T_A = 25^{\circ}C \text{ unless otherwise stated})$

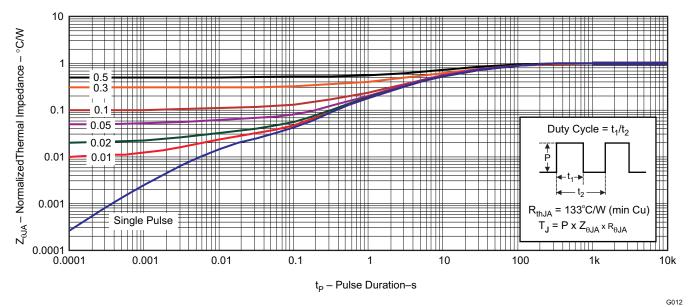


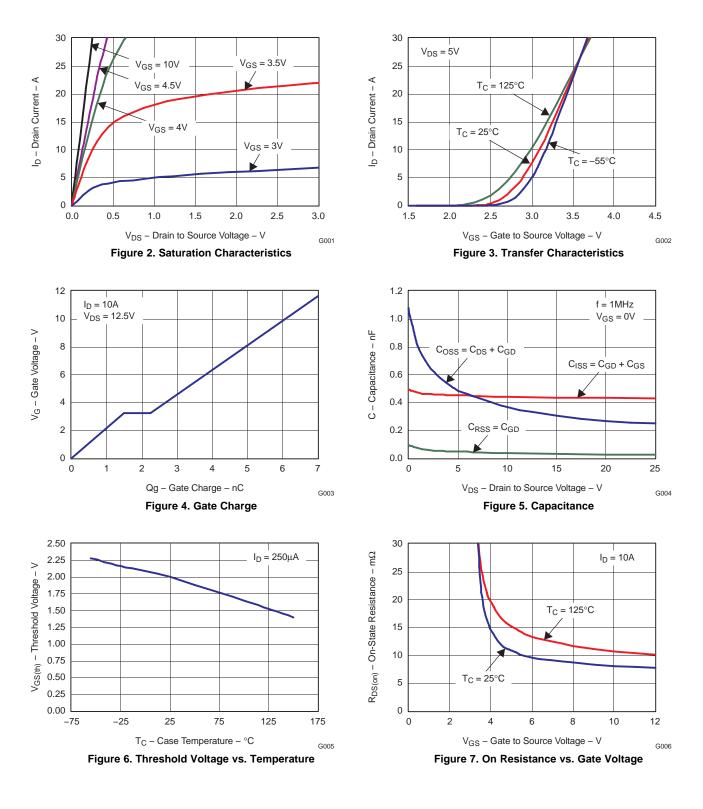
Figure 1. Transient Thermal Impedance

Pridu xt Filder Link s). CSD164 (103)

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TYPICAL MOSFET CHARACTERISTICS (continued)

$(T_A = 25^{\circ}C \text{ unless otherwise stated})$



INSTRUMENTS

FEXAS

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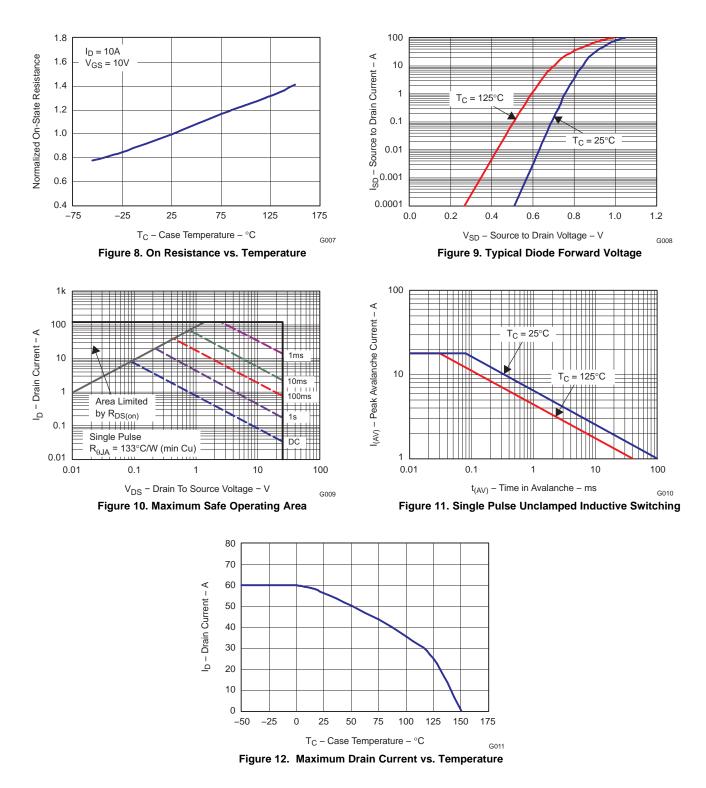


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TYPICAL MOSFET CHARACTERISTICS (continued)

$(T_A = 25^{\circ}C \text{ unless otherwise stated})$



Priduct Folder Link s). CSD1641103

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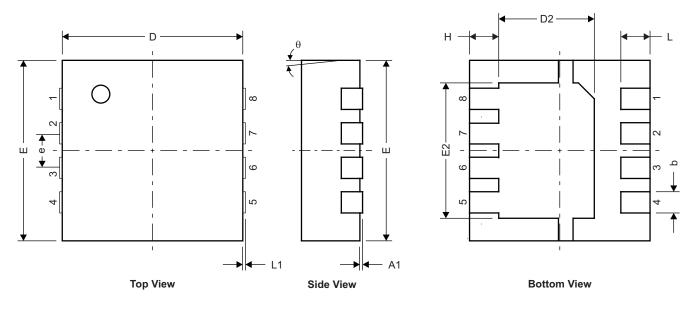
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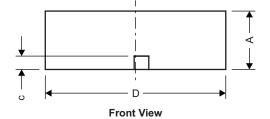
TEXAS INSTRUMENTS

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MECHANICAL DATA

Q3 Package Dimensions





M0142-01

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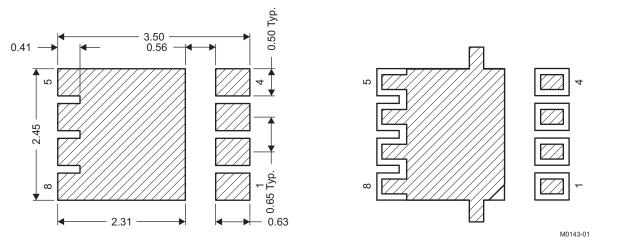
DIM	MILLIMETERS			INCHES		
DIM	MIN	NOM	MAX	MIN	NOM	МАХ
А	0.950	1.000	1.100	0.037	0.039	0.043
A1	0.000	0.000	0.050	0.000	0.000	0.002
b	0.280	0.340	0.400	0.011	0.013	0.016
С	0.150	0.200	0.250	0.006	0.008	0.010
D	3.200	3.300	3.400	0.126	0.130	0.134
D1	-	-	-	-	-	-
D2	1.650	1.750	1.800	0.065	0.069	0.071
E	3.200	3.300	3.400	0.126	0.130	0.134
E1	-	-	_	_	-	_
E2	2.350	2.450	2.550	0.093	0.096	0.100
е		0.650 TYP			0.026	
Н	0.35	0.450	0.550	0.014	0.018	0.022
L	0.35	0.450	0.550	0.014	0.018	0.022
L1	-	-	-	-	-	_
θ	-	-	-	_	-	-

Priduct Filder Link s). CSD164 (103



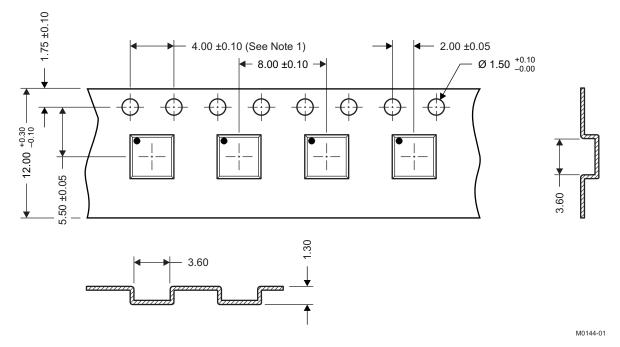
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Recommended PCB Pattern



For recommended circuit layout for PCB designs, see application note SLPA005 – Reducing Ringing Through PCB Layout Techniques.

Q3 Tape and Reel Information



Product Folder Links): CSD164 1103

Notes:

- 1. 10 sprocket hole pitch cumulative tolerance ±0.2
- 2. Camber not to exceed 1mm IN 100mm, noncumulative over 250mm
- 3. Material:black static dissipative polystyrene
- 4. All dimensions are in mm (unless otherwise specified)
- 5. Thickness: 0.30 ±0.05mm
- 6. MSL1 260°C (IR and Convection) PbF Reflow Compatible

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Package Marking Information

Location		_	_	
1st Line	8	5	5	8
CSD = Fixed Characters			1 C C C C C C C C C C C C C C C C C C C	1 - C
NNNNN = Product Code				
2nd Line (Date Code)	CSDN	NNNN		
YY = Last 2 digits of the Year				
WW = 2-digit Work Week	YYWW	C		
C = Country of Origin				
> Philippines = P				
> Taiwan = T				
> China = C				
3rd Line	1	4	4	.
LLLLL = Last 5 digits of the Wafer Lot #	Pin 1 Identifier			

M0145-01

PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing		ickage Qty	Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp ⁽³⁾
CSD16411Q3	ACTIVE	SON	DQG	8 2	2500	Pb-Free (RoHS Exempt)	CU SN	Level-1-260C-UNLIM

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

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Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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