

30V, N-Channel NexFET™ Power MOSFETs

 Check for Samples: [CSD17302Q5A](#)

FEATURES

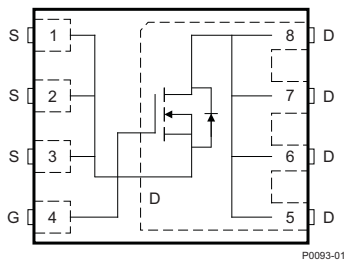
- Optimized for 5V Gate Drive
- Ultralow Q_g and Q_{gd}
- Low Thermal Resistance
- Avalanche Rated
- Pb Free Terminal Plating
- RoHS Compliant
- Halogen Free
- SON 5-mm × 6-mm Plastic Package

APPLICATIONS

- Notebook Point of Load
- Point-of-Load Synchronous Buck in Networking, Telecom and Computing Systems

DESCRIPTION

The NexFET™ power MOSFET has been designed to minimize losses in power conversion applications, and optimized for 5V gate drive applications.

Top View


PRODUCT SUMMARY

V_{DS}	Drain to Source Voltage	30	V
Q_g	Gate Charge Total (4.5V)	5.4	nC
Q_{gd}	Gate Charge Gate to Drain	1.2	nC
$R_{DS(on)}$	Drain to Source On Resistance	$V_{GS} = 3V$	9.5 mΩ
		$V_{GS} = 4.5V$	7.3 mΩ
		$V_{GS} = 8V$	6.4 mΩ
$V_{GS(th)}$	Threshold Voltage	1.2	V

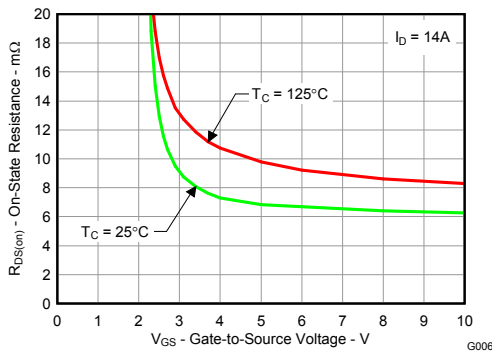
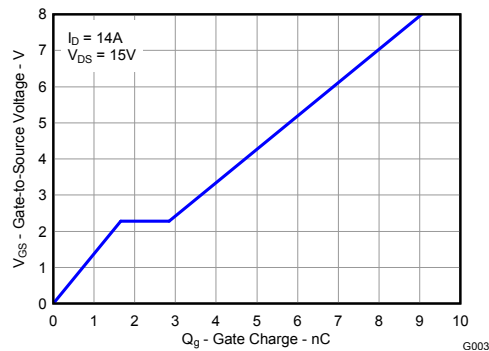
ORDERING INFORMATION

Device	Package	Media	Qty	Ship
CSD17302Q5A	SON 5-mm × 6-mm Plastic Package	13-Inch Reel	2500	Tape and Reel

ABSOLUTE MAXIMUM RATINGS

$T_A = 25^\circ\text{C}$ unless otherwise stated		VALUE	UNIT
V_{DS}	Drain to Source Voltage	30	V
V_{GS}	Gate to Source Voltage	+10 / -8	V
I_D	Continuous Drain Current, $T_C = 25^\circ\text{C}$	87	A
	Continuous Drain Current ⁽¹⁾	16	A
I_{DM}	Pulsed Drain Current, $T_A = 25^\circ\text{C}$ ⁽²⁾	104	A
P_D	Power Dissipation ⁽¹⁾	3	W
T_J, T_{STG}	Operating Junction and Storage Temperature Range	-55 to 150	$^\circ\text{C}$
E_{AS}	Avalanche Energy, single pulse $I_D = 35\text{A}, L = 0.1\text{mH}, R_G = 25\Omega$	61	mJ

- (1) Typical $R_{\theta JA} = 41^\circ\text{C/W}$ on a 1-inch² (6.45-cm²), 2-oz. (0.071-mm thick) Cu pad on a 0.06-inch (1.52-mm) thick FR4 PCB.
- (2) Pulse duration $\leq 300\mu\text{s}$, duty cycle $\leq 2\%$

 $R_{DS(on)}$ vs V_{GS}

GATE CHARGE


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These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

ELECTRICAL CHARACTERISTICS

(T_A = 25°C unless otherwise stated)

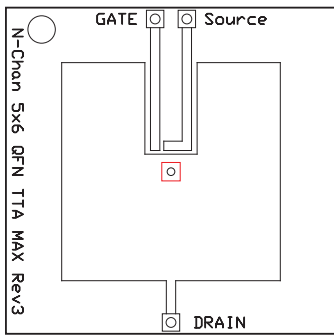
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Static Characteristics						
B _V DSS	Drain to Source Voltage	V _{GS} = 0V, I _D = 250μA	30			V
I _{DSS}	Drain to Source Leakage Current	V _{GS} = 0V, V _{DS} = 24V			1	μA
I _{GSS}	Gate to Source Leakage Current	V _{DS} = 0V, V _{GS} = +10 / -8V			100	nA
V _{GS(th)}	Gate to Source Threshold Voltage	V _{DS} = V _{GS} , I _D = 250μA	0.9	1.2	1.7	V
R _{DS(on)}	Drain to Source On Resistance	V _{GS} = 3V, I _D = 14A		9.5	12..8	mΩ
		V _{GS} = 4.5V, I _D = 14A		7.3	9	mΩ
		V _{GS} = 8V, I _D = 14A		6.4	7.9	mΩ
g _{fs}	Transconductance	V _{DS} = 15V, I _D = 14A		68		S
Dynamic Characteristics						
C _{iss}	Input Capacitance	V _{GS} = 0V, V _{DS} = 15V, f = 1MHz		730	950	pF
C _{oss}	Output Capacitance			390	510	pF
C _{rss}	Reverse Transfer Capacitance			35	45	pF
R _G	Series Gate Resistance			0.8	1.6	Ω
Q _g	Gate Charge Total (4.5V)	V _{DS} = 15V, I _D = 14A		5.4	7	nC
Q _{gd}	Gate Charge Gate to Drain			1.2		nC
Q _{gs}	Gate Charge Gate to Source			1.7		nC
Q _{g(th)}	Gate Charge at V _{th}			0.9		nC
Q _{oss}	Output Charge	V _{DS} = 13V, V _{GS} = 0V		9.5		nC
t _{d(on)}	Turn On Delay Time	V _{DS} = 15V, V _{GS} = 4.5V, I _{DS} = 14A, R _G = 2Ω		5.2		ns
t _r	Rise Time			8.4		ns
t _{d(off)}	Turn Off Delay Time			10.6		ns
t _f	Fall Time			3.1		ns
Diode Characteristics						
V _{SD}	Diode Forward Voltage	I _{SD} = 14A, V _{GS} = 0V		0.85	1	V
Q _{rr}	Reverse Recovery Charge	V _{DD} = 13V, I _F = 14A, di/dt = 300A/μs		15.4		nC
t _{rr}	Reverse Recovery Time			17.5		ns

THERMAL CHARACTERISTICS

(T_A = 25°C unless otherwise stated)

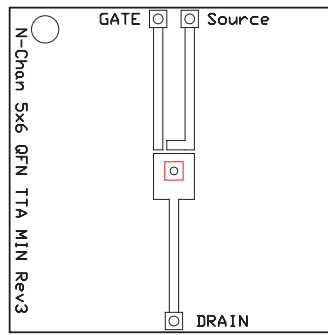
PARAMETER		MIN	TYP	MAX	UNIT
R _{θJC}	Thermal Resistance Junction to Case ⁽¹⁾			1.8	°C/W
R _{θJA}	Thermal Resistance Junction to Ambient ⁽¹⁾⁽²⁾			51	°C/W

- (1) R_{θJC} is determined with the device mounted on a 1-inch² (6.45-cm²), 2-oz. (0.071-mm thick) Cu pad on a 1.5-inch × 1.5-inch (3.81-cm × 3.81-cm), 0.06-inch (1.52-mm) thick FR4 PCB. R_{θJC} is specified by design, whereas R_{θJA} is determined by the user's board design.
- (2) Device mounted on FR4 material with 1-inch² (6.45-cm²), 2-oz. (0.071-mm thick) Cu.



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Max $R_{\theta JA} = 51^\circ\text{C/W}$ when mounted on 1 inch² (6.45 cm²) of 2-oz. (0.071-mm thick) Cu.

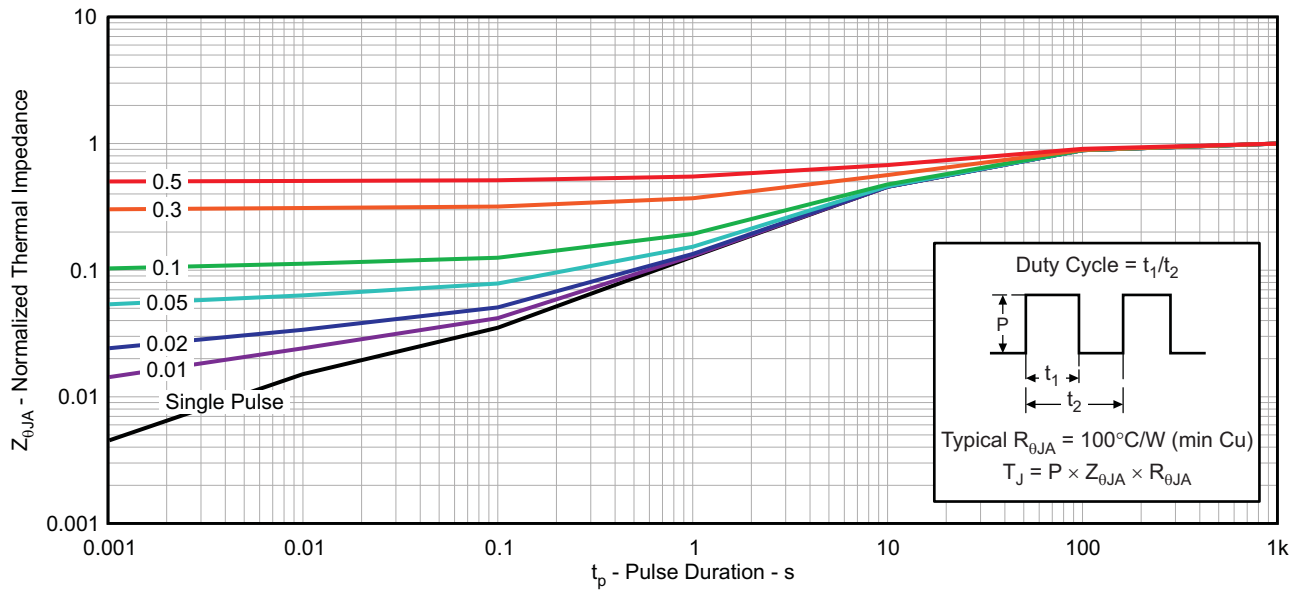


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Max $R_{\theta JA} = 125^\circ\text{C/W}$ when mounted on a minimum pad area of 2-oz. (0.071-mm thick) Cu.

TYPICAL MOSFET CHARACTERISTICS

($T_A = 25^\circ\text{C}$ unless otherwise stated)



G012

Figure 1. Transient Thermal Impedance

TYPICAL MOSFET CHARACTERISTICS (continued)

($T_A = 25^\circ\text{C}$ unless otherwise stated)

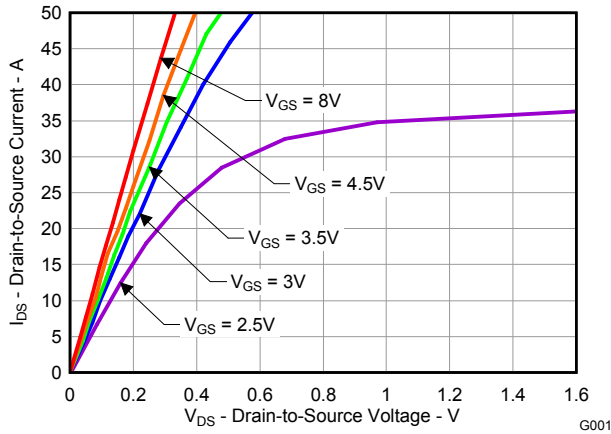


Figure 2. Saturation Characteristics

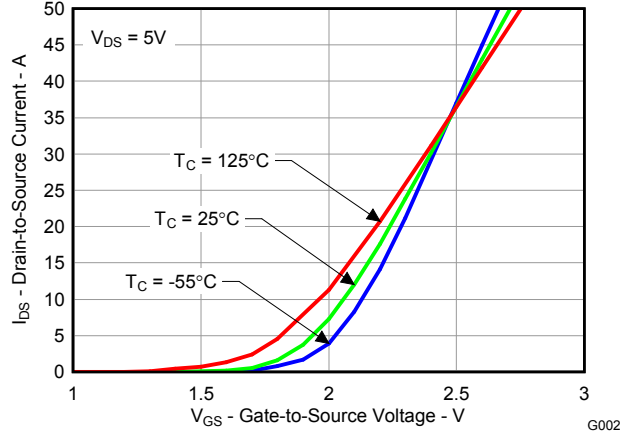


Figure 3. Transfer Characteristics

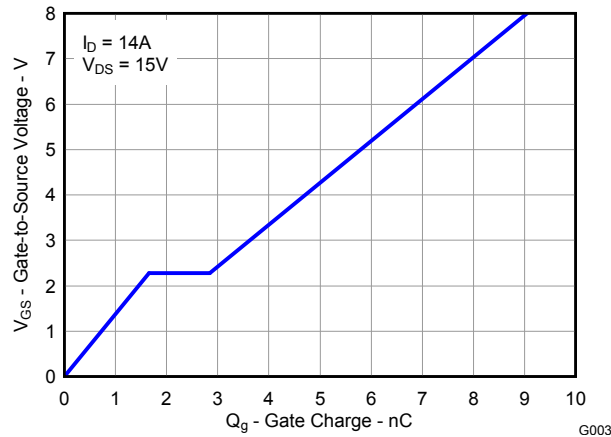


Figure 4. Gate Charge

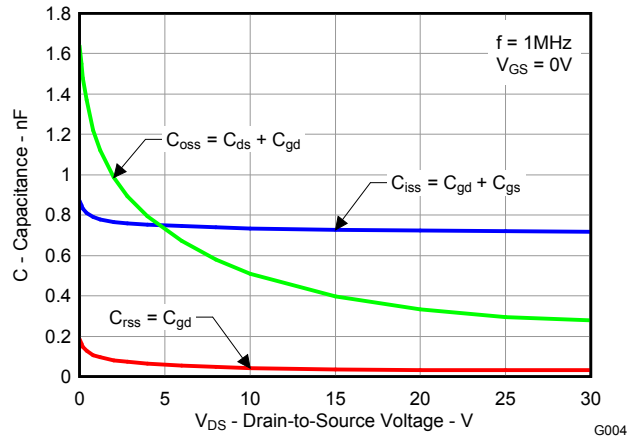


Figure 5. Capacitance

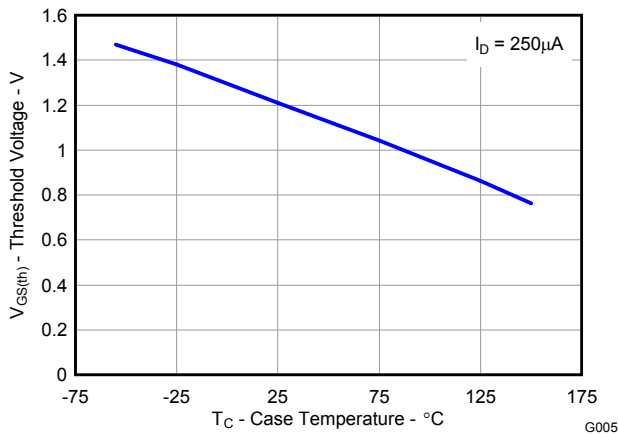


Figure 6. Threshold Voltage vs. Temperature

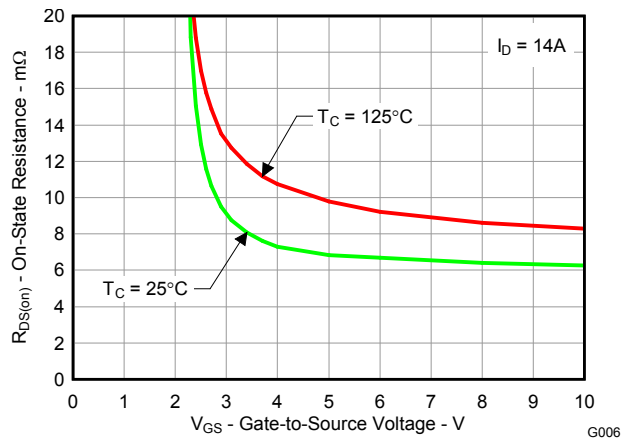


Figure 7. On-State Resistance vs. Gate-to-Source Voltage

TYPICAL MOSFET CHARACTERISTICS (continued)

($T_A = 25^\circ\text{C}$ unless otherwise stated)

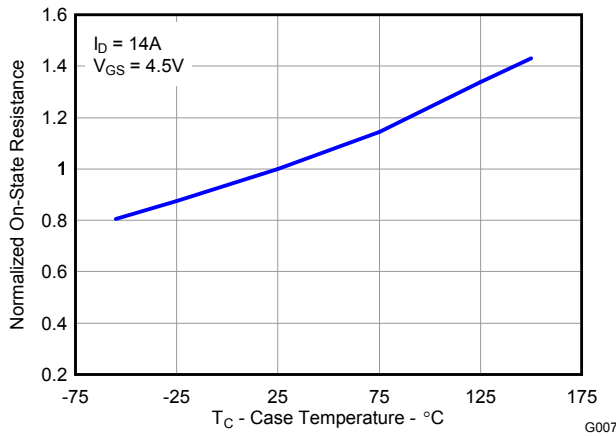


Figure 8. Normalized On-State Resistance vs. Temperature

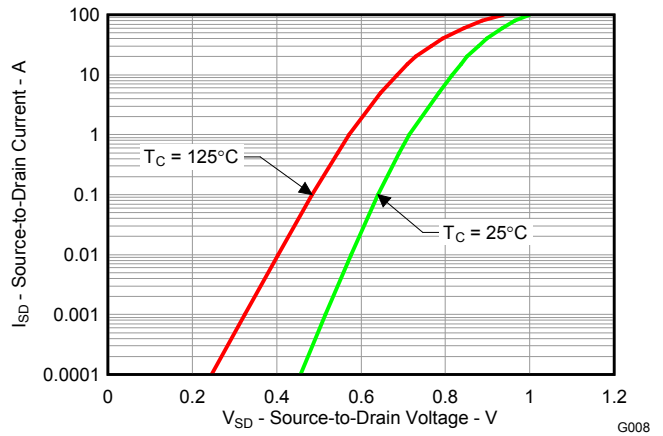


Figure 9. Typical Diode Forward Voltage

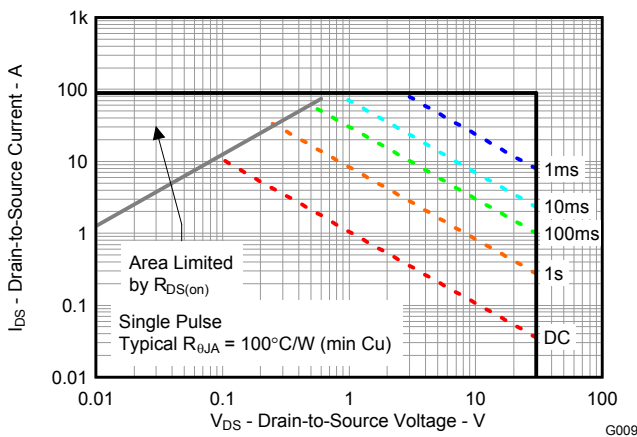


Figure 10. Maximum Safe Operating Area

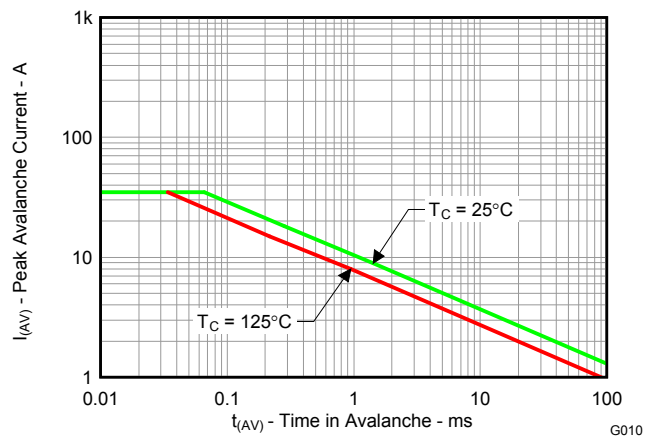


Figure 11. Single Pulse Unclamped Inductive Switching

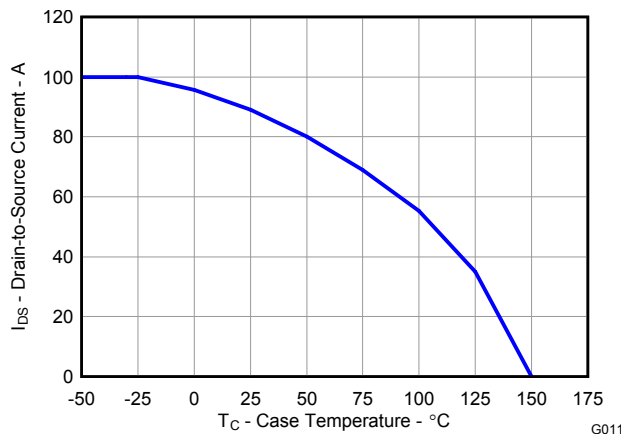
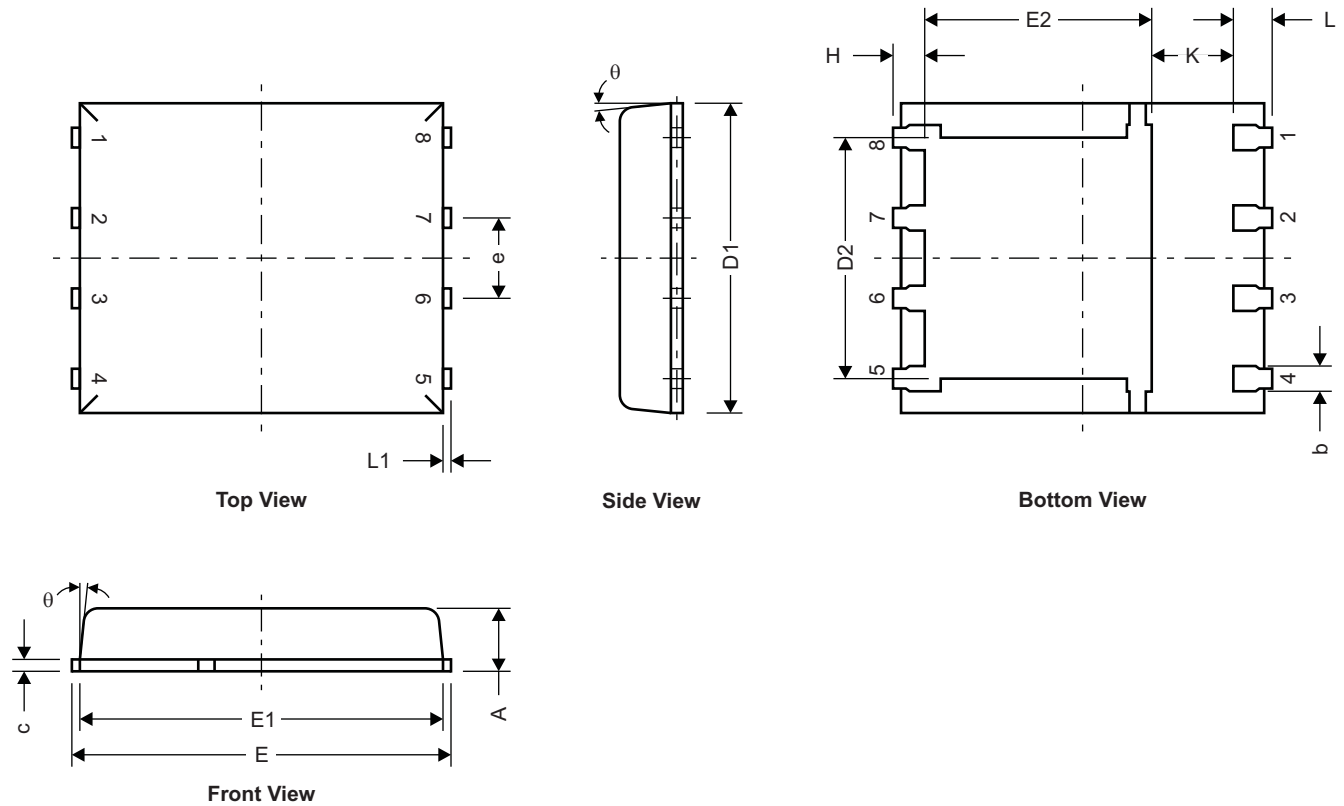


Figure 12. Maximum Drain Current vs. Temperature

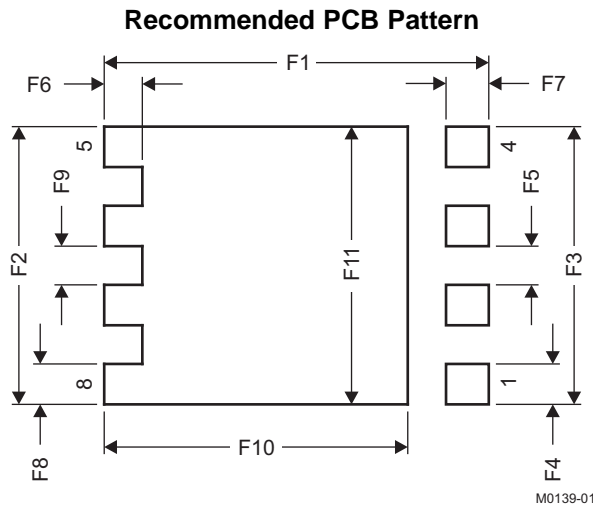
MECHANICAL DATA

Q5A Package Dimensions



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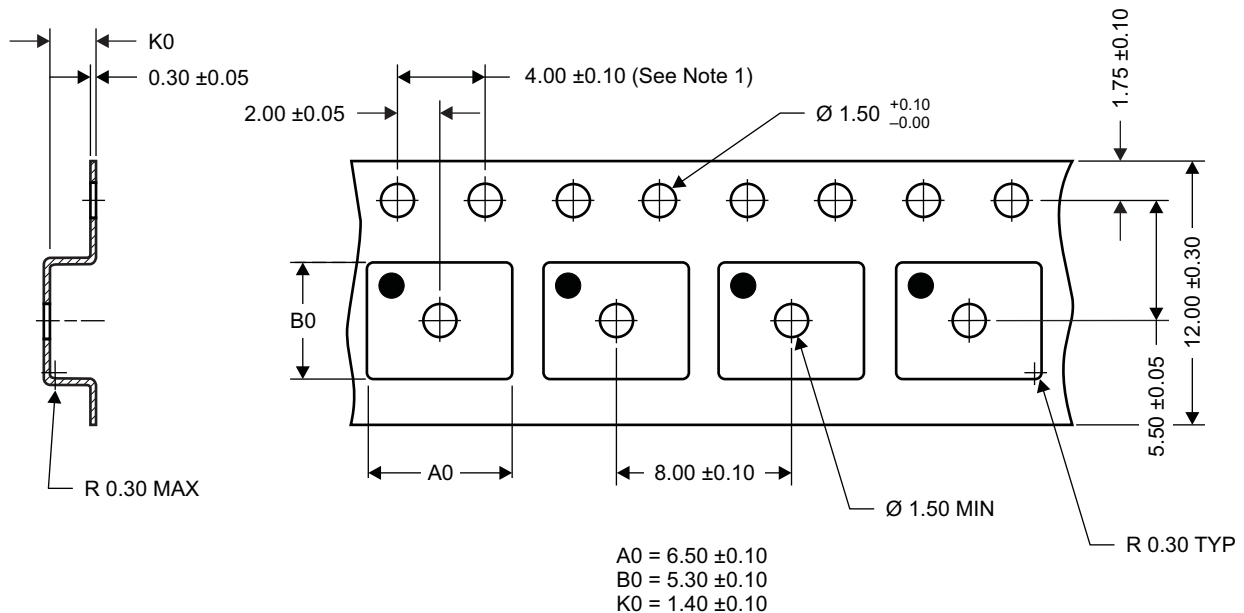
DIM	MILLIMETERS		
	MIN	NOM	MAX
A	0.90	1.00	1.10
b	0.33	0.41	0.51
c	0.20	0.25	0.30
D1	4.80	4.90	5.00
D2	3.61	3.81	3.96
E	5.90	6.00	6.10
E1	5.70	5.75	5.80
E2	3.38	3.58	3.78
e	1.27 BSC		
H	0.41	0.51	0.61
K	1.10		
L	0.51	0.61	0.71
L1	0.06	0.13	0.20
θ	0°		12°



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
F1	6.205	6.305	0.244	0.248
F2	4.46	4.56	0.176	0.18
F3	4.46	4.56	0.176	0.18
F4	0.65	0.7	0.026	0.028
F5	0.62	0.67	0.024	0.026
F6	0.63	0.68	0.025	0.027
F7	0.7	0.8	0.028	0.031
F8	0.65	0.7	0.026	0.028
F9	0.62	0.67	0.024	0.026
F10	4.9	5	0.193	0.197
F11	4.46	4.56	0.176	0.18

For recommended circuit layout for PCB designs, see application note [SLPA005 – Reducing Ringing Through PCB Layout Techniques](#).

Q5A Tape and Reel Information



M0138-01

Notes:

- 10-sprocket hole-pitch cumulative tolerance ±0.2
- Camber not to exceed 1mm in 100mm, noncumulative over 250mm
- Material: black static-dissipative polystyrene
- All dimensions are in mm (unless otherwise specified)
- A0 and B0 measured on a plane 0.3mm above the bottom of the pocket
- MSL1 260°C (IR and convection) PbF reflow compatible

Package Marking Information

Location

1st Line

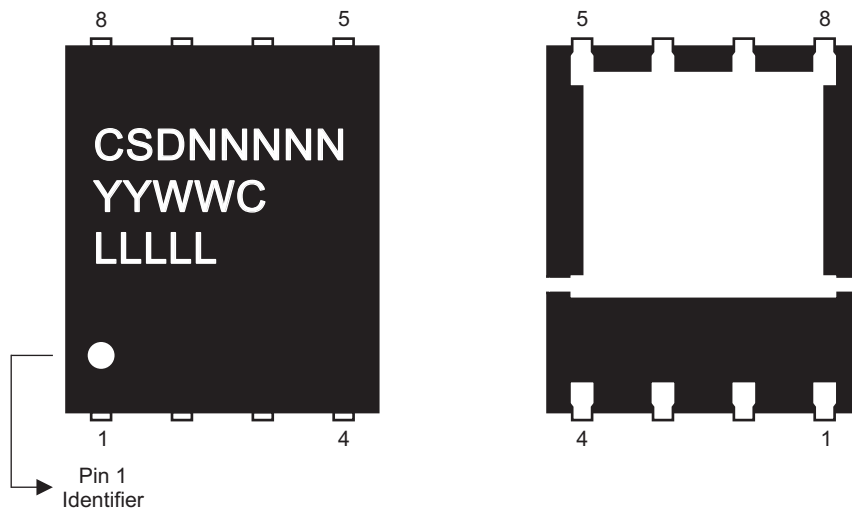
CSD = Fixed Characters
 NNNNN = Product Code

2nd Line (Date Code)

YY = Last 2 digits of the Year
 WW = 2-digit Work Week
 C = Country of Origin
 > Philippines = P
 > Taiwan = T
 > China = C

3rd Line

LLLLL = Last 5 digits of the Wafer Lot #



M0136-01

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