

P-Channel NexFET™ Power MOSFET

Check for Samples: [CSD23201W10](#)

FEATURES

- Ultra Low Qg and Qgd
- Small Footprint 1mm x 1mm
- Low Profile 0.62mm Height
- Pb Free
- Gate ESD Protection – 3kV
- RoHS Compliant
- Halogen Free

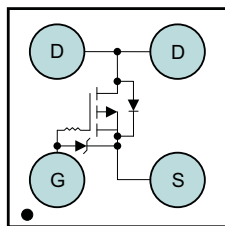
APPLICATIONS

- Battery Management
- Load Switch
- Battery Protection

DESCRIPTION

The device has been designed to deliver the lowest on resistance and gate charge in the smallest outline possible with excellent thermal characteristics in an ultra low profile.

Top View



P0097-01

PRODUCT SUMMARY

V _{DS}	Drain to Source Voltage	-12	V
Q _g	Gate Charge Total (4.5V)	1.8	nC
Q _{gd}	Gate Charge Gate to Drain	0.26	nC
R _{DS(on)}	Drain to Source On Resistance	V _{GS} = -1.5V	110 mΩ
		V _{GS} = -2.5V	77 mΩ
		V _{GS} = -4.5V	66 mΩ
V _{GS(th)}	Threshold Voltage	-0.6	V

ORDERING INFORMATION

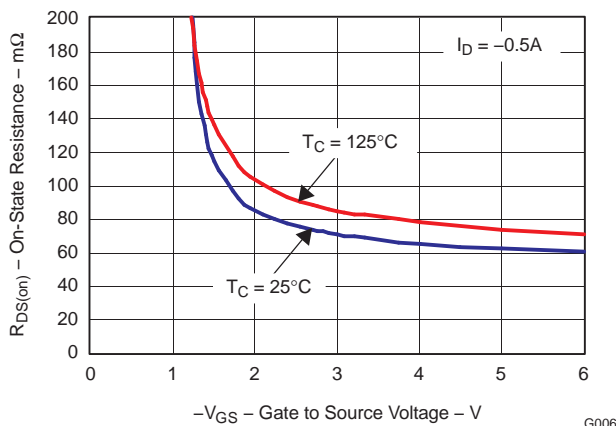
Device	Package	Media	Qty	Ship
CSD23201W10	1 x 1 Wafer Level Package	7-inch reel	3000	Tape and Reel

ABSOLUTE MAXIMUM RATINGS

T _A = 25°C unless otherwise stated		VALUE	UNIT
V _{DS}	Drain to Source Voltage	-12	V
V _{GS}	Gate to Source Voltage	-6	V
I _D	Continuous Drain Current, T _C = 25°C ⁽¹⁾	-2.2	A
I _{DM}	Pulsed Drain Current, T _A = 25°C ⁽²⁾	-8.8	A
I _G	Continuous Gate Clamp Current	-0.5	A
	Pulsed Gate Clamp Current	-7	A
P _D	Power Dissipation ⁽¹⁾	1	W
T _J , T _{STG}	Operating Junction and Storage Temperature Range	-55 to 150	°C

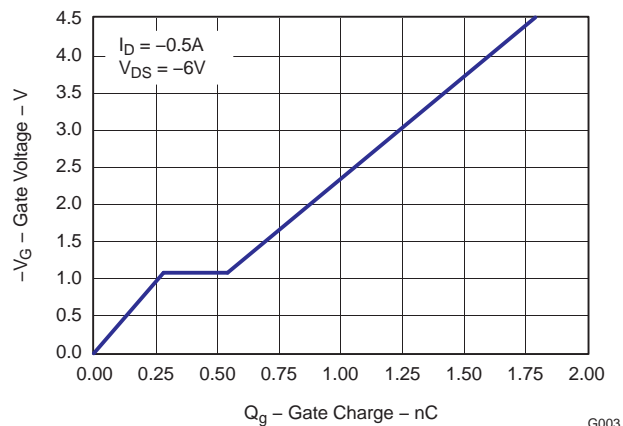
- (1) R_{θJA} = 100°C/W on 1in² Cu (2 oz.) on 0.060" thick FR4 PCB.
- (2) Pulse width ≤300μs, duty cycle ≤2%

R_{DS(ON)} vs V_{GS}



G006

Gate Charge



G003



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

ELECTRICAL CHARACTERISTICS

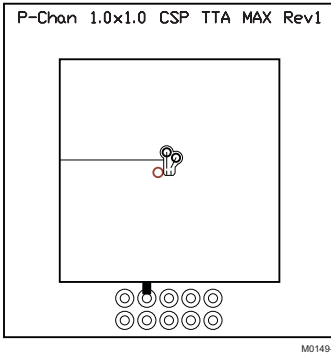
($T_A = 25^\circ\text{C}$ unless otherwise stated)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Static Characteristics						
BV_{DSS}	Drain to Source Voltage	$V_{GS} = 0V, I_D = -250\mu A$	-12			V
BV_{GSS}	Gate to Source Voltage;	$V_{DS} = 0V, I_G = -250\mu A$	-6.1		-7.2	V
I_{DSS}	Drain to Source Leakage Current	$V_{GS} = 0V, V_{DS} = -9.6V$			-1	μA
I_{GSS}	Gate to Source Leakage Current	$V_{DS} = 0V, V_{GS} = -6V$			-100	nA
$V_{GS(th)}$	Gate to Source Threshold Voltage	$V_{DS} = V_{GS}, I_D = -250\mu A$	-0.4	-0.6	-1.0	V
$R_{DS(on)}$	Drain to Source On Resistance	$V_{GS} = -1.5V, I_D = -0.5A$		110	138	m Ω
		$V_{GS} = -2.5V, I_D = -0.5A$		77	96	m Ω
		$V_{GS} = -4.5V, I_D = -0.5A$		66	82	m Ω
g_{fs}	Transconductance	$V_{DS} = -6.0V, I_D = -0.5A$		9		S
Dynamic Characteristics						
C_{ISS}	Input Capacitance	$V_{GS} = 0V, V_{DS} = -6.0V, f = 1MHz$		250	325	pF
C_{OSS}	Output Capacitance			125	155	pF
C_{RSS}	Reverse Transfer Capacitance			32	42	pF
Q_g	Gate Charge Total (-4.5V)			1.8	2.4	nC
Q_{gd}	Gate Charge Gate to Drain	$V_{DS} = -6.0V, I_D = -0.5A$		0.26		nC
Q_{gs}	Gate Charge Gate to Source			0.28		nC
$Q_{g(th)}$	Gate Charge at V_{th}			0.11		nC
Q_{OSS}	Output Charge	$V_{DS} = -6.0V, V_{GS} = 0V$		1.7		nC
$t_{d(on)}$	Turn On Delay Time	$V_{DS} = -6.0V, V_{GS} = -2.5V, I_D = -0.5A$ $R_G = 20\Omega$		24		ns
t_r	Rise Time			19		ns
$t_{d(off)}$	Turn Off Delay Time			68		ns
t_f	Fall Time			29		ns
Diode Characteristics						
V_{SD}	Diode Forward Voltage	$I_S = -0.5A, V_{GS} = 0V$	-0.77		-1.0	V
Q_{rr}	Reverse Recovery Charge	$V_{dd} = -4.0V, I_F = -0.5A, di/dt = 100A/\mu s$		2		nC
t_{rr}	Reverse Recovery Time	$V_{dd} = -4.0V, I_F = -0.5A, di/dt = 100A/\mu s$		9.5		ns

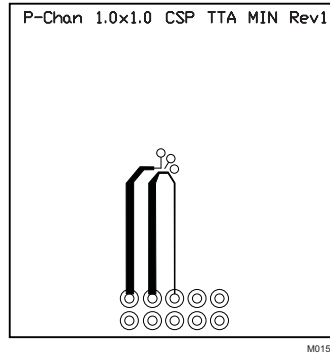
THERMAL CHARACTERISTICS

($T_A = 25^\circ\text{C}$ unless otherwise stated)

PARAMETER		MIN	TYP	MAX	UNIT
$R_{\theta JC}$	Thermal Resistance Junction to Ambient (Minimum Cu area)			245	$^\circ\text{C}/\text{W}$
$R_{\theta JA}$	Thermal Resistance Junction to Ambient (1 in ² Cu area)			125	$^\circ\text{C}/\text{W}$



Max $R_{\theta JA} = 125^{\circ}\text{C/W}$
when mounted on
1inch² of 2 oz. Cu.



Max $R_{\theta JA} = 245^{\circ}\text{C/W}$
when mounted on
minimum pad area of 2
oz. Cu.

TYPICAL MOSFET CHARACTERISTICS

($T_A = 25^{\circ}\text{C}$ unless otherwise stated)

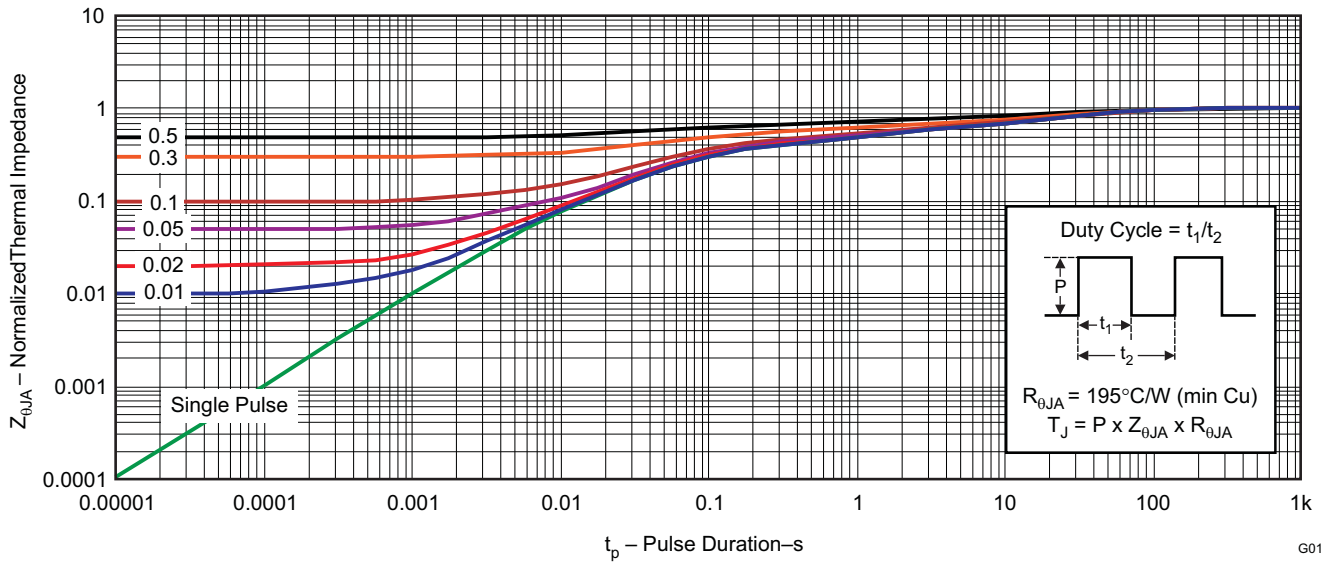


Figure 1. Transient Thermal Impedance

TYPICAL MOSFET CHARACTERISTICS (continued)

($T_A = 25^\circ\text{C}$ unless otherwise stated)

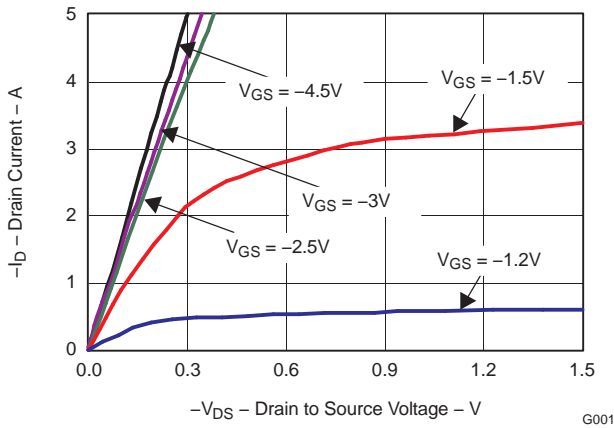


Figure 2. Saturation Characteristics

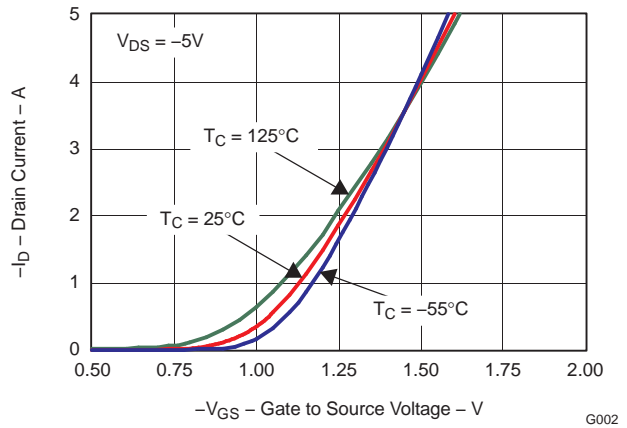


Figure 3. Transfer Characteristics

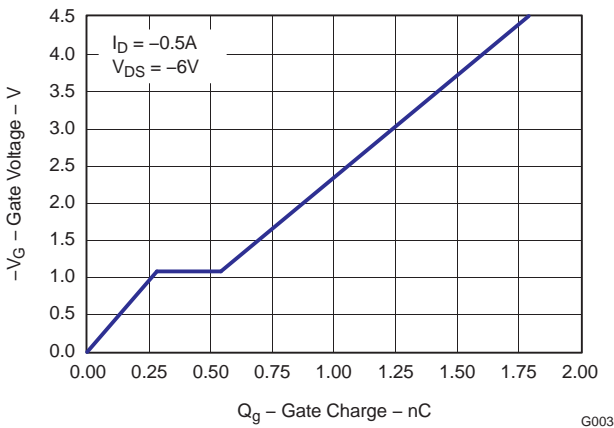


Figure 4. Gate Charge

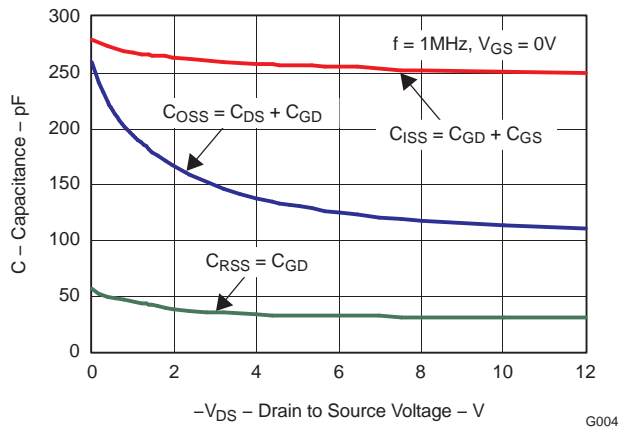


Figure 5. Capacitance

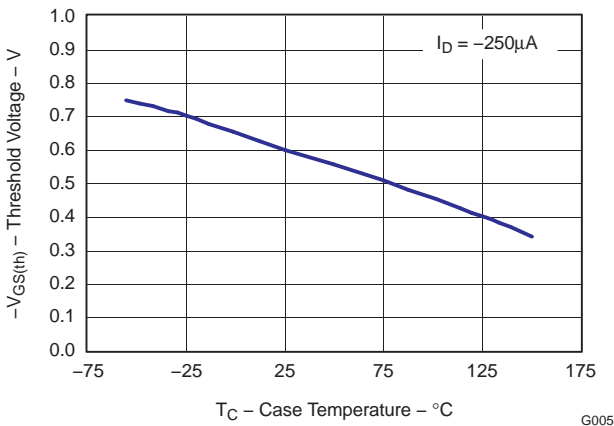


Figure 6. Threshold Voltage vs. Temperature

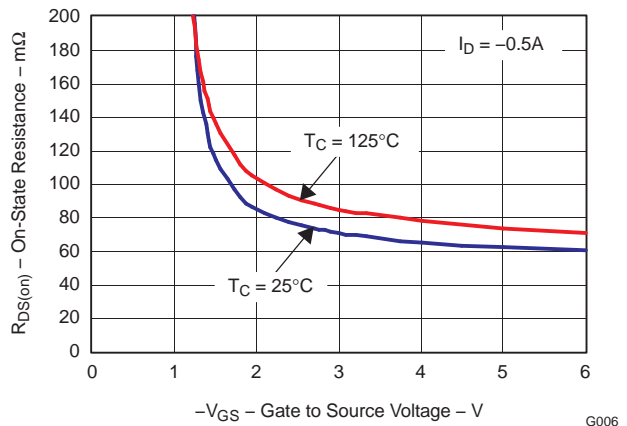


Figure 7. On Resistance vs. Gate Voltage

TYPICAL MOSFET CHARACTERISTICS (continued)

($T_A = 25^\circ\text{C}$ unless otherwise stated)

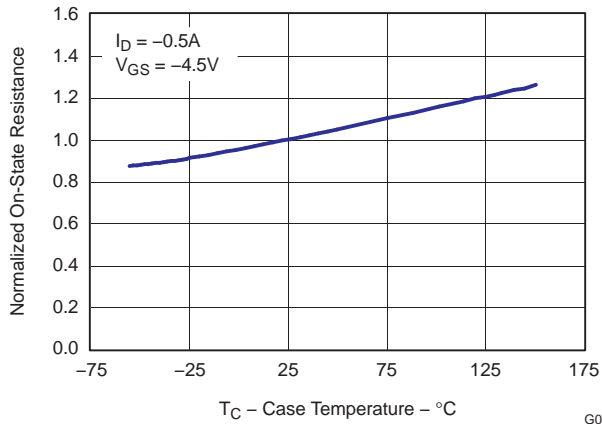


Figure 8. On Resistance vs. Temperature

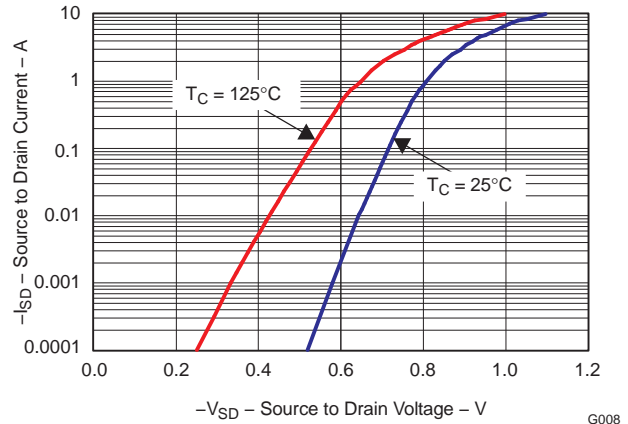


Figure 9. Typical Diode Forward Voltage

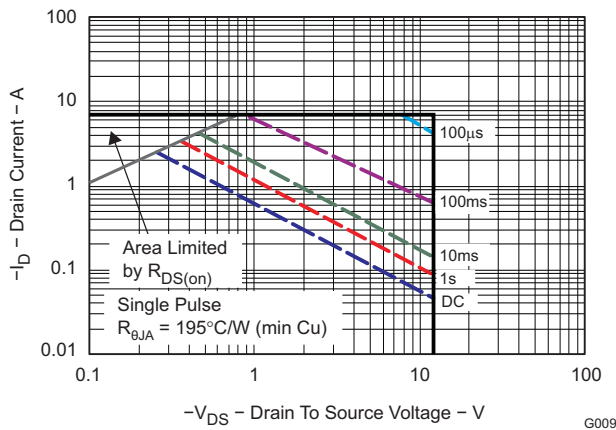


Figure 10. Maximum Safe Operating Area

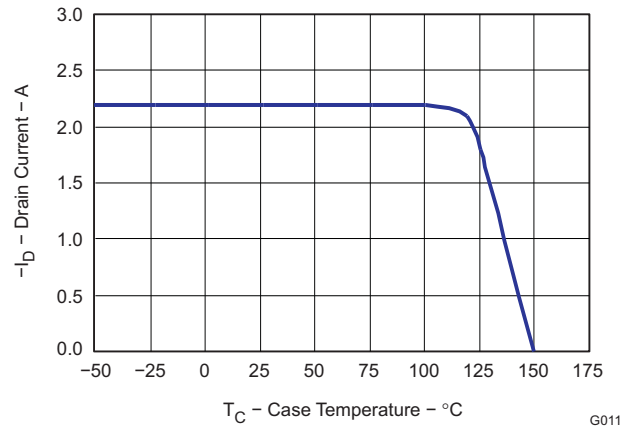
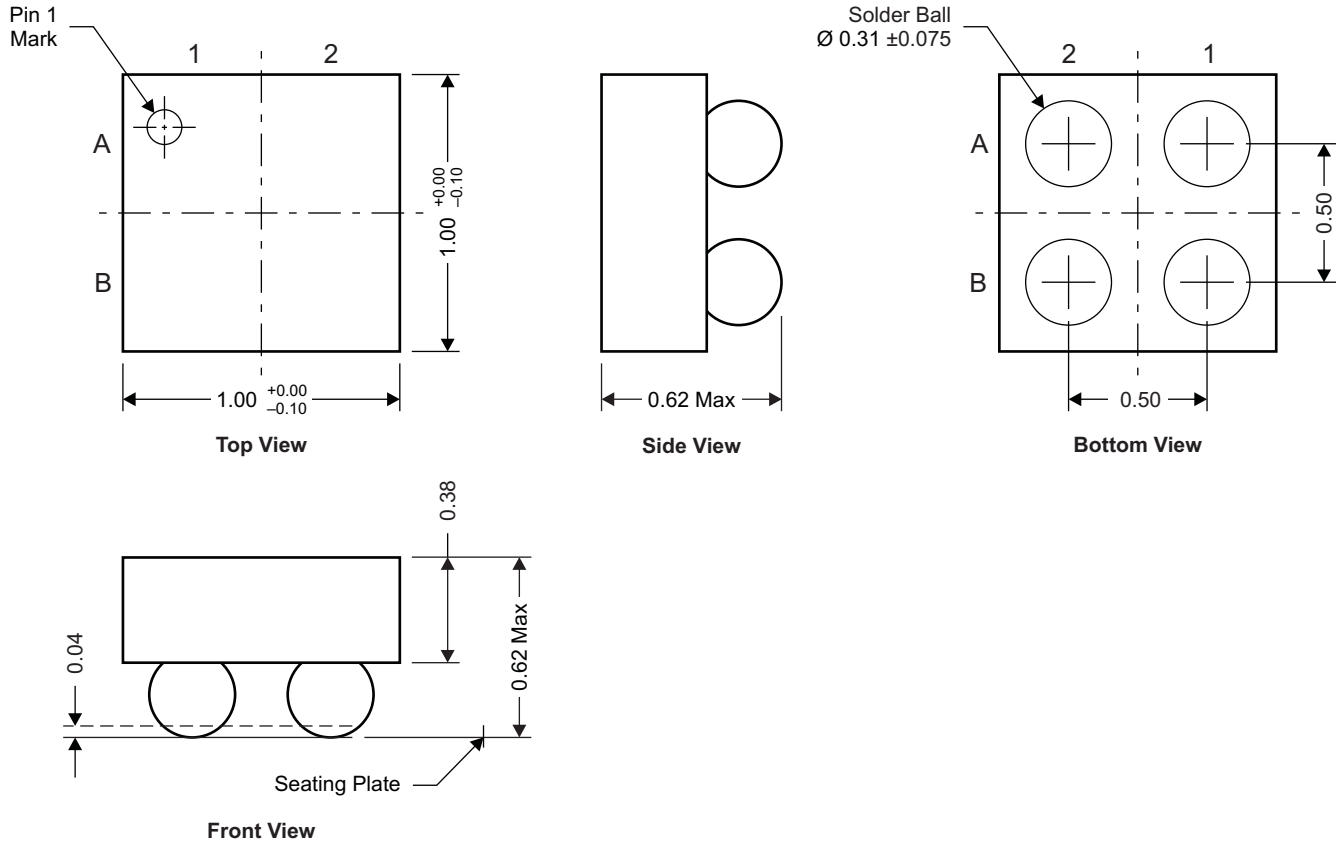


Figure 11. Maximum Drain Current vs. Temperature

MECHANICAL DATA

CSD23201W10 Package Dimensions



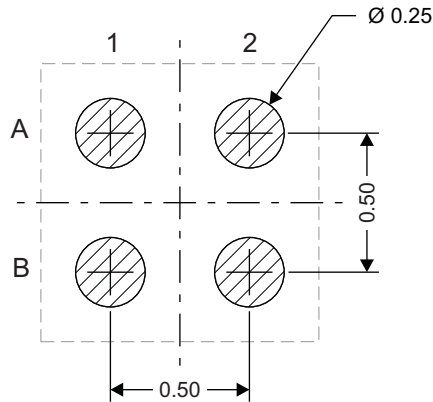
M0151-01

NOTE: All dimensions are in mm (unless otherwise specified)

Pin Configuration Table

POSITION	DESIGNATION
B1	Source
A1	Gate
A2, B2	Drain

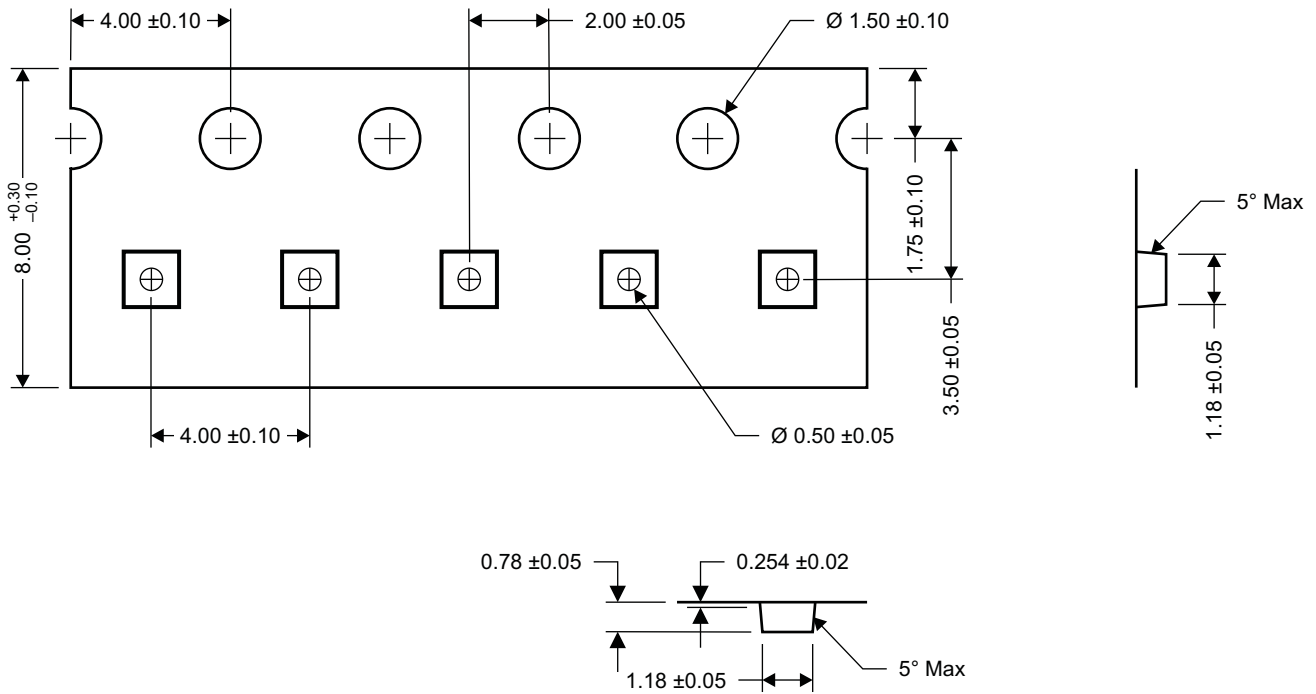
Land Pattern Recommendation



M0152-01

NOTE: All dimensions are in mm (unless otherwise specified)

Tape and Reel Information



M0153-01

NOTE: All dimensions are in mm (unless otherwise specified)

REVISION HISTORY

Changes from Original (August 2009) to Revision A	Page
Deleted the Package Marking Information section	7

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