

Dual P-Channel NexFET™ Power MOSFET

 Check for Samples: [CSD75211W1723](#)

FEATURES

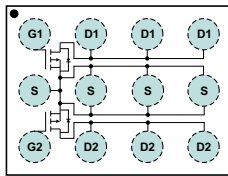
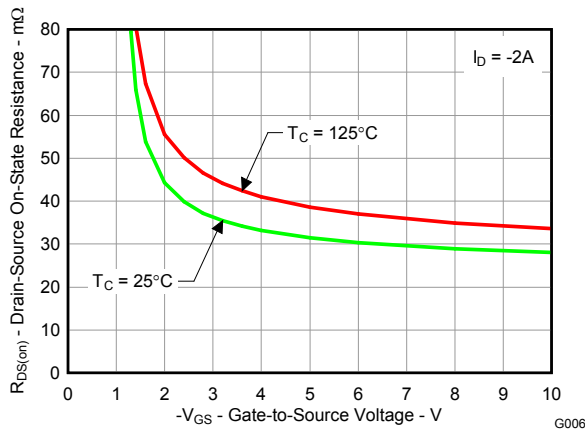
- Dual P-Ch MOSFETs
- Common Source Configuration
- Small Footprint 1.7 mm × 2.3 mm
- Ultra Low Q_g and Q_{gd}
- Pb Free
- RoHS Compliant
- Halogen Free

APPLICATIONS

- Battery Management
- Battery Protection
- DC-DC Converters

DESCRIPTION

The device has been designed to deliver the lowest on resistance and gate charge in the smallest outline possible with thermal characteristics in an ultra low profile. Low on resistance and gate charge coupled with the small footprint and low profile make the device ideal for battery operated space constrained application in load management as well as DC-DC converter applications

Top View

 $R_{DS(on)}$ vs V_{GS}


PRODUCT SUMMARY

V_{DS}	Drain to Source Voltage	-20	V
Q_g	Gate Charge Total (-4.5V)	4.5	nC
Q_{gd}	Gate Charge Gate to Drain	0.9	nC
$R_{DS(on)}$	Drain to Source On Resistance	$V_{GS} = -1.8V$	50 mΩ
		$V_{GS} = -2.5V$	39 mΩ
		$V_{GS} = -4.5V$	32 mΩ
$V_{GS(th)}$	Threshold Voltage	-0.7	V

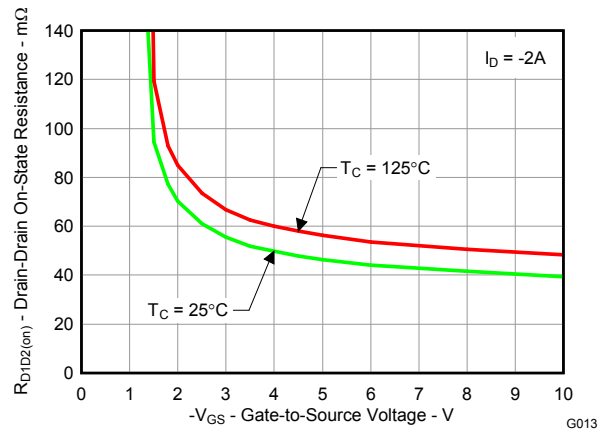
ORDERING INFORMATION

Device	Package	Media	Qty	Ship
CSD75211W1723	1.7-mm × 2.3-mm Wafer Level Package	7-Inch Reel	3000	Tape and Reel

ABSOLUTE MAXIMUM RATINGS

$T_A = 25^\circ\text{C}$ unless otherwise stated		VALUE	UNIT
V_{DS}	Drain to Source Voltage	-20	V
V_{GS}	Gate to Source Voltage	+8	V
I_D	Continuous Drain Current ⁽¹⁾ ⁽²⁾⁽³⁾	-4.5	A
	Pulsed Drain Current ⁽¹⁾ ⁽²⁾⁽³⁾		
I_G	Continupus Gate Clamp Current ⁽⁴⁾	-6	A
	Pulsed Gate Clamp Current ⁽⁴⁾		
P_D	Power Dissipation ⁽¹⁾	1.5	W
T_J, T_{STG}	Operating Junction and Storage Temperature Range	-55 to 150	$^\circ\text{C}$

- (1) May be limited by Max source current
- (2) Based on Min Cu footprint
- (3) Per MOSFET
- (4) Total for device

 $R_{D1D2(on)}$ vs V_{GS}


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These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

ELECTRICAL CHARACTERISTICS

(T_A = 25°C unless otherwise stated)

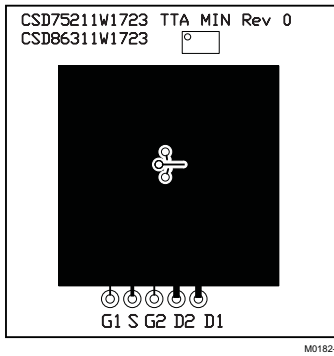
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Static Characteristics						
BV _{DSS}	Drain to Source Voltage	V _{GS} = 0V, I _D = -250μA	-20			V
I _{DSS}	Drain to Source Leakage Current	V _{GS} = 0V, V _{DS} = -16V			-1	μA
I _{GSS}	Gate to Source Leakage Current	V _{DS} = 0V, V _{GS} = ±8V			±100	nA
V _{GS(th)}	Gate to Source Threshold Voltage	V _{DS} = V _{GS} , I _D = -250μA	-0.4	-0.7	-1.1	V
R _{DS(on)}	Drain to Source On Resistance	V _{GS} = -1.8V, I _{DS} = -2A		50	70	mΩ
		V _{GS} = -2.5V, I _{DS} = -2A		39	50	mΩ
		V _{GS} = -4.5V, I _{DS} = -2A		32	40	mΩ
R _{DD(on)}	Drain to Drain On Resistance	V _{GS} = -1.8V, I _{DS} = -2A		80	110	mΩ
		V _{GS} = -2.5V, I _{DS} = -2A		61	75	mΩ
		V _{GS} = -4.5V, I _{DS} = -2A		46	55	mΩ
g _{fs}	Transconductance	V _{DS} = -10V, I _D = -2A		6.4		S
Dynamic Characteristics						
C _{ISS}	Input Capacitance	V _{GS} = 0V, V _{DS} = -10V, f = 1MHz		460	600	pF
C _{OSS}	Output Capacitance			220	290	pF
C _{RSS}	Reverse Transfer Capacitance			73	95	pF
R _G	Serialized Gate Resistance			1.6	3.2	Ω
Q _g	Gate Charge Total (-4.5V)	V _{DS} = -10V, I _D = -2A		4.5	5.9	nC
Q _{gd}	Gate Charge Gate to Drain			0.9		nC
Q _{gs}	Gate Charge Gate to Source			0.9		nC
Q _{g(th)}	Gate Charge at V _{th}			0.4		nC
Q _{OSS}	Output Charge		V _{DS} = -17V, V _{GS} = 0V		4.9	
t _{d(on)}	Turn On Delay Time	V _{DS} = -10V, V _{GS} = -4.5V, I _D = -2A, R _G = 2Ω		3.7		ns
t _r	Rise Time			4.1		ns
t _{d(off)}	Turn Off Delay Time			9.1		ns
t _f	Fall Time			1.6		ns
Diode Characteristics						
V _{SD}	Diode Forward Voltage	I _D = -2A, V _{GS} = 0V		0.7	1	V
Q _{rr}	Reverse Recovery Charge	V _{DD} = -17V, I _F = -2A, di/dt = 300A/μs		11		nC
t _{rr}	Reverse Recovery Time			19		ns

THERMAL CHARACTERISTICS

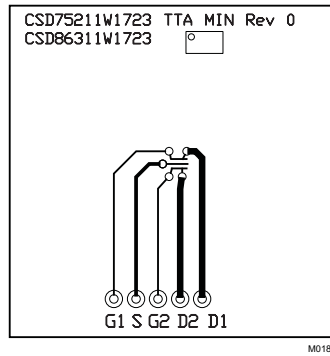
(T_A = 25°C unless otherwise stated)

PARAMETER		MIN	TYP	MAX	UNIT
R _{θJA}	Thermal Resistance Junction to Ambient (Minimum Cu area) ⁽¹⁾ ⁽²⁾			160	°C/W
R _{θJA}	Thermal Resistance Junction to Ambient (1 in ² Cu area) ⁽²⁾ ⁽³⁾			69	°C/W

- (1) Device mounted on FR4 material with minimum Cu mounting area.
- (2) Measured with both devices biased in a parallel condition.
- (3) Device mounted on FR4 material with 1 in² of 2oz. Cu.



Max $R_{\theta JA} = 69^{\circ}\text{C/W}$
when mounted on
1inch² (6.45 cm²) of
2-oz. (0.071-mm thick)
Cu.



Max $R_{\theta JA} = 160^{\circ}\text{C/W}$
when mounted on a
minimum pad area of
2-oz. (0.071-mm thick)
Cu.

TYPICAL MOSFET CHARACTERISTICS

($T_A = 25^{\circ}\text{C}$ unless otherwise stated)

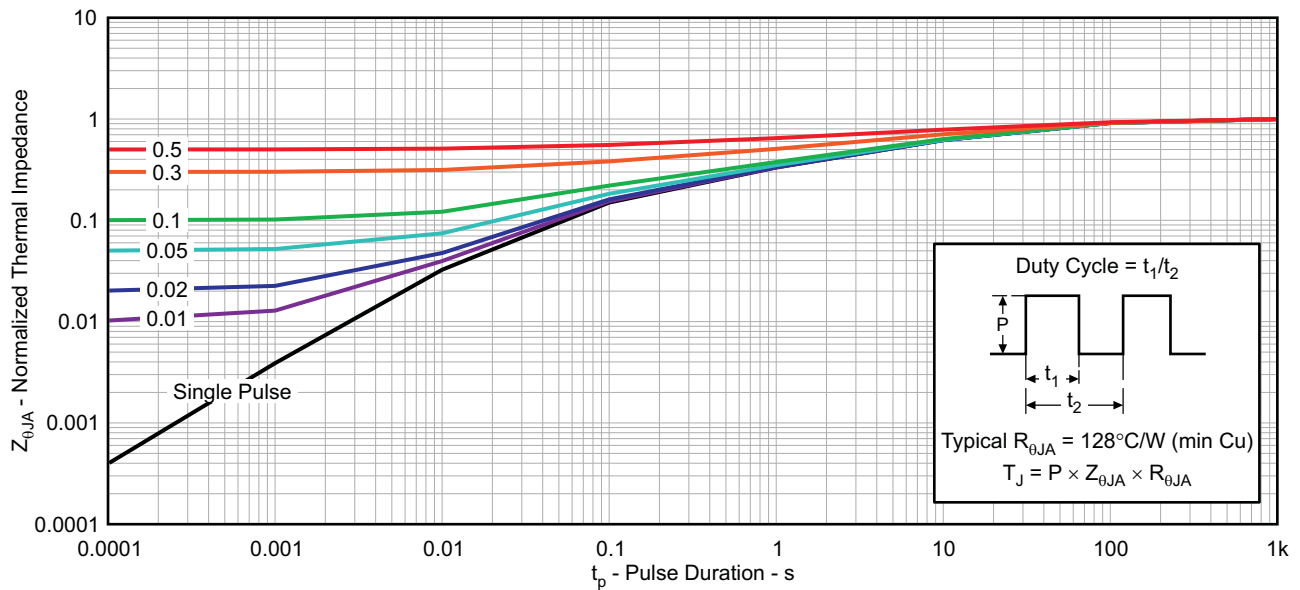


Figure 1. Transient Thermal Impedance

TYPICAL MOSFET CHARACTERISTICS (continued)

($T_A = 25^\circ\text{C}$ unless otherwise stated)

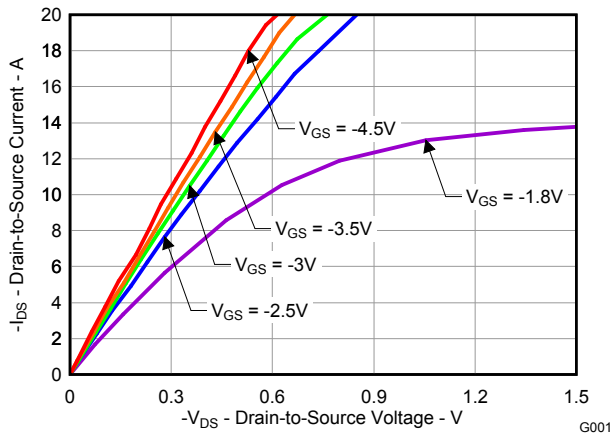


Figure 2. Saturation Characteristics

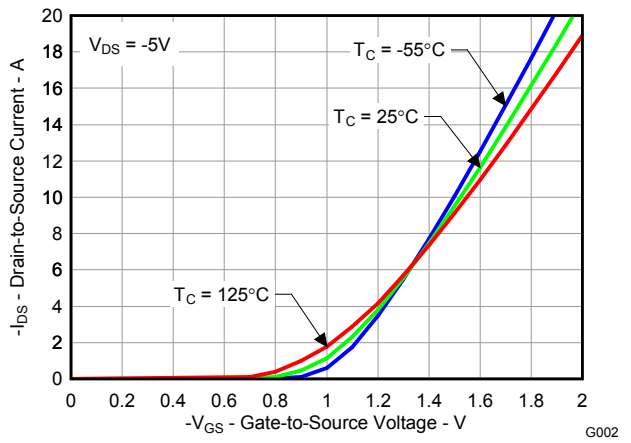


Figure 3. Transfer Characteristics

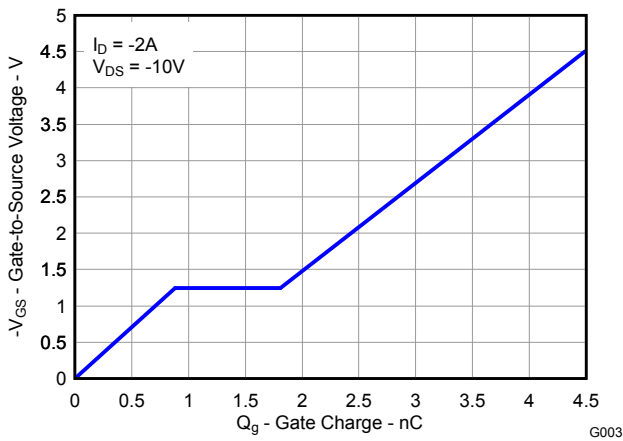


Figure 4. Gate Charge

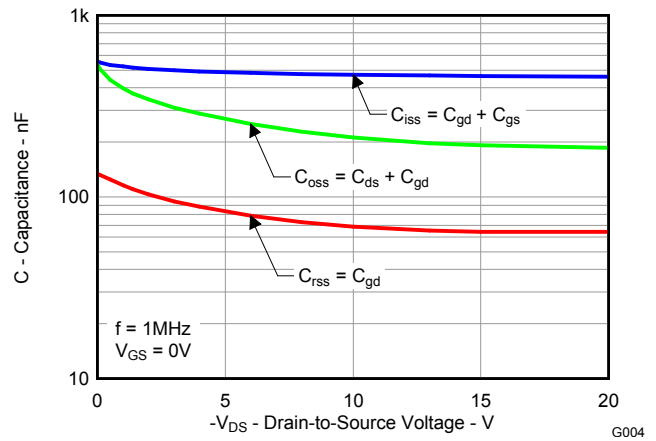


Figure 5. Capacitance

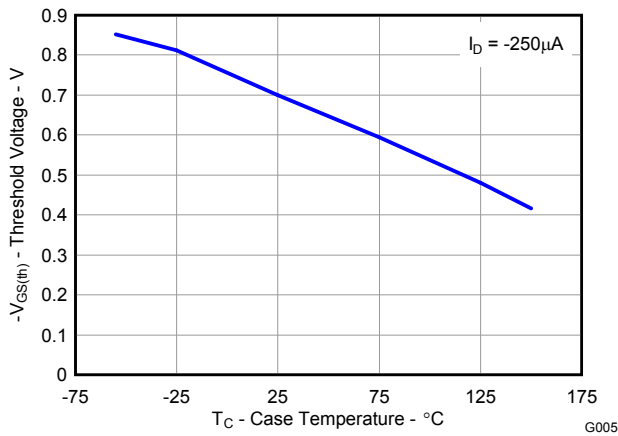


Figure 6. Threshold Voltage vs. Temperature

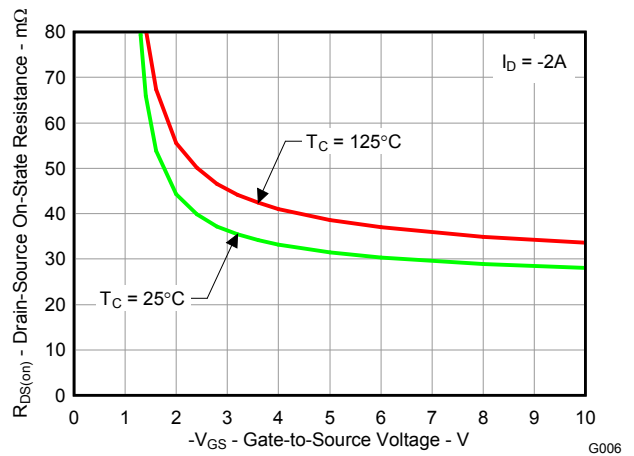


Figure 7. $R_{DS(on)}$ vs. Gate-to-Source Voltage

TYPICAL MOSFET CHARACTERISTICS (continued)

($T_A = 25^\circ\text{C}$ unless otherwise stated)

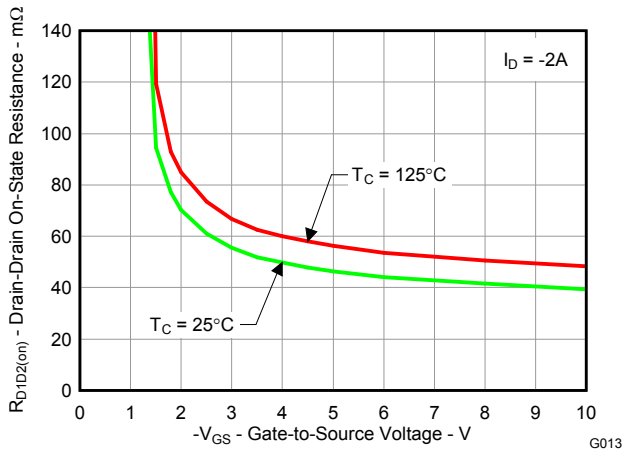


Figure 8. $R_{D1D2(on)}$ vs. Gate-to-Source Voltage

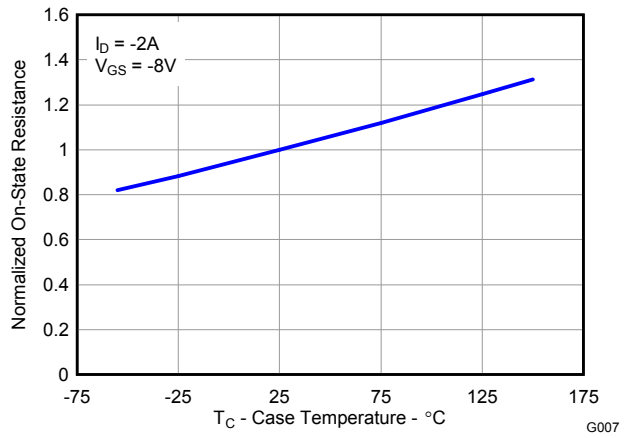


Figure 9. Normalized On-State Resistance vs. Temperature

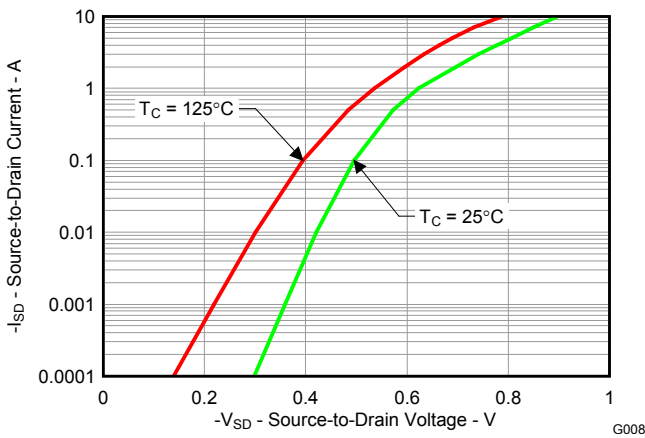


Figure 10. Typical Diode Forward Voltage

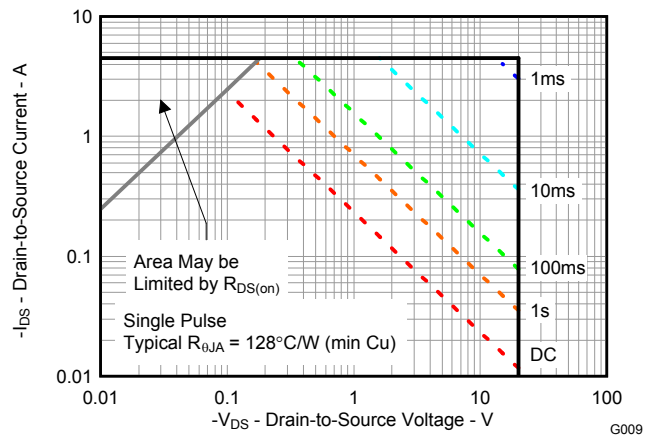


Figure 11. Maximum Safe Operating Area

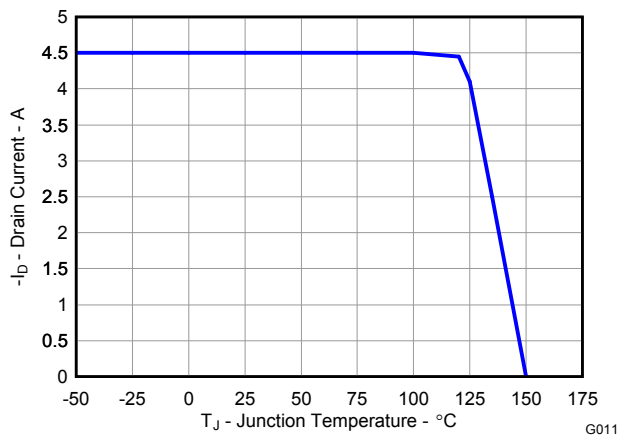
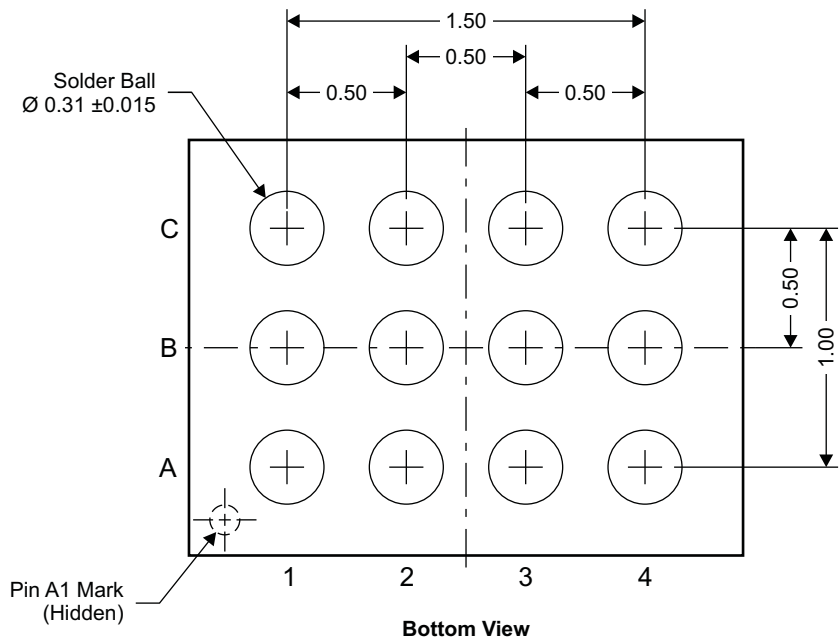
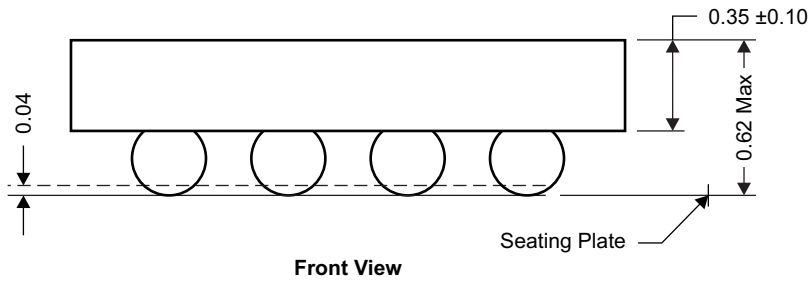
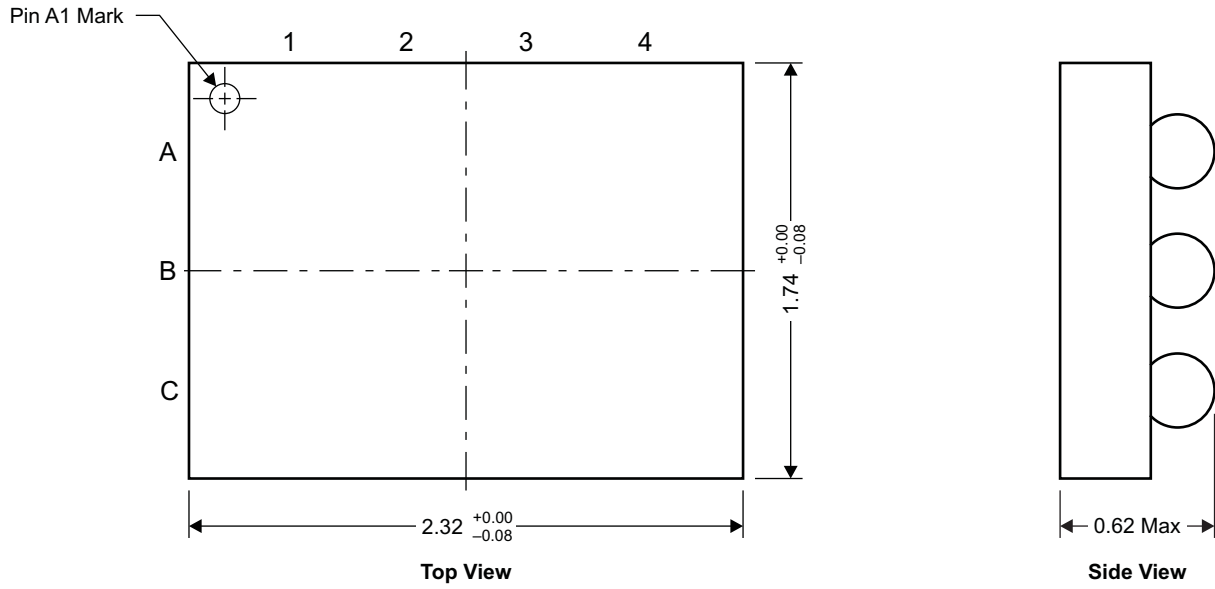


Figure 12. Maximum Drain Current vs. Temperature

MECHANICAL DATA

CSD75211W1723 Package Dimensions

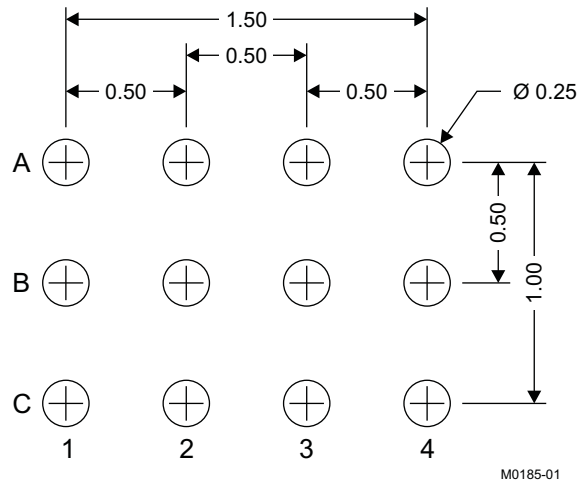


Pinout	
Position	Designation
A2, A3, A4	Drain 1
C2, C3, C4	Drain 2
A1	Gate 1
C1	Gate 2
B1, B2, B3, B4	Source

NOTE: All dimensions are in mm (unless otherwise specified)

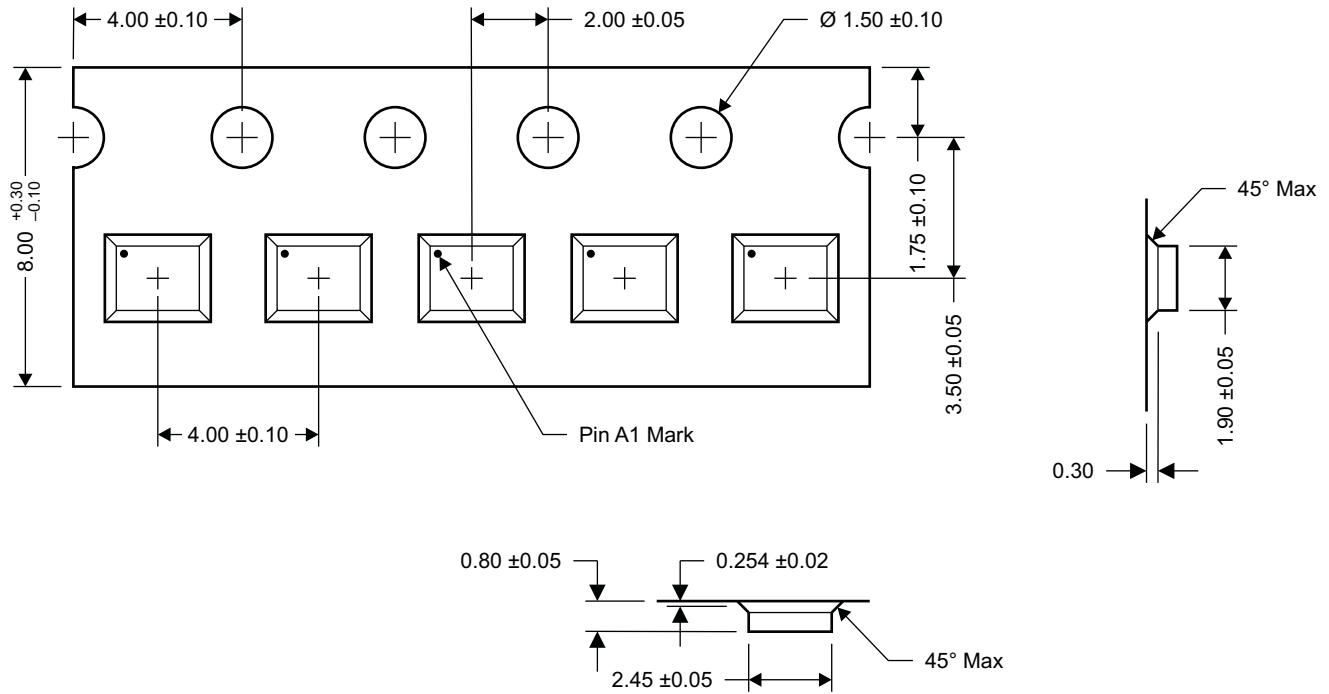
M0184-01

Land Pattern Recommendation



NOTE: All dimensions are in mm (unless otherwise specified)

Tape and Reel Information



NOTE: All dimensions are in mm (unless otherwise specified)

PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/ Ball Finish	MSL Peak Temp ⁽³⁾	Samples (Requires Login)
CSD75211W1723	ACTIVE	DSBGA	YZG	12	3000	TBD	Call TI	Call TI	Purchase Samples

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSELETE: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

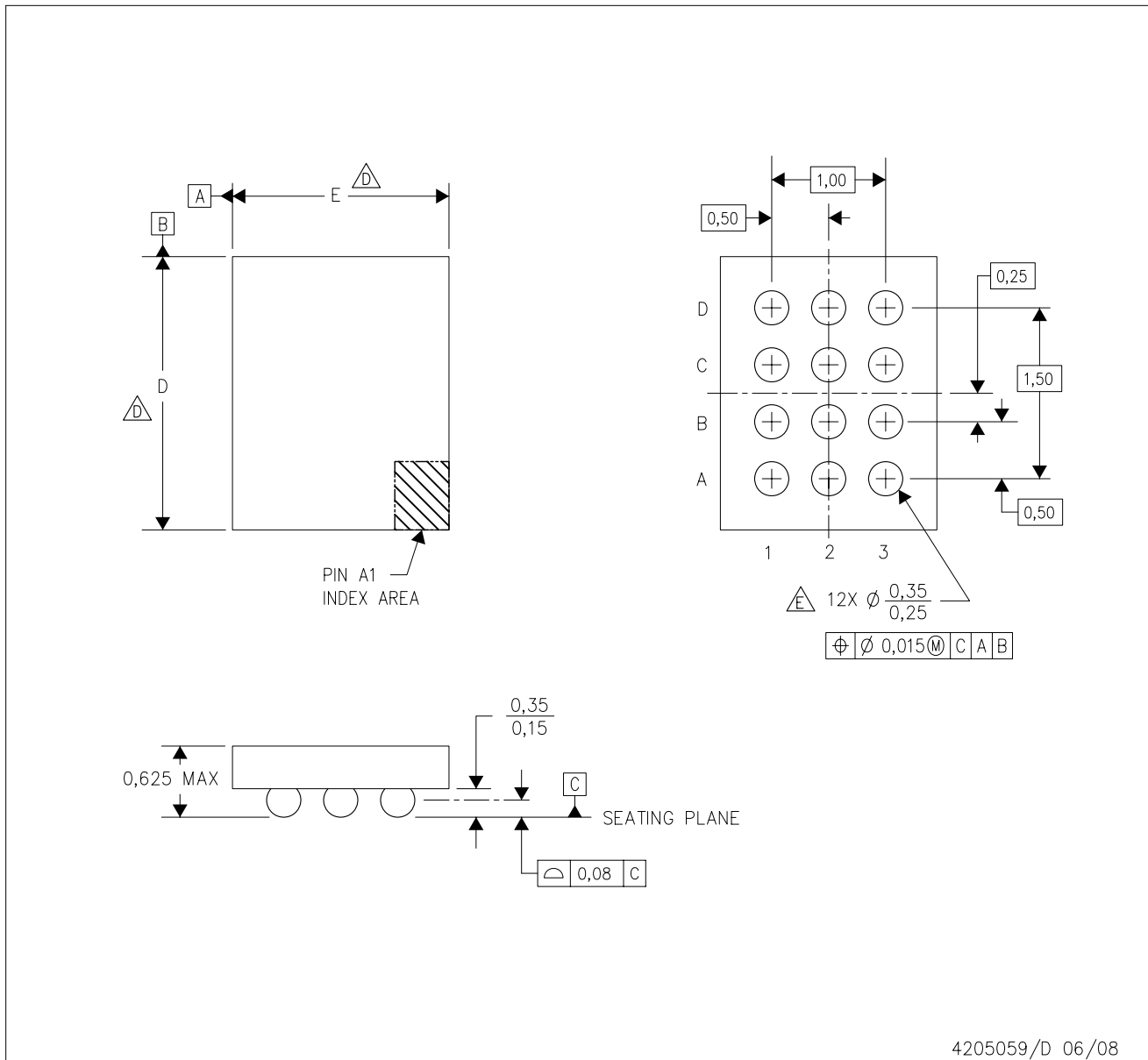
⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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YZG (R-XBGA-N12)

DIE-SIZE BALL GRID ARRAY



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. NanoFree™ package configuration.
 - $\triangle D$ Devices in YZG package can have dimension D ranging from 1.94 to 2.65 mm and dimension E ranging from 1.44 to 2.15 mm. To determine the exact package size of a particular device, refer to the device datasheet or contact a local TI representative.
 - E. Reference Product Data Sheet for array population.
4 x 3 matrix pattern is shown for illustration only.
 - F. This package contains lead-free balls.
Refer to YEG (Drawing #4204182) for tin-lead (SnPb) balls.

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