

SLPS212A - AUGUST 2009 - REVISED NOVEMBER 2009

# P-Channel NexFET™ Power MOSFET

Check for Samples: CSD75301W1015

#### **FEATURES**

- Dual P-Ch MOSFETs
- Common Source Configuration
- Small Footprint 1mm × 1.5mm
- Low Profile 0.62mm
- Ultra Low Qg and Qgd
- Pb Free / RoHS Compliant
- Halogen Free

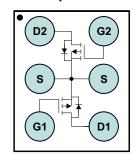
### **APPLICATIONS**

- Battery Management
- Load Switch
- Battery Protection

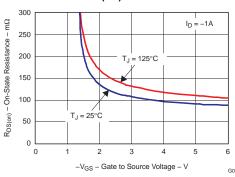
### **DESCRIPTION**

The device has been designed to deliver the lowest on resistance and gate charge in the smallest outline possible with excellent thermal characteristics in an ultra low profile.

### **Top View**



### R<sub>DS(ON)</sub> vs V<sub>GS</sub>



#### **Table 1. PRODUCT SUMMARY**

(Per MOSFET unless otherwise stated)							
$V_{DS}$	Drain to Source Voltage -20						
$Q_g$	Gate Charge Total (4.5V) 1.5						
$Q_{gd}$	Gate Charge Gate to Drain	0.3	nC				
		$V_{GS} = -1.8V$	150	mΩ			
R <sub>DS(on)</sub>	Drain to Source On Resistance	V <sub>GS</sub> = -2.5V 105		mΩ			
		V <sub>GS</sub> = -4.5V 80		mΩ			
V <sub>GS(th)</sub>	Voltage threshold	-0.7		V			

### **ORDERING INFORMATION**

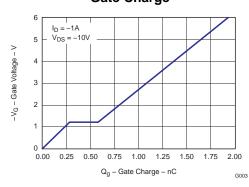
Device	Package	Media	Qty	Ship
CSD75301W1015	1 x 1.5 Wafer Level Package	7-inch reel	3000	Tape and Reel

### **ABSOLUTE MAXIMUM RATINGS**

T <sub>A</sub> = 2	5°C unless otherwise stated	VALUE	UNIT
$V_{\text{DS}}$	Drain to Source Voltage	-20	V
$V_{GS}$	Gate to Source Voltage	±8	V
I <sub>D</sub>	Continuous Drain Current, T <sub>C</sub> = 25°C <sup>(1)</sup> (2)	-1.2	Α
I <sub>DM</sub>	Pulsed Drain Current, T <sub>A</sub> = 25°C <sup>(1)</sup> (2) (3)	-17.5	Α
P <sub>D</sub>	Power Dissipation <sup>(1)</sup> (2)	0.8	W
T <sub>J</sub> , T <sub>STG</sub>	Operating Junction and Storage Temperature Range	-55 to 150	°C

- (1) Per device, both devices in conduction.
- (2)  $R_{\theta JA} = 74^{\circ}\text{C/W} \text{ on } 1\text{in}^2 \text{ Cu (2 oz.) on } 0.060^{\circ}\text{ thick FR4 PCB.}$
- (3) Pulse width ≤300µs, duty cycle ≤2%

### **Gate Charge**



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.



### **ELECTRICAL CHARACTERISTICS**

(T<sub>A</sub> = 25°C unless otherwise stated) (Per MOSFET unless otherwise stated)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Static Cl	haracteristics		,		'	
BV <sub>DSS</sub>	Drain to Source Voltage	$V_{GS} = 0V, I_D = -250\mu A$	-20			V
I <sub>DSS</sub>	Drain to Source Leakage Current	V <sub>GS</sub> = 0V, V <sub>DS</sub> = -16V			-1	μA
I <sub>GSS</sub>	Gate to Source Leakage Current	$V_{DS} = 0V, V_{GS} = -8V$			-100	nA
V <sub>GS(th)</sub>	Gate to Source Threshold Voltage	$V_{DS} = V_{GS}, I_{D} = -250 \mu A$	-0.4	-0.7	-1.0	V
		$V_{GS} = -1.8V, I_D = -1A$		150	190	mΩ
R <sub>DS(on)</sub>	Drain to Source On Resistance	$V_{GS} = -2.5V, I_D = -1A$		105	135	mΩ
		$V_{GS} = -4.5V, I_D = -1A$		80	100	mΩ
9 <sub>fs</sub>	Transconductance	$V_{DS} = -10V, I_{D} = -1A$		5.2		S
Dynamic	Characteristics		,		'	
C <sub>ISS</sub>	Input Capacitance			150	195	pF
Coss	Output Capacitance	$V_{GS} = 0V, V_{DS} = -10V, f = 1MHz$		67	87	pF
C <sub>RSS</sub>	Reverse Transfer Capacitance			24	31	pF
Qg	Gate Charge Total (-4.5V)			1.5	2.1	nC
Q <sub>gd</sub>	Gate Charge Gate to Drain	10/1		0.3		nC
Q <sub>gs</sub>	Gate Charge Gate to Source	$V_{DS} = -10V, I_{D} = -1A$		0.28		nC
Q <sub>g(th)</sub>	Gate Charge at Vth			0.12		nC
Q <sub>OSS</sub>	Output Charge	$V_{DS} = -9.5V, V_{GS} = 0V$		1.1		nC
t <sub>d(on)</sub>	Turn On Delay Time			3		ns
t <sub>r</sub>	Rise Time	$V_{DS} = -10V$ , $V_{GS} = -4.5V$ , $I_{D} = -1A$		1.7		ns
t <sub>d(off)</sub>	Turn Off Delay Time	$R_G = 30\Omega$		38		ns
t <sub>f</sub>	Fall Time			16		ns
Diode C	haracteristics		•		'	
V <sub>SD</sub>	Diode Forward Voltage	$I_S = -1A$ , $V_{GS} = 0V$		-0.81	-1	V
Q <sub>rr</sub>	Reverse Recovery Charge	$V_{dd} = -9.5V$ , $I_F = -1A$ , $di/dt = 200A/\mu s$		2		nC
t <sub>rr</sub>	Reverse Recovery Time	$V_{dd} = -9.5V$ , $I_F = -1A$ , $di/dt = 200A/\mu s$		7.5		ns

### THERMAL CHARACTERISTICS

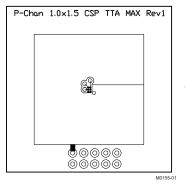
 $(T_A = 25^{\circ}C \text{ unless otherwise stated})$ 

	PARAMETER	MIN	TYP	MAX	UNIT
R <sub>0JC</sub>	Thermal Resistance Junction to Ambient <sup>(1)</sup> (2)			136	°C/W
R <sub>0JA</sub>	Thermal Resistance Junction to Ambient <sup>(2)</sup> (3)			93	°C/W

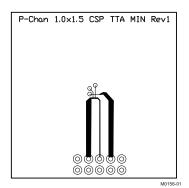
F oc of Foller Link(s 0 SD7530 W1 1.

- (1) Device mounted on FR4 material with Minimum Cu mounting area.
- (2) Measured with both devices biased in a parallel condition.
- (3) Device mounted on FR4 material with 1in<sup>2</sup> of 2 oz Cu.





Max  $R_{\theta JA} = 93$ °C/W when mounted on 1inch<sup>2</sup> of 2 oz. Cu.



Max  $R_{\theta JA} = 136^{\circ} C/W$  when mounted on minimum pad area of 2 oz. Cu.

### TYPICAL MOSFET CHARACTERISTICS

 $(T_A = 25^{\circ}C \text{ unless otherwise stated})$ 

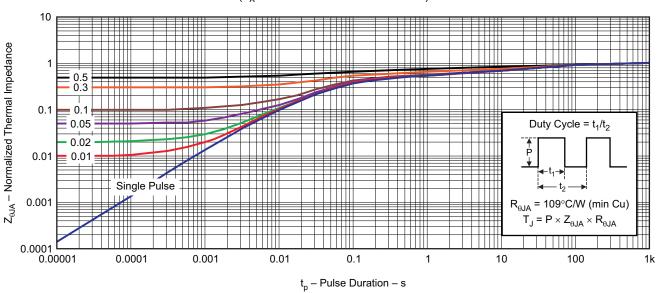


Figure 1. Transient Thermal Impedance



# **TYPICAL MOSFET CHARACTERISTICS (continued)**

F oc of Folder Link(s (SD7530 W1 1:

(T<sub>A</sub> = 25°C unless otherwise stated)

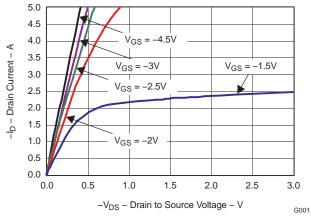


Figure 2. Saturation Characteristics

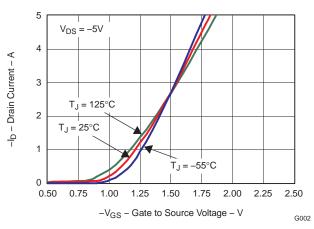


Figure 3. Transfer Characteristics

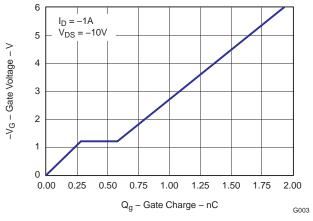


Figure 4. Gate Charge

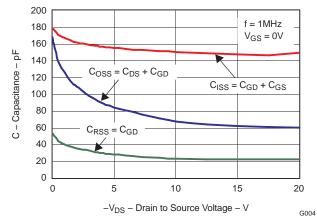


Figure 5. Capacitance



# **TYPICAL MOSFET CHARACTERISTICS (continued)**

(T<sub>A</sub> = 25°C unless otherwise stated)

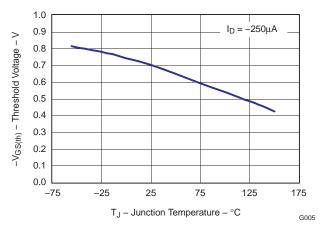


Figure 6. Threshold Voltage vs. Temperature

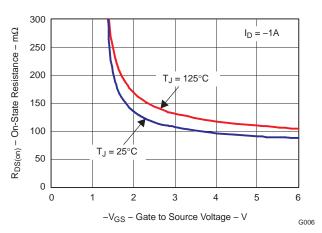


Figure 7. On Resistance vs. Gate Voltage

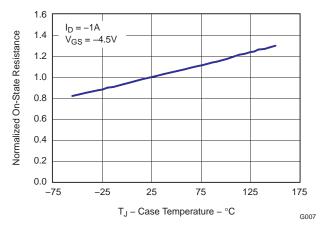


Figure 8. On Resistance vs. Temperature

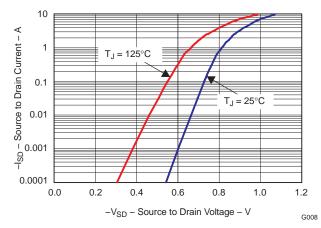


Figure 9. Typical Diode Forward Voltage



# **TYPICAL MOSFET CHARACTERISTICS (continued)**

 $(T_A = 25^{\circ}C \text{ unless otherwise stated})$ 

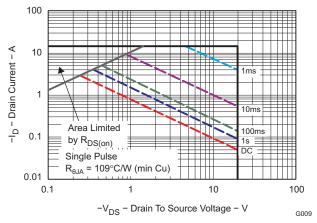


Figure 10. Maximum Safe Operating Area

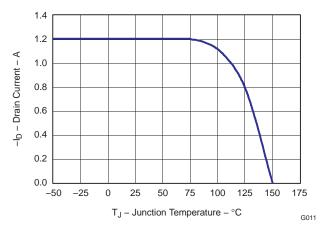
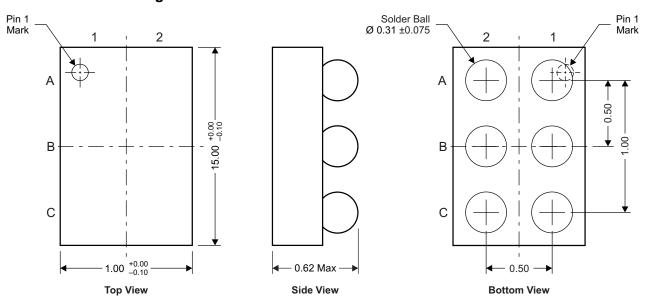


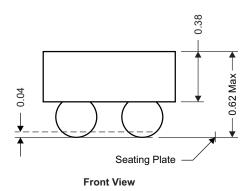
Figure 11. Maximum Drain Current vs. Temperature



### **MECHANICAL DATA**

# CSD75301W1015 Package Dimensions





M0157-01

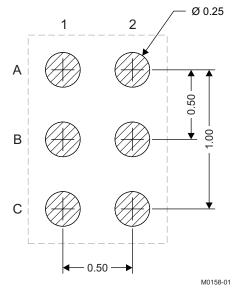
NOTE: All dimensions are in mm (unless othersse specified)

### **Pinout**

POSITION	DESIGNATION
B1, B2	Source
C1	Gate1
C2	Drain1
A2	Gate2
A1	Drain2

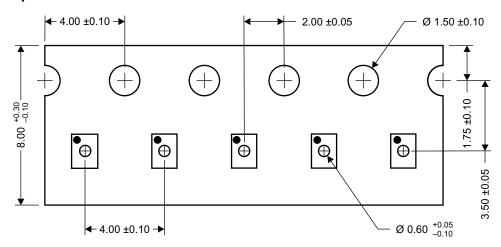


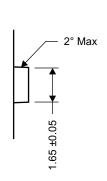
### **Land Pattern Recommendation**

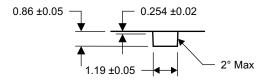


NOTE: All dimensions are in mm (unless othersse specified)

# **Tape and Reel Information**







M0159-01

NOTE: All dimensions are in mm (unless othersse specified)

www.ti.com

### **Package Marking Information**

#### Location

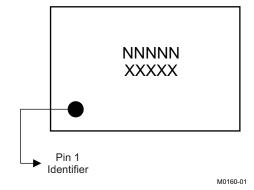
1st Line

Product Code = NNNNN, First 5 digits after

CSD (Fixed Text)

2nd Line

XXXXX = Last 5 digits of lot number



### **REVISION HISTORY**

### Changes from Original (August 2009) to Revision A

**Page** 

Changed location of the Pin 1 indicator dot in the pin out illustration.



#### PACKAGE OPTION ADDENDUM

www.ti.com 21-Dec-2009

#### **PACKAGING INFORMATION**

Orderable Device	Status <sup>(1)</sup>	Package Type	Package Drawing	Pins P	Package Qty	e Eco Plan <sup>(2)</sup>	Lead/Ball Finish	MSL Peak Temp <sup>(3)</sup>
CSD75301W1015	ACTIVE	DSBGA	YZC	6	3000	Green (RoHS & no Sb/Br)	Call TI	Level-1-260C-UNLIM

<sup>(1)</sup> The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

**Pb-Free** (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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