- **Function, Pinout, and Drive Compatible With FCT, F Logic, and AM29818**
- **Reduced V_{OH} (Typically = 3.3 V) Version of Equivalent FCT Functions**
- **Edge-Rate Control Circuitry for Significantly Improved Noise Characteristics**
- **I_{off} Supports Partial-Power-Down Mode Operation**
- **Matched Rise and Fall Times**
- **Fully Compatible With TTL Input and Output Logic Levels**
- **8-Bit Pipeline and Shadow Register**
- **ESD Protection Exceeds JESD 22**
  - **2000-V Human-Body Model (A114-A)**
  - **200-V Machine Model (A115-A)**
  - **1000-V Charged-Device Model (C101)**
- **CY29FCT818CT**
  - **64-mA Output Sink Current**
  - **32-mA Output Source Current**
- **CY29FCT818ATDMB**
  - **20-mA Output Sink Current**
  - **3-mA Output Source Current**
- **3-State Outputs**

D, P, Q, OR SO PACKAGE
(TOP VIEW)

$\overline{OE}$	1	24	V_{CC}
DCLK	2	23	MODE
D_0	3	22	Y_0
D_1	4	21	Y_1
D_2	5	20	Y_2
D_3	6	19	Y_3
D_4	7	18	Y_4
D_5	8	17	Y_5
D_6	9	16	Y_6
D_7	10	15	Y_7
SDI	11	14	SDO
GND	12	13	PCLK
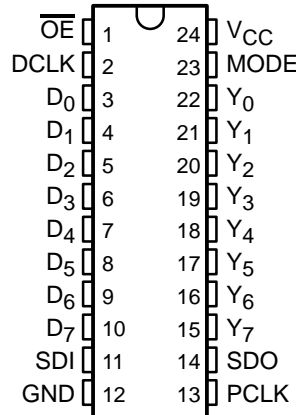
description

The CY29FCT818T contains a high-speed 8-bit general-purpose data pipeline register and a high-speed 8-bit shadow register. The general-purpose register can be used in an 8-bit-wide data path for a normal system application. The shadow register is designed for applications such as diagnostics in sequential circuits, where it is desirable to load known data at a specific location in the circuit and to read the data at that location.

The shadow register can load data from the output of the device, and can be used as a right-shift register with bit-serial input (SDI) and output (SDO), using DCLK. The data register input is multiplexed to enable loading from the shadow register or from the data input pins, using PCLK. Data can be loaded simultaneously from the shadow register to the pipeline register, and from the pipeline register to the shadow register, provided setup-time and hold-time requirements are satisfied, with respect to the two independent clock inputs.

In a typical application, the general-purpose register in this device replaces an 8-bit data register in the normal data path of a system. The shadow register is placed in an auxiliary bit-serial loop that is used for diagnostics. During diagnostic operation, data is shifted serially into the shadow register, then transferred to the general-purpose register to load a known value into the data path. To read the contents at that point in the data path, the data is transferred from the data register into the shadow register, then shifted serially in the auxiliary diagnostic loop to make it accessible to the diagnostics controller. This data then is compared with the expected value to diagnose faulty operation of the sequential circuit.

This device is fully specified for partial-power-down applications using I_{off}. The I_{off} circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

TEXAS INSTRUMENTS

POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

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ORDERING INFORMATION

T$_A$	PACKAGE†		SPEED (ns)	ORDERABLE PART NUMBER	TOP-SIDE MARKING
−40°C to 85°C	DIP – P	Tube	6	CY29FCT818CTPC	CY29FCT818CTPC
	QSOP – Q	Tape and reel	6	CY29FCT818CTQCT	29FCT818C
	SOIC – SO	Tube	6	CY29FCT818CTSOC	29FCT818C
		Tape and reel	6	CY29FCT818CTSOCT	
−55°C to 125°C	CDIP – D	Tube	12	CY29FCT818ATDMB	

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

FUNCTION TABLE

INPUTS				OUTPUT SDO	SHADOW REGISTER	PIPELINE REGISTER	OPERATION
MODE	SDI	DCLK	PCLK				
L	X	↑	X	S$_7$	S$_0$←SDI S_i←S$_{i-1}$	NA	Serial shift; D$_7$–D$_0$ output disabled
L	X	X	↑	S$_7$	NA	P$_i$←D$_i$	Load pipeline register from data input
H	L	↑	X	L	S$_i$←Y$_i$	NA	Load shadow register from Y output
H	H	↑	X	H	Hold	NA	Hold shadow register; D$_7$–D$_0$ output enabled
H	X	X	↑	SDI	NA	P$_i$←S$_i$	Load pipeline register from shadow register

H = High logic level, L = Low logic level, X = Don't care, ↑ Low-to-high transition, ← = Transfer direction, NA = Not applicable

TEXAS
INSTRUMENTS
POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

logic diagram
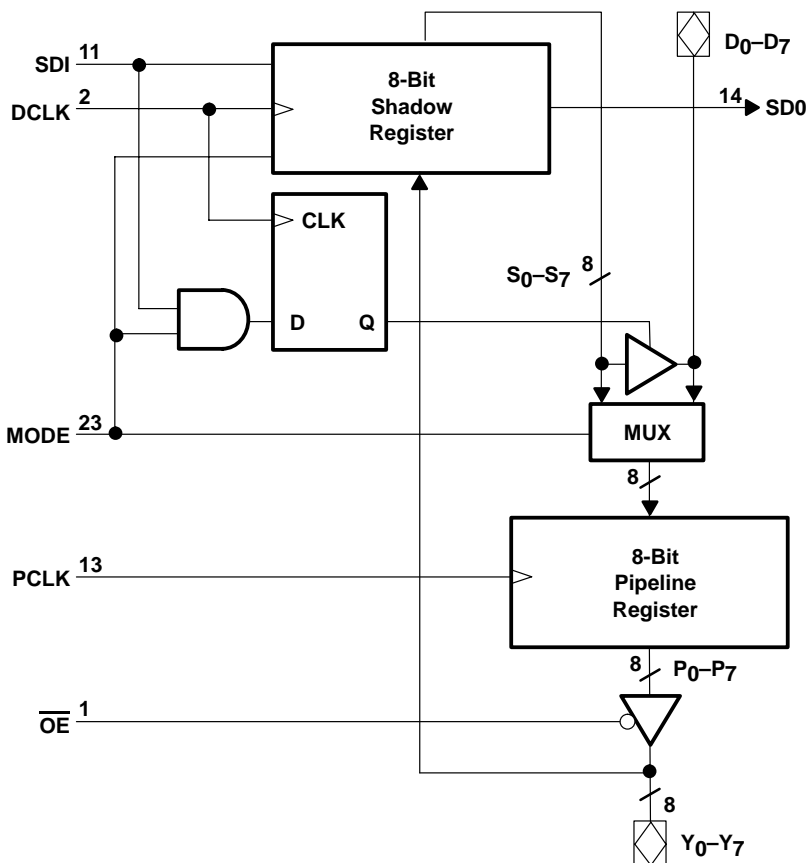
absolute maximum rating over operating free-air temperature range (unless otherwise noted)†

Supply voltage range to ground potential	−0.5 V to 7 V
DC input voltage range	−0.5 V to 7 V
DC output voltage range	−0.5 V to 7 V
DC output current (maximum sink current/pin)	120 mA
Package thermal impedance, θ_{JA} (see Note 1): P package	67°C/W
(see Note 2): Q package	61°C/W
(see Note 2): SO package	46°C/W
Ambient temperature range with power applied, T_A	−65°C to 135°C
Storage temperature range, T_{stg}	−65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1.   The package thermal impedance is calculated in accordance with JESD 51-3.
        2.   The package thermal impedance is calculated in accordance with JESD 51-7.

CY29FCT818T
DIAGNOSTIC SCAN REGISTER
WITH 3-STATE OUTPUTS
SCCS012B – MAY 1994 – REVISED NOVEMBER 2001

recommended operating conditions (see Note 3)

		CY29FCT818ATDMB			CY29FCT818T			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
I_{OH}	High-level output current			−3			−32	mA
I_{OL}	Low-level output current			20			64	mA
T_A	Operating free-air temperature	−55		125	−40		85	°C

NOTE 3: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		CY29FCT818ATDMB			CY29FCT818T			UNIT
			MIN	TYP[†]	MAX	MIN	TYP[†]	MAX	
V_{IK}	V_{CC} = 4.5 V,	I_{IN} = −18 mA		−0.7	−1.2				V
	V_{CC} = 4.75 V,	I_{IN} = −18 mA					−0.7	−1.2	
V_{OH}	V_{CC} = 4.5 V,	I_{OH} = −3 mA	2.4	3.3					V
	V_{CC} = 4.75 V	I_{OH} = −32 mA				2			
		I_{OH} = −15 mA				2.4	3.3		
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 20 mA		0.3	0.55				V
	V_{CC} = 4.75 V,	I_{OL} = 64 mA					0.3	0.55	
V_{hys}	All inputs			0.2			0.2		V
I_I	V_{CC} = 5.5 V,	V_{IN} = V_{CC}			5				μA
	V_{CC} = 5.25 V,	V_{IN} = V_{CC}						5	
I_{IH}	V_{CC} = 5.5 V,	V_{IN} = 2.7 V			±1				μA
	V_{CC} = 5.25 V,	V_{IN} = 2.7 V						±1	
I_{IL}	V_{CC} = 5.5 V,	V_{IN} = 0.5 V			±1				μA
	V_{CC} = 5.25 V,	V_{IN} = 0.5 V						±1	
I_{OZH}	V_{CC} = 5.5 V,	V_{OUT} = 2.7 V			10				μA
	V_{CC} = 5.25 V,	V_{OUT} = 2.7 V						10	
I_{OZL}	V_{CC} = 5.5 V,	V_{OUT} = 0.5 V			−10				μA
	V_{CC} = 5.25 V,	V_{OUT} = 0.5 V						−10	
I_{OS}[‡]	V_{CC} = 5.5 V,	V_{OUT} = 0 V	−60	−120	−225				mA
	V_{CC} = 5.25 V,	V_{OUT} = 0 V				−60	−120	−225	
I_{off}	V_{CC} = 0 V,	V_{OUT} = 4.5 V			±1			±1	μA
I_{CC}	V_{CC} = 5.5 V, $V_{IN} \leq$ 0.2 V,	$V_{IN} \geq V_{CC}$ − 0.2 V		0.2	1.5				mA
	V_{CC} = 5.25 V, $V_{IN} \leq$ 0.2 V,	$V_{IN} \geq V_{CC}$ − 0.2 V					0.2	1.5	
ΔI_{CC}	V_{CC} = 5.5 V, V_{IN} = 3.4 V[§], f_1 = 0, Outputs open		0.5	2				mA
	V_{CC} = 5.25 V, V_{IN} = 3.4 V[§], f_1 = 0, Outputs open					0.5	2	

[†] Typical values are at V_{CC} = 5 V, T_A = 25°C.

[‡] Not more than one output should be shorted at a time. Duration of short should not exceed one second. The use of high-speed test apparatus and/or sample-and-hold techniques are preferable to minimize internal chip heating and more accurately reflect operational values. Otherwise, prolonged shorting of a high output can raise the chip temperature well above normal and cause invalid readings in other parametric tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

[§] Per TTL-driven input (V_{IN} = 3.4 V); all other inputs at V_{CC} or GND

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted) (continued)

PARAMETER	TEST CONDITIONS			CY29FCT818ATDMB			CY29FCT818T			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
I_{CCD}¶	V_{CC} = 5.5 V, Outputs open, One input switching at 50% duty cycle, $\overline{OE}$ = GND, $V_{IN} \leq 0.2$ V or $V_{IN} \geq V_{CC} - 0.2$ V					0.25				mA/ MHz
	V_{CC} = 5.25 V, Outputs open, One input switching at 50% duty cycle, $\overline{OE}$ = GND, $V_{IN} \leq 0.2$ V or $V_{IN} \geq V_{CC} - 0.2$ V								0.25	
I_C#	V_{CC} = 5.5 V, Outputs open, f_0 = 10 MHz, $\overline{OE}$ = GND	One bit switching at f_1 = 5 MHz at 50% duty cycle	$V_{IN} \leq 0.2$ V or $V_{IN} \geq V_{CC} - 0.2$ V			5.3				mA
			V_{IN} = 3.4 V or GND			7.3				
		Eight bits and four controls switching at f_1 = 5 MHz at 50% duty cycle	$V_{IN} \leq 0.2$ V or $V_{IN} \geq V_{CC} - 0.2$ V			17.8‖				
			V_{IN} = 3.4 V or GND			30.8‖				
	V_{CC} = 5.25 V, Outputs open, f_0 = 10 MHz, $\overline{OE}$ = GND	One bit switching at f_1 = 5 MHz at 50% duty cycle	$V_{IN} \leq 0.2$ V or $V_{IN} \geq V_{CC} - 0.2$ V						5.3	
			V_{IN} = 3.4 V or GND						7.3	
		Eight bits and four controls switching at f_1 = 5 MHz at 50% duty cycle	$V_{IN} \leq 0.2$ V or $V_{IN} \geq V_{CC} - 0.2$ V						17.8‖	
			V_{IN} = 3.4 V or GND						30.8‖	
C_i				5		10	5		10	pF
C_o				9		12	9		12	pF

† Typical values are at V_{CC} = 5 V, T_A = 25°C.

¶ This parameter is derived for use in total power-supply calculations.

I_C $= I_{CC} + \Delta I_{CC} \times D_H \times N_T + I_{CCD} (f_0/2 + f_1 \times N_1)$

  Where:

  I_C = Total supply current

  I_{CC} = Power-supply current with CMOS input levels

  ΔI_{CC} = Power-supply current for a TTL high input (V_{IN} = 3.4 V)

  D_H = Duty cycle for TTL inputs high

  N_T = Number of TTL inputs at D_H

  I_{CCD} = Dynamic current caused by an input transition pair (HLH or LHL)

  f_0 = Clock frequency for registered devices, otherwise zero

  f_1 = Input signal frequency

  N_1 = Number of inputs changing at f_1

  All currents are in milliamperes and all frequencies are in megahertz.

‖ Values for these conditions are examples of the I_{CC} formula.

CY29FCT818T
DIAGNOSTIC SCAN REGISTER
WITH 3-STATE OUTPUTS
SCCS012B – MAY 1994 – REVISED NOVEMBER 2001

timing requirements over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)
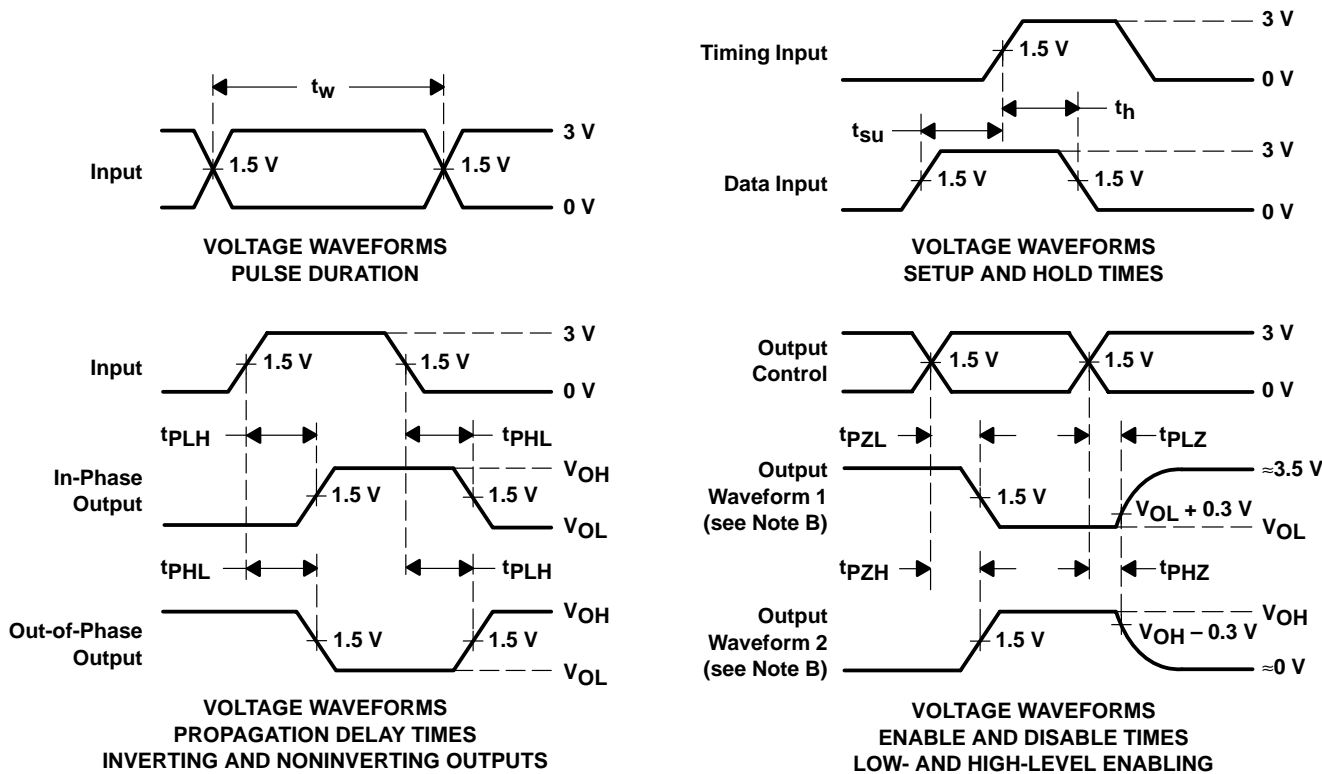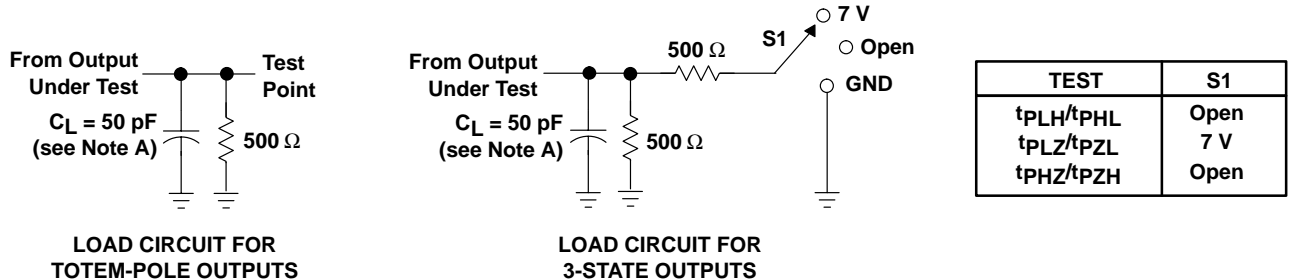
PARAMETER			CY29FCT818AT MIN	CY29FCT818AT MAX	CY29FCT818CT MIN	CY29FCT818CT MAX	UNIT
t_W	Pulse width	PCLK high and low	15		5		ns
		DCLK high and low	25		5		
t_{su}	Setup time	D before PCLK↑	6		2		ns
		MODE before PCLK↑	15		3.5		
		Y before DCLK↑	5		2		
		MODE before DCLK↑	12		3.5		
		SDI before DCLK↑	10		3.5		
		DCLK before PCLK↑	15		3.5		
		PCLK before DCLK↑	45		8.5		
t_h	Hold time	D after PCLK↑	2		1.5		ns
		MODE after PCLK↑	0		0		
		Y after DCLK↑	5		1.5		
		MODE after DCLK↑	5		1.5		
		SDI after DCLK↑	0		0		

switching characteristics over operating free-air temperature range (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	CY29FCT818AT MIN	CY29FCT818AT MAX	CY29FCT818CT MIN	CY29FCT818CT MAX	UNIT
t_{pd}	PCLK	Y		12		6	ns
	MODE	SDO		18		7.2	
	SDI	SDO		18		7.1	
	DCLK	SDO		30		7.2	
t_{PZL}	$\overline{OE}$	Y		20		8	ns
	DCLK	D		35		9	
t_{PZH}	$\overline{OE}$	Y		20		8.5	ns
	DCLK	D		30		9	
t_{PLZ}	$\overline{OE}$	Y		20		5.5	ns
	DCLK	D		45		5.5	
t_{PHZ}	$\overline{OE}$	Y		30		8	ns
	DCLK	D		90		8	

PARAMETER MEASUREMENT INFORMATION

TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	7 V
t_{PHZ}/t_{PZH}	Open

**LOAD CIRCUIT FOR
TOTEM-POLE OUTPUTS**

**LOAD CIRCUIT FOR
3-STATE OUTPUTS**

**VOLTAGE WAVEFORMS
PULSE DURATION**

**VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES**

**VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS**

**VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING**

NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control.
Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. The outputs are measured one at a time with one input transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

PACKAGING INFORMATION

Orderable Device	Status [1]	Package Type	Package Drawing	Pins	Package Qty	Eco Plan [2]	Lead/ Ball Finish	MSL Peak Temp [3]	Samples (Requires Login)
5962-9682701Q3A	ACTIVE	LCCC	FK	28	1	TBD	POST-PLATE	N / A for Pkg Type	Contact TI Distributor or Sales Office
5962-9682701QLA	ACTIVE	CDIP	JT	24	1	TBD	A42	N / A for Pkg Type	Purchase Samples
CY29FCT818ATDMB	ACTIVE	CDIP	JT	24	1	TBD	A42	N / A for Pkg Type	Contact TI Distributor or Sales Office
CY29FCT818CTQC	PREVIEW	SSOP/QSOP	DBQ	24	55	TBD	Call TI	Call TI	Samples Not Available
CY29FCT818CTSOCT	ACTIVE	SOIC	DW	24	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	Purchase Samples
CY29FCT818CTSOCTE4	ACTIVE	SOIC	DW	24	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	Purchase Samples
CY29FCT818CTSOCTG4	ACTIVE	SOIC	DW	24	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	Purchase Samples

[1] The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

[2] Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

[3] MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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![Texas Instruments logo]

PACKAGE MATERIALS INFORMATION

TAPE AND REEL INFORMATION

REEL DIMENSIONS

Reel Diameter

Reel Width (W1)

TAPE DIMENSIONS

Cavity

A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

Sprocket Holes

| Q1 | Q2 |
| Q3 | Q4 |

| Q1 | Q2 |
| Q3 | Q4 |

User Direction of Feed

Pocket Quadrants

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CY29FCT818CTSOCT	SOIC	DW	24	2000	330.0	24.4	10.75	15.7	2.7	12.0	24.0	Q1

TAPE AND REEL BOX DIMENSIONS

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CY29FCT818CTSOCT	SOIC	DW	24	2000	346.0	346.0	41.0

JT (R-GDIP-T**)

CERAMIC DUAL-IN-LINE

24 LEADS SHOWN
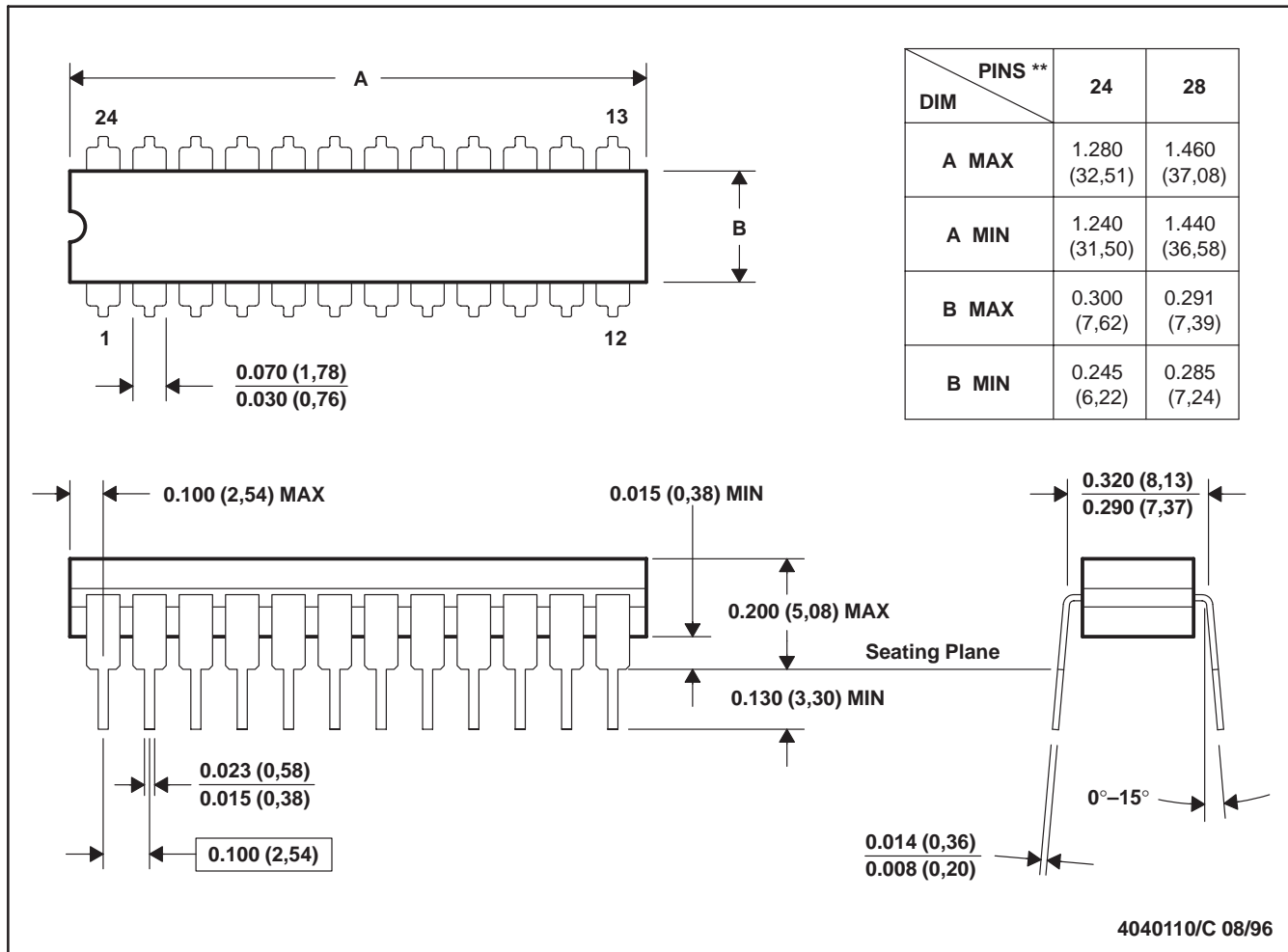
PINS ** DIM	24	28
A MAX	1.280 (32,51)	1.460 (37,08)
A MIN	1.240 (31,50)	1.440 (36,58)
B MAX	0.300 (7,62)	0.291 (7,39)
B MIN	0.245 (6,22)	0.285 (7,24)

A

24   13

B

1   12

0.070 (1,78)
0.030 (0,76)

0.100 (2,54) MAX

0.015 (0,38) MIN

0.320 (8,13)
0.290 (7,37)

0.200 (5,08) MAX

Seating Plane

0.130 (3,30) MIN

0.023 (0,58)
0.015 (0,38)

0.100 (2,54)

0°–15°

0.014 (0,36)
0.008 (0,20)

4040110/C 08/96

NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package can be hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for terminal identification.
E. Falls within MIL STD 1835 GDIP3-T24, GDIP4-T28, and JEDEC MO-058 AA, MO-058 AB

FK (S−CQCC−N**) LEADLESS CERAMIC CHIP CARRIER
28 TERMINAL SHOWN
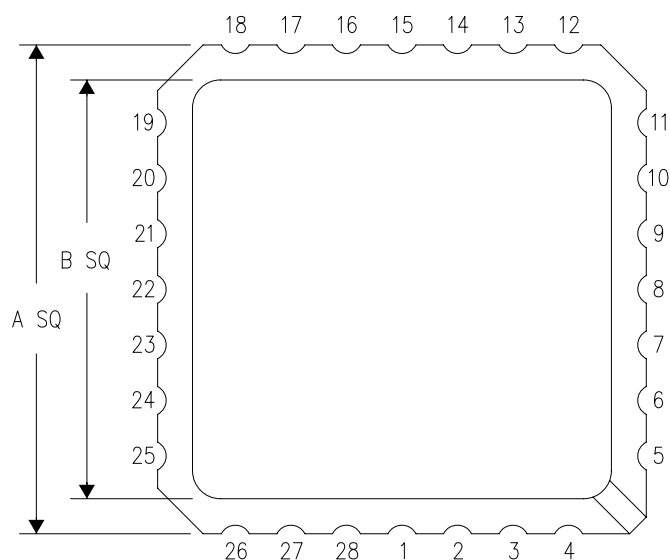
NO. OF TERMINALS **	A		B	
	MIN	MAX	MIN	MAX
20	0.342 (8,69)	0.358 (9,09)	0.307 (7,80)	0.358 (9,09)
28	0.442 (11,23)	0.458 (11,63)	0.406 (10,31)	0.458 (11,63)
44	0.640 (16,26)	0.660 (16,76)	0.495 (12,58)	0.560 (14,22)
52	0.740 (18,78)	0.761 (19,32)	0.495 (12,58)	0.560 (14,22)
68	0.938 (23,83)	0.962 (24,43)	0.850 (21,6)	0.858 (21,8)
84	1.141 (28,99)	1.165 (29,59)	1.047 (26,6)	1.063 (27,0)
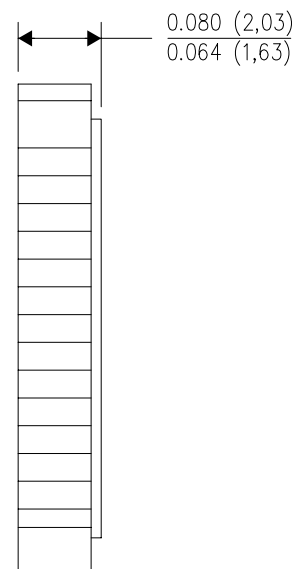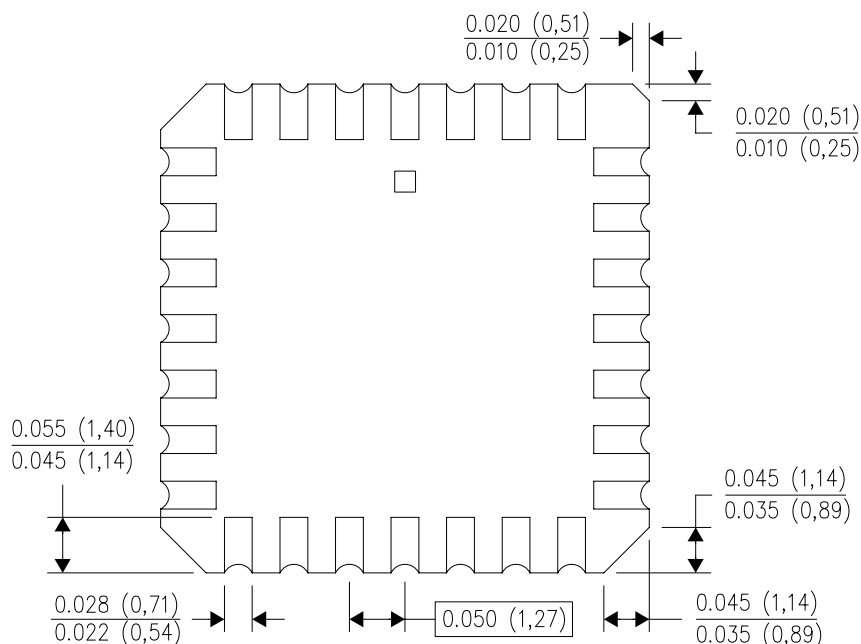
4040140/D 01/11

NOTES: A.   All linear dimensions are in inches (millimeters).
         B.   This drawing is subject to change without notice.
         C.   This package can be hermetically sealed with a metal lid.
         D.   Falls within JEDEC MS−004

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DW (R−PDSO−G24) PLASTIC SMALL OUTLINE

0.614 (15,60)
0.598 (15,20)

24 13

0.419 (10,63)
0.393 (9,97)

0.299 (7,60)
0.291 (7,40)

1 12

Pin 1
Index Area

0.050 (1,27)

0.020 (0,51)
0.012 (0,31)

⊕ 0.010 (0,25) Ⓜ

0.104 (2,65) Max

0.012 (0,30)
0.004 (0,10)

0.013 (0,33)
0.008 (0,20)

△ 0.004 (0,10)

Gauge Plane

Seating Plane

0.010 (0,25)

0°–8°

0.050 (1,27)
0.016 (0,40)

4040000−5/G 01/11
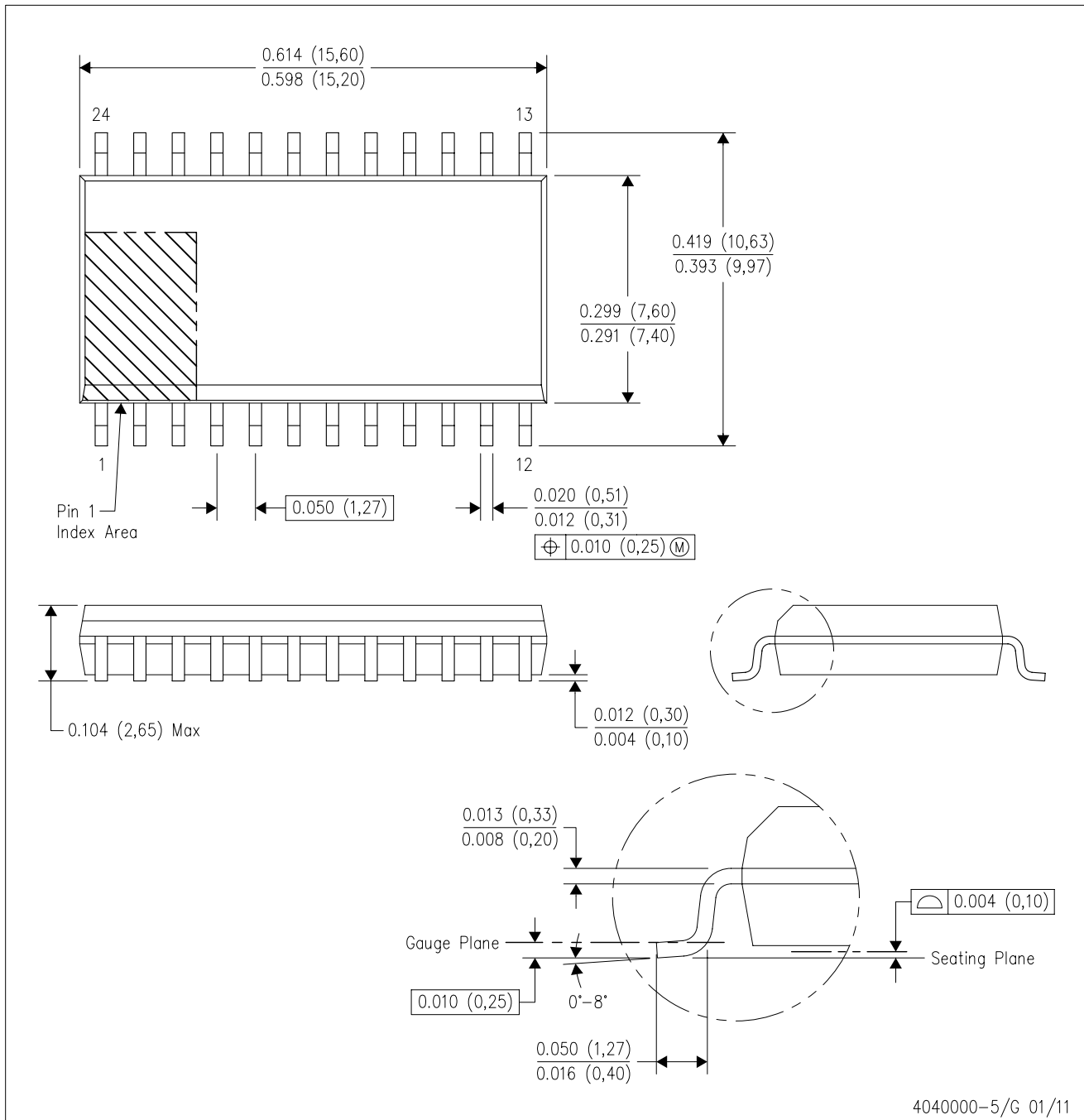
NOTES: A. All linear dimensions are in inches (millimeters). Dimensioning and tolerancing per ASME Y14.5M−1994.
   B. This drawing is subject to change without notice.
   C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
   D. Falls within JEDEC MS−013 variation AD.

TEXAS INSTRUMENTS
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DBQ (R−PDSO−G24)   PLASTIC SMALL−OUTLINE PACKAGE
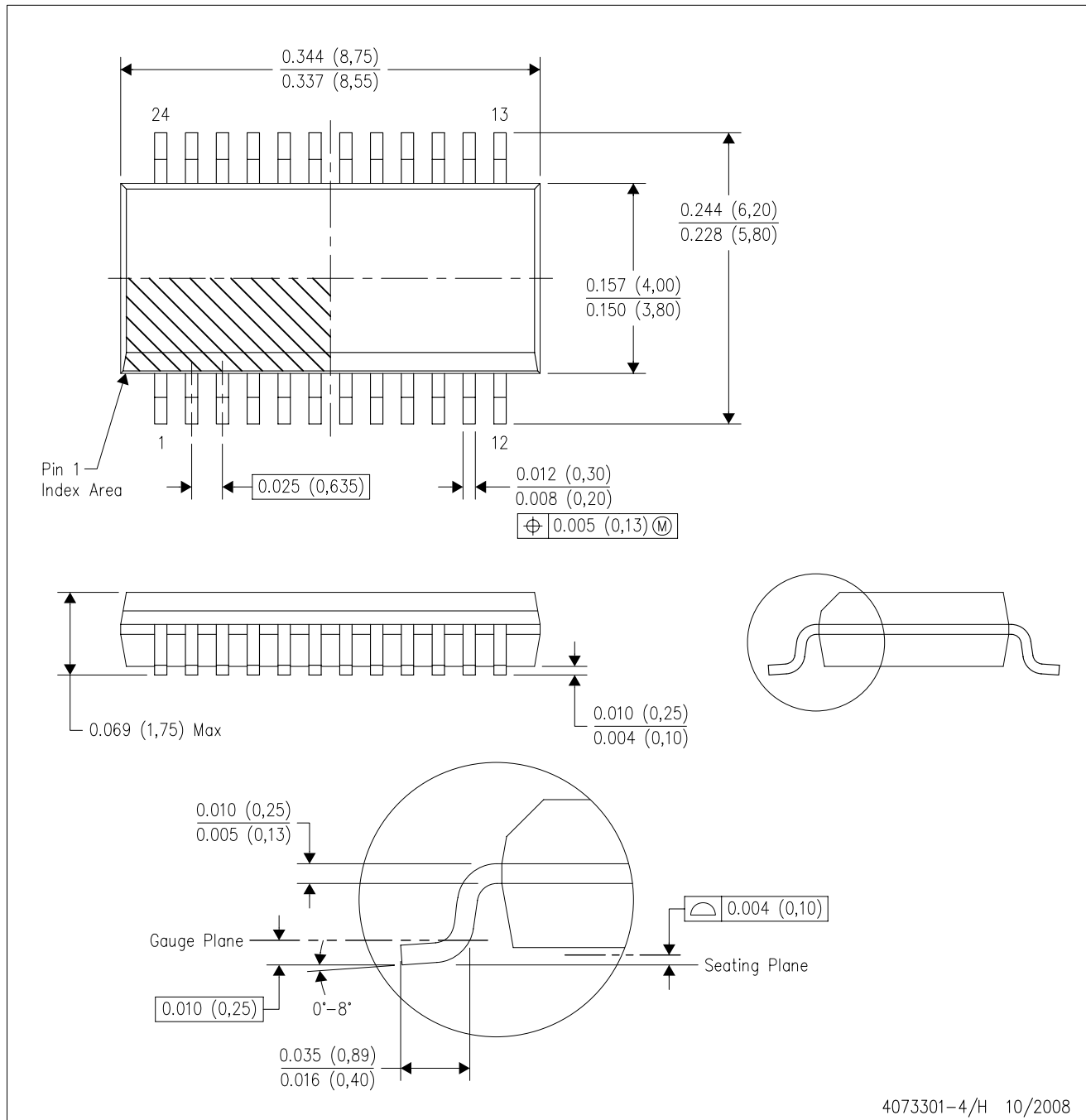
0.344 (8,75)
0.337 (8,55)

24   13

0.244 (6,20)
0.228 (5,80)

0.157 (4,00)
0.150 (3,80)

1   12

Pin 1
Index Area

0.025 (0,635)

0.012 (0,30)
0.008 (0,20)

⊕ 0.005 (0,13) Ⓜ

0.069 (1,75) Max

0.010 (0,25)
0.004 (0,10)

0.010 (0,25)
0.005 (0,13)

0.004 (0,10)

Gauge Plane

Seating Plane

0.010 (0,25)   0°−8°

0.035 (0,89)
0.016 (0,40)

4073301−4/H 10/2008

NOTES: A. All linear dimensions are in inches (millimeters).
         B. This drawing is subject to change without notice.
         C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15) per side.
         D. Falls within JEDEC MO−137 variation AE.

IMPORTANT NOTICE

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