8-/10-/12-Bit, Octal-Channel, Ultra-Low Glitch, Voltage Output, Two-Wire Interface DIGITAL-TO-ANALOG CONVERTERS

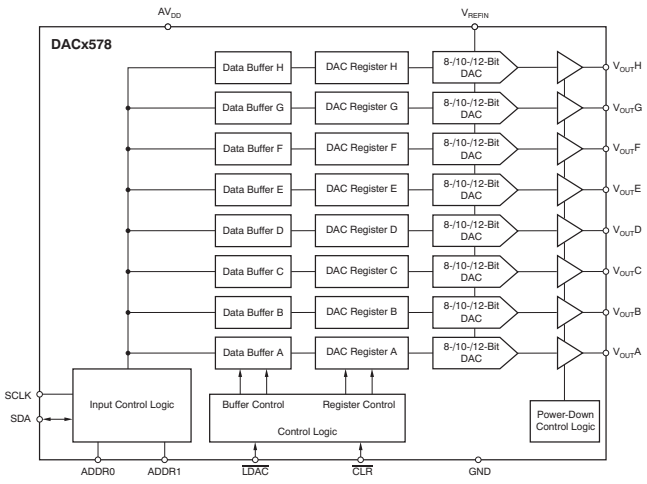
Check for Samples: DAC5578, DAC6578, DAC7578

FEATURES

- **Relative Accuracy: 1 LSB INL**
- **Glitch Energy: 0.15nV-s**
- **Power-On Reset to Zero Scale or Midscale**
- **Ultra-Low Power Operation: 150µA/ch at 5V**
- **Wide Power-Supply Range: +2.7V to +5.5V**
- **Monotonic Over Temperature Range**
- **Settling Time: 10µs to ±0.003% Full-Scale Range (FSR)**
- **Two-Wire Serial Interface (I²C™-Compatible)**
- **On-Chip Output Buffer Amplifier with Rail-to-Rail Operation**
- **Temperature Range: –40°C to +125°C**

APPLICATIONS

- **Portable Instrumentation**
- **Closed-Loop Servo Control**
- **Process Control**
- **Data Acquisition Systems**
- **Programmable Attenuation**
- **PC Peripherals**



DESCRIPTION

The DAC5578, DAC6578, and DAC7578 are low-power, voltage-output, eight-channel, 8-/10-/12-bit digital-to-analog converters (DACs). The DAC5578, DAC6578, and DAC7578 accept external reference voltages at the V_{REFIN} pin of up to AV_{DD}, giving a full-scale output voltage range up to AV_{DD}. These devices are monotonic, provide very good linearity, and minimize undesired code-to-code transient voltages (glitch).

The DAC5578, DAC6578, and DAC7578 use a versatile, two-wire serial interface that is I²C-compatible and operates at clock rates of up to 3.4MHz. Multiple devices can share the same bus.

The DAC5578, DAC6578, and DAC7578 incorporate a power-on-reset (POR) circuit that ensures the DAC output powers on at either zero-scale or midscale until a valid code is written to the device. These devices also contain a power-down feature, accessed through the serial interface, that reduces the current consumption of the devices to typically TBD µA at 5V. Power consumption is typically TBD mW at 3V, reducing to TBD µW in power-down mode. The low power consumption, two-wire interface, and small footprint make these devices ideal for portable, battery-operated equipment.

The DAC5578, DAC6578, and DAC7578 are drop-in and function-compatible with the DAC7678. All devices are available in a 4x4, QFN-24 package and a TSSOP-16 package.

RELATED DEVICES	8-BIT	10-BIT	12-BIT
Pin- and Function-Compatible (w/internal reference)	—	—	DAC7678
Pin- and Function-Compatible	DAC5578	DAC6578	DAC7578

PRODUCT PREVIEW

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

I²C is a trademark of NXP Semiconductors.
All other trademarks are the property of their respective owners.

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

PACKAGE/ORDERING INFORMATION(1)

PRODUCT	RESOLUTION	MAXIMUM RELATIVE ACCURACY (LSB)	MAXIMUM DIFFERENTIAL NONLINEARITY (LSB)	PACKAGE-LEAD	PACKAGE DESIGNATOR	SPECIFIED TEMPERATURE RANGE	PACKAGE MARKING
DAC7578	12 bits	±1	±0.25	TSSOP-16	PW	–40°C to +125°C	DAC7578
				QFN-24	RGE	–40°C to +125°C	DAC7578
DAC6578	10 bits	±0.5	±0.20	TSSOP-16	PW	–40°C to +125°C	DAC6578
				QFN-24	RGE	–40°C to +125°C	DAC6578
DAC5578	8 bits	±0.25	±0.10	TSSOP-16	PW	–40°C to +125°C	DAC5578
				QFN-24	RGE	–40°C to +125°C	DAC5578

(1) For the most current package and ordering information see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.

ABSOLUTE MAXIMUM RATINGS(1)

Over operating free-air temperature range, unless otherwise noted.

	DAC5578, DAC6578, DAC7578	UNIT
AV_{DD} to GND	–0.3 to +6	V
Digital input voltage to GND	–0.3 to +AV_{DD} + 0.3	V
V_{OUT} to GND	–0.3 to +AV_{DD} + 0.3	V
V_{REF} to GND	–0.3 to +AV_{DD} + 0.3	V
Operating temperature range	–40 to +125	°C
Storage temperature range	–65 to +150	°C
Junction temperature range (T_J max)	+150	°C
Power dissipation	(T_J max – T_A)/θ_{JA}	W
Thermal impedance, θ_{JA}	+118	°C/W
Thermal impedance, θ_{JC}	+29	°C/W

(1) Stresses above those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. Exposure to absolute maximum conditions for extended periods may affect device reliability.

PRODUCT PREVIEW

ELECTRICAL CHARACTERISTICS

At AV_{DD} = 2.7V to 5.5V and over –40°C to +125°C, unless otherwise noted.

PARAMETER		TEST CONDITIONS	DAC5578, DAC6578, DAC7578			UNIT
			MIN	TYP	MAX	
STATIC PERFORMANCE(1)						
DAC7578	Resolution		12			Bits
	Relative accuracy	Measured by the line passing through codes 30 and 4050		±0.3	±1	LSB
	Differential nonlinearity	12-bit monotonic		±0.1	±0.25	LSB
DAC6578	Resolution		10			Bits
	Relative accuracy	Measured by the line passing through codes 12 and 1012		±0.15	±0.5	LSB
	Differential nonlinearity	10-bit monotonic		±0.1	±0.20	LSB
DAC5578	Resolution		8			Bits
	Relative accuracy	Measured by the line passing through codes 3 and 252		±0.10	±0.25	LSB
	Differential nonlinearity	8-bit monotonic		±0.05	±0.10	LSB
Offset error		Extrapolated from two-point line passing through two codes(1), unloaded		±0.5	±4	mV
Offset error drift				±3		µV/°C
Full-scale error		DAC register loaded with all '1's		±0.03	±0.2	% of FSR
Full-scale error drift				±2		µV/°C
Zero-code error		DAC register loaded with all '0's		1	4	mV
Zero-code error drift				2		µV/°C
Gain error		Extrapolated from two-point line passing through two codes(1), unloaded		±0.01	±0.15	% of FSR
Gain temperature coefficient		AV_{DD} = 5V		±1		ppm of FSR/°C
		AV_{DD} = 2.7V		±1		ppm of FSR/°C
OUTPUT CHARACTERISTICS(2)						
Output voltage range			0		AV_{DD}	V
Output voltage settling time		DACs unloaded, 1/4 scale to 3/4 scale		6	10	µs
		R_L = 1MΩ		12		µs
Slew rate				0.75		V/µs
Capacitive load stability		R_L = ∞		1000		pF
		R_L = 2kΩ		3000		pF
Code change glitch impulse		1LSB change around major carry		0.1		nV-s
Digital feedthrough		SCLK toggling		0.1		nV-s
Power-on glitch impulse		R_L = 2kΩ, C_L = 470pF, AV_{DD} = 5.5V		10		mV
		R_L = 2kΩ, C_L = 470pF, AV_{DD} = 2.7V		6		mV
Channel-to-channel dc crosstalk		Full-scale swing on adjacent channel		0.1		LSB
Channel-to-channel ac crosstalk		1kHz full-scale sine wave, outputs unloaded		–109		dB
DC output impedance		At midscale input		4		Ω
Short-circuit current		DAC outputs shorted to GND		25		mA
Power-up time (including settling time)		Coming out of power-down mode, AV_{DD} = 5V		50		µs

(1) Code range of 3 to 252 for 8-bit device, 12 to 1012 for 10-bit, and 30 to 4050 for 12-bit.
(2) Specified by design or characterization; not production tested.

PRODUCT PREVIEW

ELECTRICAL CHARACTERISTICS (continued)

At AV_{DD} = 2.7V to 5.5V and over –40°C to +125°C, unless otherwise noted.

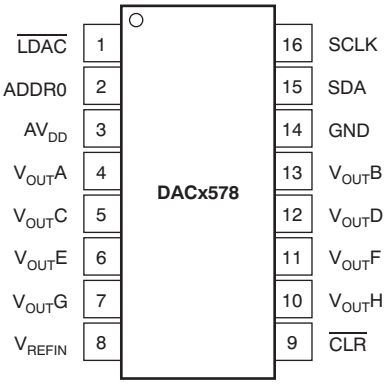
PARAMETER		TEST CONDITIONS	DAC5578, DAC6578, DAC7578 MIN	TYP	MAX	UNIT
AC PERFORMANCE(3)						
SNR(4)		T_A = +25°C, BW = 20kHz, AV_{DD} = 5V, f_{OUT} = 1kHz		TBD		dB
THD		T_A = +25°C, BW = 20kHz, AV_{DD} = 5V, f_{OUT} = 1kHz		TBD		dB
SFDR		T_A = +25°C, BW = 20kHz, AV_{DD} = 5V, f_{OUT} = 1kHz		TBD		dB
SINAD		T_A = +25°C, BW = 20kHz, AV_{DD} = 5V, f_{OUT} = 1kHz		TBD		dB
DAC output noise density		T_A = +25°C, at zero-code input, f_{OUT} = 1kHz		90		nV/√Hz
DAC output noise		T_A = +25°C, at midscale input, f = 0.1Hz to 10Hz		2.6		μV_{PP}
EXTERNAL REFERENCE						
External reference current		External V_{REF} = 2.5V, all eight channels active		90		µA
V_{REFIN} pin reference input range			0		AV_{DD}	V
Reference input impedance				8		kΩ
LOGIC INPUTS(3)						
Input current				±1		µA
$V_{IN}L$	Logic input LOW voltage				$0.3AV_{DD}$	V
$V_{IN}H$	Logic input HIGH voltage		$0.7AV_{DD}$			V
Pin capacitance				1.5	3	pF
POWER REQUIREMENTS						
AV_{DD}	Analog power supply		2.7		5.5	V
I_{DD} (5)	Normal mode	AV_{DD} = 3.6V to 5.5V $V_{IN}H = AV_{DD}$ and $V_{IN}L$ = GND		0.95	1.4	mA
		AV_{DD} = 2.7V to 3.6V $V_{IN}H = AV_{DD}$ and $V_{IN}L$ = GND		0.81	1.3	mA
	All power-down modes	AV_{DD} = 3.6V to 5.5V $V_{IN}H = AV_{DD}$ and $V_{IN}L$ = GND		0.18	3	µA
		AV_{DD} = 2.7V to 3.6V $V_{IN}H = AV_{DD}$ and $V_{IN}L$ = GND		0.10	2.5	µA
Power dissipation(5)	Normal mode	AV_{DD} = 3.6V to 5.5V $V_{IN}H = AV_{DD}$ and $V_{IN}L$ = GND		3.4	7.1	mW
		AV_{DD} = 2.7V to 3.6V $V_{IN}H = AV_{DD}$ and $V_{IN}L$ = GND		2.2	4.3	mW
	All power-down modes	AV_{DD} = 3.6V to 5.5V $V_{IN}H = AV_{DD}$ and $V_{IN}L$ = GND		0.6	16	µW
		AV_{DD} = 2.7V to 3.6V $V_{IN}H = AV_{DD}$ and $V_{IN}L$ = GND		0.3	9	µW
TEMPERATURE RANGE						
Specified performance			–40		+125	°C

(3) Specified by design or characterization; not production tested.
(4) First 19 harmonics removed for SNR calculation.
(5) Input code = midscale, no load.

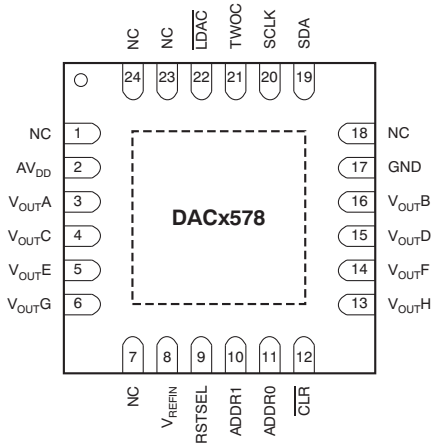
PRODUCT PREVIEW

PIN CONFIGURATIONS

PW PACKAGE
TSSOP-16
(TOP VIEW)



RGE PACKAGE
QFN-24
(TOP VIEW)



PIN DESCRIPTIONS

PACKAGE		NAME	DESCRIPTION
TSSOP	QFN		
—	1	NC	Not internally connected
3	2	AV_{DD}	Power-supply input, 2.7V to 5.5V
4	3	$V_{OUT}A$	Analog output voltage from DAC A
5	4	$V_{OUT}C$	Analog output voltage from DAC C
6	5	$V_{OUT}E$	Analog output voltage from DAC E
7	6	$V_{OUT}G$	Analog output voltage from DAC G
—	7	NC	Not internally connected
8	8	V_{REFIN}	Positive reference input
—	9	RSTSEL	Reset select pin. RSTSEL high resets device to mid-scale; RSTSEL low (default setting) resets device to zero-scale.
—	10	ADDR1	Three-state address input 1
2	11	ADDR0	Three-state address input 0
9	12	$\overline{CLR}$	Asynchronous clear input
10	13	$V_{OUT}H$	Analog output voltage from DAC H
11	14	$V_{OUT}F$	Analog output voltage from DAC F
12	15	$V_{OUT}D$	Analog output voltage from DAC D
13	16	$V_{OUT}B$	Analog output voltage from DAC B
14	17	GND	Ground reference point for all circuitry on the device
—	18	NC	Not internally connected
15	19	SDA	Serial data input. Data are clocked into or out of the input register. This pin is a bidirectional, open-drain data line that should be connected to the supply voltage with an external pull-up resistor.
16	20	SCLK	Serial clock input. Data can be transferred at rates up to 3.4MHz. Schmitt-trigger logic input.
—	21	TWOC	Twos Complement Select. If the TWOC pin is pulled high, the DAC registers use twos compliments format; if TWOC is pulled low, the DAC registers use straight binary format.
1	22	$\overline{LDAC}$	Load DACs
—	23	NC	Not internally connected
—	24	NC	Not internally connected

PRODUCT PREVIEW

TIMING DIAGRAM: TBD

Figure 1. Serial Write Operation

THEORY OF OPERATION

DIGITAL-TO-ANALOG CONVERTER (DAC)

The DAC5578, DAC6578, and DAC7578 (DACx578) architecture consists of eight string DACs each followed by an output buffer amplifier. Figure 2 shows a principal block diagram of the DAC architecture.

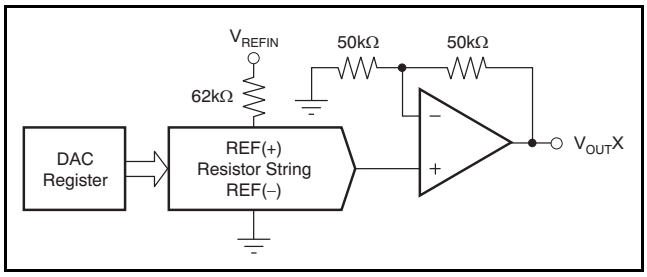


Figure 2. Device Architecture

For the TSSOP package, the input coding to the DACx578 is straight binary. For the QFN package, the TWOC pin controls the code format.

When using an external reference, the ideal output voltage is given by Equation 1:

$$V_{OUT} = \frac{D_{IN}}{4096} \times V_{REFIN} \quad (1)$$

Where:

D_{IN} = decimal equivalent of the binary code that is loaded to the DAC register. The code can range from 0 to 255 for the 8-bit DAC5578, 0 to 1023 for the 10-bit DAC6578, and 0 to 4095 for the 12-bit DAC7578.

V_{REFIN} = external reference voltage of 0V to 5V, supplied at the V_{REFIN} pin.

RESISTOR STRING

The resistor string circuitry is shown in Figure 3. It is simply a string of resistors, each of value *R*. The code loaded into the DAC register determines at which node on the string the voltage is tapped off. The voltage is then fed into the output amplifier by closing one of the switches connecting the string to the amplifier. Because it is a string of resistors, this architecture is monotonic.

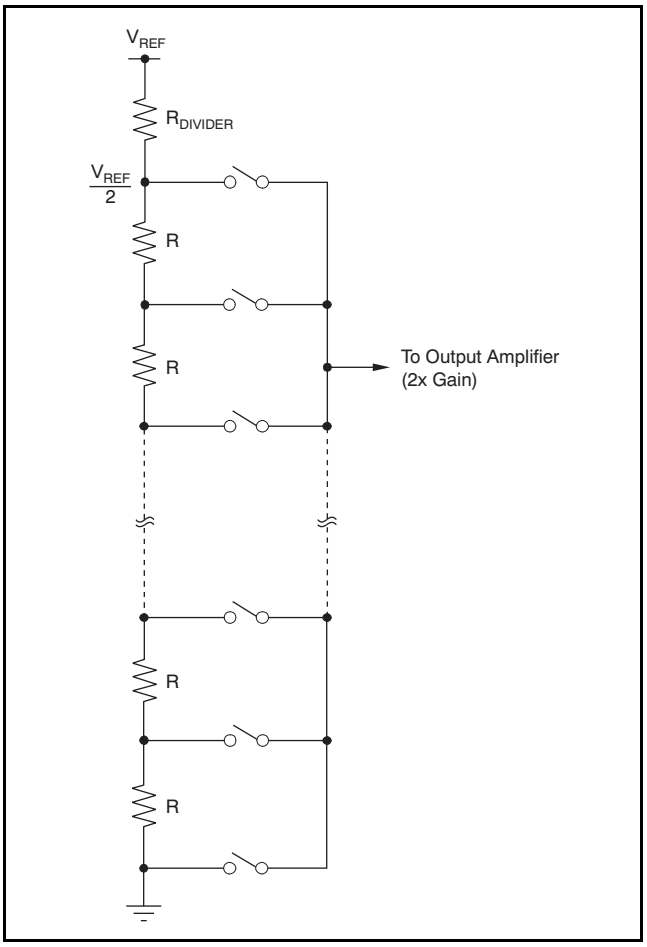


Figure 3. Resistor String

OUTPUT AMPLIFIER

The output buffer amplifier is capable of generating rail-to-rail voltages on its output, giving a maximum output range of 0V to AV_{DD}. It is capable of driving a load of 2kΩ in parallel with 1000pF to GND. The source and sink capabilities of the output amplifier can be seen in the Typical Characteristics (TBD) . The typical slew rate is 0.75V/µs, with a typical full-scale settling time of 5µs with the output unloaded.

PRODUCT PREVIEW

TWO-WIRE, I²C-COMPATIBLE INTERFACE

The two-wire serial interface used by the DACx578 is I²C-compatible (refer to the I²C Bus Specification). The bus consists of a data line (SDA) and a clock line (SCL) with pull-up resistors. When the bus is idle, both SDA and SCL lines are pulled high. All I²C-compatible devices connect to the I²C bus through open-drain I/O pins SDA and SCL.

The I²C specification states that the device that controls communication is called a master, and the devices that are controlled by the master are called slaves. The master device generates the SCL signal. The master device also generates special timing conditions (start, repeated start, and stop) on the bus to indicate the start or stop of a data transfer, as shown in Figure 4. Device addressing is also performed by the master. The master device on an I²C bus is usually a microcontroller or a digital signal processor (DSP). The DACx578 operates as a slave device on the I²C bus. A slave device acknowledges the master commands, and upon the direction of the master, either receives or transmits data.

Although the DACx578 normally operates as a slave receiver, when a master device acquires the DACx578 internal register data, the DACx578 also operates as a slave transmitter. In this case, the master device reads from the DACx578 (the slave transmitter). According to I²C terminology, read and write operations are always performed with respect to the master device.

The DACx578 supports the following data transfer modes, as defined in the I²C Bus Specification:

- Standard mode (100kbps)
- Fast mode (400kbps)
- Fast mode plus (1.0Mbps)(1)
- High-Speed mode (3.4Mbps)

The data transfer protocols for Standard and Fast modes are exactly the same; therefore, these modes are referred to as *F/S mode* in this document. The protocol for High-Speed mode is different from the F/S mode, and it is referred to as *HS mode*. The DACx578 supports 7-bit addressing. Note that 10-bit addressing and a general call address are not supported.

Other than specific timing signals, the I²C interface works with serial bytes. At the end of each byte, a ninth clock cycle is used to generate/detect an acknowledge signal, as shown in Figure 5. An *acknowledge* is when the SDA line is pulled low during the high period of the ninth clock cycle. A *not-acknowledge* is when the SDA line is left high during the high period of the ninth clock cycle.

(1) The DACx578 supports Fast mode plus speed and timing specifications only. These devices cannot support the 20mA low-level output current specification.

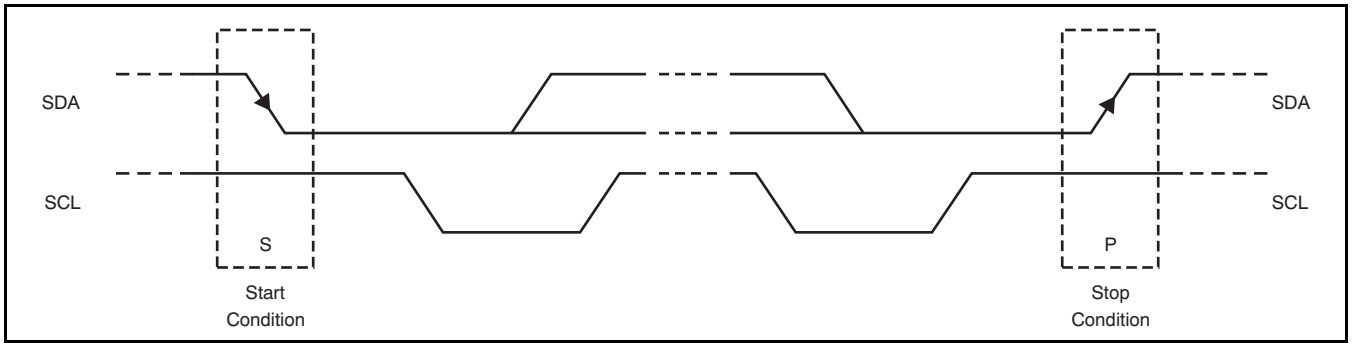


Figure 4. Start and Stop Conditions

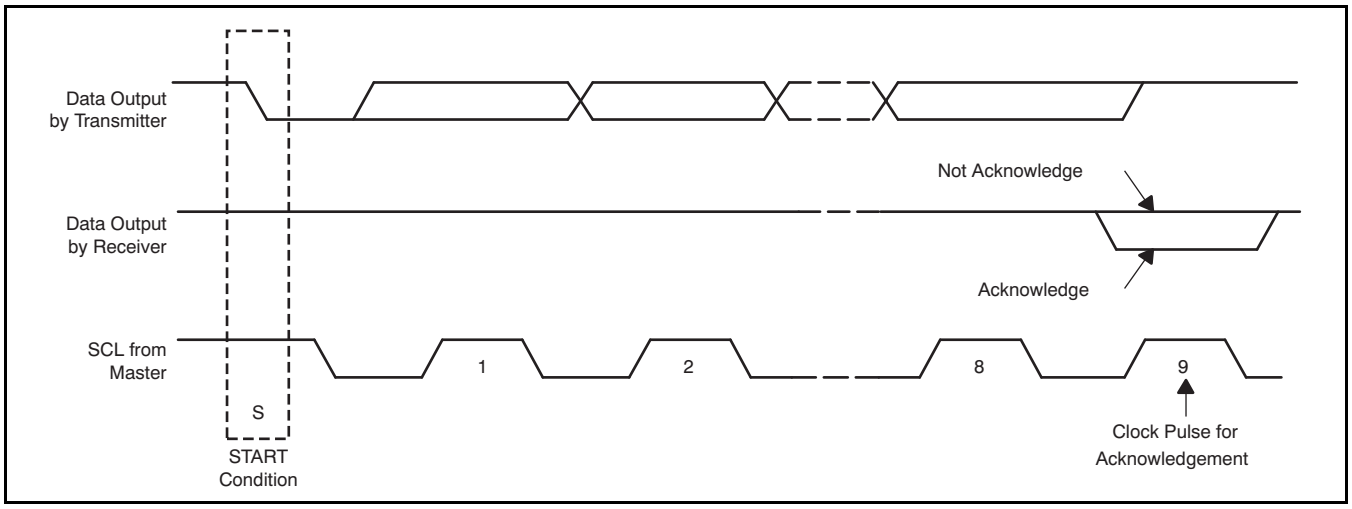


Figure 5. Acknowledge and Not Acknowledge Signals on the I²C Bus

F/S Mode Protocol

The master initiates data transfer by generating a start condition, defined as when a high-to-low transition occurs on the SDA line while SCL is high, as shown in Figure 5. All I²C-compatible devices recognize a start condition.

The master then generates the SCL pulses, and transmits the 7-bit address and the read/write direction bit (R/$\overline{W}$) on the SDA line. During all transmissions, the master ensures that data are valid. A valid data condition requires the SDA line to be stable during the entire high period of the clock pulse, as shown in Figure 6. All devices recognize the address sent by the master and compare it to the internal fixed addresses. Only the slave device with a matching address generates an acknowledge by pulling the SDA line low during the entire high period of the ninth SCL cycle, as shown in Figure 5. Upon detecting this acknowledge, the master recognizes the communication link with a slave has been established.

The master generates additional SCL cycles to either transmit data to the slave (R/$\overline{W}$ bit = '0') or receive data from the slave (R/$\overline{W}$ bit = '1'). In either case, the receiver must acknowledge the data sent by the transmitter. So the acknowledge signal can either be generated by the master or by the slave, depending on which one is the receiver. The 9-bit valid data sequences, consisting of eight data bits and one acknowledge bit, can continue as long as necessary.

To signal the end of the data transfer, the master generates a stop condition by pulling the SDA line from low to high while the SCL line is high (see Figure 4). This action releases the bus and stops the communication link with the addressed slave. All I²C-compatible devices recognize the stop condition. Upon receipt of a stop condition, the bus is released, and all slave devices then wait for a start condition followed by a matching address.

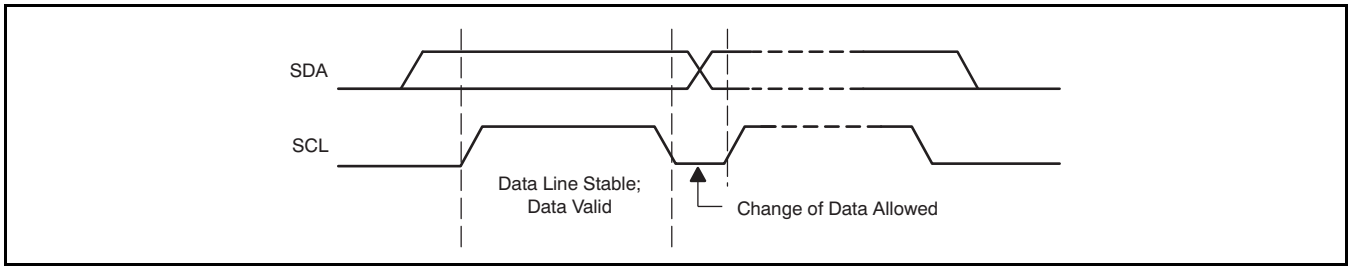


Figure 6. I²C Bus Bit Transfer

HS Mode Protocol

When the bus is idle, both the SDA and SCL lines are pulled high by the pull-up resistors.

The master generates a start condition followed by a valid serial byte containing HS mode master code *00001XXX*. This transmission is made in F/S mode at no more than 1.0Mbps. No device is allowed to acknowledge the HS mode master code, but all devices must recognize it and switch the respective internal settings to support 3.4Mbps operation.

The master then generates a repeated start condition (a repeated start condition has the same timing as the start condition). After this repeated start condition, the protocol is the same as F/S mode, except that transmission speeds up to 3.4Mbps are allowed. A stop condition ends HS mode and switches all the internal settings of the slave devices to support F/S mode. Instead of using a stop condition, repeated start conditions should be used to secure the bus in HS mode.

DACx578 I²C UPDATE SEQUENCE

For a single update, the DACx578 requires a start condition, a valid I²C address (A) byte, a command and access (CA) byte, and two data bytes, the most significant data byte (MSDB) and least significant data byte (LSDB), as shown in Table 1.

After each byte is received, the DACx578 acknowledges by pulling the SDA line low during the high period of a single clock pulse, as shown in Figure 7. A valid I²C address selects the corresponding slave device (for example, DACx578).

The CA byte sets the operational mode of the selected DACx578. When the operational mode is selected by this byte, the DACx578 must receive two data bytes, the most significant data byte (MSDB) and least significant data byte (LSDB), for data update to occur. The DACx578 performs an update on the falling edge of the acknowledge signal that follows the LSDB.

The CA byte does not have to be re-sent until a change in operational mode is required. The bits of the control byte continuously determine the type of update performed. Thus, for the first update, the DACx578 requires a start condition, a valid I²C address, the CA byte, and two data bytes (MSDB and LSDB). For all consecutive updates, the DACx578 needs only an MSDB and LSDB, as long as the CA byte command remains the same.

Table 1. Update Sequence

MSB	···	LSB	ACK	MSB	···	LSB	ACK	MSB	···	LSB	ACK	MSB	···	LSB	ACK
A Byte				CA Byte				MSDB				LSDB			

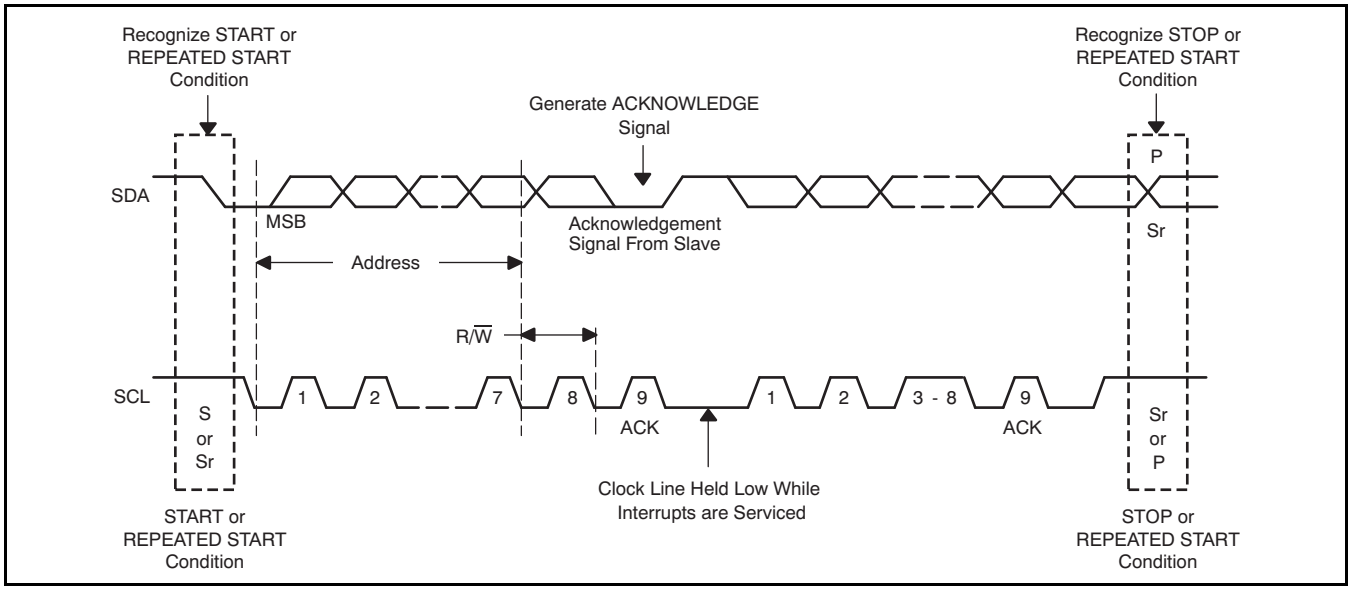


Figure 7. I²C Bus Protocol

When using the I^2C HS mode (clock = 3.4MHz), each 12-bit DAC update other than the first update can be done within 18 clock cycles (MSDB, acknowledge signal, LSDB, acknowledge signal) at 188.88kSPS. When using Fast mode (clock = 400kHz), the maximum DAC update rate is limited to 22.22kSPS. Using the Fast mode plus (clock = 1MHz), the maximum DAC update rate is limited to 55.55kSPS. When a stop condition is received, the DACx578 releases the I^2C bus and awaits a new start condition.

Address (A) Byte

The address byte, shown in Table 2, is the first byte received following the start condition from the master device. The first four most significant bits (MSBs) of the address are factory preset to '1001'. The next three bits of the address are controlled by the ADDR pin(s). The ADDR pin(s) inputs can be connected to AV_{DD}, GND, or left floating. The device address can be updated dynamically between serial commands. When using the QFN package (DAC5578RGE, DAC6578RGE, and DAC7578RGE), up to eight devices can be connected to the same I^2C bus. When using the TSSOP package (DAC5578PW. DAC6578PW, and DAC7578PW), up to three devices can be connected to the same I^2C bus.

Table 2. Address Byte

MSB							LSB
AD6	**AD5**	**AD4**	**AD3**	**AD2**	**AD1**	**AD0**	**R/$\overline{W}$**
1	0	0	1	See Table 3 or Table 4 Slave Address column			0 or 1

Table 3. Address Format For QFN-24 (RGE) Package

SLAVE ADDRESS	ADDR1	ADDR0
1001 000	0	0
1001 001	0	1
1001 010	1	0
1001 011	1	1
1001 100	Float	0
1001 101	Float	1
1001 110	0	Float
1001 111	1	Float
Not supported	Float	Float

Table 4. Address Format For TSSOP-16 (PW) Package

SLAVE ADDRESS	ADDR0
1001 000	0
1001 010	1
1001 100	Float

PRODUCT PREVIEW

Command and Access (CA) Byte

The command and access byte, as shown in Table 5, controls which command is executed and which register is being accessed when writing to or reading from the DACx578. See Table 6 for a list of write and read commands.

Table 5. Command and Access Byte

MSB							LSB
C3	**C2**	**C1**	**C0**	**A3**	**A2**	**A1**	**A0**
Command bits(1)				Access bits(1)			

(1) See Table 6 for bit selection.

Table 6. Command and Access Byte Format(1)

C3	C2	C1	C0	A3	A2	A1	A0	DESCRIPTION
Write Sequences								
0	0	0	0	A3	A2	A1	A0	Write to DAC input register channel n
0	0	0	1	A3	A2	A1	A0	Select to update DAC register channel n
0	0	1	0	A3	A2	A1	A0	Write to DAC input register channel n, and update all DAC registers (global software LDAC)
0	0	1	1	A3	A2	A1	A0	Write to DAC input register channel n, and update DAC register channel n
0	1	0	0	X	X	X	X	Power down/on DAC
0	1	0	1	X	X	X	X	Write to clear code register
0	1	1	0	X	X	X	X	Write to LDAC register
0	1	1	1	X	X	X	X	Software reset
Read Sequences								
0	0	0	0	A3	A2	A1	A0	Read from DAC input register channel n
0	0	0	1	A3	A2	A1	A0	Read from DAC register channel n
0	1	0	0	X	X	X	X	Read from DAC power down register
0	1	0	1	X	X	X	X	Read from clear code register
0	1	1	0	X	X	X	X	Read from LDAC register
Access Sequences								
C3	C2	C1	C0	0	0	0	0	DAC channel A
C3	C2	C1	C0	0	0	0	1	DAC channel B
C3	C2	C1	C0	0	0	1	0	DAC channel C
C3	C2	C1	C0	0	0	1	1	DAC channel D
C3	C2	C1	C0	0	1	0	0	DAC channel E
C3	C2	C1	C0	0	1	0	1	DAC channel F
C3	C2	C1	C0	0	1	1	0	DAC channel G
C3	C2	C1	C0	0	1	1	1	DAC channel H
C3	C2	C1	C0	1	1	1	1	All DAC channels, broadcast update

(1) Any sequences other than the ones listed are invalid; improper use can cause incorrect device operation.

PRODUCT PREVIEW

Most Significant Data Byte (MSDB) and Least Significant Data Byte (LSDB)

The MSDB and LSDB contain the data that are passed to the register(s) specified by the CA byte, as shown in Table 7 and Table 8. See Table 13 for a complete list of write sequences and Table 14 for a complete list of read sequences. The DACx578 updates at the falling edge of the acknowledge signal that follows the LSDB.

Broadcast Addressing

Broadcast addressing, as shown in Table 9, is also supported by the DACx578. Broadcast addressing can be used for synchronously updating or powering down multiple DACx578 devices. These devices are designed to work with each other, and with the DAC7678, to support multichannel synchronous updates. Using the broadcast address command, the DACx578 responds regardless of the state of the address pins. Note that broadcast addressing is supported only in write mode (master writes to the DACx578).

I²C Read Sequence

To read any register, use the following command sequence:

1. Send a start or repeated start command with a slave address and the R/$\overline{W}$ bit set to '0' for writing. The device acknowledges this event.
2. Then send a command byte for the register to be read. The device acknowledges this event again.
3. Then send a repeated start with the slave address and the R/$\overline{W}$ bit set to '1' for reading. The device also acknowledges this event.
4. Then the device writes the MSDB of the register. The master should acknowledge this byte.
5. Finally, the device writes out the LSDB.

An alternative reading method allows for reading back of the last register written to. The sequence is a start/repeated start with slave address and the R/$\overline{W}$ bit set to '1', and the two bytes of the last register are read out, as shown in Figure TBD.

Note that it is not possible to use the broadcast address for reading.

Table 7. Most Significant Data Byte (MSDB)

MSB							LSB
DB15	**DB14**	**DB13**	**DB12**	**DB11**	**DB10**	**DB9**	**DB8**
X	X	X	X	X	X	X	X

Table 8. Least Significant Data Byte (LSDB)

MSB							LSB
DB7	**DB6**	**DB5**	**DB4**	**DB3**	**DB2**	**DB1**	**DB0**
X	X	X	X	X	X	X	X

Table 9. Broadcast Address Command

MSB							LSB
AD6	**AD5**	**AD4**	**AD3**	**AD2**	**AD1**	**AD0**	**R/$\overline{W}$**
1	0	0	0	1	1	1	0

Table 10. DAC5578 Data Input Register Format

DB23								DB15							DB8								DB0
C3	C2	C1	C0	A3	A2	A1	A0	D7	D6	D5	D4	D3	D2	D1	D0	X	X	X	X	X	X	X	X
|-------- Command and Address Bits --------|							|---------- Data Bits ----------|							|---------- Don't Care ----------|								

Table 11. DAC6578 Data Input Register Format

DB23								DB15								DB6							DB0
C3	C2	C1	C0	A3	A2	A1	A0	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	X	X	X	X	X	X
|-------- Command and Address Bits --------|							|---------- Data Bits ----------|							|---------- Don't Care ----------|								

Table 12. DAC7578 Data Input Register Format

DB23								DB15											DB4				DB0
C3	C2	C1	C0	A3	A2	A1	A0	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	X	X	X	X
|-------- Command and Address Bits --------|							|---------- Data Bits ----------|										|---- Don't Care ----|								

PRODUCT PREVIEW

Table 13. Control Matrix for Write Commands (see Table 10, Table 11, and Table 12 for 8-bit, 10-bit, and 12-bit mapping)

CA BYTE								MSDB								LSDB								DESCRIPTION
C3	C2	C1	C0	A3	A2	A1	A0	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	
Write to DAC Input Register																								
0	0	0	0	0	0	0	0	Data[11:4]								Data[3:0]				X	X	X	X	Write to DAC input register for channel A
0	0	0	0	0	0	0	1	Data[11:4]								Data[3:0]				X	X	X	X	Write to DAC input register for channel B
0	0	0	0	0	0	1	0	Data[11:4]								Data[3:0]				X	X	X	X	Write to DAC input register for channel C
0	0	0	0	0	0	1	1	Data[11:4]								Data[3:0]				X	X	X	X	Write to DAC input register for channel D
0	0	0	0	0	1	0	0	Data[11:4]								Data[3:0]				X	X	X	X	Write to DAC input register for channel E
0	0	0	0	0	1	0	1	Data[11:4]								Data[3:0]				X	X	X	X	Write to DAC input register for channel F
0	0	0	0	0	1	1	0	Data[11:4]								Data[3:0]				X	X	X	X	Write to DAC input register forchannel G
0	0	0	0	0	1	1	1	Data[11:4]								Data[3:0]				X	X	X	X	Write to DAC input register for channel H
0	0	0	0	1	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	Invalid code, no action performed
0	0	0	0	1	1	1	1	Data[11:4]								Data[3:0]				X	X	X	X	Broadcast mode, write to all DAC channels
Select DAC Register to Update																								
0	0	0	1	0	0	0	0	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	Selects DAC channel A to be updated
0	0	0	1	0	0	0	1	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	Selects DAC channel B to be updated
0	0	0	1	0	0	1	0	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	Selects DAC channel C to be updated
0	0	0	1	0	0	1	1	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	Selects DAC channel D to be updated
0	0	0	1	0	1	0	0	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	Selects DAC channel E to be updated
0	0	0	1	0	1	0	1	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	Selects DAC channel F to be updated
0	0	0	1	0	1	1	0	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	Selects DAC channel G to be updated
0	0	0	1	0	1	1	1	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	Selects DAC channel H to be updated
0	0	0	1	1	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	Invalid code, no action performed
0	0	0	1	1	1	1	1	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	Broadcast mode, selects all DAC channels to be updated
Write to Selected DAC Input Register and Update Corresponding DAC Register (Individual Software LDAC)																								
0	0	1	1	0	0	0	0	Data[11:4]								Data[3:0]				X	X	X	X	Write to DAC input register for channel A and update channel A DAC register
0	0	1	1	0	0	0	1	Data[11:4]								Data[3:0]				X	X	X	X	Write to DAC input register for channel A and update channel B DAC register
0	0	1	1	0	0	1	0	Data[11:4]								Data[3:0]				X	X	X	X	Write to DAC input register for channel A and update channel C DAC register
0	0	1	1	0	0	1	1	Data[11:4]								Data[3:0]				X	X	X	X	Write to DAC input register for channel A and update channel D DAC register
0	0	1	1	0	1	0	0	Data[11:4]								Data[3:0]				X	X	X	X	Write to DAC input register for channel A and update channel E DAC register
0	0	1	1	0	1	0	1	Data[11:4]								Data[3:0]				X	X	X	X	Write to DAC input register for channel A and update channel F DAC register
0	0	1	1	0	1	1	0	Data[11:4]								Data[3:0]				X	X	X	X	Write to DAC input register for channel A and update channel G DAC register
0	0	1	1	0	1	1	1	Data[11:4]								Data[3:0]				X	X	X	X	Write to DAC input register for channel A and update channel H DAC register
0	0	1	1	1	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	Invalid code, no action performed
0	0	1	1	1	1	1	1	Data[11:4]								Data[3:0]				X	X	X	X	Broadcast mode, write to all input registers and update all DAC registers

Table 13. Control Matrix for Write Commands (see Table 10, Table 11, and Table 12 for 8-bit, 10-bit, and 12-bit mapping) (continued)

CA BYTE								MSDB								LSDB								DESCRIPTION
C3	C2	C1	C0	A3	A2	A1	A0	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	
Write to Selected DAC Input Register and Update All DAC Registers (Global Software LDAC)																								
0	0	1	0	0	0	0	0	Data[11:4]								Data[3:0]				X	X	X	X	Write to DAC input register for channel A and update all DAC registers
0	0	1	0	0	0	0	1	Data[11:4]								Data[3:0]				X	X	X	X	Write to DAC input register for channel B and update all DAC registers
0	0	1	0	0	0	1	0	Data[11:4]								Data[3:0]				X	X	X	X	Write to DAC input register for channel C and update all DAC registers
0	0	1	0	0	0	1	1	Data[11:4]								Data[3:0]				X	X	X	X	Write to DAC input register for channel D and update all DAC registers
0	0	1	0	0	1	0	0	Data[11:4]								Data[3:0]				X	X	X	X	Write to DAC input register for channel E and update all DAC registers
0	0	1	0	0	1	0	1	Data[11:4]								Data[3:0]				X	X	X	X	Write to DAC input register for channel F and update all DAC registers
0	0	1	0	0	1	1	0	Data[11:4]								Data[3:0]				X	X	X	X	Write to DAC input register for channel G and update all DAC registers
0	0	1	0	0	1	1	1	Data[11:4]								Data[3:0]				X	X	X	X	Write to DAC input register for channel H and update all DAC registers
0	0	1	0	1	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	Invalid code, no action performed
0	0	1	0	1	1	1	1	Data[11:4]								Data[3:0]				X	X	X	X	Broadcast mode, write to all input registers and update all DAC registers
Power-Down Register																								
0	1	0	0	X	X	X	X	X	PD1	PD0	DAC A	DAC B	DAC C	DAC D	DAC E	DAC F	DAC G	DAC H	X	X	X	X	X	
0	1	0	0	X	X	X	X	X	0	0	DAC A	DAC B	DAC C	DAC D	DAC E	DAC F	DAC G	DAC H	X	X	X	X	X	Each DAC bit set to '1' powers on selected DACs
0	1	0	0	X	X	X	X	X	0	1	DAC A	DAC B	DAC C	DAC D	DAC E	DAC F	DAC G	DAC H	X	X	X	X	X	Each DAC bit set to '1' powers down selected DACs. V_{OUT} connected to GND through 1kΩ pull-down resistor
0	1	0	0	X	X	X	X	X	1	0	DAC A	DAC B	DAC C	DAC D	DAC E	DAC F	DAC G	DAC H	X	X	X	X	X	Each DAC bit set to '1' powers down selected DACs. V_{OUT} connected to GND through 100kΩ pull-down resistor
0	1	0	0	X	X	X	X	X	1	1	DAC A	DAC B	DAC C	DAC D	DAC E	DAC F	DAC G	DAC H	X	X	X	X	X	Each DAC bit set to '1' powers down selected DACs. V_{OUT} is three-stated
Clear Code Register																								
0	1	0	1	X	X	X	X	X	X	X	X	X	X	X	X	X	X	CL1	CL0	X	X	X	X	
0	1	0	1	X	X	X	X	X	X	X	X	X	X	X	X	X	X	0	0	X	X	X	X	Write to clear code register, CLR pin clears to zero scale
0	1	0	1	X	X	X	X	X	X	X	X	X	X	X	X	X	X	0	1	X	X	X	X	Write to clear code register, CLR pin clears to midscale
0	1	0	1	X	X	X	X	X	X	X	X	X	X	X	X	X	X	1	0	X	X	X	X	Write to clear code register, CLR pin clears to full scale
0	1	0	1	X	X	X	X	X	X	X	X	X	X	X	X	X	X	1	1	X	X	X	X	Write to clear code register disables $\overline{CLR}$ pin
LDAC Register																								
0	1	1	0	X	X	X	X	DAC H	DAC G	DAC F	DAC E	DAC D	DAC C	DAC B	DAC A	X	X	X	X	X	X	X	X	When all DAC bits are set to '1', selected DACs ignore the $\overline{LDAC}$ pin. When all DAC bits are set to '0', selected DAC registers update according to the $\overline{LDAC}$ pin.
Software Reset																								
0	1	1	1	X	X	X	X	0	0	X	X	X	X	X	X	X	X	X	X	X	X	X	X	Software reset (default). Same as power-on reset (POR).
0	1	1	1	X	X	X	X	0	1	X	X	X	X	X	X	X	X	X	X	X	X	X	X	Software reset that sets device into High-Speed mode
0	1	1	1	X	X	X	X	1	0	X	X	X	X	X	X	X	X	X	X	X	X	X	X	Software reset that maintains High-Speed mode state

PRODUCT PREVIEW

Table 14. Control Matrix for Read Commands (see Table 10, Table 11, and Table 12 for 8-bit, 10-bit, and 12-bit mapping)

CA BYTE								MSDB								LSDB								DESCRIPTION
C3	C2	C1	C0	A3	A2	A1	A0	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	
Input Register																								
0	0	0	0	0	0	0	0	Data[11:4]								Data[3:0]				0	0	0	0	Read from DAC input register channel A
0	0	0	0	0	0	0	1	Data[11:4]								Data[3:0]				0	0	0	0	Read from DAC input register channel B
0	0	0	0	0	0	1	0	Data[11:4]								Data[3:0]				0	0	0	0	Read from DAC input register channel C
0	0	0	0	0	0	1	1	Data[11:4]								Data[3:0]				0	0	0	0	Read from DAC input register channel D
0	0	0	0	0	1	0	0	Data[11:4]								Data[3:0]				0	0	0	0	Read from DAC input register channel E
0	0	0	0	0	1	0	1	Data[11:4]								Data[3:0]				0	0	0	0	Read from DAC input register channel F
0	0	0	0	0	1	1	0	Data[11:4]								Data[3:0]				0	0	0	0	Read from DAC input register channel G
0	0	0	0	0	1	1	1	Data[11:4]								Data[3:0]				0	0	0	0	Read from DAC input register channel H
0	0	0	0	1	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	Invalid code
DAC Register																								
0	0	0	1	0	0	0	0	Data[11:4]								Data[3:0]				0	0	0	0	Read DAC A DAC register
0	0	0	1	0	0	0	1	Data[11:4]								Data[3:0]				0	0	0	0	Read DAC B DAC register
0	0	0	1	0	0	1	0	Data[11:4]								Data[3:0]				0	0	0	0	Read DAC C DAC register
0	0	0	1	0	0	1	1	Data[11:4]								Data[3:0]				0	0	0	0	Read DAC D DAC register
0	0	0	1	0	1	0	0	Data[11:4]								Data[3:0]				0	0	0	0	Read DAC E DAC register
0	0	0	1	0	1	0	1	Data[11:4]								Data[3:0]				0	0	0	0	Read DAC F DAC register
0	0	0	1	0	1	1	0	Data[11:4]								Data[3:0]				0	0	0	0	Read DAC G DAC register
0	0	0	1	0	1	1	1	Data[11:4]								Data[3:0]				0	0	0	0	Read DAC H DAC register
0	0	0	1	1	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	Invalid code
Power Down Register																								
0	1	0	0	X	X	X	X	0	0	0	0	0	0	PD1	PD0	DAC A	DAC B	DAC C	DAC D	DAC E	DAC F	DAC G	DAC H	Read power down register
Clear Code Register																								
0	1	0	1	X	X	X	X	0	0	0	0	0	0	0	0	0	0	0	0	0	0	CL1	CL0	Read clear code register
LDAC Register																								
0	1	1	0	X	X	X	X	0	0	0	0	0	0	0	0	DAC H	DAC G	DAC F	DAC E	DAC D	DAC C	DAC B	DAC A	Read LDAC register

POWER-ON RESET TO ZERO-SCALE OR MIDSCALE

The DACx578 contains a power-on reset (POR) circuit that controls the output voltage during power-on. For devices in the TSSOP package, at power-on, all DAC registers are filled with zeros and the output voltages of all DAC channels are set to zero-scale. For devices in the QFN package, all DAC registers are set to have all DAC channels power on depending of the state of the RSTSEL pin.

The RSTSEL pin value is read at power-on and should be set prior to or simultaneously with AV_{DD}. For RSTSEL set to AV_{DD}, the DAC channels are loaded with midscale code. If RSTSEL is set to ground, the DAC channels are loaded with zero-scale code. All DAC channels remain in this state until a valid write sequence and load command are sent to the respective DAC channel. The power-on reset function is useful in applications where it is important to know the output state of each DAC while the device is in the process of powering on.

LDAC FUNCTIONALITY

The DACx578 offers both software and hardware simultaneous updates and control functions. The DAC double-buffered architecture is designed so that new data can be entered for each DAC without disturbing the analog outputs.

The DACx578 data updates can be performed either in Synchronous or Asynchronous mode.

In Synchronous mode, data are updated on the falling edge of the acknowledge signal that follows LSDB. For Synchronous mode updates, the $\overline{\text{LDAC}}$ pin is not required and must be connected to GND permanently.

In Asynchronous mode, the $\overline{\text{LDAC}}$ pin is used as a negative-edge-triggered timing signal for asynchronous DAC updates. Multiple single-channel updates can be performed in order to set different channel buffers to desired values and then make a falling edge on the $\overline{\text{LDAC}}$ pin. The data buffers of all the channels must be loaded with the desired data before an $\overline{\text{LDAC}}$ falling edge. After a high-to-low $\overline{\text{LDAC}}$ transition, all DACs simultaneously update with the last contents of the corresponding data buffers. If the contents of a data buffer are not changed by the serial interface, the corresponding DAC output remains unchanged after the $\overline{\text{LDAC}}$ trigger.

Alternatively, all DAC outputs can be updated simultaneously using the built-in LDAC software function. The LDAC register offers additional flexibility and control, giving the ability to select which DAC channel(s) should update simultaneously when the hardware $\overline{\text{LDAC}}$ pin is being brought low. The LDAC register is loaded with an 8-bit word (DB15 to DB8) using control bits C3, C2, C1, and C0. The default value for each bit, and therefore each DAC channel, is zero and the external $\overline{\text{LDAC}}$ pin operates in normal mode. If the LDAC register bit for a selected DAC channel is set to '1', that DAC channel ignores the external $\overline{\text{LDAC}}$ pin and updates only through the software LDAC command. If, however, the LDAC register bit is set to '0', the DAC channel is controlled by the external $\overline{\text{LDAC}}$ pin (default).

This combination of both software and hardware simultaneous update functions is particularly useful in applications where only selective DAC channels are to be updated simultaneously, while the other channels remain unaffected and have synchronous channel updates. See table TBD for a graphical illustration and examples.

PRODUCT PREVIEW

POWER-DOWN COMMANDS

The DACx578 uses four modes of operation. These modes are accessed by using control bits C3, C2, C1, and C0. The control bits must be set to '0100'. When the control bits are set correctly, the four different power-down modes are software programmable by setting bits PD0 (DB13) and PD1 (DB14) in the control register. Table 15 shows how to control the operating mode with data bits PD0 (DB13), and PD1 (DB14). The DACx578 treats the power-down condition as data; all the operational modes are still valid for power down. It is possible to broadcast a power-down condition to all the DACx578s in a system. It is also possible to power-down a channel and update data on other channels. Further, it is possible to write to the DAC register/buffer of the DAC channel that is powered down. When the DAC channel is then powered on, it contains the new value.

When both the PD0 and PD1 bits are set to '0', the device works normally with its typical consumption of TBD mA at 5.5V. However, for the three power-down modes, the supply current falls to TBD mA at 5.5V (TBD mA at 2.7V). Not only does the supply current fall, but the output stage also switches internally from the output amplifier to a resistor network of known values.

The advantage of this switching is that the output impedance of the device is known while it is in power-down mode. As described in Table 15, there are three different power-down options. V_{OUT} can be connected internally to GND through a 1kΩ resistor, a 100kΩ resistor, or open-circuited (High-Z). The output stage is shown in Figure 2. In other words, C3, C2, C1, and C0 = '0100' and DB14 and DB13 = '11' represent a power-down condition with High-Z output impedance for a selected channel. DB14 and DB13 = '01' represents a power-down condition with 1kΩ output impedance, while DB14 and DB13 = '10' represents a power-down condition with 100kΩ output impedance.

Table 15. DAC Operating Modes

PD1 (DB14)	PD0 (DB13)	DAC OPERATING MODES
0	0	Power on selected DACs
0	1	Power down selected DACs, 1kΩ to GND
1	0	Power down selected DACs, 100kΩ to GND
1	1	Power down selected DACs, High-Z to GND

CLEAR CODE REGISTER AND $\overline{\text{CLR}}$ PIN

The DACx578 contains a clear code register. The clear code register can be accessed via the two-wire serial interface and is user-configurable. Bringing the $\overline{\text{CLR}}$ pin low clears the content of all DAC registers and all DAC buffers and replaces the code with the code determined by the clear code register. The clear code register can be written to by applying the commands showed in Table 13. The default setting of the clear code register sets the output of all DAC channels to 0V when the $\overline{\text{CLR}}$ pin is brought low. The $\overline{\text{CLR}}$ pin is falling-edge-triggered; therefore, the device exits clear code mode on the falling edge of the acknowledge signal that follows LSDB of the next write sequence. If the $\overline{\text{CLR}}$ pin is brought low during a write sequence, the write sequence is aborted and the DAC registers and DAC buffers are cleared.

When performing a software reset of the device, the clear code register is reset to the default mode (DB5 = '0', DB4 = '0'). Setting the clear code register to DB4 = '1' and DB5 = '1' ignores any activity on the external CLR pin.

SOFTWARE RESET FUNCTION

The DACx578 contains a software reset feature. When the software reset feature is executed, the device (all DAC channels) are reset to the power-on reset code. All registers within the device are reset to the respective default settings. The DAC offers the flexibility to go into High-Speed mode directly after resetting the device without sending the high-speed master code. The device can also stay in High-Speed mode after a reset if desired. See Table 13 (Software Reset subsection) for these extra feature settings.

PRODUCT PREVIEW

PACKAGING INFORMATION

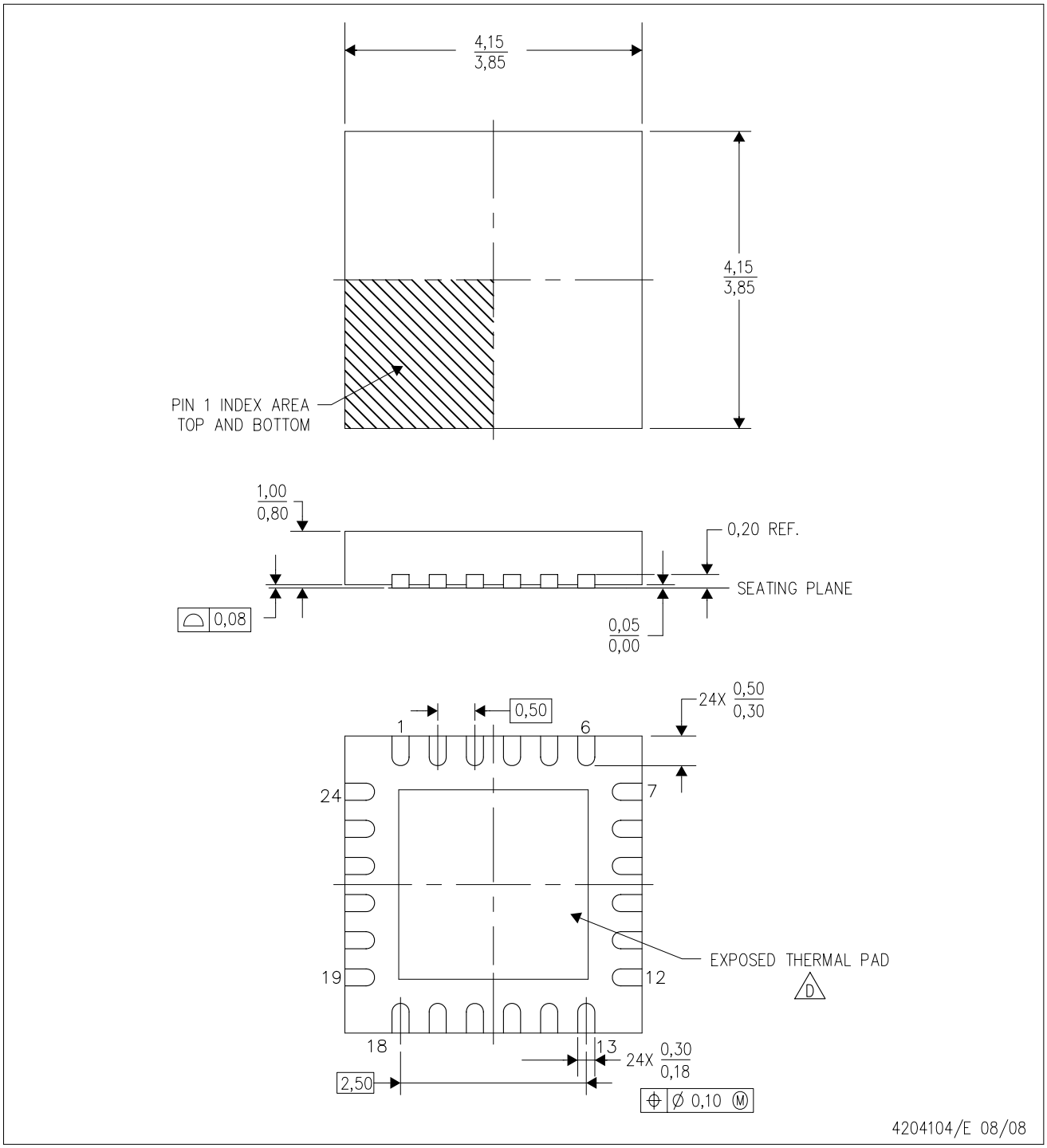
Orderable Device	Status [1]	Package Type	Package Drawing	Pins	Package Qty	Eco Plan [2]	Lead/Ball Finish	MSL Peak Temp [3]
DAC5578SPW	PREVIEW	TSSOP	PW	16	90	TBD	Call TI	Call TI
DAC5578SPWR	PREVIEW	TSSOP	PW	16	2000	TBD	Call TI	Call TI
DAC5578SRGER	PREVIEW	VQFN	RGE	24	3000	TBD	Call TI	Call TI
DAC5578SRGET	PREVIEW	VQFN	RGE	24	250	TBD	Call TI	Call TI
DAC6578SPW	PREVIEW	TSSOP	PW	16	90	TBD	Call TI	Call TI
DAC6578SPWR	PREVIEW	TSSOP	PW	16	2000	TBD	Call TI	Call TI
DAC6578SRGER	PREVIEW	VQFN	RGE	24	3000	TBD	Call TI	Call TI
DAC6578SRGET	PREVIEW	VQFN	RGE	24	250	TBD	Call TI	Call TI
DAC7578SPW	PREVIEW	TSSOP	PW	16	90	TBD	Call TI	Call TI
DAC7578SPWR	PREVIEW	TSSOP	PW	16	2000	TBD	Call TI	Call TI
DAC7578SRGER	PREVIEW	VQFN	RGE	24	3000	TBD	Call TI	Call TI
DAC7578SRGET	PREVIEW	VQFN	RGE	24	250	TBD	Call TI	Call TI

[1] The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

[2] Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

[3] MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

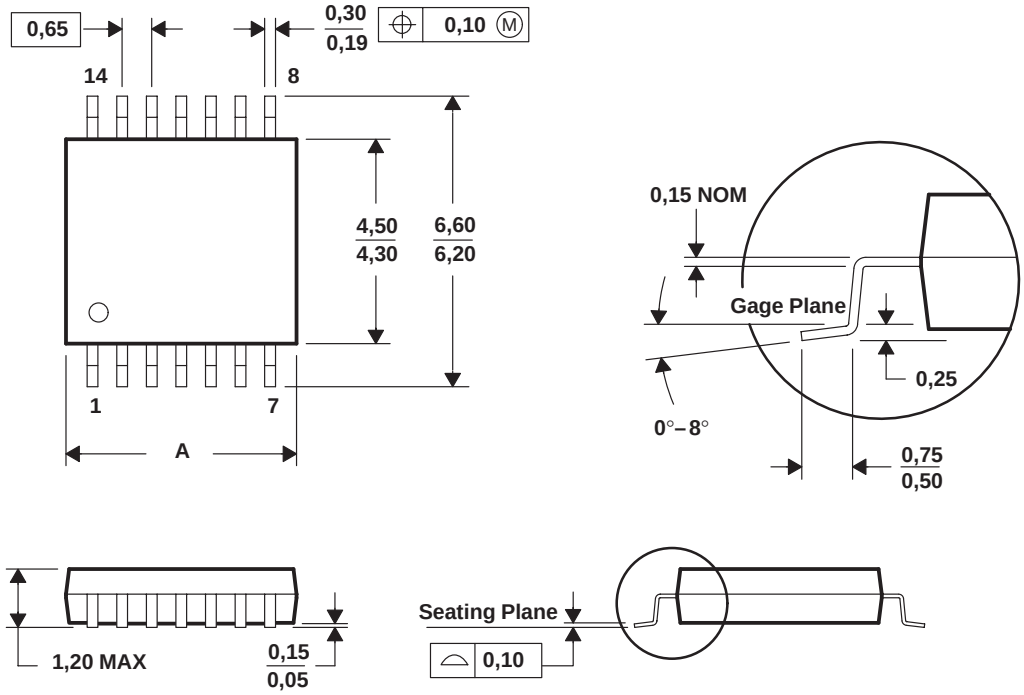
RGE (S–PVQFN–N24) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Quad Flatpack, No–Leads (QFN) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance. See the Product Data Sheet for details regarding the exposed thermal pad dimensions.
E. Falls within JEDEC MO–220.

PW (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

14 PINS SHOWN



DIM \ PINS **	8	14	16	20	24	28
A MAX	3,10	5,10	5,10	6,60	7,90	9,80
A MIN	2,90	4,90	4,90	6,40	7,70	9,60

4040064/F 01/97

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
D. Falls within JEDEC MO-153

IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, modifications, enhancements, improvements, and other changes to its products and services at any time and to discontinue any product or service without notice. Customers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All products are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its hardware products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by government requirements, testing of all parameters of each product is not necessarily performed.

TI assumes no liability for applications assistance or customer product design. Customers are responsible for their products and applications using TI components. To minimize the risks associated with customer products and applications, customers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any TI patent right, copyright, mask work right, or other TI intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information published by TI regarding third-party products or services does not constitute a license from TI to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of TI information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. Reproduction of this information with alteration is an unfair and deceptive business practice. TI is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

Resale of TI products or services with statements different from or beyond the parameters stated by TI for that product or service voids all express and any implied warranties for the associated TI product or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

TI products are not authorized for use in safety-critical applications (such as life support) where a failure of the TI product would reasonably be expected to cause severe personal injury or death, unless officers of the parties have executed an agreement specifically governing such use. Buyers represent that they have all necessary expertise in the safety and regulatory ramifications of their applications, and acknowledge and agree that they are solely responsible for all legal, regulatory and safety-related requirements concerning their products and any use of TI products in such safety-critical applications, notwithstanding any applications-related information or support that may be provided by TI. Further, Buyers must fully indemnify TI and its representatives against any damages arising out of the use of TI products in such safety-critical applications.

TI products are neither designed nor intended for use in military/aerospace applications or environments unless the TI products are specifically designated by TI as military-grade or "enhanced plastic." Only products designated by TI as military-grade meet military specifications. Buyers acknowledge and agree that any such use of TI products which TI has not designated as military-grade is solely at the Buyer's risk, and that they are solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI products are neither designed nor intended for use in automotive applications or environments unless the specific TI products are designated by TI as compliant with ISO/TS 16949 requirements. Buyers acknowledge and agree that, if they use any non-designated products in automotive applications, TI will not be responsible for any failure to meet such requirements.

Following are URLs where you can obtain information on other Texas Instruments products and application solutions:

Products		**Applications**	
Amplifiers	amplifier.ti.com	Audio	www.ti.com/audio
Data Converters	dataconverter.ti.com	Automotive	www.ti.com/automotive
DLP® Products	www.dlp.com	Communications and Telecom	www.ti.com/communications
DSP	dsp.ti.com	Computers and Peripherals	www.ti.com/computers
Clocks and Timers	www.ti.com/clocks	Consumer Electronics	www.ti.com/consumer-apps
Interface	interface.ti.com	Energy	www.ti.com/energy
Logic	logic.ti.com	Industrial	www.ti.com/industrial
Power Mgmt	power.ti.com	Medical	www.ti.com/medical
Microcontrollers	microcontroller.ti.com	Security	www.ti.com/security
RFID	www.ti-rfid.com	Space, Avionics & Defense	www.ti.com/space-avionics-defense
RF/IF and ZigBee® Solutions	www.ti.com/lprf	Video and Imaging	www.ti.com/video
		Wireless	www.ti.com/wireless-apps

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265