

SBAS271 - MARCH 2004

16-Bit, Quad Voltage Output Digital-to-Analog Converter

FEATURES

Low Glitch: 1nV-s (typ)Low Power: 18mW

Unipolar or Bipolar Operation
 Settling Time: 12μs to 0.003%

16-Bit Linearity and Monotonicity:
 -40°C to +85°C

 Programmable Reset to Mid-Scale or Zero-Scale

Data Readback

Double-Buffered Data Inputs

Internal Bandgap Voltage Reference

Power-On Reset

3V to 5V Logic Interface

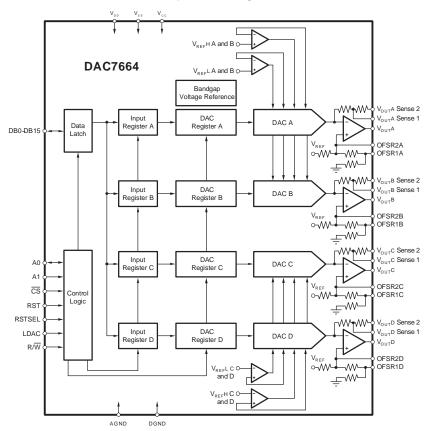
APPLICATIONS

- Process Control
- Closed-Loop Servo Control
- Motor Control
- Data Acquisition Systems
- DAC-per-Pin Programmers

DESCRIPTION

The DAC7664 is a 16-bit, quad voltage output digital-to-analog converter (DAC) with 16-bit monotonic performance over the specified temperature range. It accepts 16-bit parallel input data, has double-buffered DAC input logic (allowing simultaneous update of all DACs), and provides a readback mode of the internal input registers. Programmable asynchronous reset clears all registers to a mid-scale code of 8000h or to a zero-scale of 0000h. The DAC7664 can operate from a single +5V supply or from +5V and –5V supplies.

Low power and small size per DAC make the DAC7664 ideal for automatic test equipment, DAC-per-pin programmers, data acquisition systems, and closed-loop servo control. The DAC7664 is available in an LQFP-64 package and is specified for operation over the –40°C to +85°C temperature range.





This device has ESD-CDM sensitivity and special handling precautions must be taken.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

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ORDERING INFORMATION(1)

PRODUCT	PACKAGE-LEAD	PACKAGE DESIGNATOR	SPECIFIED TEMPERATURE RANGE	PACKAGE MARKING	ORDERING NUMBER	TRANSPORT MEDIA, QUANTITY
DA07004V	1 OED 04	DM	4000 1 0500	D 4 0 7 0 0 4 V	DAC7664YT	Tape and Reel, 250
DAC7664Y LQ	LQFP-64	PM	-40°C to +85°C	DAC7664Y	DAC7664YR	Tape and Reel, 1500
D 4 0 700 4 1/D			4000 / 0500	D.4.0700.43/D	DAC7664YBT	Tape and Reel, 250
DAC7664YB	LQFP-64	PM	−40°C to +85°C	DAC7664YB	DAC7664YBR	Tape and Reel, 1500
D.4.0700.4V0	1 OFD 04	DM	4000 1 0500	D 4 0 7 0 0 4 V 0	DAC7664YCT	Tape and Reel, 250
DAC7664YC	LQFP-64	PM	-40°C to +85°C	DAC7664YC	DAC7664YCR	Tape and Reel, 1500

⁽¹⁾ For the most current package and ordering information, see the Package Option Addendum located at the end of this data sheet.

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range unless otherwise noted(1)

	DAC7664	UNIT
IOV_{DD} , V_{CC} and V_{DD} to V_{SS}	-0.3 to 11	V
IOV _{DD} , V _{CC} and V _{DD} to GND	-0.3 to 5.5	V
Digital Input Voltage to GND	-0.3 to $V_{DD} + 0.3$	V
Digital Output Voltage to GND	-0.3 to $V_{DD} + 0.3$	V
ESD-CDM	200	V
Maximum Junction Temperature	+150	°C
Operating Temperature Range	-40 to +85	°C
Storage Temperature Range	-65 to +125	°C
Lead Temperature (soldering, 10s)	+300	°C

⁽¹⁾ Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to absolute maximum conditions for extended periods may degrade device reliability. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those specified is not implied.



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe

proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.



		'	DAC7664Y		D/	C7664	ΥB	DA	C7664		
PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	UNIT
Accuracy		-1									
Linearity error			±3	±4		±2	±3		*	*	LSB
Linearity match			±4			±2			*		LSB
Differential linearity error			±2	±3		±1	±2	-1		+2	LSB
Monotonicity, T _{MIN} to T _{MAX}		14			15			16			Bit
Unipolar zero error			±1	±5		*	*		*	*	mV
Unipolar zero error drift			5	10		*	*		*	*	ppm/°C
Full-scale error			±6	±20		±4	±12.5		*	*	mV
Full-scale error drift			7	15		*	*		*	*	ppm/°C
Unipolar zero matching	Channel-to-channel matching		±3	±7		±2	±5		*	*	mV
Full-scale matching	Channel-to-channel matching		±4	±10		±2	±8		*	*	mV
Power-supply rejection ratio (PSRR)	At full-scale		10	100		*	*		*	*	ppm/V
Analog Output											
Voltage output	R _L = 10kΩ	0		2.5	*		*	*		*	V
Output current	_ · · · · · ·	-1.25		+1.25	*		*	*		*	mA
Maximum load capacitance	No oscillation	1	500		<u> </u>	*	•	<u> </u>	*		pF
Short-circuit current	140 COMMUNITY		±20			*			*		mA
Short-circuit duration	GND or V _{CC}		Indefinite			*			*		1117 (
Dynamic Performance	GIVE OF VCC		macimile			-1-					
Settling time	To ±0.003%, 2.5V output step		12	15		*	*		*	*	μs
Channel-to-channel crosstalk	10 ±0.00076, 2.5V Output Step		0.5	10		*	-11		*	71.	LSB
Digital feedthrough			2			*			*		nV-s
Output noise voltage	f = 10kHz		130			*			*		nV/√Hz
Output hoise voitage			130			小			<u>т</u>		IIV/VIIZ
DAC glitch	7FFFh to 8000h or 8000h to 7FFFh		1	5		*	*		*	*	nV-s
Digital Input											
V_{IH}		$0.7 \times IOV_{I}$	DD		*			*			V
V _{IL}			0.3	\times IOV _{DD}			*			*	V
IIH				±10			*			*	μΑ
IIL				±10			*			*	μΑ
Digital Output	l	·									
VOH	I _{OH} = -0.8mA, IOV _{DD} = 5V	3.6	4.5		*	*		*	*		V
V _{OL}	I _{OL} = 1.6mA, IOV _{DD} = 5V		0.3	0.4		*	*		*	*	V
VOH	$I_{OH} = -0.4$ mA, $IOV_{DD} = 3V$	2.4	2.6		*	*		*	*		V
V _{OL}	I _{OL} = 0.8mA, IOV _{DD} = 3V		0.3	0.4		*	*		*	*	V
Power Supply	102 00										
V _{DD}		+4.75	+5.0	+5.25	*	*	*	*	*	*	V
IOV _{DD}		+2.7	+5.0	+5.25	*	*	*	*	*	*	V
VCC		+4.75	+5.0	+5.25	*	*	*	*	*	*	V
V _{SS}		0	0	0	*	*	*	*	*	*	V
ICC		1	3.5	5		*	*		*	*	mA
I _{DD}			50			*	•		*	•	μА
I(IOV _{DD})			50			*		-	*		μΑ
Power			18	25		*	*		*		mW
Temperature Range	<u> </u>	1	10			-1-	-1-		-1-		11144
Specified performance		40		, 05	Ψ.		*	*		*	°C
opeomed periormance	1	-40		+85	*		*	~		4	

 * specifications same as the grade to the left



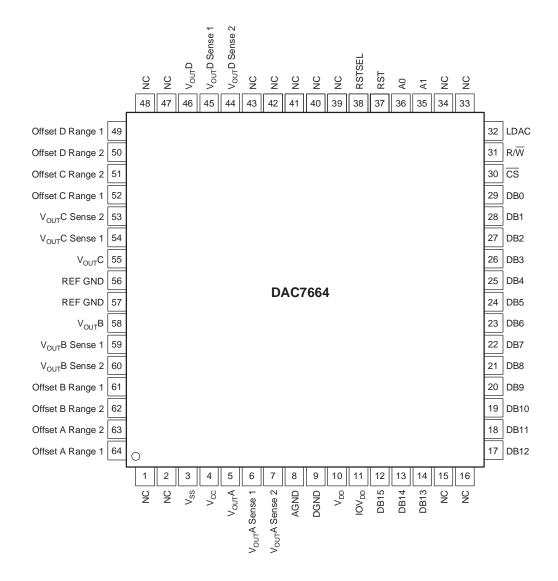
			DAC7664Y		DA	C7664	YB	DAC7664YC			
PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	UNIT
Accuracy	l										ı
Linearity error			±3	±4		±2	±3		*	*	LSB
Linearity match			±4			<u>+2</u>			*		LSB
Differential linearity error			±2	±3		±1	±2	-1		+2	LSB
Monotonicity, T _{MIN} to T _{MAX}		14			15			16			Bit
Bipolar zero error		+	±1	±5		*	*		*	*	mV
Bipolar zero error drift		+	5	10		*	*		*	*	ppm/°C
Full-scale error			±6	±20		±4	±12.5		*	*	mV
Full-scale error drift			7	15		*	*		*	*	ppm/°C
Bipolar zero matching	Channel-to-channel matching		±3	±7		±2	±5		*	*	mV
Full-scale matching	Channel-to-channel matching		±4	±10		±2	±8		*	*	mV
Power-supply rejection ratio (PSRR)	At full-scale	+	10	100		*	*		*	*	ppm/V
Analog Output	At Itili-scale		10	100		-1	- T				ррпі, у
Voltage output	R 10k0	-2.5		+2.5	*		*	*		*	V
Output current	$R_L = 10k\Omega$	-2.5 -1.25		+2.5	*		*	*		*	mA
*	No cocillation	-1.25	E00	+1.25	*	*	不	*	-1-	不	
Maximum load capacitance	No oscillation		500						*		pF
Short-circuit current	OND W		-15, +30			*			*		mA
Short-circuit duration	GND or V _{CC} or V _{SS}		Indefinite			*			*		
Dynamic Performance	T=	1			1			ı			ı
Settling time	To ±0.003%, 5V output step		12	15		*	*		*	*	μs
Channel-to-channel crosstalk			0.5			*			*		LSB
Digital feedthrough			2			*			*		nV-s
Output noise voltage	f = 10kHz		200			*			*		nV/√Hz
DAC glitch	7FFFh to 8000h or 8000h to 7FFFh		2	7		*	*		*	*	nV-s
Digital Input											
VIH		0.7 × IOV	DD		*			*			V
V_{IL}			0.3	× IOV _{DD}			*			*	V
IH				±10			*			*	μА
				±10			*			*	μA
Digital Output								l .			
VOH	I _{OH} = -0.8mA, IOV _{DD} = 5V	3.6	4.5		*	*		*	*		V
V _{OL}	I _{OL} = 1.6mA, IOV _{DD} = 5V	+	0.3	0.4		*	*		*	*	V
VOH	$I_{OH} = -0.4$ mA, $IOV_{DD} = 3V$	2.4	2.6	0.1	*	*		*	*		V
VOL	I _{OL} = 0.8mA, IOV _{DD} = 3V		0.3	0.4		*	*		*	*	V
Power Supply	ЮГ = 0:0ШУ, Ю ДД = 34		0.5	0.4		-11	٠٠ <u>-</u>			71	V
V _{DD}		+4.75	+5.0	+5.25	*	*	*	*	*	*	V
IOV _{DD}		+2.7	+5.0	+5.25	*	*	*	*	*	*	V
VCC		+4.75	+5.0	+5.25	*	*	*	*	*	*	V
VSS		-5.25	-5.0	-4.75	*	*	*	*	*	*	V
ICC			4	5.5		*	*	<u> </u>	*	*	mA
IDD		+	50			*			*		μА
I(IOV _{DD})		+	50			*			*		μΑ
ISS		-3.5	-2.0		*	*		*	*		mA
Power		+	30	45		*	*		*		mW
Temperature Range	1										I.
Specified performance	ı	-40		+85	*		*	*		*	°C

 $[\]boldsymbol{\ast}$ specifications same as the grade to the left



PIN ASSIGNMENTS

LQFP PACKAGE (TOP VIEW)





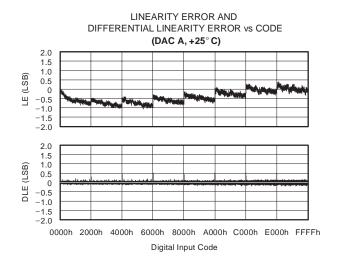
Terminal Functions

PIN	NAME	DESCRIPTION
1	NC	No Connection
2	NC	No Connection
3	Vss	Analog –5V power supply or 0V single supply
4	Vcc	Analog +5V power supply
5	VoutA	DAC A output voltage
6	V _{OUT} A Sense 1	Connect to VOUTA for unipolar mode
7	V _{OUT} A Sense 2	Connect to VOUTA for bipolar mode
8	AGND	Analog ground
9	DGND	Digital ground
10	V_{DD}	Digital +5V power supply
11	IOV _{DD}	Interface power supply
12	DB15	Data bit 15 (MSB)
13	DB14	Data bit 14
14	DB13	Data bit 13
15	NC	No connection
16	NC	No connection
17	DB12	Data bit 12
18	DB11	Data bit 11
19	DB10	Data bit 10
20	DB9	Data bit 9
21	DB8	Data bit 8
22	DB7	Data bit 7
23	DB6	Data bit 6
24	DB5	Data bit 5
25	DB4	Data bit 4
26	DB3	Data bit 3
27	DB2	Data bit 2
28	DB1	Data bit 1
29	DB0	Data bit 0
30	CS	Chip select, active low
31	R/W	Enabled by CS; controls the data read and data write.
32	LDAC	DAC register load control, rising edge triggered.
33	NC	No connection
34	NC	No connection
35	A1	Enabled by CS; in combination with A0, selects the individual DAC input registers.
36	A0	Enabled by CS; in combination with A1, selects the individual DAC input registers.
37	RST	Reset, rising edge triggered. Depending on the state of RSTSEL, the DAC registers are set to either mid-scale or zero.

RSTSEL Reset select. Determines the action of R If high, an RST command sets the DAC registers to mid-scale (8000h). If low, an command sets the DAC registers to zero (0000h). NC No connection Ad VOUTD Connect to VOUTD for bipolar mode Sense 2 NC No connection NC No connect to Offset D Range 2 for unipolar mode Connect to Offset D Range 1 for unipolar mode To Offset C Connect to Offset C Range 1 for unipolar mode Connect to Offset C Range 2 for unipolar mode NC NOUTC Connect to VOUTC for bipolar mode NC NOUTC Connect to VOUTC for unipolar mode NC NOUTC DAC C output NC No connect to VOUTC for unipolar mode NC NOUTC DAC C output NC No connect to VOUTC for unipolar mode NC NOUTC DAC B output NC No connect to VOUTC for unipolar mode NC NOUTC Connect to VOUTC for unipolar mode NC NC NOUTC DAC B output NC NO COUTC Connect to VOUTC for unipolar mode NC N	PIN	NAME	DESCRIPTION
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49 Offset D Range 1 mode 50 Offset D Range 2 Connect to Offset D Range 1 for unipolar mode 51 Offset C Range 2 Connect to Offset C Range 1 for unipolar mode 52 Offset C Range 1 mode 53 VOUTC Sense 2 54 VOUTC Sense 1 55 VOUTC DAC Coutput 56 REF GND Reference ground 57 REF GND Reference ground 58 VOUTB Sense 1 59 VOUTB Sense 1 60 VOUTB Sense 2 61 Offset B Range 1 Connect to VOUTB for bipolar mode Connect to VOUTB Sense 2 61 Offset B Range 1 Connect to VOUTB for unipolar mode	47	NC	No connection
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53 VOUTC Sense 2 54 VOUTC Sense 1 55 VOUTC DAC C output 56 REF GND Reference ground 57 REF GND Reference ground 58 VOUTB DAC B output 59 VOUTB Sense 1 60 VOUTB Sense 2 61 Offset B Range 1 Connect to VOUTC for unipolar mode Connect to VOUTB for unipolar mode Connect to VOUTB for unipolar mode Connect to VOUTB for bipolar mode	52		Connect to Offset C Range 2 for unipolar
Sense 2 54 VOUTC Sense 1 55 VOUTC DAC C output 56 REF GND Reference ground 57 REF GND Reference ground 58 VOUTB DAC B output 59 VOUTB Connect to VOUTB for unipolar mode 60 VOUTB Connect to VOUTB for bipolar mode 60 VOUTB Sense 2 61 Offset B Range 1 Connect to Offset B Range 2 for unipolar mode			
Sense 1 55 VOUTC DAC C output 56 REF GND Reference ground 57 REF GND Reference ground 58 VOUTB DAC B output 59 VOUTB Connect to VOUTB for unipolar mode 60 VOUTB Sense 1 60 VOUTB Connect to VOUTB for bipolar mode 61 Offset B Range 1 Connect to Offset B Range 2 for unipolar mode	53		
56 REF GND Reference ground 57 REF GND Reference ground 58 VOUTB DAC B output 59 VOUTB Connect to VOUTB for unipolar mode 60 VOUTB Sense 2 61 Offset B Range 1 60 Connect to Offset B Range 2 for unipolar mode	54		Connect to VOUTC for unipolar mode
57 REF GND Reference ground 58 VOUTB DAC B output 59 VOUTB Sense 1 60 VOUTB Connect to VOUTB for unipolar mode 60 VOUTB Sense 2 61 Offset B Range 1 60 Connect to Offset B Range 2 for unipolar mode	55	VoutC	DAC C output
58 VOUTB DAC B output 59 VOUTB Connect to VOUTB for unipolar mode 60 VOUTB Connect to VOUTB for bipolar mode 61 Offset B Connect to Offset B Range 2 for unipolar mode	56	REF GND	Reference ground
59 VOUTB Sense 1 Connect to VOUTB for unipolar mode VOUTB Sense 2 Connect to VOUTB for bipolar mode Connect to VOUTB for bipolar mode Sense 2 Connect to Offset B Range 2 for unipolar mode mode	57	REF GND	Reference ground
Sense 1 60 VOUTB Connect to VOUTB for bipolar mode Sense 2 61 Offset B Connect to Offset B Range 2 for unipolar mode	58	V _{OUT} B	
Sense 2 61 Offset B Connect to Offset B Range 2 for unipolar mode	59		Connect to V _{OUT} B for unipolar mode
Range 1 mode	60		Connect to VOUTB for bipolar mode
	61		Connect to Offset B Range 2 for unipolar mode
62 Offset B Connect to Offset B Range 1 for unipolar Range 2 mode	62	Offset B Range 2	Connect to Offset B Range 1 for unipolar mode
63 Offset A Connect to Offset A Range 1 for unipolar Range 2 mode	63		Connect to Offset A Range 1 for unipolar mode
	64	Offset A	Connect to Offset A Range 2 for unipolar mode



TYPICAL CHARACTERISTICS: $V_{SS} = 0V (+25^{\circ}C)$



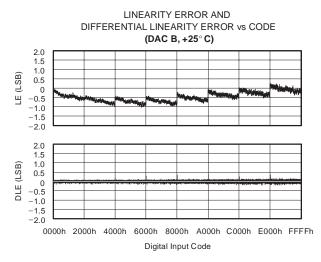
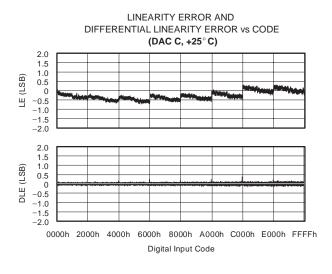


Figure 1

Figure 2



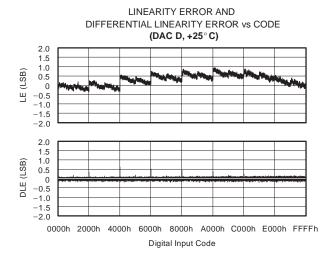
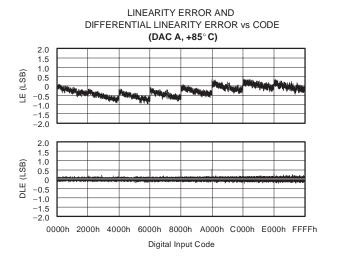


Figure 3

Figure 4



TYPICAL CHARACTERISTICS: V_{SS} = 0V (+85°C)



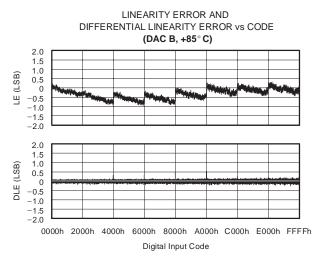
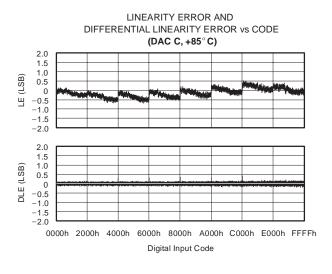


Figure 5

Figure 6



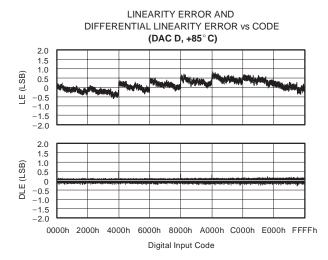
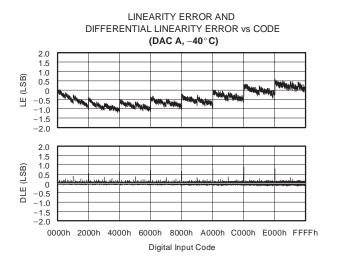


Figure 7

Figure 8



TYPICAL CHARACTERISTICS: $V_{SS} = 0V (-40^{\circ}C)$



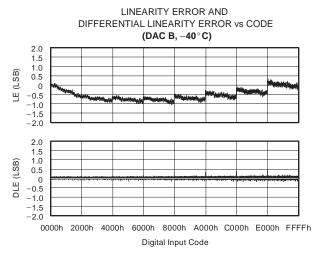
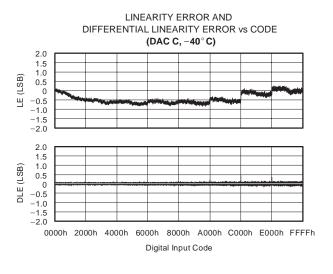


Figure 9

Figure 10



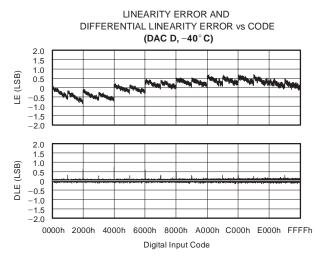


Figure 11

Figure 12



TYPICAL CHARACTERISTICS: V_{SS} = 0V

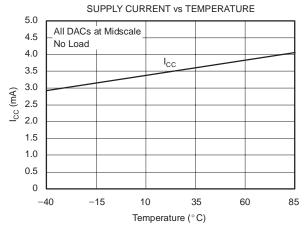


Figure 13

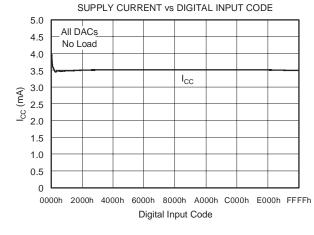


Figure 14

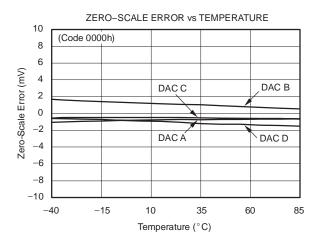


Figure 15

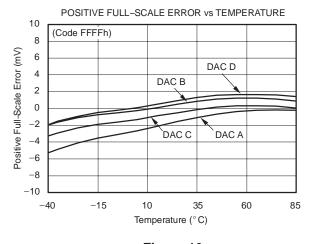


Figure 16

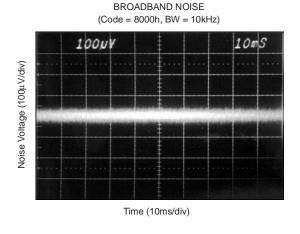


Figure 17

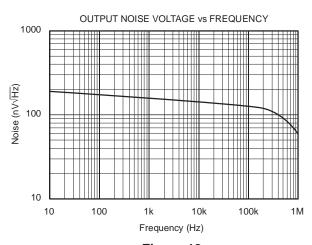


Figure 18



TYPICAL CHARACTERISTICS: $V_{SS} = 0V$ (continued)

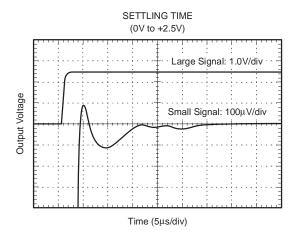


Figure 19

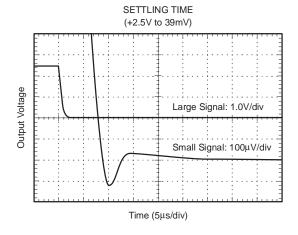


Figure 20

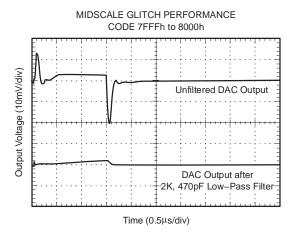


Figure 21

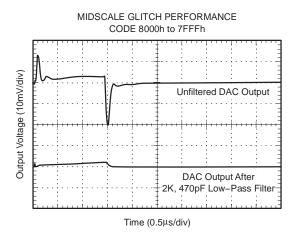


Figure 22

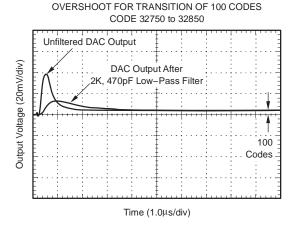


Figure 23

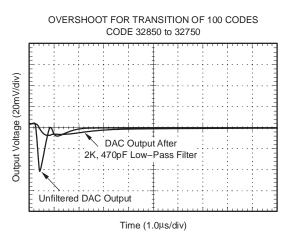


Figure 24



TYPICAL CHARACTERISTICS: V_{SS} = 0V (continued)

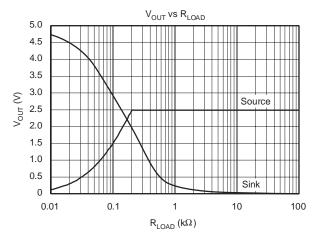


Figure 25

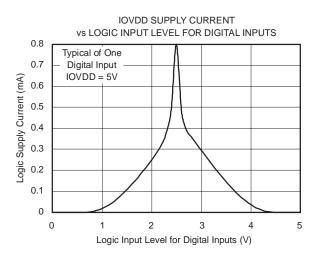


Figure 26



2.0 1.5 1.0 0.5 0

-0.5 -1.0 -1.5 -2.0

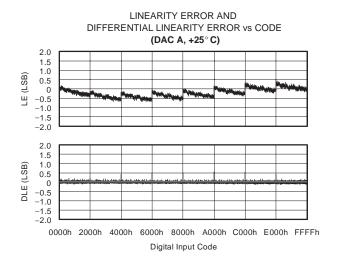
1.5 1.0 0.5 0 -0.5 -1.0

-1.5

LE (LSB)

DLE (LSB)

TYPICAL CHARACTERISTICS: $V_{SS} = -5V$ (+25°C)



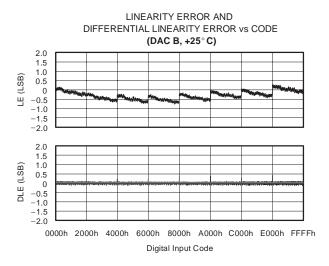


Figure 27

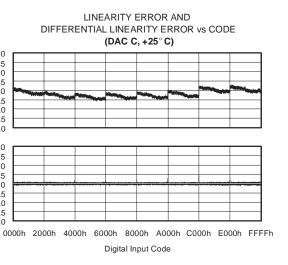


Figure 28

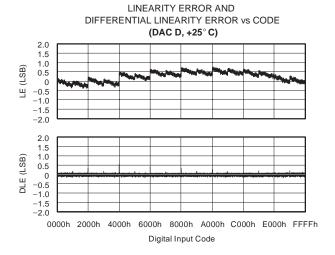
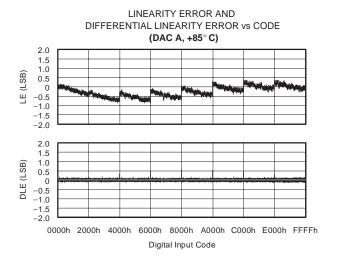


Figure 29

Figure 30



TYPICAL CHARACTERISTICS: $V_{SS} = -5V$ (+85°C)



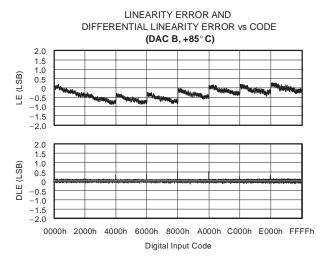
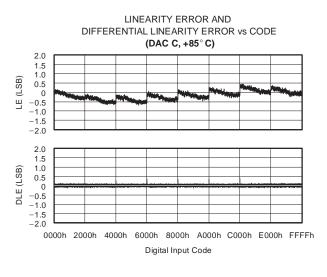


Figure 31

Figure 32



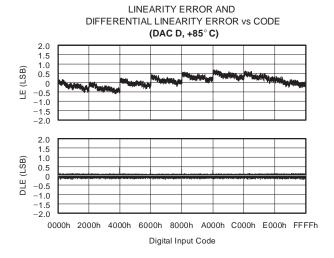
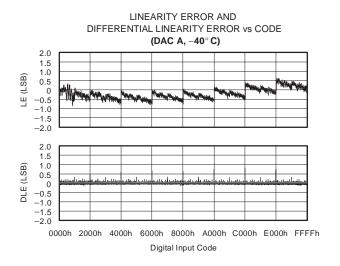


Figure 33

Figure 34



TYPICAL CHARACTERISTICS: $V_{SS} = -5V$ (-40°C)



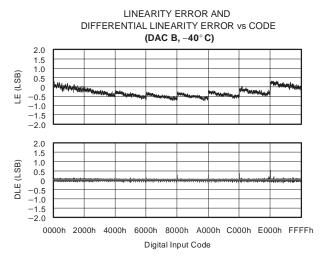
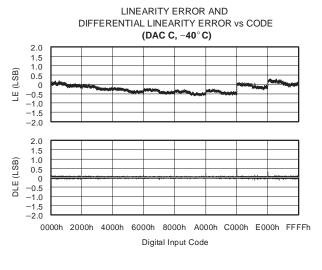


Figure 35

Figure 36



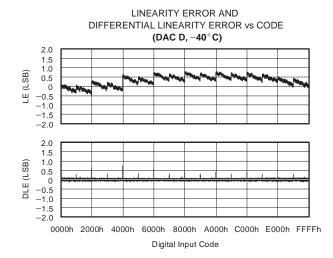
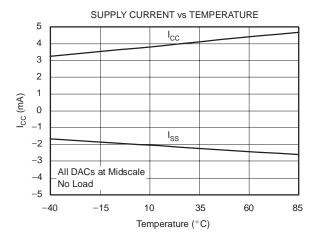


Figure 37

Figure 38



TYPICAL CHARACTERISTICS: V_{SS} = -5V



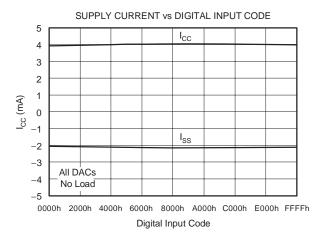
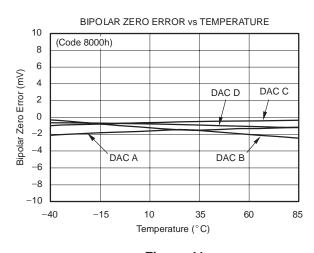


Figure 39





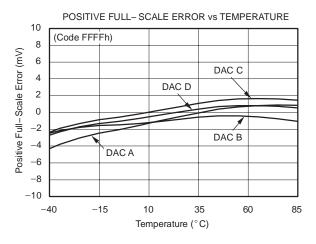


Figure 41

Figure 42

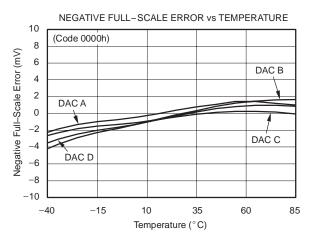
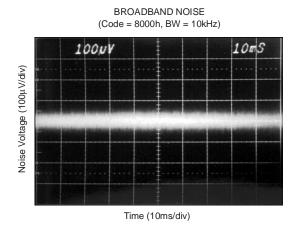


Figure 43



TYPICAL CHARACTERISTICS: $V_{SS} = -5V$ (continued)



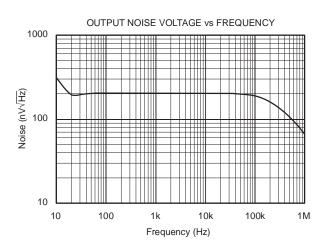
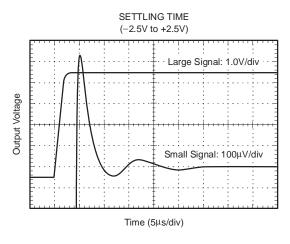


Figure 44

Figure 45



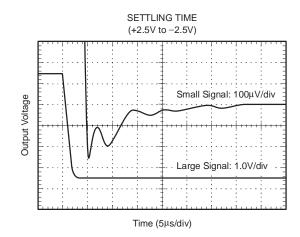
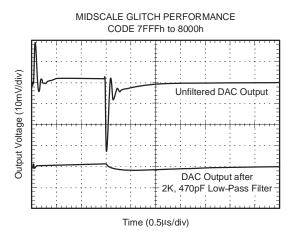


Figure 46

Figure 47



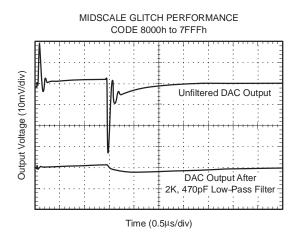
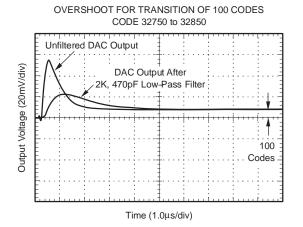


Figure 48 Figure 49



TYPICAL CHARACTERISTICS: $V_{SS} = -5V$ (continued)

All specifications at $T_A = 25^{\circ}C$, $IOV_{DD} = V_{DD} = V_{CC} = +5V$, $V_{SS} = -5V$, representative unit, unless otherwise noted.



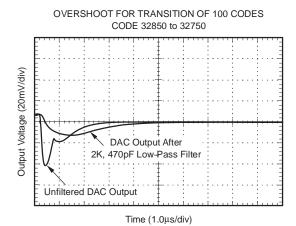


Figure 50

Figure 51

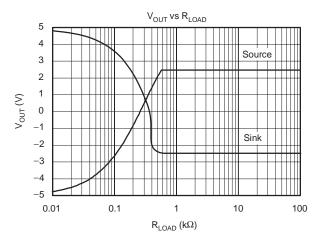


Figure 52



THEORY OF OPERATION

The DAC7664 is a quad voltage output 16-bit DAC. The architecture is an R–2R ladder configuration with the three most significant bits (MSBs) segmented, followed by an operational amplifier that serves as a buffer. Each DAC has its own R–2R ladder network, segmented MSBs, and output op amp, as shown in Figure 53. The minimum voltage output (zero-scale) and maximum voltage output (full-scale) are set by the internal voltage references and the resistors associated with the output operational amplifier.

The digital input is a 16-bit parallel word and the DAC input registers offer readback capability. The converters can be powered from either a single +5V supply or a dual ± 5 V supply. The device offers a reset function that immediately sets all DAC output voltages and DAC registers to mid-scale (code 8000h) or to zero-scale, code 0000h. See Figure 54 and Figure 55 for the basic operation of the DAC7664.

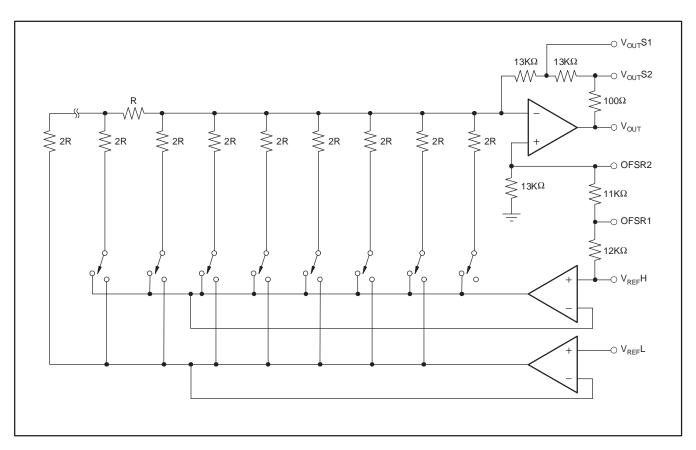


Figure 53. DAC7664 Architecture



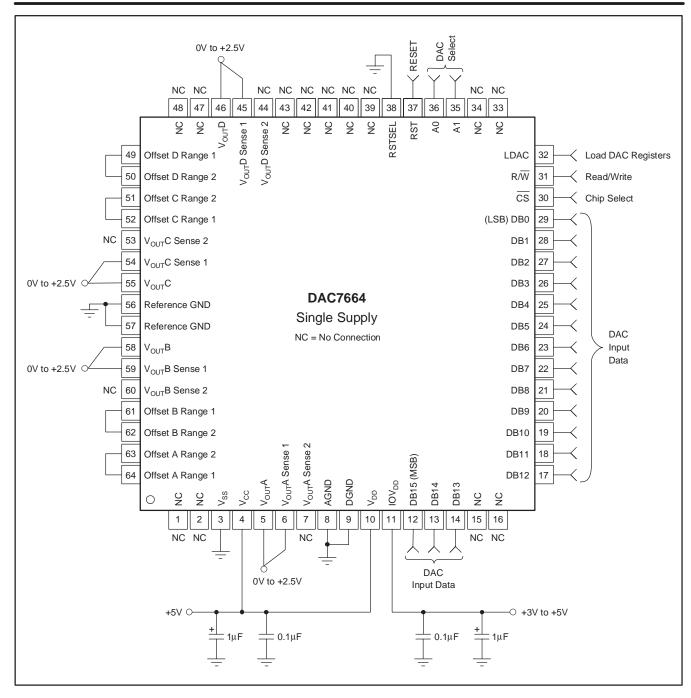


Figure 54. Basic Single-Supply Operation of the DAC7664



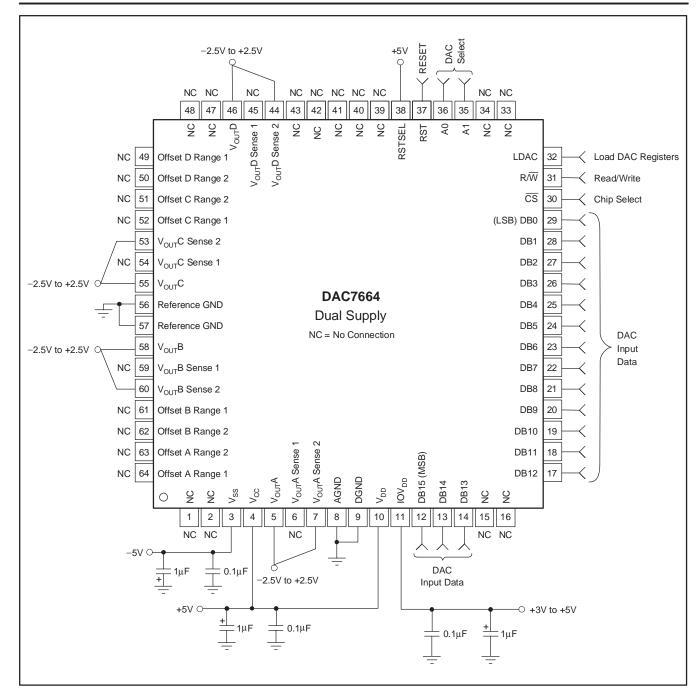


Figure 55. Basic Dual-Supply Operation of the DAC7664



ANALOG OUTPUTS

When $V_{SS} = -5V$ (dual-supply operation), the output amplifier can swing to within 2.25V of the supply rails over a range of -40° C to $+85^{\circ}$ C. When $V_{SS} = 0V$ (single-supply operation), and with R_{LOAD} also connected to ground, the output can swing to within 5mV of ground. Care must be taken when measuring the zero-scale error when $V_{SS} = 0V$. Since the output voltage cannot swing below ground, the output voltage may not change for the first few digital input codes (0000h, 0001h, 0002h, etc.) if the output amplifier has a negative offset.

Due to the high accuracy of these DACs, system design problems such as grounding and contact resistance are very important. A 16-bit converter with a 2.5V full-scale range has a 1LSB value of $38\mu V$. With a load current of 1mA, series wiring and connector resistance of only $40m\Omega$ (R_{W2}) will cause a voltage drop of $40\mu V$, as shown in Figure 56. To understand what this means in terms of system layout, the resistivity of a typical 1-ounce copper-clad printed circuit board is 1/2 $m\Omega$ per square. For a 1mA load, a 0.01-inch-wide printed circuit conductor 0.6 inches long will result in a voltage drop of $30\mu V$.

The DAC7664 offers a force and sense output configuration for the high open-loop gain output amplifier. This feature allows the loop around the output amplifier to be closed at the load (as shown in Figure 56), thus ensuring an accurate output voltage.

DIGITAL INTERFACE

Table 1 shows the basic control logic for the DAC7664. Note that each internal register is edge-triggered and not level-triggered. When the LDAC signal is transitioned to high, the digital word currently in the register is latched. The first set of registers (the input registers) are triggered via the A0, A1, R/\overline{W} , and \overline{CS} inputs. Only one of these registers is transparent at any given time.

The double-buffered architecture is designed mainly so each DAC input register can be written to at any time and then all DAC voltages updated simultaneously by the rising edge of LDAC. It also allows a DAC input register to be written to at any point and the DAC voltages to be synchronously changed via a trigger signal connected to LDAC.

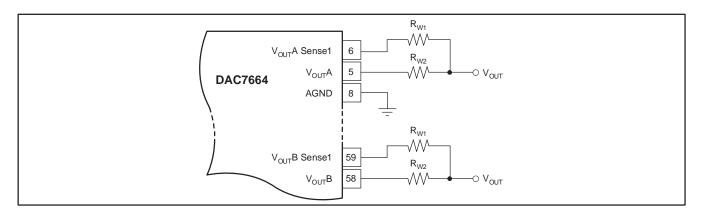


Figure 56. Analog Output Closed-Loop Configuration (1/2 DAC7664). RW represents wiring resistances.

				10	1010 1. D/	101001	Logio matti iak			
A1	A0	R/W	cs	RST	RSTSEL	LDAC	INPUT REGISTER	DAC REGISTER	MODE	DAC
L	L	L	L	Н	Х	Х	Write	Hold	Write input	Α
L	Н	L	L	Н	Х	Х	Write Hold Write inpu		Write input	В
Н	L	L	L	Н	Х	Х	Write Hold Write		Write input	С
Н	Н	L	L	Н	Х	Х	Write Hold		Write input	D
L	L	Н	L	Н	Х	Х	Read Hold		Read input	Α
L	Н	Н	L	Н	Х	Х	Read Hold		Read input	В
Н	L	Н	L	Н	Х	Х	Read	Hold	Read input	С
Н	Н	Н	L	Н	Х	Х	Read	Hold	Read input	D
Х	Х	Х	Н	Н	Х	1	Hold	Write	Update	All
Х	Х	Х	Н	Н	Х	Н	Hold	Hold	Hold	All
Х	Х	Х	Х	1	L	Х	Reset to zero	Reset to zero	Reset to zero	All
Χ	Х	Х	Х	1	Н	Х	Reset to mid-scale	Reset to mid-scale	Reset to mid-scale	All

Table 1. DAC7664 Logic Truth Table



3V TO 5V LOGIC INTERFACE

All of the digital input and output pins are compatible with any logic supply voltage between 3V and 5V. Connect the interface logic supply voltage to the IOV_{DD} pin. Note that the internal digital logic operates from 5V, so the VDD pin must connect to a 5V supply.

GLITCH SUPPRESSION CIRCUIT

Figure 21, Figure 22, Figure 48, and Figure 49 show the typical DAC output when switching between codes 7FFFh and 8000h. For R-2R ladder DACs, this is potentially the worst-case glitch condition, since every switch in the DAC changes state. To minimize the glitch energy at this and other code pairs with possible high-glitch outputs, an internal track-and-hold circuit is used to maintain the DAC ouput voltage at a nearly constant level during the internal switching interval. This track-and-hold circuit is activated only when the transition is at, or close to, one of the code pairs with the high-glitch possibility.

It is advisable to avoid digital transitions within $1\mu s$ of the rising edge of the LDAC signal. These signals can affect the charge on the track-and-hold capacitor, thus increasing the glitch energy.

DIGITAL TIMING

Figure 57 and Table 2 provide detailed timing information for the digital interface of the DAC7664.

DIGITAL INPUT CODING

The DAC7664 input data is in straight binary format. The output voltage for single-supply operation is given by Equation 1:

$$V_{OUT} = \frac{2.5 \times N}{65,536} \tag{1}$$

where N is the digital input code.

This equation does not include the effects of offset (zero-scale) or gain (full-scale) errors.

The output for the dual supply operation is given by Equation 2:

$$V_{OUT} = \frac{5 \times N}{65,536} - 2.5 \tag{2}$$



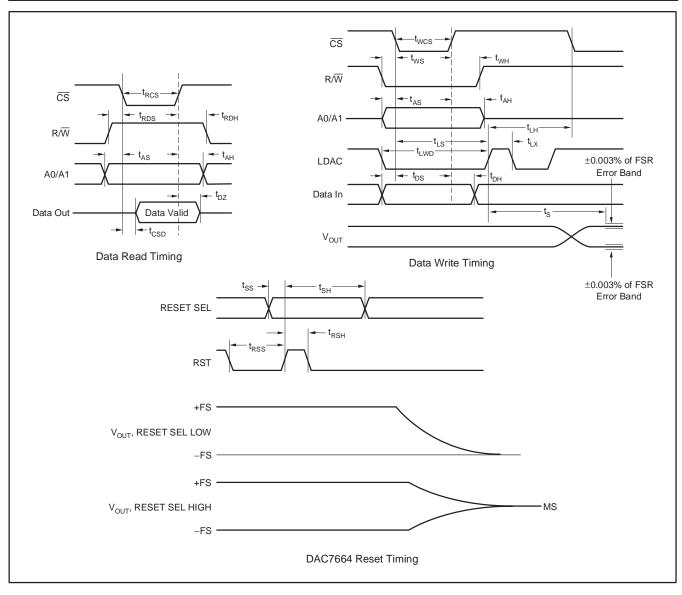


Figure 57. Digital Input and Output Timing



Table 2. Timing Specifications for Figure 57

SYMBOL	DESCRIPTION	MIN	TYP	MAX	UNITS
tRCS	CS low for read	150			ns
t _{RDS}	R/W high to CS low	10			ns
^t RDH	R/W high after CS high	10			ns
t _{DZ}	CS high to data bus in high impedance	10		100	ns
^t CSD	CS low to data bus valid		100	150	ns
twcs	CS low for write	40			ns
tws	R/W low to CS low	0			ns
^t WH	R/W low after CS high	10			ns
tAS	Address valid to CS low	0			ns
t _{AH}	Address valid after CS high	10			ns
tLS	CS low to LDAC high	30			ns
t _L H	CS low after LDAC high	100			ns
tLX	LDAC high	100			ns
t _{DS}	Data valid to CS low	0			ns
^t DH	Data valid after CS low	10			ns
tLWD	LDAC low	100			ns
tss	RSTSEL valid before RST high	0			ns
^t SH	RSTSEL valid after RST high	200			ns
^t RSS	RSTSEL low before RST high	10			ns
^t RSH	RSTSEL low after RST high	10			ns
ts	Settling time		12		μs



PACKAGE OPTION ADDENDUM

www.ti.com 16-Apr-2009

PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Packag Qty	e Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp ⁽³⁾
DAC7664YBR	ACTIVE	LQFP	PM	64	1500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
DAC7664YBRG4	ACTIVE	LQFP	PM	64	1500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
DAC7664YBT	ACTIVE	LQFP	PM	64	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
DAC7664YBTG4	ACTIVE	LQFP	PM	64	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
DAC7664YCR	ACTIVE	LQFP	PM	64	1500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
DAC7664YCRG4	ACTIVE	LQFP	PM	64	1500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
DAC7664YCT	ACTIVE	LQFP	PM	64	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
DAC7664YCTG4	ACTIVE	LQFP	PM	64	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
DAC7664YR	ACTIVE	LQFP	PM	64	1500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
DAC7664YRG4	ACTIVE	LQFP	PM	64	1500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
DAC7664YT	ACTIVE	LQFP	PM	64	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
DAC7664YTG4	ACTIVE	LQFP	PM	64	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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PACKAGE OPTION ADDENDUM

www.ti.com 16-Apr-2009

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

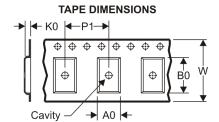




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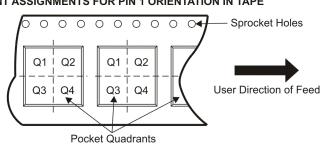
TAPE AND REEL INFORMATION





	Dimension designed to accommodate the component width
В0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing		SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
DAC7664YBR	LQFP	PM	64	1500	330.0	24.8	12.3	12.3	2.5	16.0	24.0	Q2
DAC7664YBT	LQFP	PM	64	250	330.0	24.8	12.3	12.3	2.5	16.0	24.0	Q2
DAC7664YCR	LQFP	PM	64	1500	330.0	24.8	12.3	12.3	2.5	16.0	24.0	Q2
DAC7664YCT	LQFP	PM	64	250	330.0	24.8	12.3	12.3	2.5	16.0	24.0	Q2
DAC7664YR	LQFP	PM	64	1500	330.0	24.8	12.3	12.3	2.5	16.0	24.0	Q2
DAC7664YT	LQFP	PM	64	250	330.0	24.8	12.3	12.3	2.5	16.0	24.0	Q2

PACKAGE MATERIALS INFORMATION

11-Mar-2008

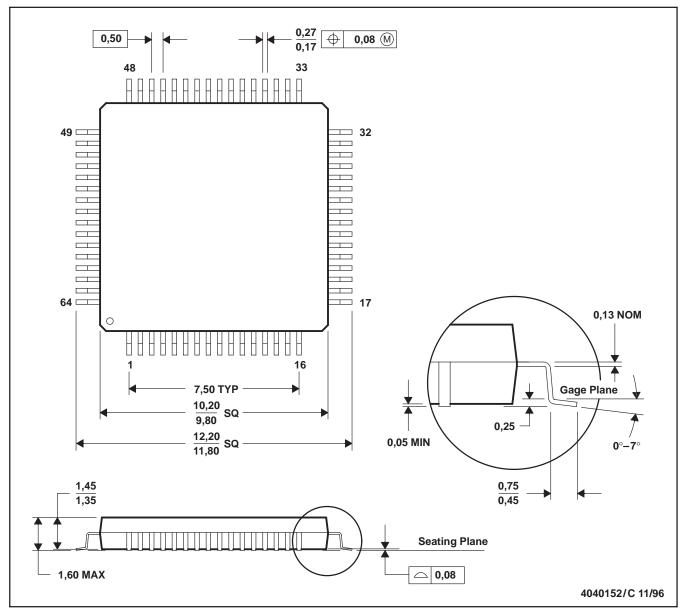


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
DAC7664YBR	LQFP	PM	64	1500	346.0	346.0	41.0
DAC7664YBT	LQFP	PM	64	250	346.0	346.0	41.0
DAC7664YCR	LQFP	PM	64	1500	346.0	346.0	41.0
DAC7664YCT	LQFP	PM	64	250	346.0	346.0	41.0
DAC7664YR	LQFP	PM	64	1500	346.0	346.0	41.0
DAC7664YT	LQFP	PM	64	250	346.0	346.0	41.0

PM (S-PQFP-G64)

PLASTIC QUAD FLATPACK



- NOTES: A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Falls within JEDEC MS-026
 - D. May also be thermally enhanced plastic with leads connected to the die pads.

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