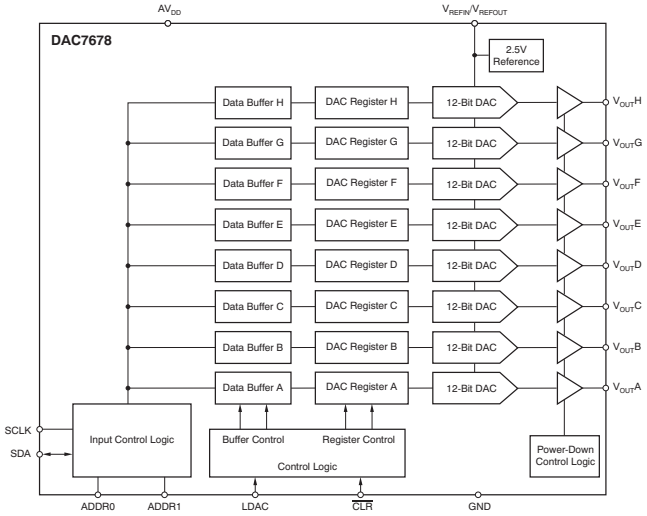
12-Bit, Octal-Channel, Ultra-Low Glitch, Voltage Output, Two-Wire Interface DIGITAL-TO-ANALOG CONVERTER with 2.5V Internal Reference

Check for Samples: DAC7678

FEATURES

- **Relative Accuracy: 1 LSB INL**
- **Glitch Energy: 0.15nV-s**
- **Internal Reference:**
  - **2.5V Reference Voltage (disabled by default)**
  - **±1mV Initial Accuracy**
  - **2ppm/°C Temperature Drift (typ)**
  - **25ppm/°C Temperature Drift (max)**
  - **20mA Sink/Source Capability**
- **Power-On Reset to Zero Scale or Midscale**
- **Ultra-Low Power Operation: 0.15mA/Channel at 5V**
- **Wide Power-Supply Range: +2.7V to +5.5V**
- **16-Bit Monotonic Over Temperature Range**
- **Settling Time: 10µs to ±0.003% Full-Scale Range (FSR)**
- **Two-Wire Serial Interface (I²C™ compatible)**
- **On-Chip Output Buffer Amplifier with Rail-to-Rail Operation**
- **Temperature Range: –40°C to +125°C**



APPLICATIONS

- **Portable Instrumentation**
- **Closed-Loop Servo-Control**
- **Process Control**
- **Data Acquisition Systems**
- **Programmable Attenuation**
- **PC Peripherals**

DESCRIPTION

The DAC7678 is a low-power, voltage-output, eight-channel, 12-bit digital-to-analog converter (DAC). The DAC7678 includes a 2.5V internal reference (disabled by default), giving a full-scale output voltage range of 5V. The internal reference initial accuracy is ±1mV and can source up to 20mA at the V_{REFIN}/V_{REFOUT} pin. The device is monotonic, provides very good linearity, and minimizes undesired code-to-code transient voltages (glitch).

The DAC7678 uses a versatile, two-wire serial interface that is I²C-compatible and operates at clock rates of up to 3.4MHz. Multiple devices can share the same bus.

The DAC7678 incorporates a power-on-reset circuit that ensures the DAC output powers on at either zero-scale or midscale until a valid code is written to the device. This device contains a power-down feature, accessed through the serial interface, that reduces the current consumption of the device to typically TBDµA at 5V. Power consumption is typically TBDmW at 3V, reducing to TBDµW in power-down mode. The low power consumption, internal reference, and small footprint make this device ideal for portable, battery-operated equipment.

The DAC7678 is drop-in and function compatible with the DAC5578, DAC6578, and DAC7578. This device is available in a 4x4 QFN-24 package and a TSSOP-16 package.

RELATED DEVICES	8-BIT	10-BIT	12-BIT
Pin- and Function-Compatible (w/internal reference)	—	—	DAC7678
Pin- and Function-Compatible	DAC5578	DAC6578	DAC7578

PRODUCT PREVIEW

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

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This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

PACKAGE/ORDERING INFORMATION(1)

PRODUCT	MAXIMUM RELATIVE ACCURACY (LSB)	MAXIMUM DIFFERENTIAL NONLINEARITY (LSB)	MAXIMUM REFERENCE DRIFT (ppm/°C)	PACKAGE-LEAD	PACKAGE DESIGNATOR	SPECIFIED TEMPERATURE RANGE	PACKAGE MARKING
DAC7678	±1	±0.25	25	TSSOP-16	PW	–40°C to +125°C	DAC7678
				QFN-24	RGE	–40°C to +125°C	DAC7678

(1) For the most current package and ordering information see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.

ABSOLUTE MAXIMUM RATINGS(1)

Over operating free-air temperature range, unless otherwise noted.

	DAC7678	UNIT
AV_{DD} to GND	–0.3 to +6	V
Digital input voltage to GND	–0.3 to +AV_{DD} + 0.3	V
V_{OUT} to GND	–0.3 to +AV_{DD} + 0.3	V
V_{REF} to GND	–0.3 to +AV_{DD} + 0.3	V
Operating temperature range	–40 to +125	°C
Storage temperature range	–65 to +150	°C
Junction temperature range (T_J max)	+150	°C
Power dissipation	(T_J max – T_A)/θ_{JA}	W
Thermal impedance, θ_{JA}	+118	°C/W
Thermal impedance, θ_{JC}	+29	°C/W

(1) Stresses above those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. Exposure to absolute maximum conditions for extended periods may affect device reliability.

PRODUCT PREVIEW

ELECTRICAL CHARACTERISTICS

At AV_{DD} = 2.7V to 5.5V and over –40°C to +125°C, unless otherwise noted.

PARAMETER	TEST CONDITIONS	DAC7678			UNIT
		MIN	TYP	MAX	
STATIC PERFORMANCE(1)					
Resolution		12			Bits
Relative accuracy	Measured by the line passing through codes 30 and 4050		±0.3	±1	LSB
Differential nonlinearity	12-bit monotonic		±0.1	±0.25	LSB
Offset error	Extrapolated from two-point line(2), unloaded		±0.5	±4	mV
Offset error drift			±3		µV/°C
Full-scale error	DAC register loaded with all '1's		±0.03	±0.2	% of FSR
Full-scale error drift			±2		µV/°C
Zero-code error	DAC register loaded with all '0's		1	4	mV
Zero-code error drift			2		µV/°C
Gain error	Extrapolated from two-point line(2), unloaded		±0.01	±0.15	% of FSR
Gain temperature coefficient	AV_{DD} = 5V		±1		ppm of FSR/°C
	AV_{DD} = 2.7V		±1		ppm of FSR/°C
OUTPUT CHARACTERISTICS(3)					
Output voltage range		0		AV_{DD}	V
Output voltage settling time	DACs unloaded, 1/4 scale to 3/4 scale		6	10	µs
	R_L = 1MΩ		12		µs
Slew rate			0.75		V/µs
Capacitive load stability	R_L = ∞		1000		pF
	R_L = 2kΩ		3000		pF
Code change glitch impulse	1LSB change around major carry		0.1		nV-s
Digital feedthrough	SCLK toggling		0.1		nV-s
Power-on glitch impulse	R_L = 2kΩ, C_L = 470pF, AV_{DD} = 5.5V		10		mV
	R_L = 2kΩ, C_L = 470pF, AV_{DD} = 2.7V		6		mV
Channel-to-channel dc crosstalk	Full-scale swing on adjacent channel		0.1		LSB
Channel-to-channel ac crosstalk	1kHz full-scale sine wave, outputs unloaded		–109		dB
DC output impedance	At midscale input		4		Ω
Short-circuit current	DAC outputs shorted to GND		25		mA
Power-up time (including settling time)	Coming out of power-down mode, AV_{DD} = 5V		50		µs

(1) Linearity calculated using a reduced code range; output unloaded.
(2) Codes 30 and 4050.
(3) Specified by design or characterization; not production tested.

PRODUCT PREVIEW

ELECTRICAL CHARACTERISTICS (continued)

At AV_{DD} = 2.7V to 5.5V and over –40°C to +125°C, unless otherwise noted.

PARAMETER	TEST CONDITIONS	DAC7678 MIN	DAC7678 TYP	DAC7678 MAX	UNIT
AC PERFORMANCE(4)					
SNR(5)	T_A = +25°C, BW = 20kHz, AV_{DD} = 5V, f_{OUT} = 1kHz		TBD		dB
THD	T_A = +25°C, BW = 20kHz, AV_{DD} = 5V, f_{OUT} = 1kHz		TBD		dB
SFDR	T_A = +25°C, BW = 20kHz, AV_{DD} = 5V, f_{OUT} = 1kHz		TBD		dB
SINAD	T_A = +25°C, BW = 20kHz, AV_{DD} = 5V, f_{OUT} = 1kHz		TBD		dB
DAC output noise density	T_A = +25°C, at zero-code input, f_{OUT} = 1kHz		90		nV/√Hz
DAC output noise	T_A = +25°C, at midscale input, f = 0.1Hz to 10Hz		2.6		μV_{PP}
INTERNAL REFERENCE(6)					
Output voltage	T_A = +25°C	2.499	2.5	2.501	V
Initial accuracy	T_A = +25°C	–1	±0.01	1	mV
Output voltage temperature drift			5	25	ppm/°C
Output voltage noise	f = 0.1Hz to 10Hz		12		μV_{PP}
Output voltage noise density (high-frequency noise)	T_A = +25°C, f = 1MHz, C_L = 0µF		50		nV/√Hz
	T_A = +25°C, f = 1MHz, C_L = 1µF		20		nV/√Hz
	T_A = +25°C, f = 1MHz, C_L = 4µF		16		nV/√Hz
Load regulation(7)	Sourcing, T_A = +25°C		30		µV/mA
	Sinking, T_A = +25°C		15		µV/mA
Output current load capability(4)			±20		mA
Line regulation	T_A = +25°C		10		µV/V
Long-term stability/drift (aging)(7)	T_A = +25°C, time = 0 to 1900 hours		50		ppm
Thermal hysteresis(7)	First cycle		100		ppm
	Additional cycles		25		ppm
Internal reference current consumption	AV_{DD} = 5.5V		360		µA
	AV_{DD} = 3.6V		348		µA
External reference current	External V_{REF} = 2.5V (when internal reference is disabled), all eight channels active		90		µA
V_{REFIN} pin reference input range	TBD	0		AV_{DD}	V
Reference input impedance			8		kΩ
LOGIC INPUTS(4)					
Input current			±1		µA
$V_{IN}L$ Logic input LOW voltage	3.6V ≤ AV_{DD} ≤ 5.5V			0.8	V
	2.7V ≤ AV_{DD} ≤ 3.6V			0.5	V
$V_{IN}H$ Logic input HIGH voltage	3.6V ≤ AV_{DD} ≤ 5.5V	1.8			V
	2.7V ≤ AV_{DD} ≤ 3.6V	1.1			V
Pin capacitance			1.5	3	pF

(4) Specified by design or characterization; not production tested.
(5) First 19 harmonics removed for SNR calculation.
(6) Reference is trimmed and tested at room temperature, and is characterized from –40°C to +125°C.
(7) Explained in more detail in the *Application Information* TBD section of this data sheet.

PRODUCT PREVIEW

ELECTRICAL CHARACTERISTICS (continued)

At AV_{DD} = 2.7V to 5.5V and over –40°C to +125°C, unless otherwise noted.

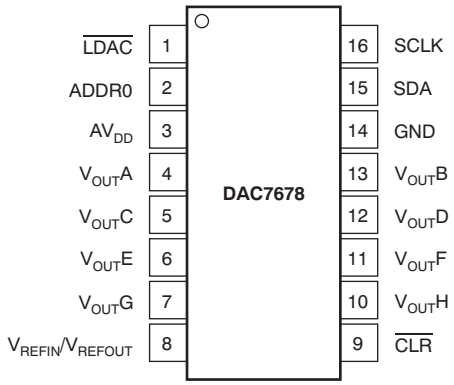
PARAMETER		TEST CONDITIONS	DAC7678 MIN	DAC7678 TYP	DAC7678 MAX	UNIT
POWER REQUIREMENTS						
AV_{DD}	Analog power supply		2.7		5.5	V
I_{DD} (8)	Normal mode, internal reference switched off	AV_{DD} = 3.6V to 5.5V $V_{IN}H = AV_{DD}$ and $V_{IN}L$ = GND		0.95	1.4	mA
		AV_{DD} = 2.7V to 3.6V $V_{IN}H = AV_{DD}$ and $V_{IN}L$ = GND		0.81	1.3	mA
	Normal mode, internal reference switched on	AV_{DD} = 3.6V to 5.5V $V_{IN}H = AV_{DD}$ and $V_{IN}L$ = GND		1.25	2.0	mA
		AV_{DD} = 2.7V to 3.6V $V_{IN}H = AV_{DD}$ and $V_{IN}L$ = GND		1.1	1.9	mA
	All power-down modes	AV_{DD} = 3.6V to 5.5V $V_{IN}H = AV_{DD}$ and $V_{IN}L$ = GND		0.18	3	µA
		AV_{DD} = 2.7V to 3.6V $V_{IN}H = AV_{DD}$ and $V_{IN}L$ = GND		0.10	2.5	µA
Power dissipation(8)	Normal mode, internal reference switched off	AV_{DD} = 3.6V to 5.5V $V_{IN}H = AV_{DD}$ and $V_{IN}L$ = GND		3.4	7.1	mW
		AV_{DD} = 2.7V to 3.6V $V_{IN}H = AV_{DD}$ and $V_{IN}L$ = GND		2.2	4.3	mW
	Normal mode, internal reference switched on	AV_{DD} = 3.6V to 5.5V $V_{IN}H = AV_{DD}$ and $V_{IN}L$ = GND		4.5	11	mW
		AV_{DD} = 2.7V to 3.6V $V_{IN}H = AV_{DD}$ and $V_{IN}L$ = GND		3	6.8	mW
	All power-down modes	AV_{DD} = 3.6V to 5.5V $V_{IN}H = AV_{DD}$ and $V_{IN}L$ = GND		0.6	16	µW
		AV_{DD} = 2.7V to 3.6V $V_{IN}H = AV_{DD}$ and $V_{IN}L$ = GND		0.3	9	µW
TEMPERATURE RANGE						
Specified performance			–40		+125	°C

(8) Input code = midscale, no load.

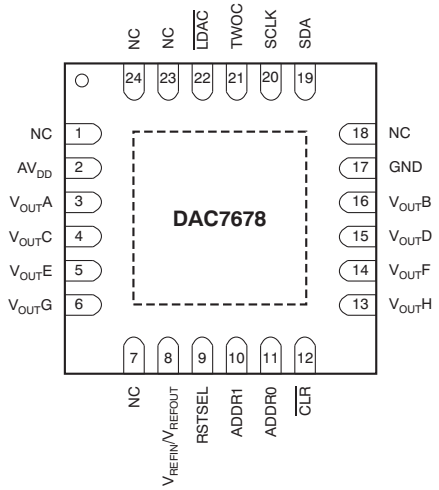
PRODUCT PREVIEW

PIN CONFIGURATIONS

PW PACKAGE
TSSOP-16
(TOP VIEW)



RGE PACKAGE
QFN-24
(TOP VIEW)



PIN DESCRIPTIONS

16-PIN	24-PIN	NAME	DESCRIPTION
—	1	NC	Not internally connected.
3	2	AV_{DD}	Power-supply input, 2.7V to 5.5V
4	3	$V_{OUT}A$	Analog output voltage from DAC A
5	4	$V_{OUT}C$	Analog output voltage from DAC C
6	5	$V_{OUT}E$	Analog output voltage from DAC E
7	6	$V_{OUT}G$	Analog output voltage from DAC G
—	7	NC	Not internally connected.
8	8	V_{REFIN}/ V_{REFOUT}	Positive reference input or reference output of 2.5V, if internal reference used.
—	9	RSTSEL	Reset select pin. RSTSEL high resets device to mid-scale; RSTSEL low (default setting) resets device to zero-scale.
—	10	ADDR1	Three-state address input 1
2	11	ADDR0	Three-state address input 0
9	12	$\overline{CLR}$	Asynchronous clear input
10	13	$V_{OUT}H$	Analog output voltage from DAC H
11	14	$V_{OUT}F$	Analog output voltage from DAC F
12	15	$V_{OUT}D$	Analog output voltage from DAC D
13	16	$V_{OUT}B$	Analog output voltage from DAC B
14	17	GND	Ground reference point for all circuitry on the device
—	18	NC	Not internally connected.
15	19	SDA	Serial data input. Data are clocked into or out of the input register. This pin is a bidirectional, open-drain data line that should be connected to the supply voltage with an external pull-up resistor.
16	20	SCLK	Serial clock input. Data can be transferred at rates up to 3.4MHz. Schmitt-trigger logic input.
—	21	TWOC	Twos Complement Select. If the TWOC pin is pulled high, the DAC registers use twos compliments format; if TWOC is pulled low, the DAC registers use straight binary format.
1	22	$\overline{LDAC}$	Load DACs.
—	23	NC	Not internally connected.
—	24	NC	Not internally connected.

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TIMING DIAGRAM: TBD

Figure 1. Serial Write Operation

THEORY OF OPERATION

DIGITAL-TO-ANALOG CONVERTER (DAC)

The DAC7678 architecture consists of eight string DACs each followed by an output buffer amplifier. The DAC7678 also includes an internal 2.5V reference with typical 5ppm/°C temperature drift performance, offering a 5V, full-scale output voltage. Figure 2 shows a principal block diagram of the DAC architecture.

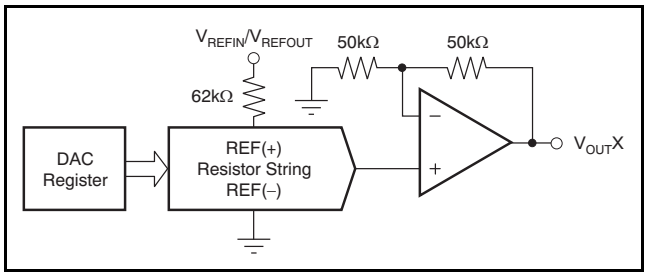

Figure 2. Device Architecture

For the TSSOP package, the input coding to the DAC7678 is straight binary. For the QFN package, the TWOC pin controls the code format.

When using the internal reference, the ideal output voltage is given by Equation 1:

$$V_{OUT} = \frac{D_{IN}}{4096} \times 2 \times V_{REFOUT} \quad (1)$$

When using an external reference, the ideal output voltage is given by Equation 2:

$$V_{OUT} = \frac{D_{IN}}{4096} \times V_{REFIN} \quad (2)$$

Where:

D_{IN} = decimal equivalent of the binary code that is loaded to the DAC register. It can range from 0 to 4095.

V_{REFOUT} = internal reference voltage of 2.5V, supplied at the V_{REFOUT}/V_{REFIN} pin.

V_{REFIN} = external reference voltage of 0V to 5V, supplied at the V_{REFOUT}/V_{REFIN} pin.

RESISTOR STRING

The resistor string circuitry is shown in Figure 3. It is simply a string of resistors, each of value *R*. The code loaded into the DAC register determines at which node on the string the voltage is tapped off. The voltage is then fed into the output amplifier by closing one of the switches connecting the string to the amplifier. Because it is a string of resistors, this architecture is monotonic.

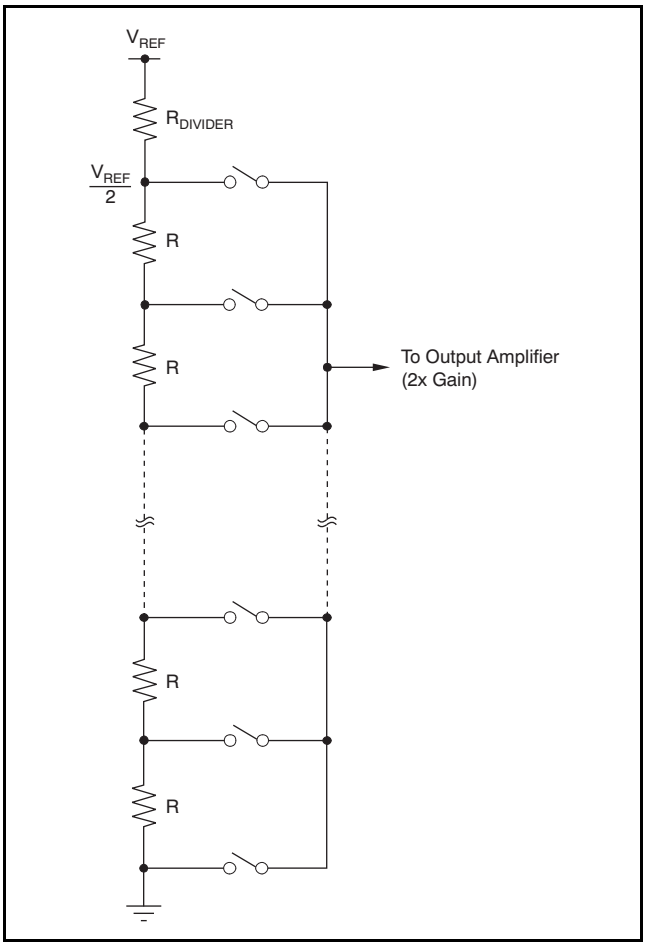

Figure 3. Resistor String

OUTPUT AMPLIFIER

The output buffer amplifier is capable of generating rail-to-rail voltages on its output, giving a maximum output range of 0V to AV_{DD}. It is capable of driving a load of 2kΩ in parallel with 1000pF to GND. The source and sink capabilities of the output amplifier can be seen in the Typical Characteristics (TBD) . The typical slew rate is 0.75V/µs, with a typical full-scale settling time of 5µs with the output unloaded.

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INTERNAL REFERENCE

The DAC7678 includes a 2.5V internal reference that is disabled by default. The internal reference is available externally at the V_{REFIN}/V_{REFOUT} pin. A minimum 100nF capacitor is recommended between the reference output and GND for noise filtering. The internal reference of the DAC7678 is a bipolar, transistor-based, precision bandgap voltage reference. Figure 4 shows the basic bandgap topology. Transistors Q_1 and Q_2 are biased such that the current density of Q_1 is greater than that of Q_2. The difference of the two base-emitter voltages ($V_{BE1} – V_{BE2}$) has a positive temperature coefficient and is forced across resistor R_1. This voltage is gained up and added to the base-emitter voltage of Q_2, which has a negative temperature coefficient. The resulting output voltage is virtually independent of temperature. The short-circuit current is limited by design to approximately 100mA.

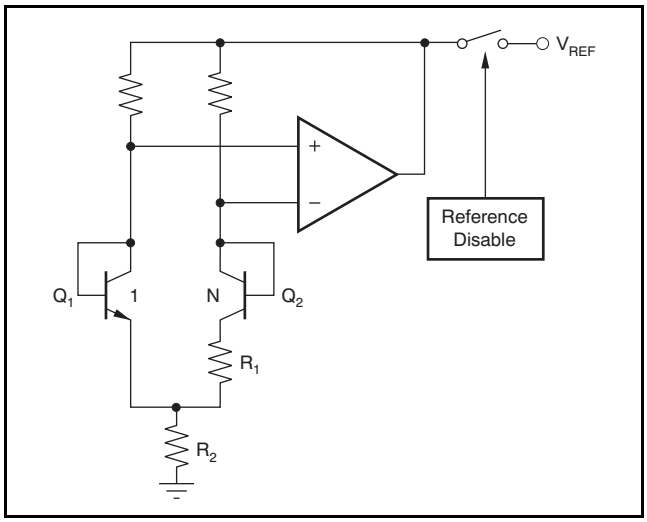

Figure 4. Bandgap Reference Simplified Schematic

Enable/Disable Internal Reference

The internal reference in the DAC7678 is disabled by default for debugging, evaluation purposes, or when using an external reference. The internal reference can be powered on and powered down using a serial command that requires a 32-bit write sequence, which consists of an 8-bit address byte plus a 24-bit serial command, as shown in Table 1. While the internal reference is disabled, the DAC functions normally using an external reference. However, when switching to the external reference, the internal gain is dynamically switched to one. Therefore, appropriate value for the external reference should be used per the desired output voltage.

When switching to the external reference, the internal reference is disconnected from the V_{REFIN}/V_{REFOUT} pin (3-state output). Do not attempt to drive the V_{REFIN}/V_{REFOUT} pin both externally and internally at the same time indefinitely.

There are two modes that allow communication with the internal reference: Regular/Static and Flexible. In Flexible mode, DB14 must be set to '1'.

Regular/Static Mode (see Table 1 and Table 2)

Enabling Internal Reference:

To enable the internal reference, write the 24-bit serial command shown in Table 1. When performing a power cycle to reset the device, the internal reference is switched off (default mode). In the default mode, the internal reference is powered down until a valid write sequence is applied to power on the internal reference. If the internal reference is powered on, it automatically powers down when all DACs power down in any of the power-down modes (see the *Power Down Modes* section). The internal reference automatically powers on when any DAC is powered on.

Disabling Internal Reference:

To disable the internal reference, address the device by writing the 8-bit address byte and then writing the 24-bit serial command shown in Table 1. When performing a power cycle to reset the device, the internal reference is put back into the default mode (switched off).

Table 1. Write Sequence for Enabling Internal Reference (Static Mode) (Internal Reference Powered On)

COMMAND AND ACCESS BYTE								MOST SIGNIFICANT DATA BYTE (MSDB)								LEAST SIGNIFICANT DATA BYTE (LSDB)							
C3	C2	C1	C0	A3	A2	A1	A0	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
1	0	0	0	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	1	X	X	X	X

Table 2. Write Sequence for Disabling Internal Reference (Static Mode) (Internal Reference Powered Off)

COMMAND AND ACCESS BYTE								MOST SIGNIFICANT DATA BYTE (MSDB)								LEAST SIGNIFICANT DATA BYTE (LSDB)							
C3	C2	C1	C0	A3	A2	A1	A0	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
1	0	0	0	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	0	X	X	X	X

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Flexible Mode (see Table 3, Table 4, and Table 5)

Enabling Internal Reference:

Method 1) To enable the internal reference, write the 24-bit serial command shown in Table 3. When performing a power cycle to reset the device, the internal reference is switched off (default mode). In the default mode, the internal reference remains powered down until a valid write sequence is applied to power on the internal reference. If the internal reference is powered on, it automatically powers down when all DACs power down in any of the power-down modes (see the Power Down Modes section). The internal reference powers on automatically when any DAC is powered on.

Method 2) To always enable the internal reference, write the 24-bit serial command shown in Table 4. When the internal reference is always enabled, any power-down command to the DAC channels does not change the internal reference operating mode. When performing a power cycle to reset the device, the internal reference is switched off (default mode). In the default mode, the internal reference remains powered down until a valid write sequence is applied to power up the internal reference. When the internal reference is powered on, it remains powered on, regardless of the state of the DACs.

Disabling Internal Reference:

To disable the internal reference, write the 24-bit serial command shown in Table 5. When performing a power cycle to reset the device, the internal reference is switched off (default mode). When the internal reference is operated in Flexible mode, Static mode is disabled and does not work. To switch from Flexible mode to Static mode, use the command shown in Table 6.

Table 3. Write Sequence for Enabling Internal Reference (Flexible Mode) (Internal Reference Powered On)

COMMAND AND ACCESS BYTE								MOST SIGNIFICANT DATA BYTE (MSDB)								LEAST SIGNIFICANT DATA BYTE (LSDB)							
C3	C2	C1	C0	A3	A2	A1	A0	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
1	0	0	1	X	X	X	X	X	1	0	0	X	X	X	X	X	X	X	X	X	X	X	X

Table 4. Write Sequence for Enabling Internal Reference (Flexible Mode) (Internal Reference Always Powered On)

COMMAND AND ACCESS BYTE								MOST SIGNIFICANT DATA BYTE (MSDB)								LEAST SIGNIFICANT DATA BYTE (LSDB)							
C3	C2	C1	C0	A3	A2	A1	A0	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
1	0	0	1	X	X	X	X	X	1	0	1	X	X	X	X	X	X	X	X	X	X	X	X

Table 5. Write Sequence for Disabling Internal Reference (Flexible Mode) (Internal Reference Always Powered Down)

COMMAND AND ACCESS BYTE								MOST SIGNIFICANT DATA BYTE (MSDB)								LEAST SIGNIFICANT DATA BYTE (LSDB)							
C3	C2	C1	C0	A3	A2	A1	A0	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
1	0	0	1	X	X	X	X	X	1	1	0	X	X	X	X	X	X	X	0	X	X	X	X

Table 6. Write Sequence for Switching from Flexible Mode to Static Mode for Internal Reference (Internal Reference Always Powered Down)

COMMAND AND ACCESS BYTE								MOST SIGNIFICANT DATA BYTE (MSDB)								LEAST SIGNIFICANT DATA BYTE (LSDB)							
C3	C2	C1	C0	A3	A2	A1	A0	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
1	0	0	1	X	X	X	X	X	0	X	X	X	X	X	X	X	X	X	X	X	X	X	X

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TWO-WIRE, I²C-COMPATIBLE INTERFACE

The two-wire serial interface used by the DAC7678 is I²C-compatible (refer to the I²C Bus Specification). The bus consists of a data line (SDA) and a clock line (SCL) with pull-up resistors. When the bus is idle, both SDA and SCL lines are pulled high. All I²C-compatible devices connect to the I²C bus through open-drain I/O pins SDA and SCL.

The I²C specification states that the device that controls communication is called a master, and the devices that are controlled by the master are called slaves. The master device generates the SCL signal. The master device also generates special timing conditions (start, repeated start, and stop) on the bus to indicate the start or stop of a data transfer, as shown in Figure 5. Device addressing is also performed by the master. The master device on an I²C bus is usually a microcontroller or a digital signal processor (DSP). The DAC7678 operates as a slave device on the I²C bus. A slave device acknowledges the master commands, and upon the direction of the master, either receives or transmits data.

Although the DAC7678 normally operates as a slave receiver, when a master device acquires the DAC7678 internal register data, the DAC7678 also operates as a slave transmitter. In this case, the master device reads from the DAC7678, the slave transmitter. According to I²C terminology, read and write are always with respect to the master device.

The DAC7678 supports the following data transfer modes, as defined in the I²C Bus Specification:

- Standard mode (100kbps)
- Fast mode (400kbps)
- Fast mode plus (1.0Mbps)(1)
- High-Speed mode (3.4Mbps)

The data transfer protocol for Standard and Fast modes is exactly the same; therefore, these modes are referred to as F/S mode in this document. The protocol for High-Speed mode is different from the F/S mode, and it is referred to as HS mode. The DAC7678 supports 7-bit addressing. Note that 10-bit addressing and a general call address are not supported.

Other than specific timing signals, the I²C interface works with serial bytes. At the end of each byte, a ninth clock cycle is used to generate/detect an acknowledge signal, as shown in Figure 6. An *acknowledge* is when the SDA line is pulled low during the high period of the ninth clock cycle. A *not-acknowledge* is when the SDA line is left high during the high period of the ninth clock cycle.

(1) The DAC7678 supports Fast mode plus speed and timing specifications only. The device can not support the 20mA low-level output current specification.

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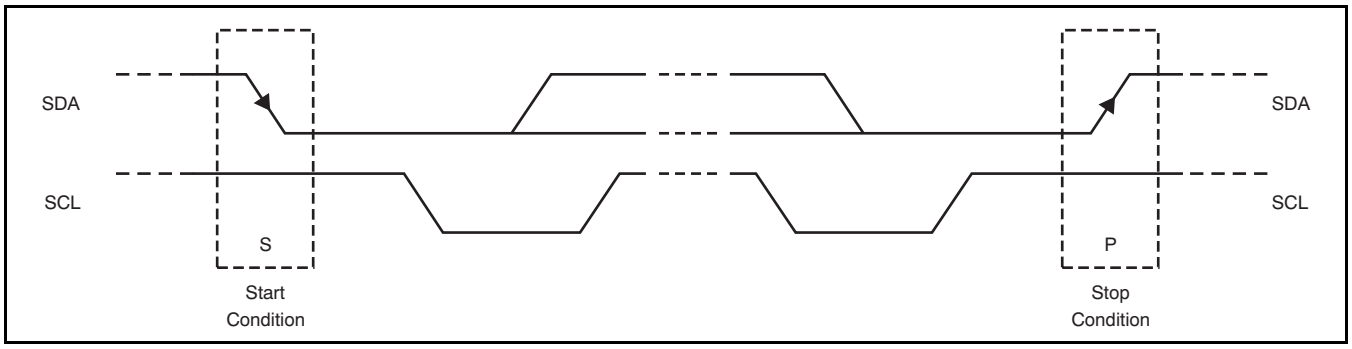

Figure 5. Start and Stop Conditions

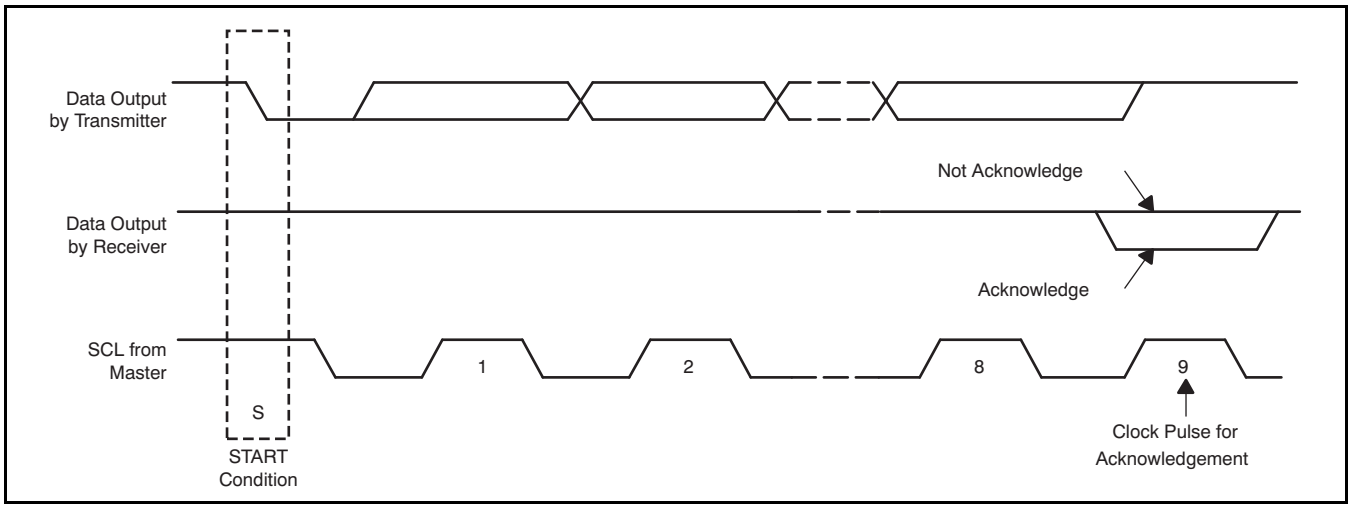

Figure 6. Acknowledge and Not Acknowledge on the I²C Bus

F/S Mode Protocol

The master initiates data transfer by generating a start condition, defined as when a high-to-low transition occurs on the SDA line while SCL is high, as shown in Figure 6. All I²C-compatible devices recognize a start condition.

The master then generates the SCL pulses, and transmits the 7-bit address and the read/write direction bit (R/$\overline{W}$) on the SDA line. During all transmissions, the master ensures that data are valid. A valid data condition requires the SDA line to be stable during the entire high period of the clock pulse, as shown in Figure 7. All devices recognize the address sent by the master and compare it to their internal fixed addresses. Only the slave device with a matching address generates an acknowledge by pulling the SDA line low during the entire high period of the ninth SCL cycle, as shown in Figure 6. Upon detecting this acknowledge, the master knows the communication link with a slave has been established.

The master generates further SCL cycles to either transmit data to the slave (R/$\overline{W}$ bit = '0') or receive data from the slave (R/$\overline{W}$ bit = '1'). In either case, the receiver needs to acknowledge the data sent by the transmitter. So the acknowledge signal can either be generated by the master or by the slave, depending on which one is the receiver. The 9-bit valid data sequences, consisting of eight data bits and one acknowledge bit, can continue as long as necessary.

To signal the end of the data transfer, the master generates a stop condition by pulling the SDA line from low to high while the SCL line is high (see Figure 5). This action releases the bus and stops the communication link with the addressed slave. All I²C-compatible devices recognize the stop condition. Upon receipt of a stop condition, the bus is released, and all slave devices then wait for a start condition followed by a matching address.

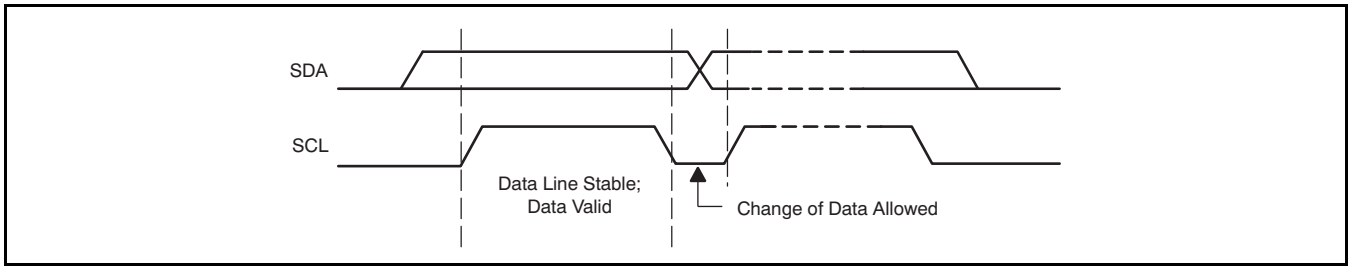

Figure 7. Bit Transfer on the I²C Bus

HS Mode Protocol

When the bus is idle, both the SDA and SCL lines are pulled high by the pull-up resistors.

The master generates a start condition followed by a valid serial byte containing HS mode master code 00001XXX. This transmission is made in F/S mode at no more than 1.0Mbps. No device is allowed to acknowledge the HS mode master code, but all devices must recognize it and switch their internal setting to support 3.4Mbps operation.

The master then generates a repeated start condition (a repeated start condition has the same timing as the start condition). After this repeated start condition, the protocol is the same as F/S mode, except that transmission speeds up to 3.4Mbps are allowed. A stop condition ends HS mode and switches all the internal settings of the slave devices to support F/S mode. Instead of using a stop condition, repeated start conditions should be used to secure the bus in HS mode.

DAC7678 I²C UPDATE SEQUENCE

For a single update, the DAC7678 requires a start condition, a valid I²C address (A) byte, a command and access (CA) byte, and two data bytes, the most significant data byte (MSDB) and least significant data byte (LSDB), as shown in Table 7.

After each byte is received, the DAC7678 acknowledges by pulling the SDA line low during the high period of a single clock pulse, as shown in Figure 8. A valid I²C address selects the corresponding slave device (for example, DAC7678).

The CA byte sets the operational mode of the selected DAC7678. When the operational mode is selected by this byte, the DAC7678 must receive two data bytes, the most significant data byte (MSDB) and least significant data byte (LSDB), for data update to occur. The DAC7678 performs an update on the falling edge of the acknowledge signal that follows the LSDB.

The CA byte does not have to be resent until a change in operational mode is required. The bits of the control byte continuously determine the type of update performed. Thus, for the first update, the DAC7678 requires a start condition, a valid I²C address, the CA byte, and two data bytes (MSDB and LSDB). For all consecutive updates, the DAC7678 needs only an MSDB and LSDB, as long as the CA byte command remains the same.

Table 7. Update Sequence

MSB	…	LSB	ACK	MSB	…	LSB	ACK	MSB	…	LSB	ACK	MSB	…	LSB	ACK
A Byte				CA Byte				MSDB				LSDB			

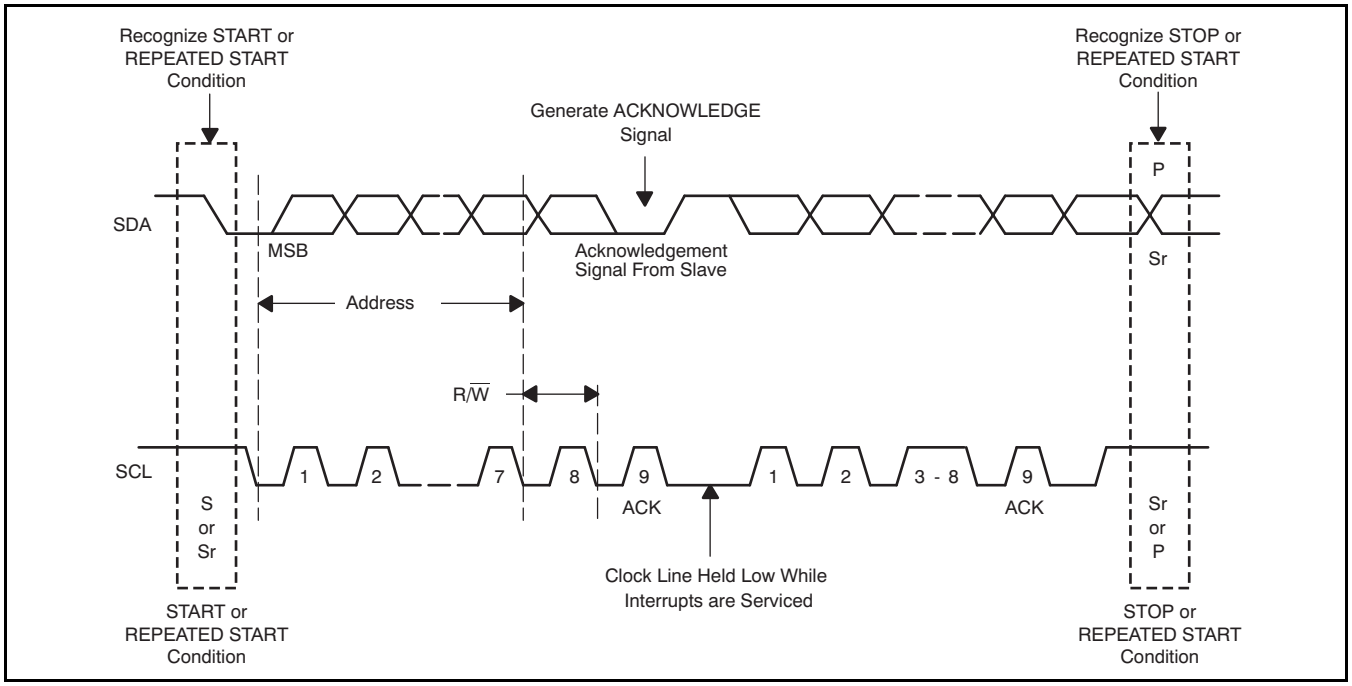

Figure 8. I²C Bus Protocol

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When using the I²C HS mode (clock = 3.4MHz), each 12-bit DAC update other than the first update can be done within 18 clock cycles (MSDB, acknowledge signal, LSDB, acknowledge signal) at 188.88kSPS. When using Fast mode (clock = 400kHz), the maximum DAC update rate is limited to 22.22kSPS. Using the Fast mode plus (clock = 1MHz), the maximum DAC update rate is limited to 55.55kSPS. When a stop condition is received, the DAC7678 releases the I²C bus and awaits a new start condition.

Address (A) Byte

The address byte, as shown in Table 8, is the first byte received following the start condition from the master device. The first four most significant bits (MSBs) of the address are factory preset to '1001'. The next three bits of the address are controlled by the ADDR pin(s). The ADDR pin(s) inputs can be connected to AV_{DD}, GND, or left floating. The device address can be updated dynamically between serial commands. When using the QFN package (DAC7678RGE), up to eight devices can be connected to the same I²C bus. When using the TSSOP package (DAC7678PW), up to three devices can be connected to the same I²C bus.

Table 8. Address Byte

MSB							LSB
AD6	**AD5**	**AD4**	**AD3**	**AD2**	**AD1**	**AD0**	**R/$\overline{W}$**
1	0	0	1	X	X	X	X

Table 9. Address Format For QFN-24 (RGE) Package

SLAVE ADDRESS	ADDR1	ADDR0
1001 000	0	0
1001 001	0	1
1001 010	1	0
1001 011	1	1
1001 100	Float	0
1001 101	Float	1
1001 110	0	Float
1001 111	1	Float
Not supported	Float	Float

Table 10. Address Format For TSSOP-16 (PW) Package

SLAVE ADDRESS	ADDR0
1001 000	0
1001 010	1
1001 100	Float

Command and Access (CA) Byte

The command and access byte, as shown in Table 11, controls which command is executed and which register is being accessed when writing to or reading from the DAC7678. See Table 12 for a list of write and read commands.

Table 11. Command and Access Byte

MSB							LSB
C3	**C2**	**C1**	**C0**	**A3**	**A2**	**A1**	**A0**
X	X	X	X	X	X	X	X
Command bits				Access bits			

Table 12. Command and Access Byte Format(1)

C3	C2	C1	C0	A3	A2	A1	A0	DESCRIPTION
Write Sequences								
0	0	0	0	A3	A2	A1	A0	Write to DAC input register channel n
0	0	0	1	A3	A2	A1	A0	Select to update DAC register channel n
0	0	1	0	A3	A2	A1	A0	Write to DAC input register channel n, and update all DAC registers (global software LDAC)
0	0	1	1	A3	A2	A1	A0	Write to DAC input register channel n, and update DAC register channel n
0	1	0	0	X	X	X	X	Power down/on DAC
0	1	0	1	X	X	X	X	Write to clear code register
0	1	1	0	X	X	X	X	Write to LDAC register
0	1	1	1	X	X	X	X	Software reset
1	0	0	0	X	X	X	X	Write to internal reference register
1	0	0	1	X	X	X	X	Write to additional internal reference register
Read Sequences								
0	0	0	0	A3	A2	A1	A0	Read from DAC input register channel n
0	0	0	1	A3	A2	A1	A0	Read from DAC register channel n
0	1	0	0	X	X	X	X	Read from DAC power down register
0	1	0	1	X	X	X	X	Read from clear code register
0	1	1	0	X	X	X	X	Read from LDAC register
1	0	0	0	X	X	X	X	Read from internal reference register
1	0	0	1	X	X	X	X	Read from additional internal reference register
Access Sequences								
C3	C2	C1	C0	0	0	0	0	DAC channel A
C3	C2	C1	C0	0	0	0	1	DAC channel B
C3	C2	C1	C0	0	0	1	0	DAC channel C
C3	C2	C1	C0	0	0	1	1	DAC channel D
C3	C2	C1	C0	0	1	0	0	DAC channel E
C3	C2	C1	C0	0	1	0	1	DAC channel F
C3	C2	C1	C0	0	1	1	0	DAC channel G
C3	C2	C1	C0	0	1	1	1	DAC channel H
C3	C2	C1	C0	1	1	1	1	All DAC channels, broadcast update

(1) Any sequences other than the ones listed are invalid; improper use can cause incorrect device functionality.

Most Significant Data Byte (MSDB) and Least Significant Data Byte (LSDB)

The MSDB and LSDB contain the data that are passed to the register(s) specified by the CA byte, as shown in Table 13 and Table 14. See Table 16 for a complete list of write sequences and Table 17 for a complete list of read sequences. The DAC7678 updates at the falling edge of the acknowledge signal that follows the LSDB.

Broadcast Addressing

Broadcast addressing, as shown in Table 15, is also supported by the DAC7678. Broadcast addressing can be used for synchronously updating or powering down multiple DAC7678 devices. The DAC7678 is designed to work with other members of the DACx578 family to support multichannel synchronous updates. Using the broadcast address command, the DAC7678 responds regardless of the state of the address pins. Note that broadcast addressing is supported only in write mode (master writes to the DAC7678).

I²C READ SEQUENCE

To read any register, the following command sequence should be used:

1. Send a start or repeated start command with a slave address and the R/$\overline{W}$ bit set to '0' for writing. The device will acknowledge this event.
2. Then send a command byte for the register to be read. The device will acknowledge this event again.
3. Then send a repeated start with the slave address and the R/$\overline{W}$ bit set to '1' for reading. The device will also acknowledge this event.
4. Then the device writes the MSDB of the register. The master should acknowledge this byte.
5. Finally, the device writes out the LSDB of the register.

An alternative reading method allows for reading back of the last register written to. The sequence is a start/repeated start with slave address and the R/$\overline{W}$ bit set to '1', and the two bytes of the last register are read out, as shown in Figure TBD.

Note that it is not possible to use the broadcast address for reading.

Table 13. MSDB

MSB							LSB
DB15	**DB14**	**DB13**	**DB12**	**DB11**	**DB10**	**DB9**	**DB8**
X	X	X	X	X	X	X	X

Most Significant Data Byte (MSDB)

Table 14. LSDB

MSB							LSB
DB7	**DB6**	**DB5**	**DB4**	**DB3**	**DB2**	**DB1**	**DB0**
X	X	X	X	X	X	X	X

Least Significant Data Byte (LSDB)

Table 15. Broadcast Address Command

MSB							LSB
AD6	**AD5**	**AD4**	**AD3**	**AD2**	**AD1**	**AD0**	**R/$\overline{W}$**
1	0	0	0	1	1	1	0

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Table 16. Control Matrix for Write Commands

CA BYTE								MSDB								LSDB								DESCRIPTION
C3	C2	C1	C0	A3	A2	A1	A0	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	
Write to DAC Input Register																								
0	0	0	0	0	0	0	0	Data[11:4]								Data[3:0]				X	X	X	X	Write to DAC input register for channel A
0	0	0	0	0	0	0	1	Data[11:4]								Data[3:0]				X	X	X	X	Write to DAC input register for channel B
0	0	0	0	0	0	1	0	Data[11:4]								Data[3:0]				X	X	X	X	Write to DAC input register for channel C
0	0	0	0	0	0	1	1	Data[11:4]								Data[3:0]				X	X	X	X	Write to DAC input register for channel D
0	0	0	0	0	1	0	0	Data[11:4]								Data[3:0]				X	X	X	X	Write to DAC input register for channel E
0	0	0	0	0	1	0	1	Data[11:4]								Data[3:0]				X	X	X	X	Write to DAC input register for channel F
0	0	0	0	0	1	1	0	Data[11:4]								Data[3:0]				X	X	X	X	Write to DAC input register forchannel G
0	0	0	0	0	1	1	1	Data[11:4]								Data[3:0]				X	X	X	X	Write to DAC input register for channel H
0	0	0	0	1	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	Invalid code, no action performed
0	0	0	0	1	1	1	1	Data[11:4]								Data[3:0]				X	X	X	X	Broadcast mode—write to all DAC channels
Select DAC Register to Update																								
0	0	0	1	0	0	0	0	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	Selects DAC channel A to be updated
0	0	0	1	0	0	0	1	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	Selects DAC channel B to be updated
0	0	0	1	0	0	1	0	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	Selects DAC channel C to be updated
0	0	0	1	0	0	1	1	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	Selects DAC channel D to be updated
0	0	0	1	0	1	0	0	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	Selects DAC channel E to be updated
0	0	0	1	0	1	0	1	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	Selects DAC channel F to be updated
0	0	0	1	0	1	1	0	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	Selects DAC channel G to be updated
0	0	0	1	0	1	1	1	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	Selects DAC channel H to be updated
0	0	0	1	1	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	Invalid code, no action performed
0	0	0	1	1	1	1	1	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	Broadcast mode—selects all DAC channels to be updated
Write to Selected DAC Input Register and Update Corresponding DAC Register (Individual Software LDAC)																								
0	0	1	1	0	0	0	0	Data[11:4]								Data[3:0]				X	X	X	X	Write to DAC input register for channel A and update channel A DAC register
0	0	1	1	0	0	0	1	Data[11:4]								Data[3:0]				X	X	X	X	Write to DAC input register for channel A and update channel B DAC register
0	0	1	1	0	0	1	0	Data[11:4]								Data[3:0]				X	X	X	X	Write to DAC input register for channel A and update channel C DAC register
0	0	1	1	0	0	1	1	Data[11:4]								Data[3:0]				X	X	X	X	Write to DAC input register for channel A and update channel D DAC register
0	0	1	1	0	1	0	0	Data[11:4]								Data[3:0]				X	X	X	X	Write to DAC input register for channel A and update channel E DAC register
0	0	1	1	0	1	0	1	Data[11:4]								Data[3:0]				X	X	X	X	Write to DAC input register for channel A and update channel F DAC register
0	0	1	1	0	1	1	0	Data[11:4]								Data[3:0]				X	X	X	X	Write to DAC input register for channel A and update channel G DAC register
0	0	1	1	0	1	1	1	Data[11:4]								Data[3:0]				X	X	X	X	Write to DAC input register for channel A and update channel H DAC register
0	0	1	1	1	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	Invalid code, no action performed
0	0	1	1	1	1	1	1	Data[11:4]								Data[3:0]				X	X	X	X	Broadcast mode—write to all input registers and update all DAC registers

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Table 16. Control Matrix for Write Commands (continued)

CA BYTE								MSDB								LSDB								DESCRIPTION
C3	C2	C1	C0	A3	A2	A1	A0	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	
Write to Selected DAC Input Register and Update All DAC Registers (Global Software LDAC)																								
0	0	1	0	0	0	0	0	Data[11:4]								Data[3:0]				X	X	X	X	Write to DAC input register for channel A and update all DAC registers
0	0	1	0	0	0	0	1	Data[11:4]								Data[3:0]				X	X	X	X	Write to DAC input register for channel B and update all DAC registers
0	0	1	0	0	0	1	0	Data[11:4]								Data[3:0]				X	X	X	X	Write to DAC input register for channel C and update all DAC registers
0	0	1	0	0	0	1	1	Data[11:4]								Data[3:0]				X	X	X	X	Write to DAC input register for channel D and update all DAC registers
0	0	1	0	0	1	0	0	Data[11:4]								Data[3:0]				X	X	X	X	Write to DAC input register for channel E and update all DAC registers
0	0	1	0	0	1	0	1	Data[11:4]								Data[3:0]				X	X	X	X	Write to DAC input register for channel F and update all DAC registers
0	0	1	0	0	1	1	0	Data[11:4]								Data[3:0]				X	X	X	X	Write to DAC input register for channel G and update all DAC registers
0	0	1	0	0	1	1	1	Data[11:4]								Data[3:0]				X	X	X	X	Write to DAC input register for channel H and update all DAC registers
0	0	1	0	1	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	Invalid code, no action performed
0	0	1	0	1	1	1	1	Data[11:4]								Data[3:0]				X	X	X	X	Broadcast mode—write to all input registers and update all DAC registers
Power-Down Register																								
0	1	0	0	X	X	X	X	X	PD1	PD0	DAC A	DAC B	DAC C	DAC D	DAC E	DAC F	DAC G	DAC H	X	X	X	X	X	
0	1	0	0	X	X	X	X	X	0	0	DAC A	DAC B	DAC C	DAC D	DAC E	DAC F	DAC G	DAC H	X	X	X	X	X	Each DAC bit set to '1' powers on selected DACs
0	1	0	0	X	X	X	X	X	0	1	DAC A	DAC B	DAC C	DAC D	DAC E	DAC F	DAC G	DAC H	X	X	X	X	X	Each DAC bit set to '1' powers down selected DACs. V_{OUT} connected to GND through 1kΩ pull-down resistor
0	1	0	0	X	X	X	X	X	1	0	DAC A	DAC B	DAC C	DAC D	DAC E	DAC F	DAC G	DAC H	X	X	X	X	X	Each DAC bit set to '1' powers down selected DACs. V_{OUT} connected to GND through 100kΩ pull-down resistor
0	1	0	0	X	X	X	X	X	1	1	DAC A	DAC B	DAC C	DAC D	DAC E	DAC F	DAC G	DAC H	X	X	X	X	X	Each DAC bit set to '1' powers down selected DACs. V_{OUT} is three-stated
Clear Code Register																								
0	1	0	1	X	X	X	X	X	X	X	X	X	X	X	X	X	X	CL1	CL0	X	X	X	X	
0	1	0	1	X	X	X	X	X	X	X	X	X	X	X	X	X	X	0	0	X	X	X	X	Write to clear code register, CLR pin will clear to zero scale
0	1	0	1	X	X	X	X	X	X	X	X	X	X	X	X	X	X	0	1	X	X	X	X	Write to clear code register, CLR pin will clear to midscale
0	1	0	1	X	X	X	X	X	X	X	X	X	X	X	X	X	X	1	0	X	X	X	X	Write to clear code register, CLR pin will clear to full scale
0	1	0	1	X	X	X	X	X	X	X	X	X	X	X	X	X	X	1	1	X	X	X	X	Write to clear code register disables $\overline{CLR}$ pin
LDAC Register																								
0	1	1	0	X	X	X	X	DAC H	DAC G	DAC F	DAC E	DAC D	DAC C	DAC B	DAC A	X	X	X	X	X	X	X	X	When all DAC bits are set to '1', selected DACs ignore the $\overline{LDAC}$ pin. When all DAC bits are set to '0', selected DAC registers update according to the $\overline{LDAC}$ pin.

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Table 16. Control Matrix for Write Commands (continued)

CA BYTE								MSDB								LSDB								
C3	C2	C1	C0	A3	A2	A1	A0	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	DESCRIPTION
Software Reset																								
0	1	1	1	X	X	X	X	0	0	X	X	X	X	X	X	X	X	X	X	X	X	X	X	Software reset (default). Equivalent to power-on reset (POR).
0	1	1	1	X	X	X	X	0	1	X	X	X	X	X	X	X	X	X	X	X	X	X	X	Software reset that sets device into High-Speed mode
0	1	1	1	X	X	X	X	1	0	X	X	X	X	X	X	X	X	X	X	X	X	X	X	Software reset that maintains High-Speed mode state
Internal Reference in Regular/Static Mode																								
1	0	0	0	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	AR	X	X	X	X	
1	0	0	0	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	0	X	X	X	X	Disable internal reference (Regular/Static mode)
1	0	0	0	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	1	X	X	X	X	Enable internal reference (Regular/Static mode). If any DACs are powered on, the reference is on. If all DACS are powered down, then reference is off.
Internal Reference in Flexible Mode																								
1	0	0	1	X	X	X	X	X	TR2	TR1	TR0	X	X	X	X	X	X	X	X	X	X	X	X	
1	0	0	1	X	X	X	X	X	1	0	0	X	X	X	X	X	X	X	X	X	X	X	X	Reference powers down when all DACs power down. Reference powers on when any DACs are powered on.
1	0	0	1	X	X	X	X	X	1	0	1	X	X	X	X	X	X	X	X	X	X	X	X	Reference is powered on regardless of DAC power state
1	0	0	1	X	X	X	X	X	1	1	0	X	X	X	X	X	X	X	X	X	X	X	X	Reference is powered down regardless of DAC power state
1	0	0	1	X	X	X	X	X	0	X	X	X	X	X	X	X	X	X	X	X	X	X	X	Reference follows Regular/Static mode reference register

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Table 17. Control Matrix for Read Commands

CA BYTE								MSDB								LSDB								DESCRIPTION
C3	C2	C1	C0	A3	A2	A1	A0	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	
Input Register																								
0	0	0	0	0	0	0	0	Data[11:4]								Data[3:0]				X	X	X	X	Read from DAC input register channel A
0	0	0	0	0	0	0	1	Data[11:4]								Data[3:0]				X	X	X	X	Read from DAC input register channel B
0	0	0	0	0	0	1	0	Data[11:4]								Data[3:0]				X	X	X	X	Read from DAC input register channel C
0	0	0	0	0	0	1	1	Data[11:4]								Data[3:0]				X	X	X	X	Read from DAC input register channel D
0	0	0	0	0	1	0	0	Data[11:4]								Data[3:0]				X	X	X	X	Read from DAC input register channel E
0	0	0	0	0	1	0	1	Data[11:4]								Data[3:0]				X	X	X	X	Read from DAC input register channel F
0	0	0	0	0	1	1	0	Data[11:4]								Data[3:0]				X	X	X	X	Read from DAC input register channel G
0	0	0	0	0	1	1	1	Data[11:4]								Data[3:0]				X	X	X	X	Read from DAC input register channel H
0	0	0	0	1	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	Invalid code
DAC Register																								
0	0	0	1	0	0	0	0	Data[11:4]								Data[3:0]				X	X	X	X	Read DAC A DAC register
0	0	0	1	0	0	0	1	Data[11:4]								Data[3:0]				X	X	X	X	Read DAC B DAC register
0	0	0	1	0	0	1	0	Data[11:4]								Data[3:0]				X	X	X	X	Read DAC C DAC register
0	0	0	1	0	0	1	1	Data[11:4]								Data[3:0]				X	X	X	X	Read DAC D DAC register
0	0	0	1	0	1	0	0	Data[11:4]								Data[3:0]				X	X	X	X	Read DAC E DAC register
0	0	0	1	0	1	0	1	Data[11:4]								Data[3:0]				X	X	X	X	Read DAC F DAC register
0	0	0	1	0	1	1	0	Data[11:4]								Data[3:0]				X	X	X	X	Read DAC G DAC register
0	0	0	1	0	1	1	1	Data[11:4]								Data[3:0]				X	X	X	X	Read DAC H DAC register
0	0	0	1	1	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	Invalid code
Power Down Register																								
0	1	0	0	X	X	X	X	0	0	0	0	0	0	PD1	PD0	DAC A	DAC B	DAC C	DAC D	DAC E	DAC F	DAC G	DAC H	Read power down register
Clear Code Register																								
0	1	0	1	X	X	X	X	0	0	0	0	0	0	0	0	0	0	0	0	0	0	CL1	CL0	Read clear code register
LDAC Register																								
0	1	1	0	X	X	X	X	0	0	0	0	0	0	0	0	DAC H	DAC G	DAC F	DAC E	DAC D	DAC C	DAC B	DAC A	Read LDAC register
Internal Reference in Regular/Static Mode																								
1	0	0	0	X	X	X	X	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	AR	Read reference register
Internal Reference in Flexible Mode																								
1	0	0	1	X	X	X	X	0	0	0	0	0	0	0	0	0	0	0	0	0	TR2	TR1	TR0	Read additional reference register

POWER-ON RESET TO ZERO-SCALE OR MIDSCALE

The DAC7678 contains a power-on reset (POR) circuit that controls the output voltage during power-on. For devices housed in the TSSOP package, at power-on, all DAC registers are filled with zeros and the output voltages of all DAC channels are set to zero-scale. For devices housed in the QFN package, all DAC registers are set to have all DAC channels power on depending of the state of the RSTSEL pin.

The RSTSEL pin value is read at power-on and should be set prior to or simultaneously with AV_{DD}. For RSTSEL set to AV_{DD}, the DAC channels are loaded with midscale code. If RSTSEL is set to ground, the DAC channels are loaded with zero-scale code. All DAC channels remain in this state until a valid write sequence and load command are sent to the respective DAC channel. The power-on reset function is useful in applications where it is important to know the output state of each DAC while the device is in the process of powering on.

The internal reference is powered down by default, and remains that way until a valid reference change command is executed.

LDAC FUNCTIONALITY

The DAC7678 offers both software and hardware simultaneous updates and control functions. The DAC double-buffered architecture is designed so that new data can be entered for each DAC without disturbing the analog outputs.

The DAC7678 data updates can be performed either in Synchronous or Asynchronous mode.

In Synchronous mode, data are updated on the falling edge of the acknowledge signal that follows LSDB. For Synchronous mode updates, the $\overline{\text{LDAC}}$ pin is not required and must be connected to GND permanently.

In Asynchronous mode, the $\overline{\text{LDAC}}$ pin is used as a negative-edge-triggered timing signal for asynchronous DAC updates. Multiple single-channel updates can be performed in order to set different channel buffers to desired values and then make a falling edge on the $\overline{\text{LDAC}}$ pin. The data buffers of all the channels must be loaded with the desired data before an $\overline{\text{LDAC}}$ falling edge. After a high-to-low $\overline{\text{LDAC}}$ transition, all DACs are simultaneously updated with the last contents of the corresponding data buffers. If the contents of a data buffer are not changed by the serial interface, the corresponding DAC output remains unchanged after the $\overline{\text{LDAC}}$ trigger.

Alternatively, all DAC outputs can be updated simultaneously using the built-in LDAC software function. The LDAC register offers additional flexibility and control, giving the ability to select which DAC channel(s) should be updated simultaneously when the hardware $\overline{\text{LDAC}}$ pin is being brought low. The LDAC register is loaded with an 8-bit word (DB15 to DB8) using control bits C3, C2, C1, and C0. The default value for each bit, and therefore each DAC channel, is zero and the external $\overline{\text{LDAC}}$ pin operates in normal mode. If the LDAC register bit for a selected DAC channel is set to '1', that DAC channel ignores the external $\overline{\text{LDAC}}$ pin and updates only through the software LDAC command. If, however, the LDAC register bit is set to '0', the DAC channel is controlled by the external $\overline{\text{LDAC}}$ pin (default).

This combination of a software and hardware simultaneous update function is particularly useful in applications where only selective DAC channels are to be updated simultaneously, while keeping the other channels unaffected and updating those channels synchronously. See table TBD for a graphical illustration and examples.

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POWER-DOWN MODES

The DAC7678 has two separate sets of power-down commands. One set is for the DAC channels and the other set is for the internal reference. For more information on powering down the reference see the *Enable/Disable Internal Reference* section.

DAC Power-Down Commands

The DAC7678 uses four modes of operation. These modes are accessed by using control bits C3, C2, C1, and C0. The control bits must be set to '0100'. When the control bits are set correctly, the four different power-down modes are software programmable by setting bits PD0 (DB13) and PD1 (DB14) in the control register. Table 18 shows how to control the operating mode with data bits PD0 (DB13), and PD1 (DB14). The DAC7678 treats the power-down condition as data; all the operational modes are still valid for power down. It is possible to broadcast a power-down condition to all the DAC7678s in a system. It is also possible to power-down a channel and update data on other channels. Further, it is possible to write to the DAC register/buffer of the DAC channel that is powered down. When the DAC channel is then powered on, it will contain this new value.

When both the PD0 and PD1 bits are set to '0', the device works normally with its typical consumption of TBD mA at 5.5V. The reference is included with the operation of all eight channels. However, for the three power-down modes, the supply current falls to TBD mA at 5.5V (TBD mA at 2.7V). Not only does the supply current fall, but the output stage also switches internally from the output amplifier to a resistor network of known values.

The advantage of this switching is that the output impedance of the device is known while it is in power-down mode. As described in Table 18, there are three different power-down options. V_{OUT} can be connected internally to GND through a 1kΩ resistor, a 100kΩ resistor, or open-circuited (High-Z). The output stage is shown in Figure 2. In other words, C3, C2, C1, and C0 = '0100' and DB14 and DB13 = '11' represent a power-down condition with High-Z output impedance for a selected channel. DB14 and DB13 = '01' represents a power-down condition with 1kΩ output impedance, while DB14 and DB13 = '10' represents a power-down condition with 100kΩ output impedance.

Table 18. DAC Operating Modes

PD1 (DB14)	PD0 (DB13)	DAC OPERATING MODES
0	0	Power on selected DACs
0	1	Power down selected DACs, 1kΩ to GND
1	0	Power down selected DACs, 100kΩ to GND
1	1	Power down selected DACs, High-Z to GND

CLEAR CODE REGISTER AND CLR PIN

The DAC7678 contains a clear code register. The clear code register can be accessed via the two-wire serial interface and is user-configurable. Bringing the CLR pin low clears the content of all DAC registers and all DAC buffers and replaces the code with the code determined by the clear code register. The clear code register can be written to by applying the commands showed in Table 16. The default setting of the clear code register sets the output of all DAC channels to 0V when the CLR pin is brought low. The CLR pin is falling-edge-triggered; therefore, the device exits clear code mode on the falling edge of the acknowledge signal that follows LSDB of the next write sequence. If the CLR pin is brought low during a write sequence, the write sequence is aborted and the DAC registers and DAC buffers are cleared.

When performing a software reset of the device, the clear code register is reset to the default mode (DB5 = '0', DB4 = '0'). Setting the clear code register to DB4 = '1' and DB5 = '1' ignores any activity on the external CLR pin.

SOFTWARE RESET FUNCTION

The DAC7678 contains a software reset feature. When the software reset feature is executed, the device (all DAC channels) are reset to the power-on reset code. All registers inside the device are reset to the respective default settings. The DAC offers the flexibility to go into High-Speed mode directly after resetting the device without sending the high-speed master code. The device can also stay in High-Speed mode after a reset if desired. See Table 16 (Software Reset subsection) for these extra feature settings.

PACKAGING INFORMATION

Orderable Device	Status [1]	Package Type	Package Drawing	Pins	Package Qty	Eco Plan [2]	Lead/Ball Finish	MSL Peak Temp [3]
DAC7678SPW	PREVIEW	TSSOP	PW	16	90	TBD	Call TI	Call TI
DAC7678SPWR	PREVIEW	TSSOP	PW	16	2000	TBD	Call TI	Call TI
DAC7678SRGER	PREVIEW	VQFN	RGE	24	3000	TBD	Call TI	Call TI
DAC7678SRGET	PREVIEW	VQFN	RGE	24	250	TBD	Call TI	Call TI

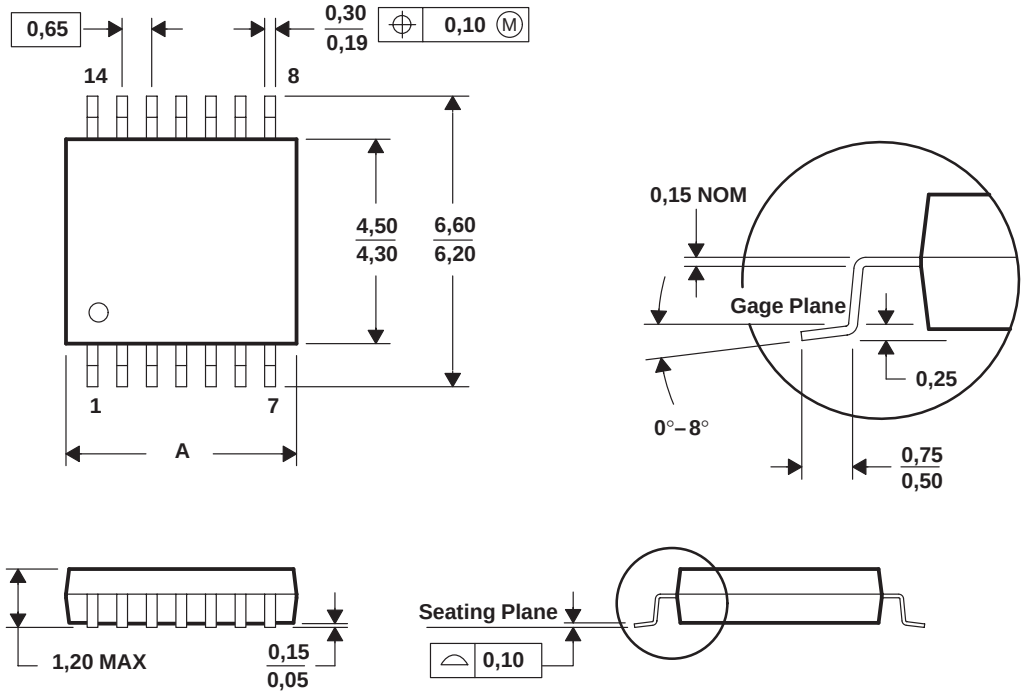
[1] The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

[2] Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

[3] MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

PW (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

14 PINS SHOWN

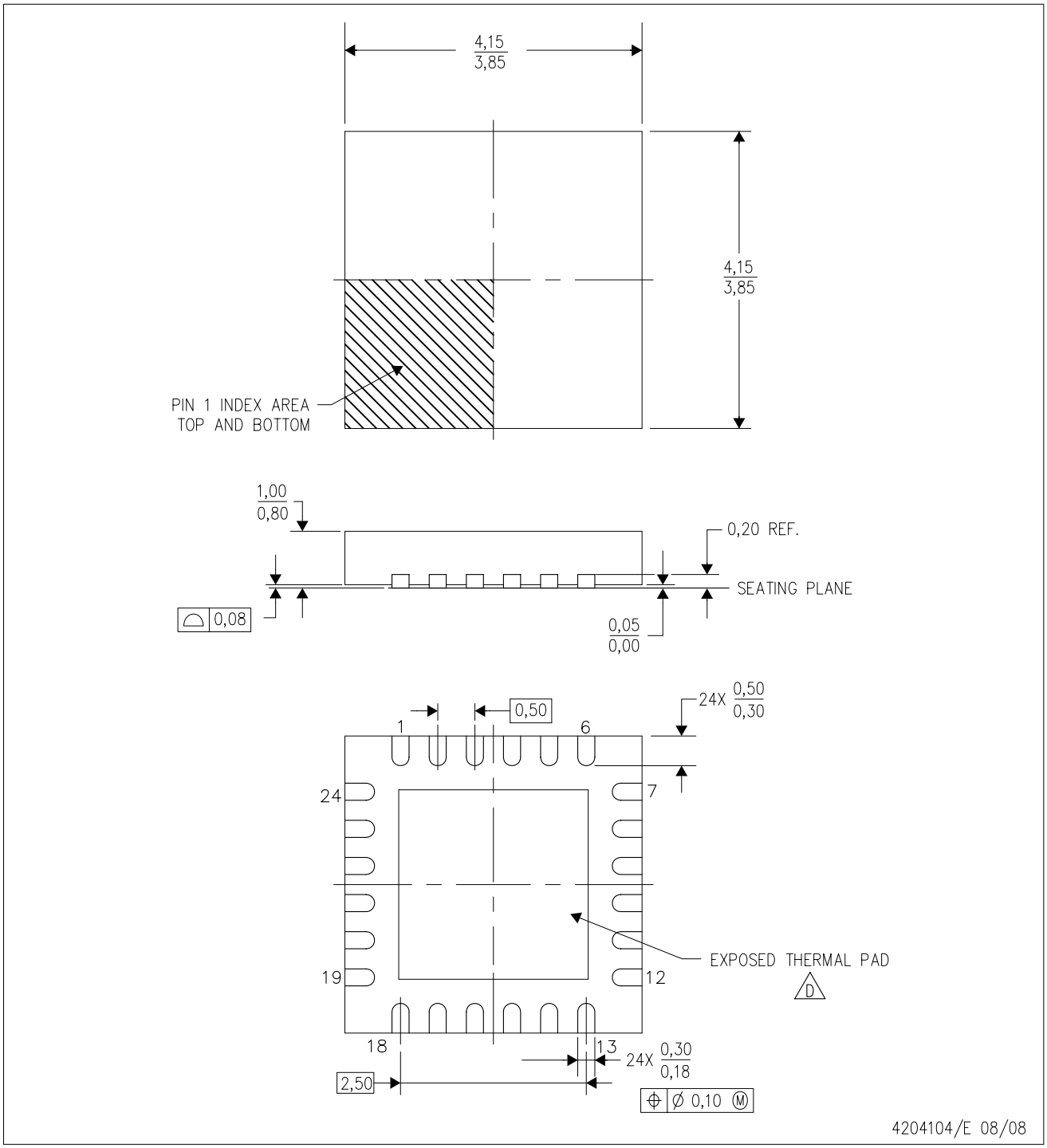


DIM \ PINS **	8	14	16	20	24	28
A MAX	3,10	5,10	5,10	6,60	7,90	9,80
A MIN	2,90	4,90	4,90	6,40	7,70	9,60

4040064/F 01/97

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
D. Falls within JEDEC MO-153

RGE (S–PVQFN–N24) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Quad Flatpack, No–Leads (QFN) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance. See the Product Data Sheet for details regarding the exposed thermal pad dimensions.
E. Falls within JEDEC MO–220.

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