MINIATURE, 1-W, 3-kV ISOLATED UNREGULATED DC/DC CONVERTERS

FEATURES

- **Up To 78% Efficiency**
- **3-kVDC Isolation**
- **UL60950 Certified Product**
- **Industry Standard Footprint**
- **JEDEC SIP-7 Package**

APPLICATIONS

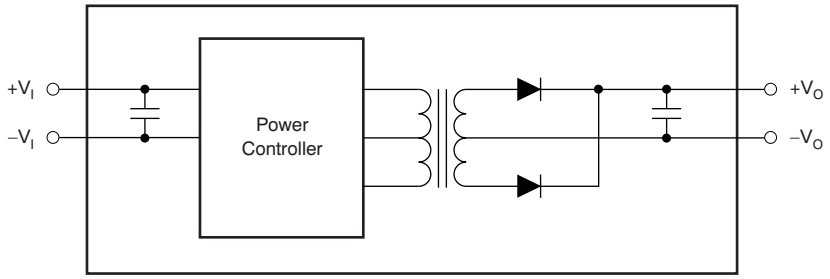
- **Point-of-Use Power Conversion**
- **Ground Loop Elimination**
- **Data Acquisition**
- **Industrial Control and Instrumentation**
- **Test Equipment™**

DESCRIPTION

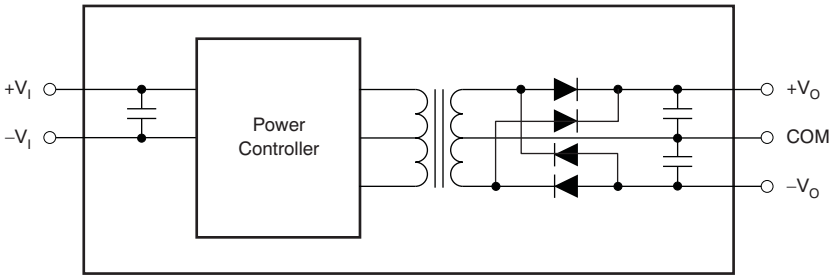
The DCH01 series is a family of miniature, 1-W, 3-kV isolated DC/DC converters. Featured in an industry standard SIP-7 footprint, the DCH01 series requires minimal external components, reducing board space. The DCH01 series provides both single and dual split-supply outputs.

The use of a highly integrated package design results in highly reliable products with high power densities. High performance and small size makes the DCH01 suitable for a wide range of applications including signal chain applications and ground loop elimination.

Single Output Block Diagram



Dual Output Block Diagram



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

ORDERING INFORMATION

For the most current package and ordering information, see the Package Option Addendum at the end of this data sheet, or see the TI website at www.ti.com.

Part Numbering Scheme

PRODUCT LINE	POWER	INPUT VOLTAGE	OUTPUT VOLTAGE	SINGLE/DUAL	PACKAGE	PIN CONFIG	TRANSPORT MEDIA
DCH	**01**	**05**	**05**	**S**	**N**	**7**	
H = 3 kV, unregulated output	01 = 1 W	05 = 5 V	05 = 5 V 12 =12 V 15 = 15 V	S = Single D = Dual	N = SIP Thru-hole	7 = SIP-7	Blank = Tray T = Tape & Reel

DCH01 Products

MODEL	INPUT VOLTAGE (V)	OUTPUT VOLTAGE (V)	OUTPUT CURRENT (mA)	OUTPUT POWER (W)	ISOLATION VOLTAGE (kVDC)	PACKAGE-LEAD
DCH010505S	5 ± 10%	5	200	1	3	SIP-7
DCH010512S	5 ± 10%	12	83	1	3	SIP-7
DCH010515S	5 ± 10%	15	67	1	3	SIP-7
DCH010505D	5 ± 10%	±5	±100	1	3	SIP-7
DCH010512D	5 ± 10%	±12	±42	1	3	SIP-7
DCH010515D	5 ± 10%	±15	±33	1	3	SIP-7

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted) (1)

		DCH01 SERIES	UNIT
Input Voltage	5V input models	7	V
Wave soldering temperature	Surface temperature of module body or pins for 5 seconds maximum	260	°C
Storage temperature range		–55 to +125	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated is not implied. Exposure to absolute maximum rated conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

At T_A = +25°C, V_I = 5V unless otherwise noted.

PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
OUTPUT						
Power	100% full load				1(1)	W
	Over current duration(1)				1	sec
INPUT						
Voltage range on V_I			–10		10	%
ISOLATION						
Voltage	100% tested for 1 second		3.5			kVDC
LINE						
Regulation	1% change in V_I			1%		
SWITCHING						
Switching frequency (f_{SW})				70		kHz
RELIABILITY						
Calculated	Per Telcordia SR-332; 50% stress; T_A = +40C	Single Output	18			FITS
		Dual Output	22			
TEMPERATURE RANGE						
Operating			–40		+85	°C

(1) This converter does not have continuous over-current protection.

ELECTRICAL CHARACTERISTICS PER DEVICE

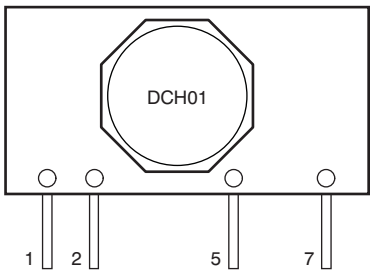
At T_A = +25°C, V_I = 5V unless otherwise noted.

	INPUT VOLTAGE (V)	OUTPUT VOLTAGE (V)	LOAD REGULATION (%)	OUTPUT RIPPLE(1) (mV_{PP})	NO LOAD INPUT CURRENT (mA)	EFFICIENCY (%)	BARRIER CAPACITANCE (pF)
	V_I	V_{NOM}			I_Q		C_{ISO}
	NOMINAL	100% LOAD(2)	10% TO 100% LOAD(3)	100% LOAD(2)	0% LOAD	100% LOAD(2)	
PRODUCT	TYP	TYP	TYP	TYP	TYP	TYP	TYP
DCH010505S	5	5.1	10	35	60	72	3
DCH010505D	5	±5.2	9	20	60	72	3
DCH010512S	5	12.4	6	18	65	74	4
DCH010512D	5	±12.5	5	19	65	75	4
DCH010515S	5	15.2	6	31	65	75	3
DCH010515D	5	±15.3	5	22	65	76	3

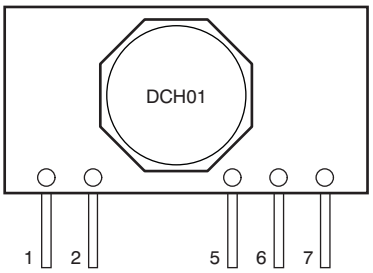
(1) 20MHz bandwidth.
(2) 100% load current = 1W/V_{NOM} typ.
(3) Load Regulation = (V_O at 10% load - V_O at 100% load) / V_O at 100% load.

DEVICE INFORMATION

EDJ PACKAGE
SIP-7 (Single)
(Top View)



EDJ PACKAGE
SIP-7 (Dual)
(Top View)



Pin Description (Single)

TERMINAL		
NAME	NO.	DESCRIPTION
$+V_I$	1	Voltage input
$-V_I$	2	Input side common
$-V_O$	5	–Voltage out
$+V_O$	7	+Voltage out

Pin Descriptions (Dual)

TERMINAL		
NAME	NO.	DESCRIPTION
$+V_I$	1	Voltage input
$-V_I$	2	Input side common
$-V_O$	5	–Voltage out
COM	6	Output side common
$+V_O$	7	+Voltage out

TYPICAL CHARACTERISTICS

At T_A = +25°C, and V_{IN} = 5V unless otherwise noted.

DCH010505S EFFICIENCY

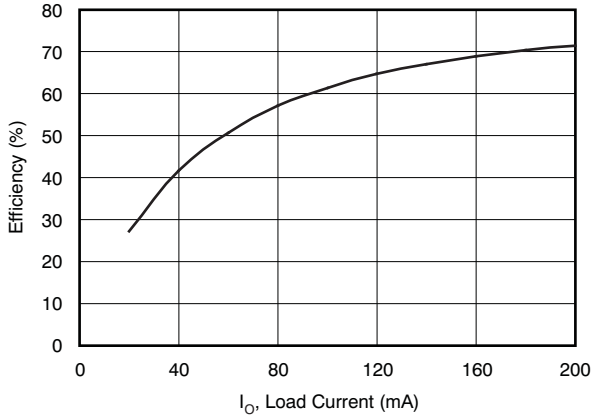


Figure 1.

DCH010505D EFFICIENCY

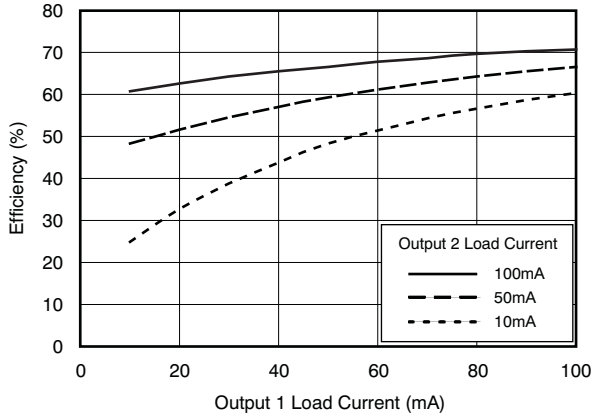


Figure 2.

DCH010505S LOAD REGULATION

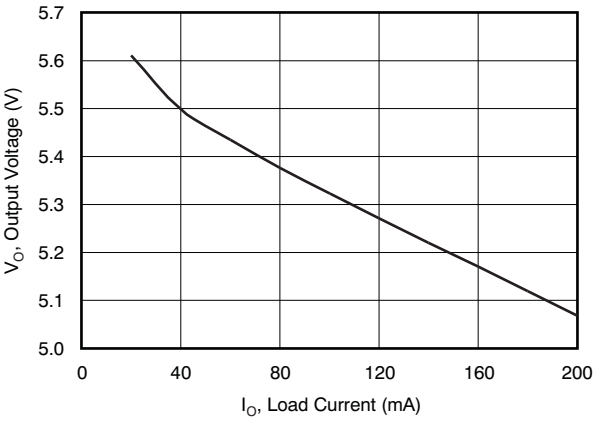


Figure 3.

DCH010505D LOAD REGULATION

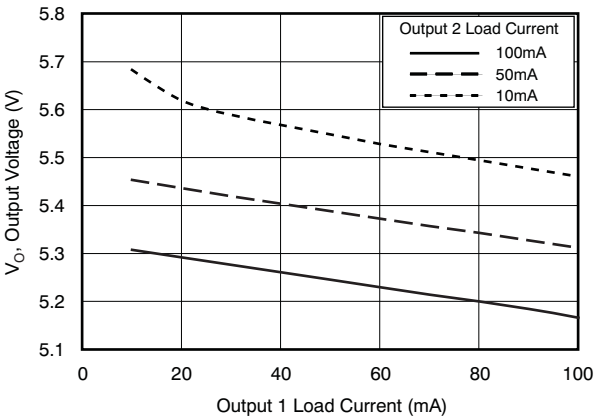


Figure 4.

DCH010505S RIPPLE VOLTAGE

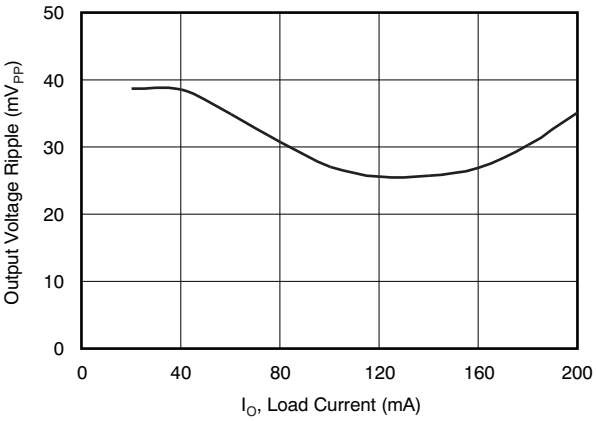


Figure 5.

DCH010505D RIPPLE VOLTAGE

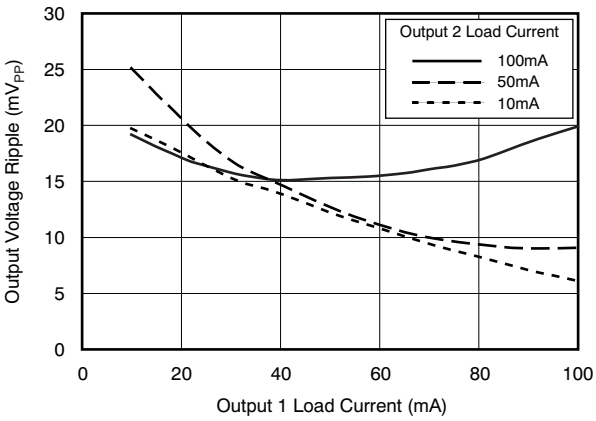


Figure 6.

TYPICAL CHARACTERISTICS (continued)

At T_A = +25°C, and V_{IN} = 5V unless otherwise noted.

DCH010512S EFFICIENCY

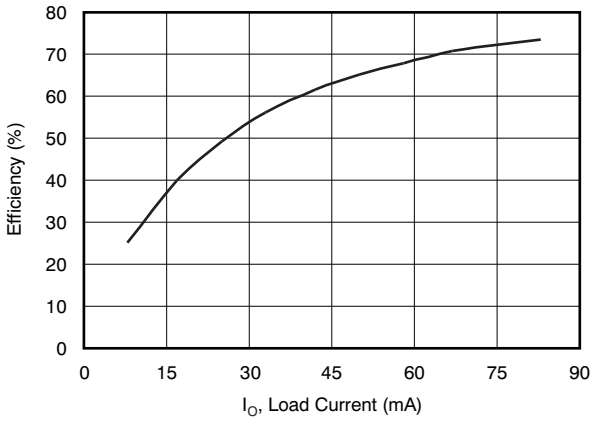


Figure 7.

DCH010512D EFFICIENCY

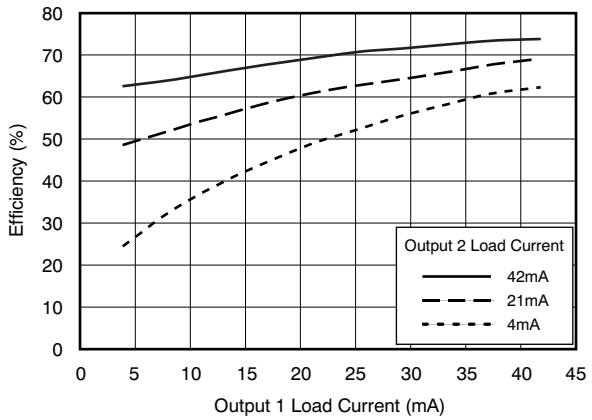


Figure 8.

DCH010512S LOAD REGULATION

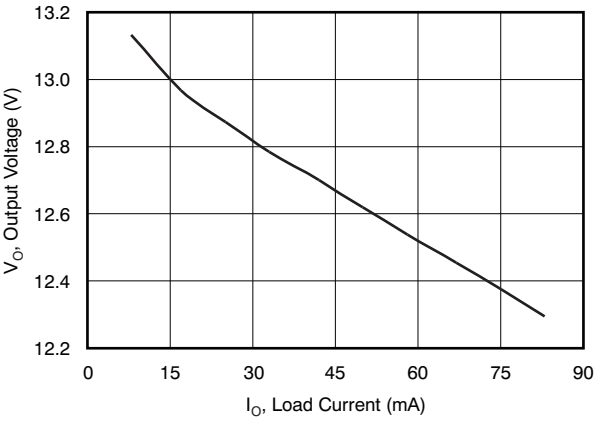


Figure 9.

DCH010512D LOAD REGULATION

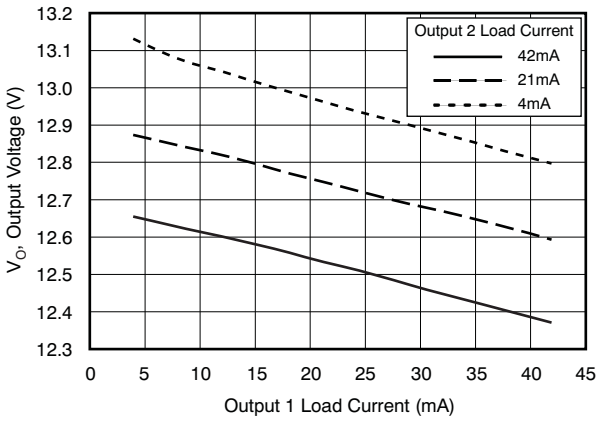


Figure 10.

DCH010512S RIPPLE VOLTAGE

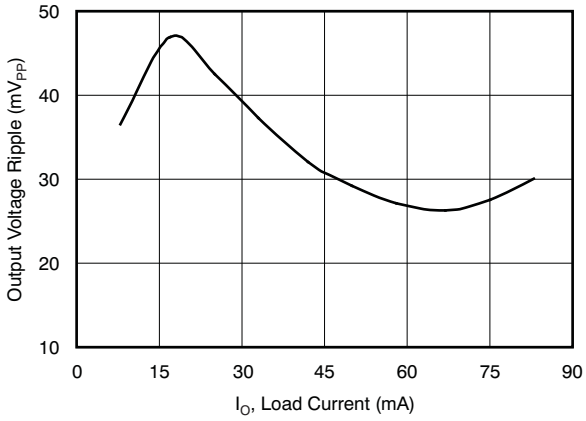


Figure 11.

DCH010512D RIPPLE VOLTAGE

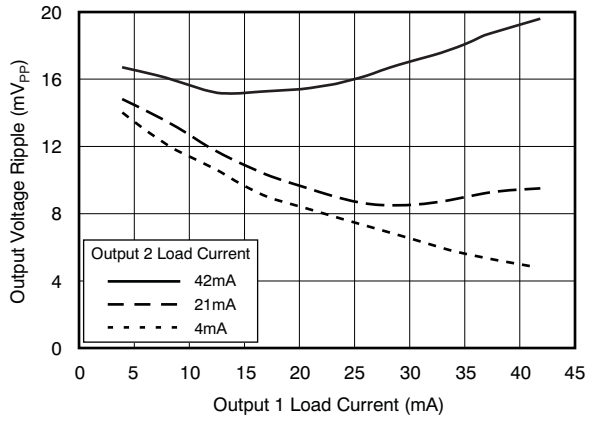


Figure 12.

TYPICAL CHARACTERISTICS (continued)

At T_A = +25°C, and V_{IN} = 5V unless otherwise noted.

DCH010515S EFFICIENCY

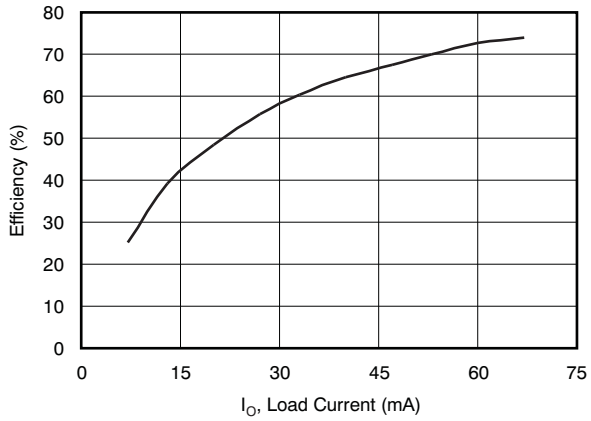


Figure 13.

DCH010515D EFFICIENCY

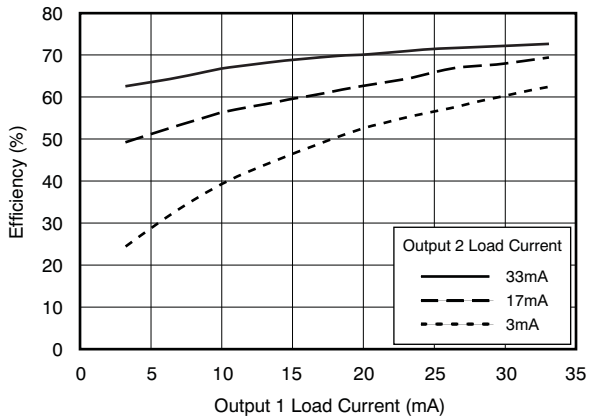


Figure 14.

DCH010515S LOAD REGULATION

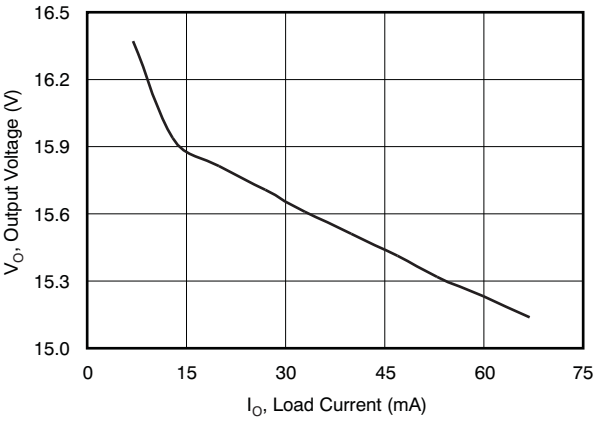


Figure 15.

DCH010515D LOAD REGULATION

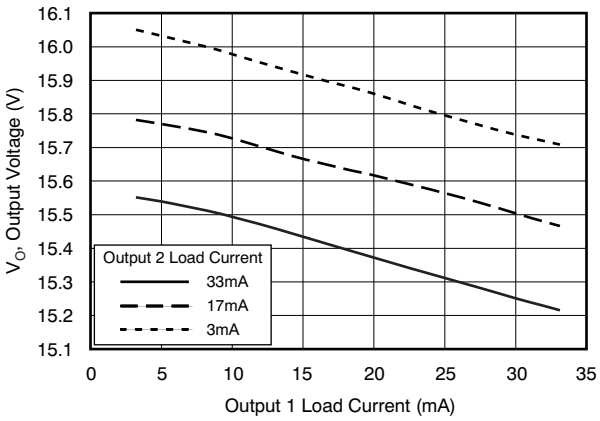


Figure 16.

DCH010515S RIPPLE VOLTAGE

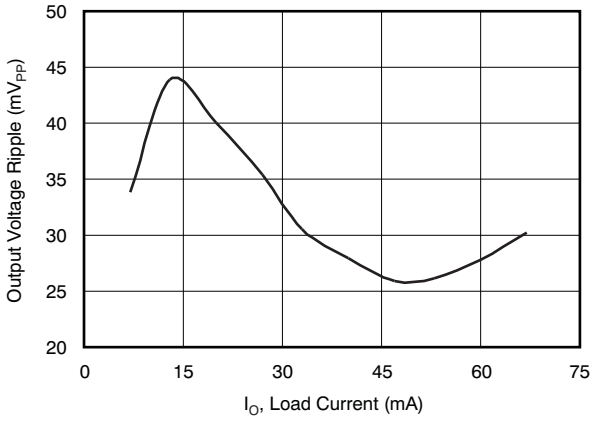


Figure 17.

DCH010515D RIPPLE VOLTAGE

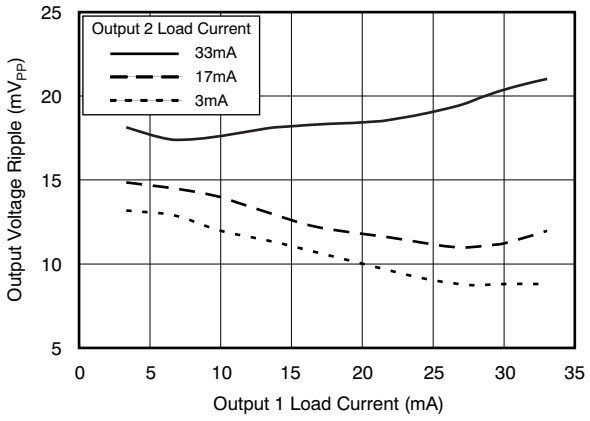


Figure 18.

TYPICAL CHARACTERISTICS (continued)

At T_A = +25°C, and V_{IN} = 5V unless otherwise noted.

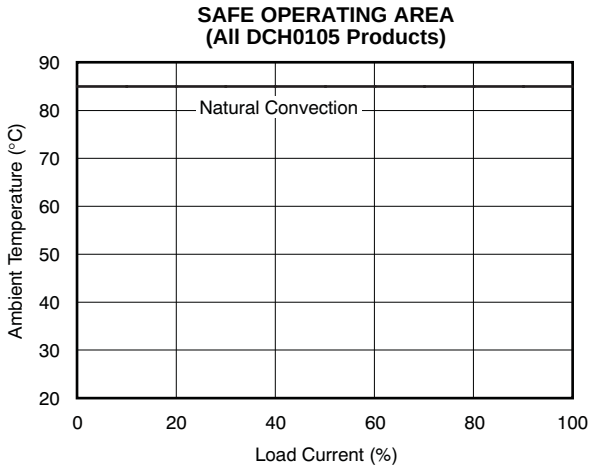


Figure 19.

FUNCTIONAL DESCRIPTION

ISOLATION VOLTAGE

The DCH01 series of DC/DC converters are 100% production tested at 3.5 kVDC for 1 second. The isolation test voltage represents an operational isolation to transient voltages and should not be relied upon for safety isolation.

The continuous voltage that can be applied across the DCH01 during normal operation must be < 60 VDC, within SELV limits.

Repeated High-Voltage Isolation Testing

Repeated high-voltage isolation testing can degrade the isolation capability of the DCH01.

APPLICATION INFORMATION

OPTIONAL INPUT/OUTPUT FILTERS

DCH01 power modules include internal input and output ceramic capacitors in all their designs. However, some applications require much lower levels of either input reflected or output ripple/noise. This application note describes various filters and design techniques found to be successful in reducing both input and output ripple/noise.

INPUT/OUTPUT CAPACITORS

The easiest way to reduce output ripple and noise is to add one or more ceramic capacitors each with a value of 4.7-µF or greater. Ceramic capacitors should be placed close to the output power terminals. A single 4.7-µF ceramic capacitor reduces the output ripple/noise by 10% to 30%.

Switching regulators draw current from the input line in pulses at their operating frequency. The amount of reflected (input) ripple/noise generated is directly proportional to the equivalent source impedance of the power source including the impedance of any input lines. The addition of a 4.7-µF ceramic capacitor, near the input power pins, reduces reflected conducted ripple/noise by 30% to 50%.

The recommended capacitve load on the output of the DCH01 is 100 µF.

Figure 20. DCH01 Series π Filter

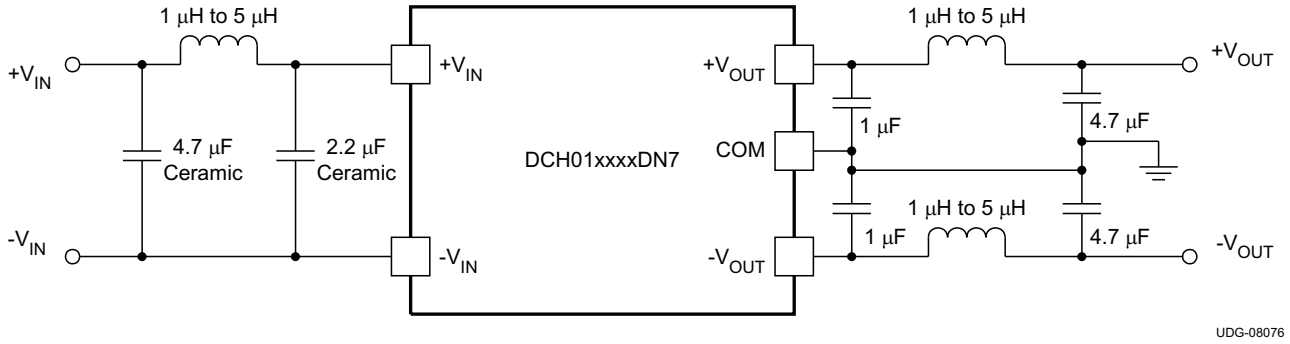


Figure 21. DCH01 Series π Filter (5 V at 1 W)

π FILTERS

If a further reduction in ripple/noise level is required for an application, higher order filters must be used. A π (pi) filter, employing a ferrite bead inductor in series with the input or output terminals of the regulator reduces the ripple/noise by at least 20 db (see Figure 20 and Figure 21). Ceramic capacitors are required for the inductor to be effective in reduction of ripple and noise.

These inductors plus ceramic capacitors form an excellent filter because of the rejection at the switching frequency. The placement of this filter is critical. It must be located as close as possible to the input or output pins to be efffective. The ferrite bead is small (12,5 mm x 3 mm), easy to use, low cost, and has low dc resistance. Fair-Rite manufactures a surface-mount bead (part number 2773021447) or through hole (part number 2673000701) rated to 5 A. Inductors with a value between 1 µH and 5 µH can be used in place of the ferrite bead inductor.

DCH01 START-UP

Start-up waveforms.

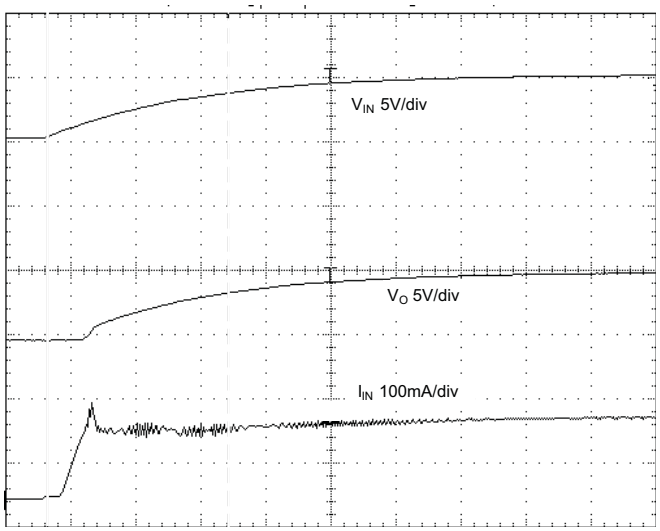


Figure 22. Startup Waveforms

CONNECTING THE DCH01 IN SERIES

It is possible to connect the outputs of multiple DCH01s in series to provide non-standard voltage rails. The outputs of dual output DCH01 versions can also be connected in series to provide 2 × the magnitude of V_O, as shown in Figure 23. For example, a dual 5-V DCH01 could be connected to provide a 10-V rail.

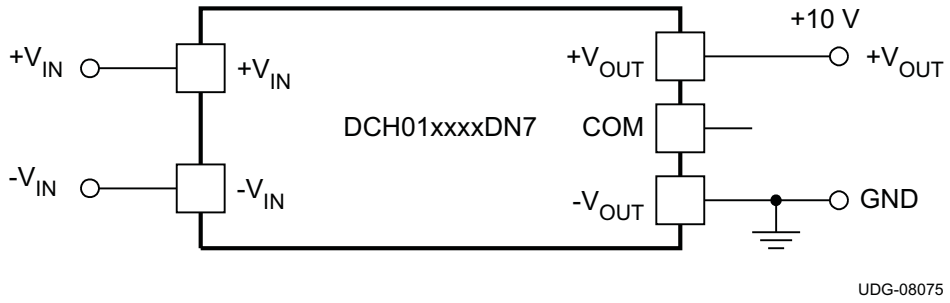


Figure 23. Connecting Dual Outputs in Series

CONNECTING THE DCH01 IN PARALLEL

If the output power from one DCH01 is not sufficient, it is possible to parallel the outputs of multiple DCH01s, as shown in Figure 24.

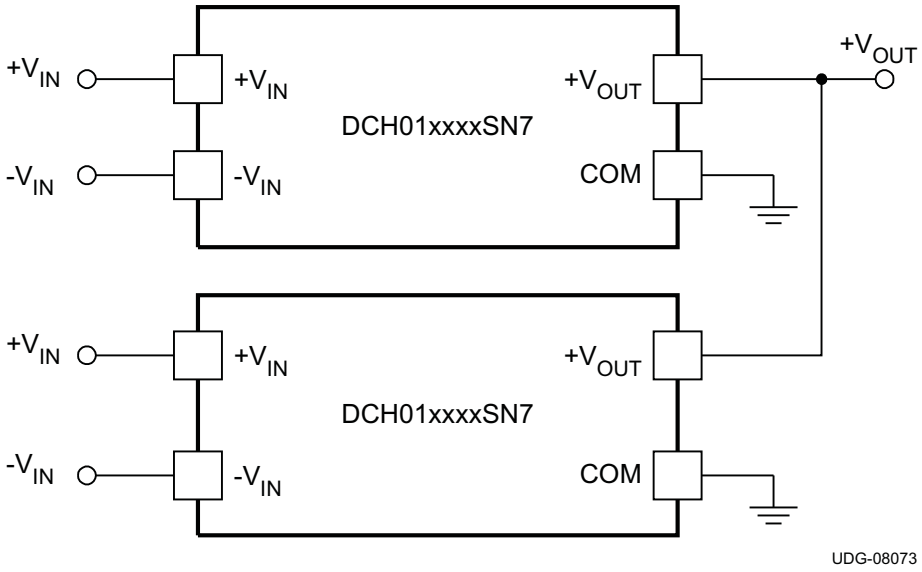


Figure 24. Connecting Multiple DCH01s in Parallel

PACKAGING INFORMATION

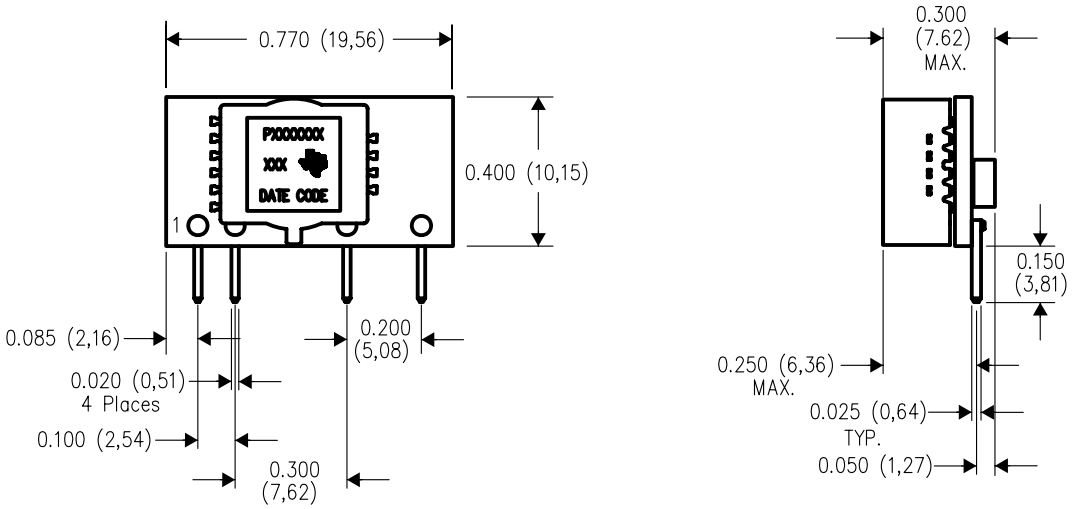
Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)
DCH010505DN7	ACTIVE	SIP MODULE	EDJ	5	70	Pb-Free (RoHS)	Call TI	N / A for Pkg Type
DCH010505SN7	ACTIVE	SIP MODULE	EDJ	4	70	Pb-Free (RoHS)	Call TI	N / A for Pkg Type
DCH010512DN7	ACTIVE	SIP MODULE	EDJ	5	70	Pb-Free (RoHS)	Call TI	N / A for Pkg Type
DCH010512SN7	ACTIVE	SIP MODULE	EDJ	4	70	Pb-Free (RoHS)	Call TI	N / A for Pkg Type
DCH010515DN7	ACTIVE	SIP MODULE	EDJ	5	70	Pb-Free (RoHS)	Call TI	N / A for Pkg Type
DCH010515SN7	ACTIVE	SIP MODULE	EDJ	4	70	Pb-Free (RoHS)	Call TI	N / A for Pkg Type

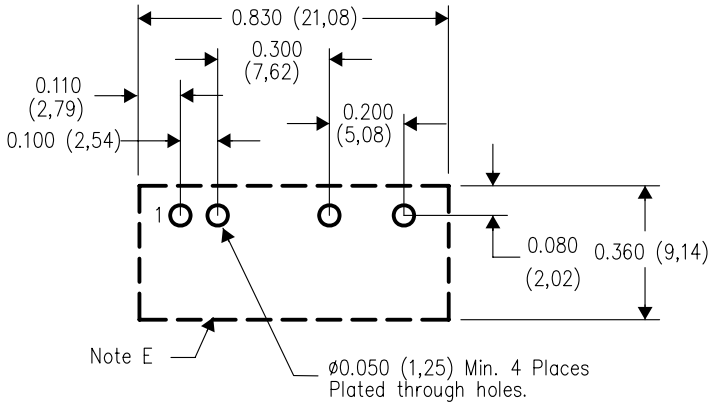
(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

EDJ (R–PDSS–T4) DOUBLE SIDED MODULE

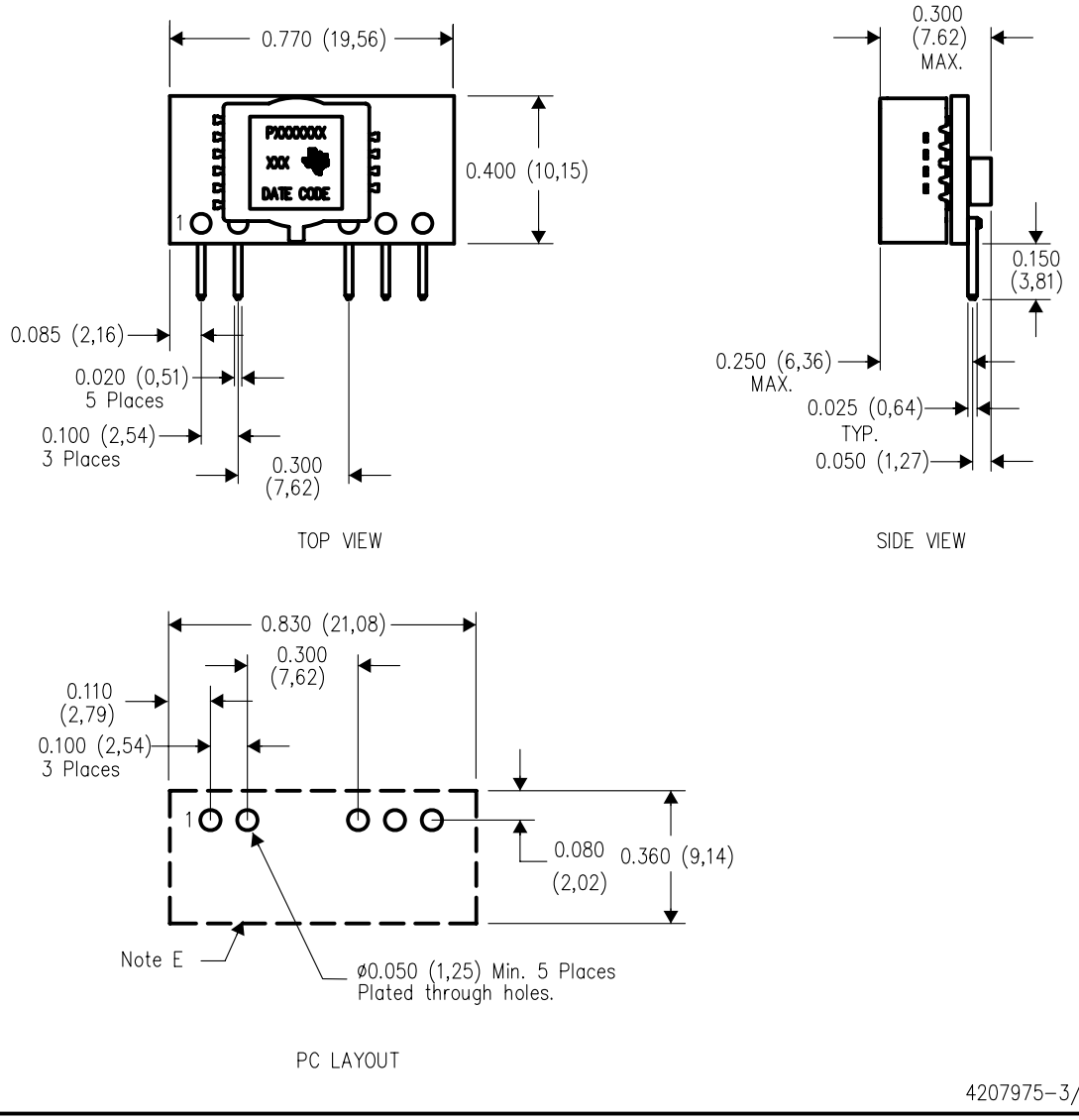




4207975–2/C 08/07

NOTES:
A. All linear dimensions are in inches (mm).
B. This drawing is subject to change without notice.
C. 2 place decimals are ±0.030 (±0,76mm).
D. 3 place decimals are ±0.010 (±0,25mm).
E. Recommended keep out area for user components.
F. Pins are 0.020" (0,51) x 0.025" (0,64).
G. All pins: Material – Copper Alloy
Finish – Tin (100%) over Nickel plate

EDJ (R–PDSS–T5) DOUBLE SIDED MODULE



4207975–3/C 08/07

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Finish – Tin (100%) over Nickel plate

IMPORTANT NOTICE

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