QUAD SERIAL INTERFACE LOW-SIDE DRIVER IC

Check for Samples: DRV8804

FEATURES

- **4-Channel Protected Low-Side Driver**
  - **Four NMOS FETs With Overcurrent Protection**
  - **Integrated Inductive Catch Diodes**
  - **Serial Interface**
- **1.5-A (Single Channel On) / 800-mA (Four Channels On) Maximum Drive Current per Channel (at 25°C)**
- **8.2-V to 60-V Operating Supply Voltage Range**
- **Thermally Enhanced Surface Mount Package**

APPLICATIONS

- **Relay Drivers**
- **Unipolar Stepper Motor Drivers**
- **Solenoid Drivers**
- **General Low-Side Switch Applications**

DESCRIPTION

The DRV8804 provides a 4-channel low side driver with overcurrent protection. It has built-in diodes to clamp turn-off transients generated by inductive loads and can be used to drive unipolar stepper motors, DC motors, relays, solenoids, or other loads.

The DRV8804 can supply up to 1.5-A (single channel on) or 800-mA (four channels on) continuous output current (with adequate PCB heatsinking at 25°C).

A serial interface is provided including a serial data output, which can be daisy-chained to control multiple devices with one serial interface.

Internal shutdown functions are provided for over current protection, short circuit protection, under voltage lockout and overtemperature and faults are indicated by a fault output pin.

The DRV8804 is available in a 20-pin thermally-enhanced SOIC package and a 16-pin HTSSOP package (Eco-friendly: RoHS & no Sb/Br).

ORDERING INFORMATION(1)

T_A	PACKAGE(2)		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 85°C	(SOIC) - DW	Reel of 2000	DRV8804DWR	DRV8804
		Tube of 25	DRV8804DW	DRV8804
	(HTSSOP) - PWP	Consult Factory		

(1) For the most current packaging and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.

(2) Package drawings, thermal data, and symbolization are available at www.ti.com/packaging.

DEVICE INFORMATION

Functional Block Diagram

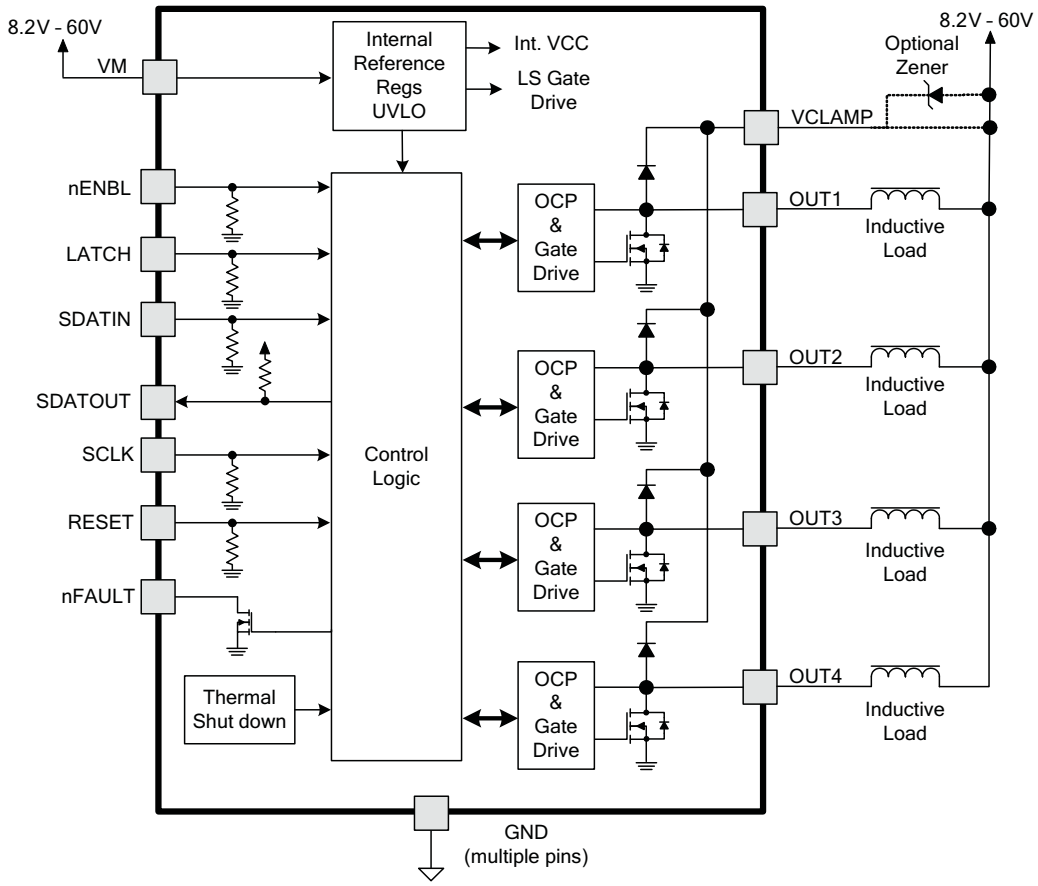
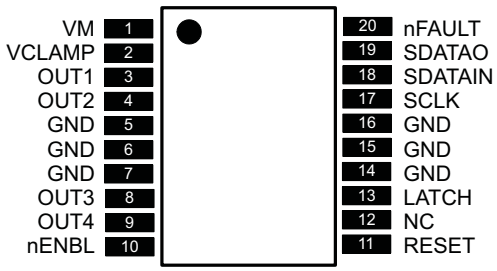


Table 1. TERMINAL FUNCTIONS

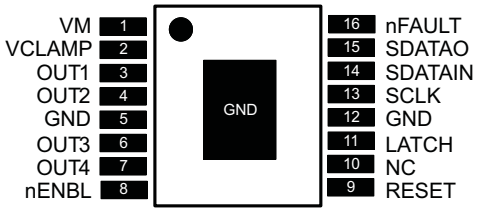
NAME	PIN (SOIC)	PIN (HTSSOP)	I/O(1)	DESCRIPTION	EXTERNAL COMPONENTS OR CONNECTIONS
POWER AND GROUND					
GND	5, 6, 7, 14, 15, 16	5, 12, PPAD	-	Device ground	All pins must be connected to GND.
VM	1	1	-	Device power supply	Connect to motor supply (8.2 V - 60 V).
CONTROL					
nENBL	10	8	I	Enable input	Active low enables outputs – internal pulldown
RESET	11	9	I	Reset input	Active-high reset input initializes internal logic – internal pulldown
LATCH	13	11	I	Latch input	Rising edge latches shift register to output stage – internal pulldown
SDATIN	18	14	I	Serial data input	Serial data input – internal pulldown
SDATOUT	19	15	O	Serial data output	Serial data output – has weak internal pullup – see serial interface section for details
SCLK	17	13	I	Serial clock	Serial clock input – internal pulldown
STATUS					
nFAULT	20	16	OD	Fault	Logic low when in fault condition (overtemp, overcurrent)
OUTPUT					
OUT1	3	3	O	Output 1	Connect to load 1
OUT2	4	4	O	Output 2	Connect to load 2
OUT3	8	6	O	Output 3	Connect to load 3
OUT4	9	7	O	Output 4	Connect to load 4
VCLAMP	2	2	-	Output clamp voltage	Connect to VM supply, or zener diode to VM supply

(1) Directions: I = input, O = output, OD = open-drain output

DW (WIDE SOIC) PACKAGE
(TOP SIDE)



PWP (HTSSOP) PACKAGE
(TOP SIDE)



ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted) (1) (2)

		VALUE	UNIT
VM	Power supply voltage range	–0.3 to 65	V
VOUTx	Output voltage range	–0.3 to 65	V
VCLAMP	Clamp voltage range	–0.3 to 65	V
SDATOUT, nFAULT	Output current	20	mA
	Peak clamp diode current	1.5	A
	DC or RMS clamp diode current	1	A
	Digital input pin voltage range	–0.5 to 7	V
SDATOUT, nFAULT	Digital output pin voltage range	–0.5 to 7	V
	Peak motor drive output current, t < 1 µS	Internally limited	A
	Continuous total power dissipation	See Dissipation Ratings table	
T_J	Operating virtual junction temperature range	–40 to 150	°C
T_{stg}	Storage temperature range	–60 to 150	°C

(1) Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under recommended operating conditions is not implied. Exposure to absolute–maximum–rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to network ground terminal.

THERMAL INFORMATION

THERMAL METRIC		DRV8804 DW 20 PINS	UNITS
θ_{JA}	Junction-to-ambient thermal resistance (1)	67.7	°C/W
θ_{JCtop}	Junction-to-case (top) thermal resistance (2)	32.9	
θ_{JB}	Junction-to-board thermal resistance (3)	35.4	
ψ_{JT}	Junction-to-top characterization parameter (4)	8.2	
ψ_{JB}	Junction-to-board characterization parameter (5)	34.9	
θ_{JCbot}	Junction-to-case (bottom) thermal resistance (6)	N/A	

(1) The junction-to-ambient thermal resistance under natural convection is obtained in a simulation on a JEDEC-standard, high-K board, as specified in JESD51-7, in an environment described in JESD51-2a.
(2) The junction-to-case (top) thermal resistance is obtained by simulating a cold plate test on the package top. No specific JEDEC-standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.
(3) The junction-to-board thermal resistance is obtained by simulating in an environment with a ring cold plate fixture to control the PCB temperature, as described in JESD51-8.
(4) The junction-to-top characterization parameter, ψ_{JT}, estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining θ_{JA}, using a procedure described in JESD51-2a (sections 6 and 7).
(5) The junction-to-board characterization parameter, ψ_{JB}, estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining θ_{JA} , using a procedure described in JESD51-2a (sections 6 and 7).
(6) The junction-to-case (bottom) thermal resistance is obtained by simulating a cold plate test on the exposed (power) pad. No specific JEDEC standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.

RECOMMENDED OPERATING CONDITIONS

		MIN	NOM	MAX	UNIT
V_M	Power supply voltage range	8.2		60	V
V_{CLAMP}	Output clamp voltage range	8.2		60	V
I_{OUT}	Continuous output current, single channel on, T_A = 25°C, SOIC package(1)			1.5	A
	Continuous output current, four channels on, T_A = 25°C, SOIC package(1)			0.8	
	Continuous output current, single channel on, T_A = 25°C, HTSSOP package(1)			1.5	
	Continuous output current, four channels on, T_A = 25°C, HTSSOP package(1)			0.8	

(1) Power dissipation and thermal limits must be observed.

ELECTRICAL CHARACTERISTICS

T_A = 25°C, over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
POWER SUPPLIES						
I_{VM}	VM operating supply current	V_M = 24 V		1.6	2.1	mA
V_{UVLO}	VM undervoltage lockout voltage	V_M rising			8.2	V
LOGIC-LEVEL INPUTS (SCHMITT TRIGGER INPUTS WITH HYSTERESIS)						
V_{IL}	Input low voltage			0.6	0.7	V
V_{IH}	Input high voltage		2			V
V_{HYS}	Input hysteresis			0.45		V
I_{IL}	Input low current	VIN = 0	–20		20	µA
I_{IH}	Input high current	VIN = 3.3 V			100	µA
R_{PD}	Pulldown resistance			100		kΩ
nFAULT OUTPUT (OPEN-DRAIN OUTPUT)						
V_{OL}	Output low voltage	I_O = 5 mA			0.5	V
I_{OH}	Output high leakage current	V_O = 3.3 V			1	µA
SDATAOUT OUTPUT (OPEN-DRAIN OUTPUT WITH INTERNAL PULLUP)						
V_{OL}	Output low voltage	I_O = 5 mA			0.5	V
V_{OH}	Output high voltage	I_O = 100 µA, V_M = 24 V		4.5		V
I_{OH}	Output high leakage current	V_O = 3.3 V			1	µA
LOW-SIDE FETS						
$R_{DS(ON)}$	FET on resistance	V_M = 24 V, I_O = 700 mA, T_J = 25°C		0.5		Ω
		V_M = 24 V, I_O = 700 mA, T_J = 85°C		0.75	0.8	
I_{OFF}	Off-state leakage current		–50		50	µA
HIGH-SIDE DIODES						
V_F	Diode forward voltage	V_M = 24 V, I_O = 700 mA, T_J = 25°C		1.2		V
I_{OFF}	Off-state leakage current	V_M = 24 V, T_J = 25°C	–50		50	µA
OUTPUTS						
t_R	Rise time	V_M = 24 V, I_O = 700 mA, Resistive load	50		300	ns
t_F	Fall time	V_M = 24 V, I_O = 700 mA, Resistive load	50		300	ns
PROTECTION CIRCUITS						
I_{OCP}	Overcurrent protection trip level		2.3		3.8	A
t_{OCP}	Overcurrent protection deglitch time			3.5		µs
t_{RETRY}	Overcurrent protection retry time			1.2		ms
t_{TSD}	Thermal shutdown temperature	Die temperature(1)	150	160	180	°C

(1) Not production tested.

TIMING REQUIREMENTS

over operating free-air temperature range (unless otherwise noted)(1)

NO.	PARAMETER	DESCRIPTION	MIN	MAX	UNIT
1	t_{CYC}	Clock cycle time	62		ns
2	t_{CLKH}	Clock high time	25		ns
3	t_{CLKL}	Clock low time	25		ns
4	$t_{SU(SDATIN)}$	Setup time, SDATIN to SCLK	5		ns
5	$t_{H(SDATIN)}$	Hold time, SDATIN to SCLK	1		ns
6	$t_{D(SDATOUT)}$	Delay time, SCLK to SDATOUT		15	ns
7	$t_{W(LATCH)}$	Pulse width, LATCH	200		ns
8	$t_{OE(ENABLE)}$	Enable time, nENBL to output low		50	ns
9	$t_{D(LATCH)}$	Delay time, LATCH to output change		50	ns
-	t_{RESET}	RESET pulse width	20		µs
10	$t_{D(RESET)}$	Reset delay before clock	20		µs
11	$t_{STARTUP}$	Startup delay VM applied before clock	55		µs

(1) Not production tested.

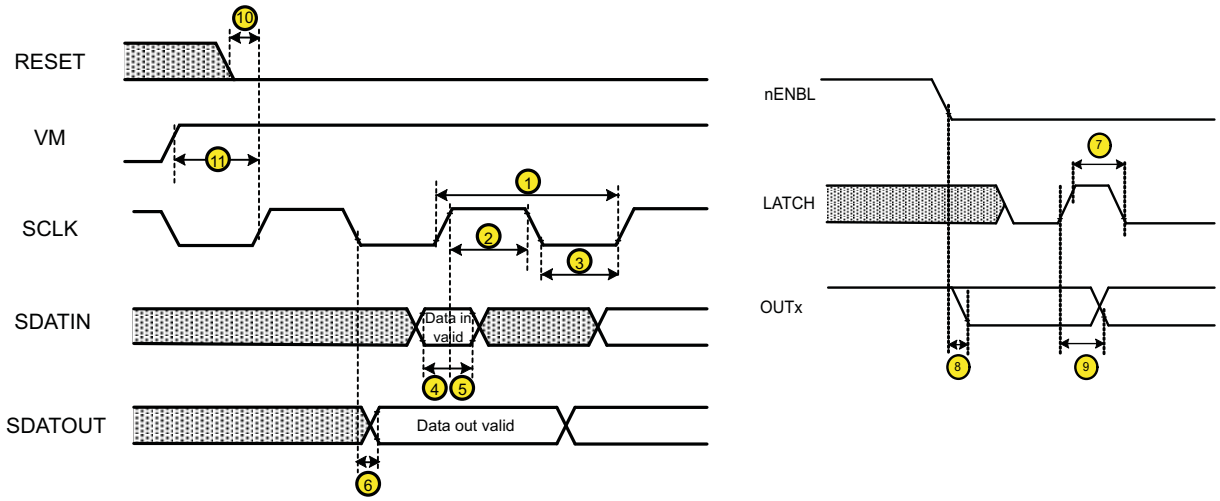


Figure 1. DRV8804 Timing Requirements

FUNCTIONAL DESCRIPTION

Output Drivers

The DRV8804 contains four protected low-side drivers. Each output has an integrated clamp diode connected to a common pin, VCLAMP.

VCLAMP can be connected to the main power supply voltage, VM. It can also be connected to a zener or TVS diode to VM, allowing the switch voltage to exceed the main supply voltage VM. This connection can be beneficial when driving loads that require very fast current decay, such as unipolar stepper motors.

In all cases, the voltage on the outputs must not be allowed to exceed the maximum output voltage specification.

Serial Interface Operation

The DRV8804 is controlled with a simple serial interface. Logically, the interface is shown in Figure 2.

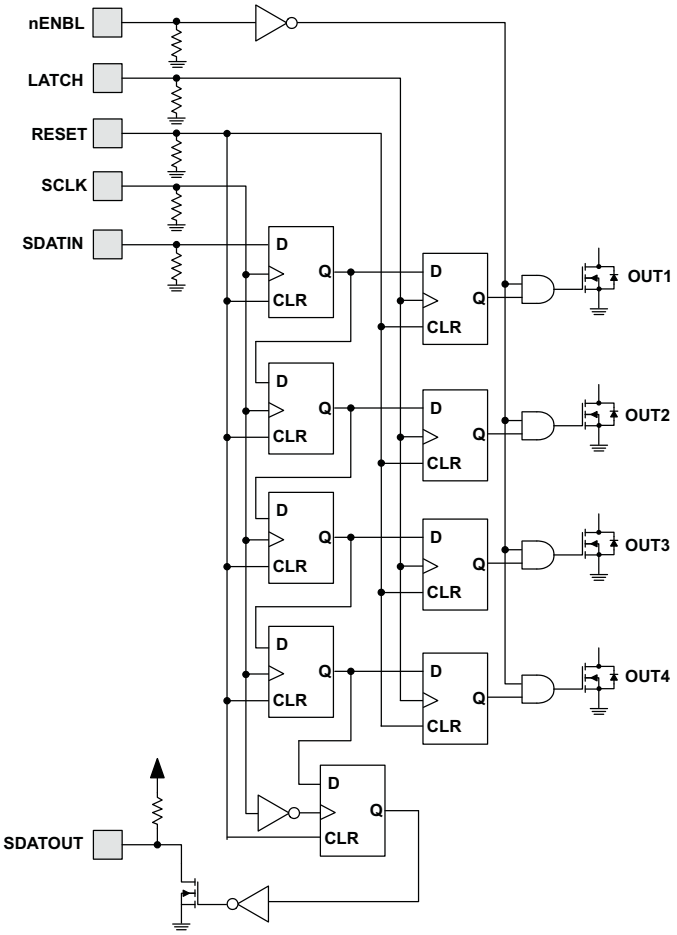


Figure 2. Serial Interface Operation

Data is shifted into a temporary holding shift register in the part using the SDATIN pin, one bit at each rising edge of the SCLK pin. Data is simultaneously shifted out of the SDATOUT pin, allowing multiple devices to be daisy-chained onto one serial port. Note that the SDTAOUT pin has a weak pullup to an internal power supply, which can support driving another DRV8804 SDATAIN pin at clock frequencies of up to 1 MHz without an external pullup. To operate at faster than 1-MHz clock frequency, or to interface to devices operating at other supply voltages, a pullup resistor of approximately 1 kΩ to the chosen logic supply voltage should be used.

A rising edge on the LATCH pin latches the data from the temporary shift register into the output stage.

nENBL and RESET Operation

The nENBL pin enables or disables the output drivers. nENBL must be low to enable the outputs. nENBL does not affect the operation of the serial interface logic. Note that nENBL has an internal pulldown.

The RESET pin, when driven active high, resets internal logic, including the OCP fault. All serial interface registers are cleared. Note that RESET has an internal pulldown. An internal power-up reset is also provided, so it is not required to drive RESET at power-up.

Protection Circuits

The DRV8804 is fully protected against undervoltage, overcurrent and overtemperature events.

Overcurrent Protection (OCP)

An analog current limit circuit on each FET limits the current through the FET by removing the gate drive. If this analog current limit persists for longer than the t_{OCP} deglitch time (approximately 3.5 µs), the driver will be disabled and the nFAULT pin will be driven low. The driver will remain disabled for the t_{RETRY} retry time (approximately 1.2 ms), then the fault will be automatically cleared. The fault will be cleared immediately if either RESET pin is activated or VM is removed and re-applied.

Thermal Shutdown (TSD)

If the die temperature exceeds safe limits, all output FETs will be disabled and the nFAULT pin will be driven low. Once the die temperature has fallen to a safe level, operation will automatically resume.

Undervoltage Lockout (UVLO)

If at any time the voltage on the VM pin falls below the undervoltage lockout threshold voltage, all circuitry in the device will be disabled, and internal logic will be reset. Operation will resume when VM rises above the UVLO threshold.

THERMAL INFORMATION

Thermal Protection

The DRV8804 has thermal shutdown (TSD) as described above. If the die temperature exceeds approximately 150°C, the device will be disabled until the temperature drops to a safe level.

Any tendency of the device to enter TSD is an indication of either excessive power dissipation, insufficient heatsinking, or too high an ambient temperature.

Power Dissipation

Power dissipation in the DRV8804 is dominated by the power dissipated in the output FET resistance, or RDS(ON). Average power dissipation of each FET when running a static load can be roughly estimated by Equation 1:

$$P = R_{DS(ON)} \bullet (I_{OUT})^2 \quad (1)$$

where P is the power dissipation of one FET, $R_{DS(ON)}$ is the resistance of each FET, and I_{OUT} is equal to the average current drawn by the load. Note that at start-up and fault conditions this current is much higher than normal running current; these peak currents and their duration also need to be taken into consideration. When driving more than one load simultaneously, the power in all active output stages must be summed.

The maximum amount of power that can be dissipated in the device is dependent on ambient temperature and heatsinking.

Note that $R_{DS(ON)}$ increases with temperature, so as the device heats, the power dissipation increases. This must be taken into consideration when sizing the heatsink.

Heatsinking

The DRV8804 package uses a standard SOIC outline, but has the center pins internally fused to the die pad in order to more efficiently remove heat from the device. The two center leads on each side of the package should be connected together to as large a copper area on the PCB as is possible to remove heat from the device. If the copper area is on the opposite side of the PCB from the device, thermal vias are used to transfer the heat between top and bottom layers.

In general, the more copper area that can be provided, the more power can be dissipated.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/ Ball Finish	MSL Peak Temp (3)	Samples (Requires Login)
DRV8804DW	PREVIEW	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	
DRV8804DWR	PREVIEW	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
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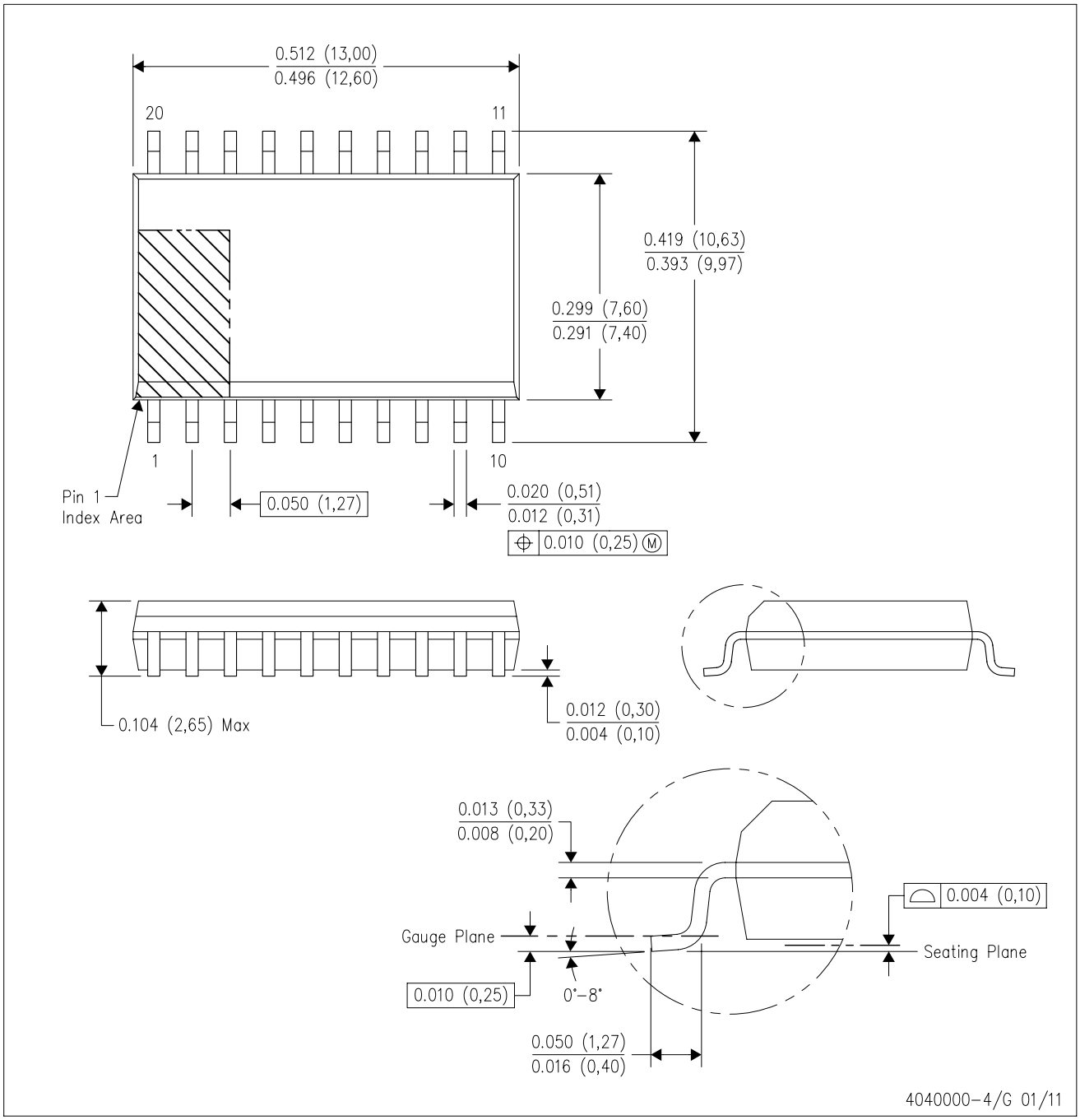
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

DW (R–PDSO–G20) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in inches (millimeters). Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
D. Falls within JEDEC MS–013 variation AC.

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