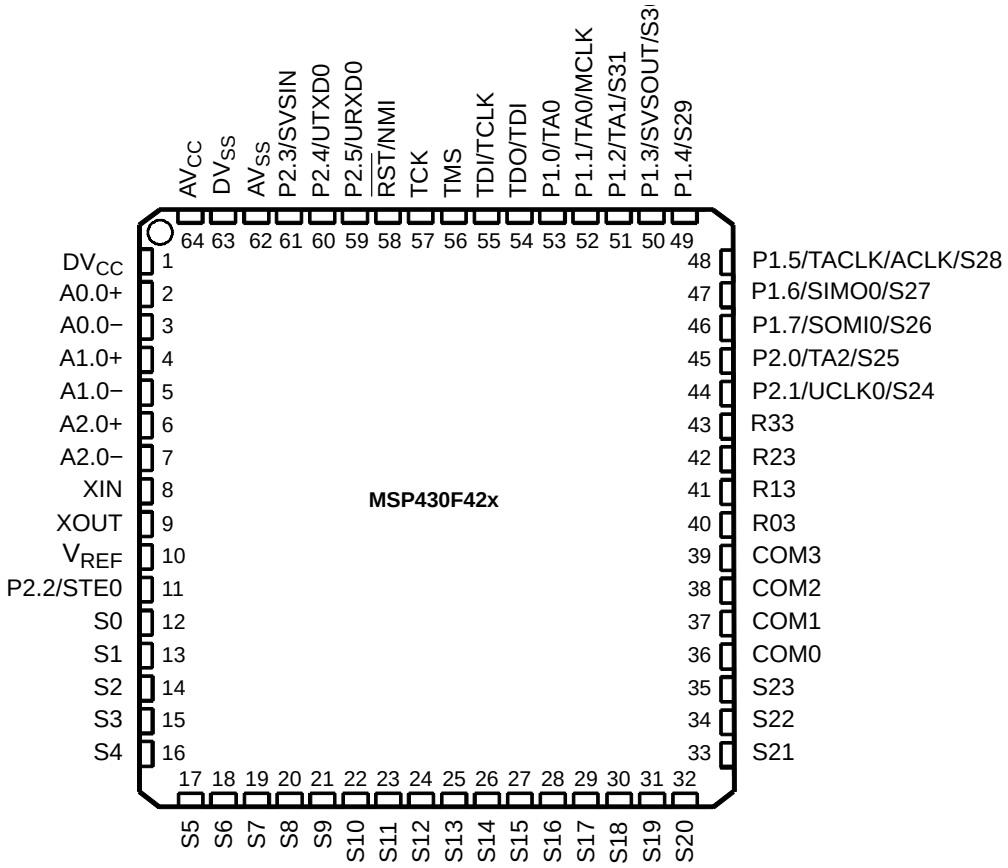
AVAILABLE OPTIONS

T_A	PACKAGED DEVICES
	PLASTIC 64-PIN QFP (PM)
−40°C to 85°C	MSP430F423IPM MSP430F425IPM MSP430F427IPM

pin designation†



† Open connection recommended for all unused analog inputs.

electrical characteristics over recommended operating free-air temperature (unless otherwise noted) (continued)

Schmitt-trigger inputs − Ports P1 and P2; $\overline{\text{RST}}$/NMI; JTAG: TCK, TMS, TDI/TCLK, TDO/TDI

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IT+}	Positive-going input threshold voltage	V_{CC} = 3 V	1.5		1.98	V
V_{IT-}	Negative-going input threshold voltage	V_{CC} = 3 V	0.9		1.3	V
V_{hys}	Input voltage hysteresis (V_{IT+} − V_{IT-})	V_{CC} = 3 V	0.45		1	V

inputs Px.x, TAx

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
$t_{(int)}$	External interrupt timing	Port P1, P2: P1.x to P2.x, External trigger signal for the interrupt flag, (see Note 1)	3 V	1.5			cycle
			3 V	50			ns
$t_{(cap)}$	Timer_A, capture timing	TAx	3 V	50			ns
$f_{(TAext)}$	Timer_A clock frequency externally applied to pin	TACLK, INCLK $t_{(H)} = t_{(L)}$	3 V			10	MHz
$f_{(TAint)}$	Timer_A clock frequency	SMCLK or ACLK signal selected	3 V			10	MHz

NOTES: 1. The external signal sets the interrupt flag every time the minimum $t_{(int)}$ cycle and time parameters are met. It may be set even with trigger signals shorter than $t_{(int)}$. Both the cycle and timing specifications must be met to ensure the flag is set. $t_{(int)}$ is measured in MCLK cycles.

leakage current (see Note 1)

PARAMETER			TEST CONDITIONS		MIN	NOM	MAX	UNIT
$I_{lkg(P1.x)}$	Leakage current	Port P1	Port 1: $V_{(P1.x)}$ (see Note 2)	V_{CC} = 3 V			±50	nA
$I_{lkg(P2.x)}$		Port P2	Port 2: $V_{(P2.x)}$ (see Note 2)				±50	

NOTES: 1. The leakage current is measured with V_{SS} or V_{CC} applied to the corresponding pin(s), unless otherwise noted.
2. The port pin must be selected as an input.

outputs − Ports P1 and P2

PARAMETER		TEST CONDITIONS			MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage	$I_{OH(max)}$ = −1.5 mA,	V_{CC} = 3 V,	See Note 1	V_{CC}−0.25		V_{CC}	V
		$I_{OH(max)}$ = −6 mA,	V_{CC} = 3 V,	See Note 2	V_{CC}−0.6		V_{CC}	
V_{OL}	Low-level output voltage	$I_{OL(max)}$ = 1.5 mA,	V_{CC} = 3 V,	See Note 1	V_{SS}		V_{SS}+0.25	V
		$I_{OL(max)}$ = 6 mA,	V_{CC} = 3 V,	See Note 2	V_{SS}		V_{SS}+0.6	

NOTES: 1. The maximum total current, $I_{OH(max)}$ and $I_{OL(max)}$, for all outputs combined, should not exceed ±12 mA to satisfy the maximum specified voltage drop.
2. The maximum total current, $I_{OH(max)}$ and $I_{OL(max)}$, for all outputs combined, should not exceed ±48 mA to satisfy the maximum specified voltage drop.

output frequency

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
$f_{Px.y}$	(1 ≤ x ≤ 2, 0 ≤ y ≤ 7)	C_L = 20 pF, I_L = ± 1.5mA	V_{CC} = 3 V	DC		12	MHz
f_{ACLK}, f_{MCLK}, f_{SMCLK}	P1.1/TA0/MCLK P1.5/TACLK/ACLK/S28	C_L = 20 pF	V_{CC} = 3 V			12	MHz
t_{Xdc}	Duty cycle of output frequency	P1.5/TACLK/ACLK/ S28, C_L = 20 pF V_{CC} = 3 V	$f_{ACLK} = f_{LFXT1} = f_{XT1}$	40%		60%	
			$f_{ACLK} = f_{LFXT1} = f_{LF}$	30%		70%	
			$f_{ACLK} = f_{LFXT1}$		50%		
		P1.1/TA0/MCLK, C_L = 20 pF, V_{CC} = 3 V	$f_{MCLK} = f_{DCOCLK}$	50%− 15 ns	50%	50%+ 15 ns	

electrical characteristics over recommended operating free-air temperature (unless otherwise noted) (continued)

crystal oscillator, LFXT1 oscillator (see Notes 1 and 2)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
C_{XIN}	Integrated input capacitance (see Note 4)	OSCCAPx = 0h	3 V		0		pF
		OSCCAPx = 1h	3 V		10		
		OSCCAPx = 2h	3 V		14		
		OSCCAPx = 3h	3 V		18		
C_{XOUT}	Integrated output capacitance (see Note 4)	OSCCAPx = 0h	3 V		0		pF
		OSCCAPx = 1h	3 V		10		
		OSCCAPx = 2h	3 V		14		
		OSCCAPx = 3h	3 V		18		
V_{IL}	Input levels at XIN	see Note 3	3 V	V_{SS}		$0.2 \times V_{CC}$	V
V_{IH}				$0.8 \times V_{CC}$		V_{CC}	

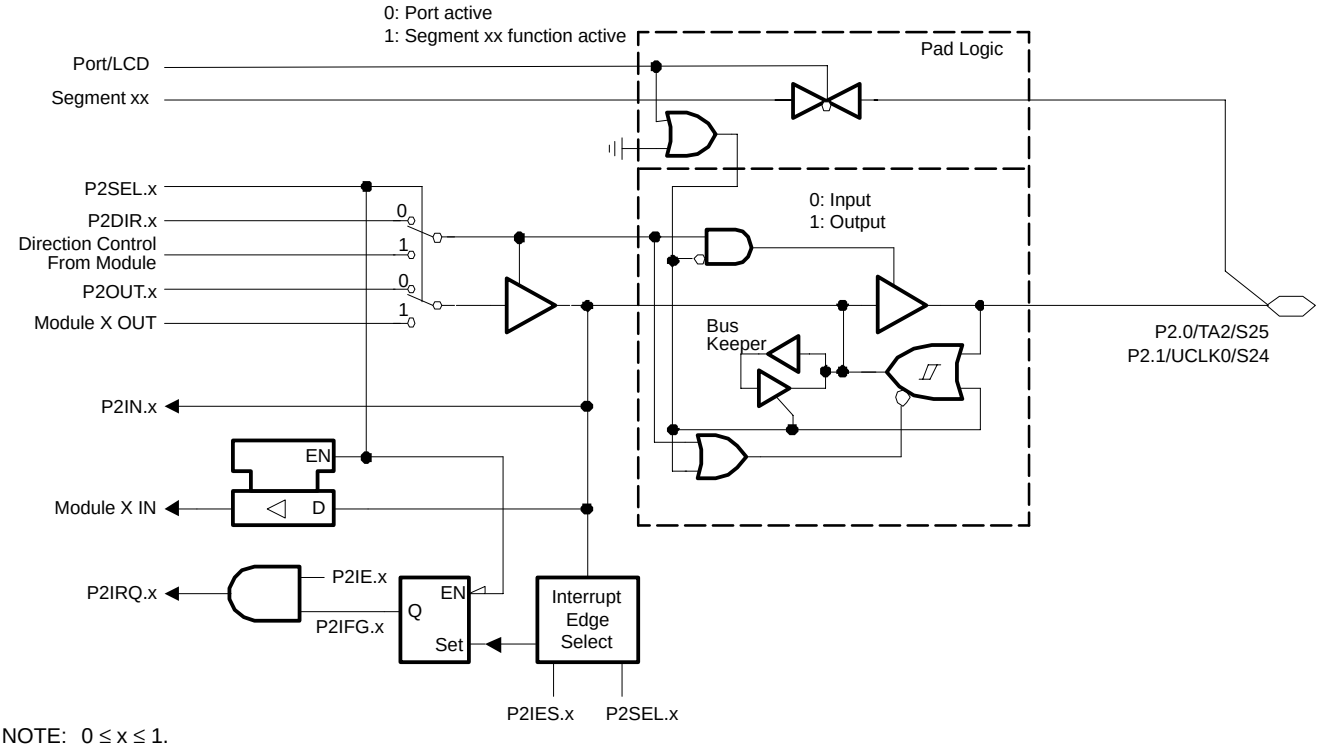
NOTES: 1. The parasitic capacitance from the package and board may be estimated to be 2pF. The effective load capacitor for the crystal is (C_{XIN} x C_{XOUT}) / (C_{XIN} + C_{XOUT}). It is independent of XTS_FLL.

2. To improve EMI on the low-power LFXT1 oscillator, particularly in the LF mode (32 kHz), the following guidelines must be observed:
   - Keep as short a trace as possible between the ’F42x and the crystal.
   - Design a good ground plane around oscillator pins.
   - Prevent crosstalk from other clock or data lines into oscillator pins XIN and XOUT.
   - Avoid running PCB traces underneath or adjacent to XIN an XOUT pins.
   - Use assembly materials and praxis to avoid any parasitic load on the oscillator XIN and XOUT pins.
   - If conformal coating is used, ensure that it does not induce capacitive/resistive leakage between the oscillator pins.
   - Do not route the XOUT line to the JTAG header to support the serial programming adapter as shown in other documentation. This signal is no longer required for the serial programming adapter.
3. Applies only when using an external logic-level clock source. XTS_FLL must be set. Not applicable when using a crystal or resonator.
4. External capacitance is recommended for precision real-time clock applications; OSCCAPx = 0h.

APPLICATION INFORMATION

input/output schematic (continued)

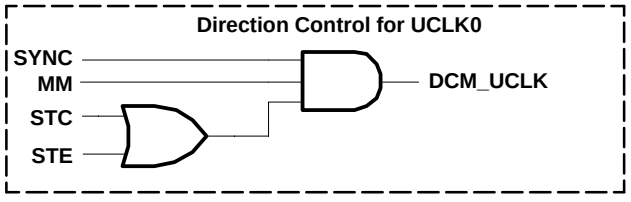
port P2, P2.0 to P2.1, input/output with Schmitt-trigger



NOTE: $0 \le x \le 1$.
Port Function is Active if Port/LCD = 0

PnSel.x	PnDIR.x	Dir. Control from module	PnOUT.x	Module X OUT	PnIN.x	Module X IN	PnIE.x	PnIFG.x	PnIES.x	Port/LCD	Segment
P2Sel.0	P2DIR.0	P2DIR.0	P2OUT.0	Out2sig.†	P2IN.0	CCI2A †	P2IE.0	P2IFG.0	P2IES.0	0: LCDM < 0E0h	S25
P2Sel.1	P2DIR.1	DCM_UCLK	P2OUT.1	UCLK0(o)‡	P2IN.1	UCLK0(i)‡	P2IE.1	P2IFG.1	P2IES.1	1: LCDM ≥ 0E0h	S24

† Timer_A3
‡ USART0



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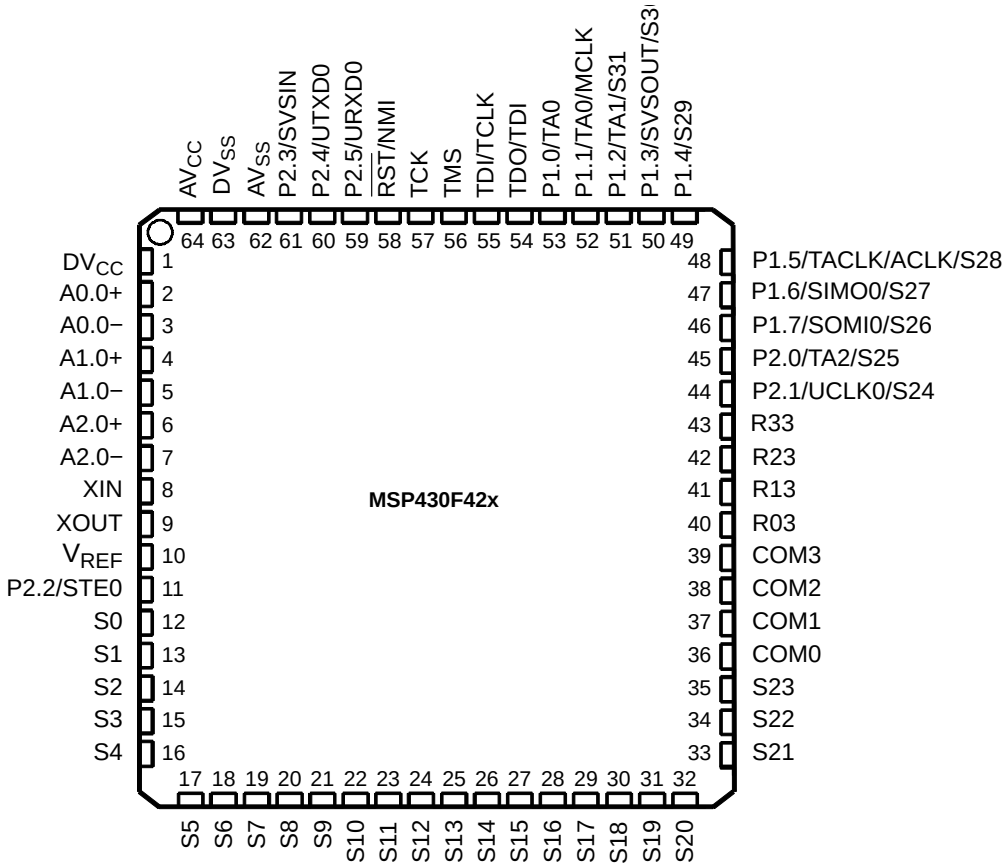
AVAILABLE OPTIONS

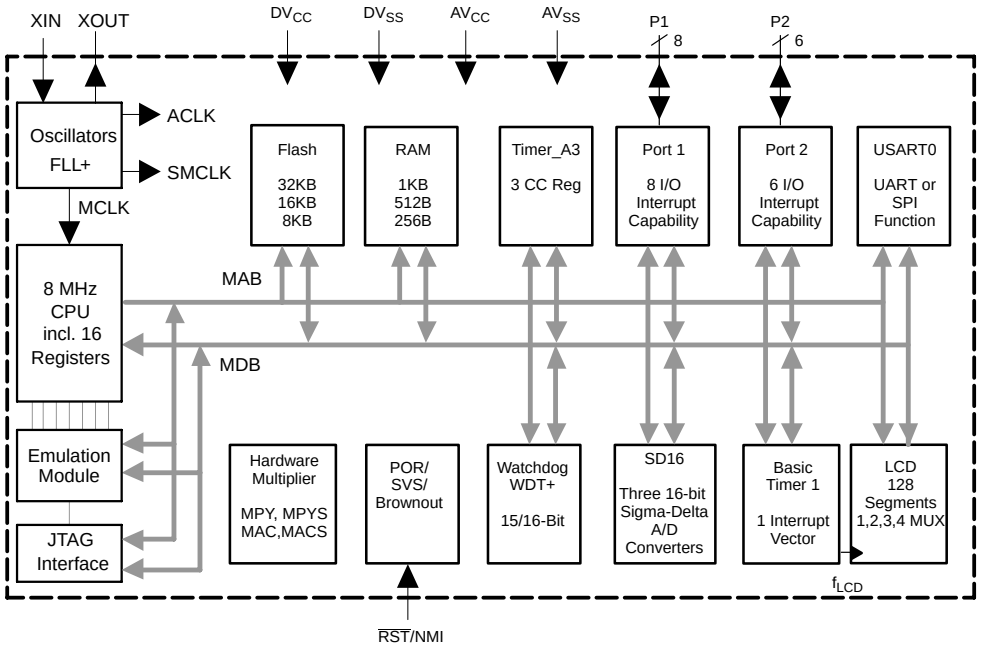
T_A	PACKAGED DEVICES
	PLASTIC 64-PIN QFP (PM)
−40°C to 85°C	MSP430F423IPM MSP430F425IPM MSP430F427IPM

pin designation†



† Open connection recommended for all unused analog inputs.

functional block diagram



MSP430F42x Terminal Functions

TERMINAL NAME	TERMINAL PN NO.	I/O	DESCRIPTION
DV_{CC}	1		Digital supply voltage, positive terminal.
A0.0+	2	I	Internal connection to SD16 Channel 0, input 0 +. (see Note 1)
A0.0−	3	I	Internal connection to SD16 Channel 0, input 0 −. (see Note 1)
A1.0+	4	I	Internal connection to SD16 Channel 1, input 0 +. (see Note 1)
A1.0−	5	I	Internal connection to SD16 Channel 1, input 0 −. (see Note 1)
A2.0+	6	I	Internal connection to SD16 Channel 2, input 0 +. (see Note 1)
A2.0−	7	I	Internal connection to SD16 Channel 2, input 0 −. (see Note 1)
XIN	8	I	Input port for crystal oscillator XT1. Standard or watch crystals can be connected.
XOUT	9	O	Output terminal of crystal oscillator XT1
V_{REF}	10	I/O	Input for an external reference voltage / internal reference voltage output (can be used as mid-voltage)
P2.2/STE0	11	I/O	General-purpose digital I/O / slave transmit enable—USART0/SPI mode
S0	12	O	LCD segment output 0
S1	13	O	LCD segment output 1
S2	14	O	LCD segment output 2
S3	15	O	LCD segment output 3
S4	16	O	LCD segment output 4
S5	17	O	LCD segment output 5
S6	18	O	LCD segment output 6
S7	19	O	LCD segment output 7
S8	20	O	LCD segment output 8
S9	21	O	LCD segment output 9
S10	22	O	LCD segment output 10
S11	23	O	LCD segment output 11
S12	24	O	LCD segment output 12
S13	25	O	LCD segment output 13
S14	26	O	LCD segment output 14
S15	27	O	LCD segment output 15
S16	28	O	LCD segment output 16
S17	29	O	LCD segment output 17
S18	30	O	LCD segment output 18
S19	31	O	LCD segment output 19
S20	32	O	LCD segment output 20
S21	33	O	LCD segment output 21
S22	34	O	LCD segment output 22
S23	35	O	LCD segment output 23
COM0	36	O	Common output, COM0−3 are used for LCD backplanes.
COM1	37	O	Common output, COM0−3 are used for LCD backplanes.
COM2	38	O	Common output, COM0−3 are used for LCD backplanes.
COM3	39	O	Common output, COM0−3 are used for LCD backplanes.
R03	40	I	Input port of fourth positive (lowest) analog LCD level (V5)

NOTE 1: Open connection recommended for all unused analog inputs.