AVAILABLE OPTIONS

T_A	PACKAGED DEVICES†‡	
	PLASTIC BGA 113-BALL (ZQW)§	PLASTIC 80-PIN QFP (PN)
−40 °C to 85 °C	MSP430F477IZQW MSP430F478IZQW MSP430F479IZQW	MSP430F477IPN MSP430F478IPN MSP430F479IPN

† For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.
‡ Package drawings, thermal data, and symbolization are available at www.ti.com/packaging.
§ Product Preview

DEVELOPMENT TOOL SUPPORT

All MSP430 microcontrollers include an Embedded Emulation Module (EEM) allowing advanced debugging and programming through easy to use development tools. Recommended hardware options include the following:

- Debugging and Programming Interface
  - MSP−FET430UIF (USB)
  - MSP−FET430PIF (Parallel Port)
- Debugging and Programming Interface with Target Board
  - MSP−FET430U80
- Production Programmer
  - MSP−GANG430

PRODUCT PREVIEW

watchdog timer (WDT+)

The primary function of the WDT+ module is to perform a controlled system restart after a software problem occurs. If the selected time interval expires, a system reset is generated. If the watchdog function is not needed in an application, the module can be configured as an interval timer and can generate interrupts at selected time intervals.

Basic Timer1 and real-time clock

The Basic Timer1 has two independent 8-bit timers that can be cascaded to form a 16-bit timer/counter. Both timers can be read and written by software. The Basic Timer1 is extended to provide an integrated real-time clock (RTC). An internal calendar compensates for month with less than 31 days and includes leap year correction.

LCD_A driver with regulated charge pump

The LCD_A driver generates the segment and common signals required to drive an LCD display. The LCD_A controller has dedicated data memory to hold segment drive information. Common and segment signals are generated as defined by the mode. Static, 2-MUX, 3-MUX, and 4-MUX LCDs are supported by this peripheral. The module can provide a LCD voltage independent of the supply voltage via an integrated charge pump. Furthermore, it is possible to control the level of the LCD voltage and, thus, contrast in software.

Timer_A3

Timer_A3 is a 16-bit timer/counter with three capture/compare registers. Timer_A3 can support multiple capture/compares, PWM outputs, and interval timing. Timer_A3 also has extensive interrupt capabilities. Interrupts may be generated from the counter on overflow conditions and from each of the capture/compare registers.

TIMER_A3 SIGNAL CONNECTIONS

INPUT PIN NUMBER		DEVICE INPUT SIGNAL	MODULE INPUT NAME	MODULE BLOCK	MODULE OUTPUT SIGNAL	OUTPUT PIN NUMBER	
PN	ZQW					PN	ZQW
P1.5 – 51	F11	TACLK	TACLK	Timer	NA		
		ACLK	ACLK				
		SMCLK	SMCLK				
P1.5 – 51	F11	TAINCLK	INCLK				
P1.0 – 58	C11	TA0	CCI0A	CCR0	TA0	P1.0 – 58	C11
P1.1 – 57	C12	TA0	CCI0B			P1.1 – 57	C12
		DV_{SS}	GND				
		DV_{CC}	V_{CC}				
P1.2 – 56	D11	TA1	CCI1A	CCR1	TA1	P1.2 – 56	D11
		CAOUT (internal)	CCI1B				
		DV_{SS}	GND				
		DV_{CC}	V_{CC}				
P2.0 – 4	C2	TA2	CCI2A	CCR2	TA2	P2.0 – 4	C2
		ACLK (internal)	CCI2B				
		DV_{SS}	GND				
		DV_{CC}	V_{CC}				

PRODUCT PREVIEW

PRODUCT PREVIEW

Timer_B3

Timer_B3 is a 16-bit timer/counter with three capture/compare registers. Timer_B3 can support multiple capture/compares, PWM outputs, and interval timing. Timer_B3 also has extensive interrupt capabilities. Interrupts may be generated from the counter on overflow conditions and from each of the capture/compare registers.

TIMER_B3 SIGNAL CONNECTIONS							
INPUT PIN NUMBER		DEVICE INPUT SIGNAL	MODULE INPUT NAME	MODULE BLOCK	MODULE OUTPUT SIGNAL	OUTPUT PIN NUMBER	
PN	ZQW					PN	ZQW
P1.4 – 54	E11	TBCLK	TBCLK	Timer	NA		
		ACLK	ACLK				
		SMCLK	SMCLK				
P1.4 – 54	E11	$\overline{\text{TBCLK}}$ (See Note 1)	INCLK				
P2.1 – 3	C1	TB0	CCI0A	CCR0	TB0	P2.1 – 3	C1
P2.1 – 3	C1	TB0	CCI0B				
		V_{SS}	GND				
		V_{CC}	V_{CC}				
P2.2 – 2	B1	TB1	CCI1A	CCR1	TB1	P2.2 – 2	B1
P2.2 – 2	B1	TB1	CCI1B				
		V_{SS}	GND				
		V_{CC}	V_{CC}				
P2.3 – 77	B4	TB2	CCI2A	CCR2	TB2	P2.3 – 77	B4
		ACLK (internal)	CCI2B				
		V_{SS}	GND				
		V_{CC}	V_{CC}				

NOTE 1: The inversion of TBCLK is done inside the module.

universal serial communication interfaces (USCIs) (USCI_A0, USCI_B0)

The USCI module is used for serial data communication. The USCI module supports synchronous communication protocols such as SPI (3 pin or 4 pin), I2C, and asynchronous communication protocols such as UART, enhanced UART with automatic baudrate detection (LIN), and IrDA.

USCI_A0 provides support for SPI (3 pin or 4 pin), UART, enhanced UART and IrDA.

USCI_B0 provides support for SPI (3 pin or 4 pin) and I2C.

Comparator_A

The primary function of the Comparator_A module is to support precision slope analog-to-digital conversions, battery-voltage supervision, and monitoring of external analog signals.

peripheral file map (continued)

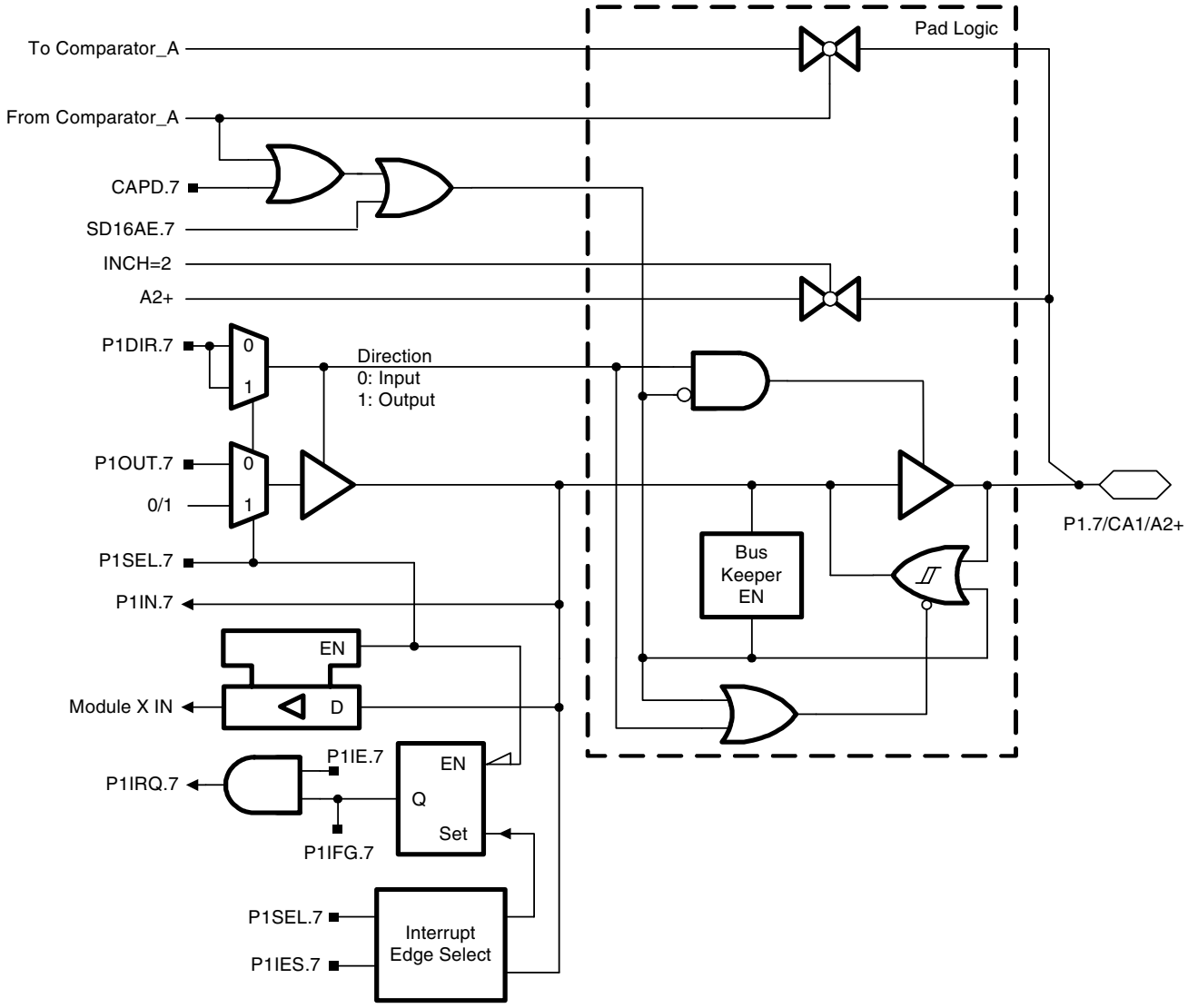
PERIPHERALS WITH BYTE ACCESS			
RTC (Basic Timer1)	Real-time clock year high byte	RTCYEARH	04Fh
	Real-time clock year low byte	RTCYEARL	04Eh
	Real-time clock month	RTCMON	04Dh
	Real-time clock day of month	RTCDAY	04Ch
	Basic Timer1 counter	BTCNT2	047h
	Basic Timer1 counter	BTCNT1	046h
	Real-time counter 4	RTCNT4	045h
	(Real-time clock day of week)	(RTCDOW)	
	Real-time counter 3	RTCNT3	044h
	(Real-time clock hour)	(RTCHOUR)	
	Real-time counter 2	RTCNT2	043h
	(Real-time clock minute)	(RTCMIN)	
	Real-time counter 1	RTCNT1	042h
	(Real-time clock second)	(RTCSEC)	
	Real-time clock control	RTCCTL	041h
	Basic Timer1 control	BTCTL	040h
Port P6	Port P6 selection	P6SEL	037h
	Port P6 direction	P6DIR	036h
	Port P6 output	P6OUT	035h
	Port P6 input	P6IN	034h
Port P5	Port P5 selection	P5SEL	033h
	Port P5 direction	P5DIR	032h
	Port P5 output	P5OUT	031h
	Port P5 input	P5IN	030h
Port P4	Port P4 selection	P4SEL	01Fh
	Port P4 direction	P4DIR	01Eh
	Port P4 output	P4OUT	01Dh
	Port P4 input	P4IN	01Ch
Port P3	Port P3 selection	P3SEL	01Bh
	Port P3 direction	P3DIR	01Ah
	Port P3 output	P3OUT	019h
	Port P3 input	P3IN	018h
Port P2	Port P2 selection	P2SEL	02Eh
	Port P2 interrupt enable	P2IE	02Dh
	Port P2 interrupt-edge select	P2IES	02Ch
	Port P2 interrupt flag	P2IFG	02Bh
	Port P2 direction	P2DIR	02Ah
	Port P2 output	P2OUT	029h
	Port P2 input	P2IN	028h

PRODUCT PREVIEW

PRODUCT PREVIEW

APPLICATION INFORMATION

Port P1 pin schematic: P1.7, input/output with Schmitt trigger



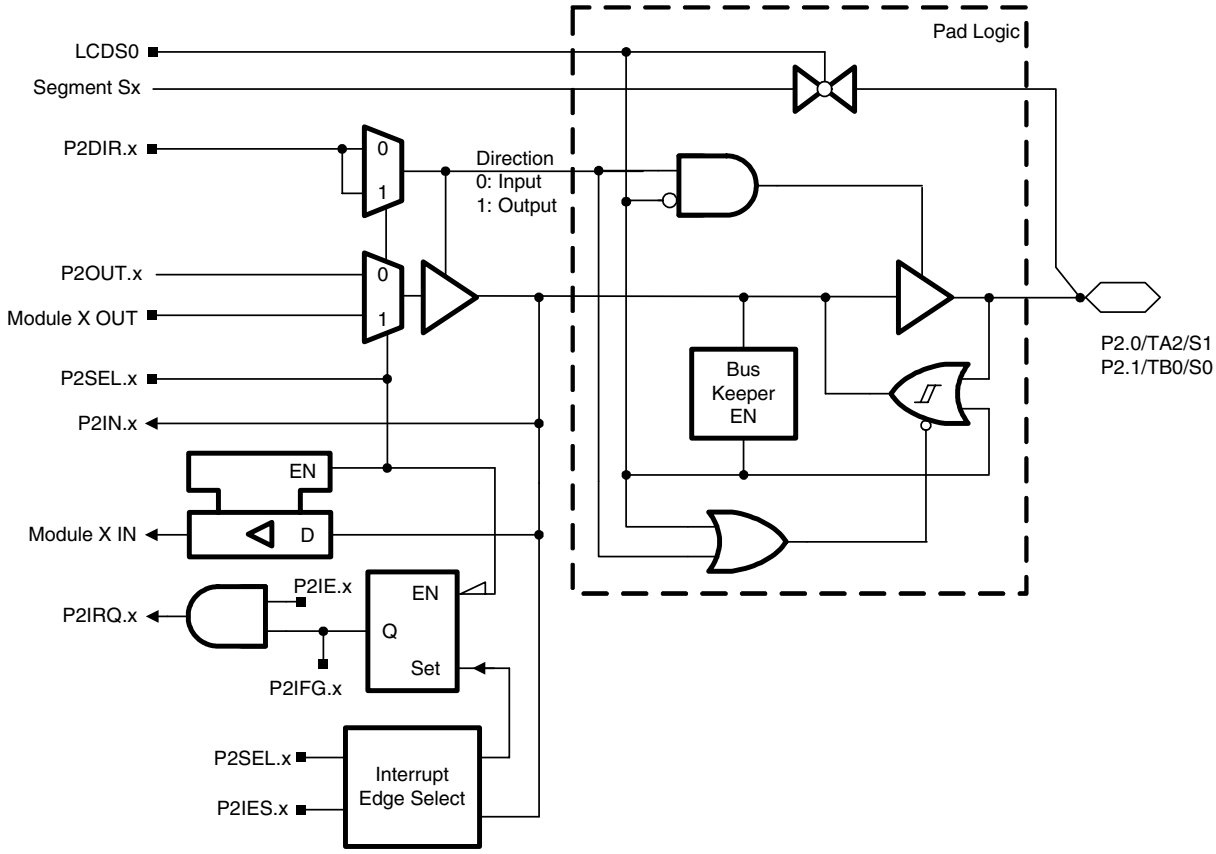
Port P1 (P1.7) pin functions

PIN NAME (P1.X)	X	FUNCTION	CONTROL BITS / SIGNALS			
			P1DIR.x	P1SEL.x	P1SEL2.x = 0 CAPD.x	P1SEL2.x = 0 SD16AE.x
P1.7/CA1/A2+	7	P1.x (I/O)	I: 0; O: 1	0	0	0
		CA1	x	x	1 or selected	x
		A2+	x	x	x	1

NOTES: 1. x: Don't care

APPLICATION INFORMATION

Port P2 pin schematic: P2.0 to P2.1, input/output with Schmitt trigger



Port P2 (P2.0 to P2.1) pin functions

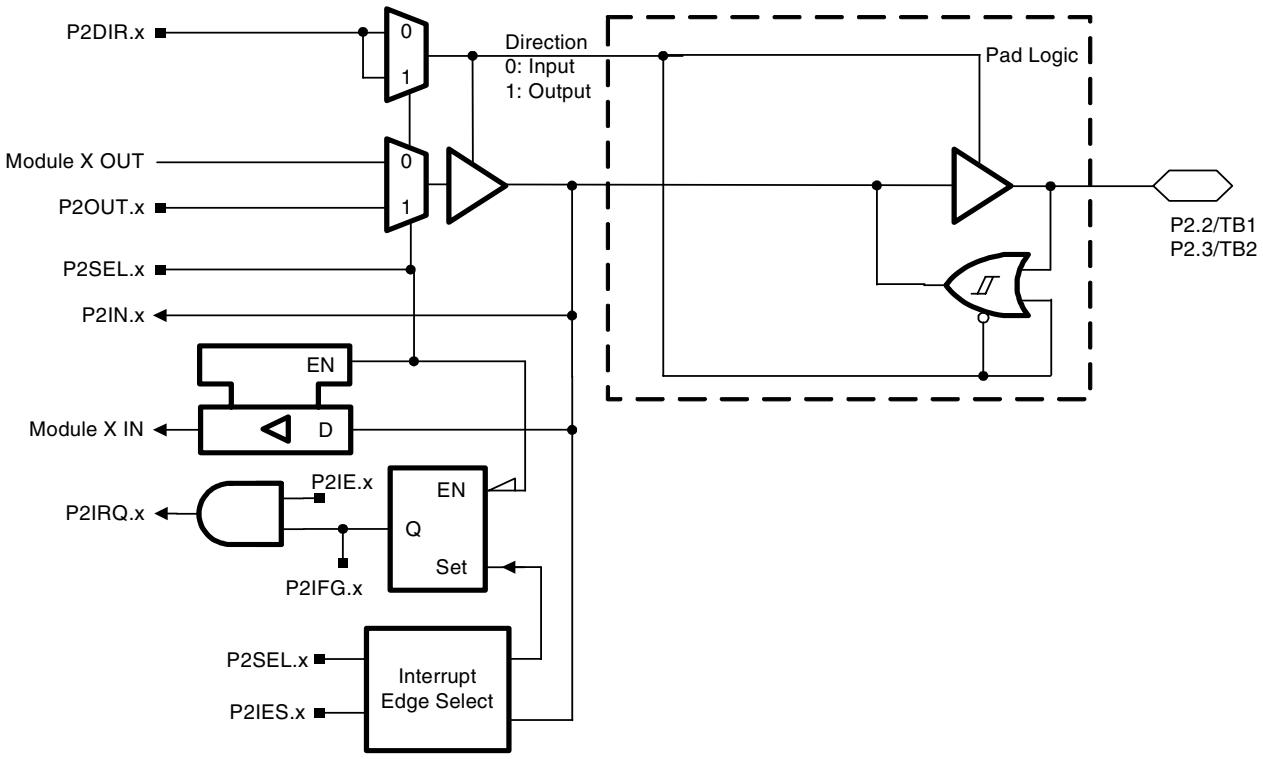
PIN NAME (P2.X)	X	FUNCTION	CONTROL BITS / SIGNALS		
			P2DIR.x	P2SEL.x	LCDS0
P2.0/TA2/S1	0	P2.x (I/O)	I: 0; O: 1	0	0
		Timer_A3.CCI2A	0	1	0
		Timer_A3.TA2	1	1	0
		S1	x	x	1
P2.1/TB0/S0	1	P2.x (I/O)	I: 0; O: 1	0	0
		Timer_B3.CCI0A	0	1	0
		Timer_B3.TB0	1	1	0
		S0	x	x	1

NOTES: 1. x: Don't care

PRODUCT PREVIEW

APPLICATION INFORMATION

Port P2 pin schematic: P2.2 to P2.3, input/output with Schmitt trigger



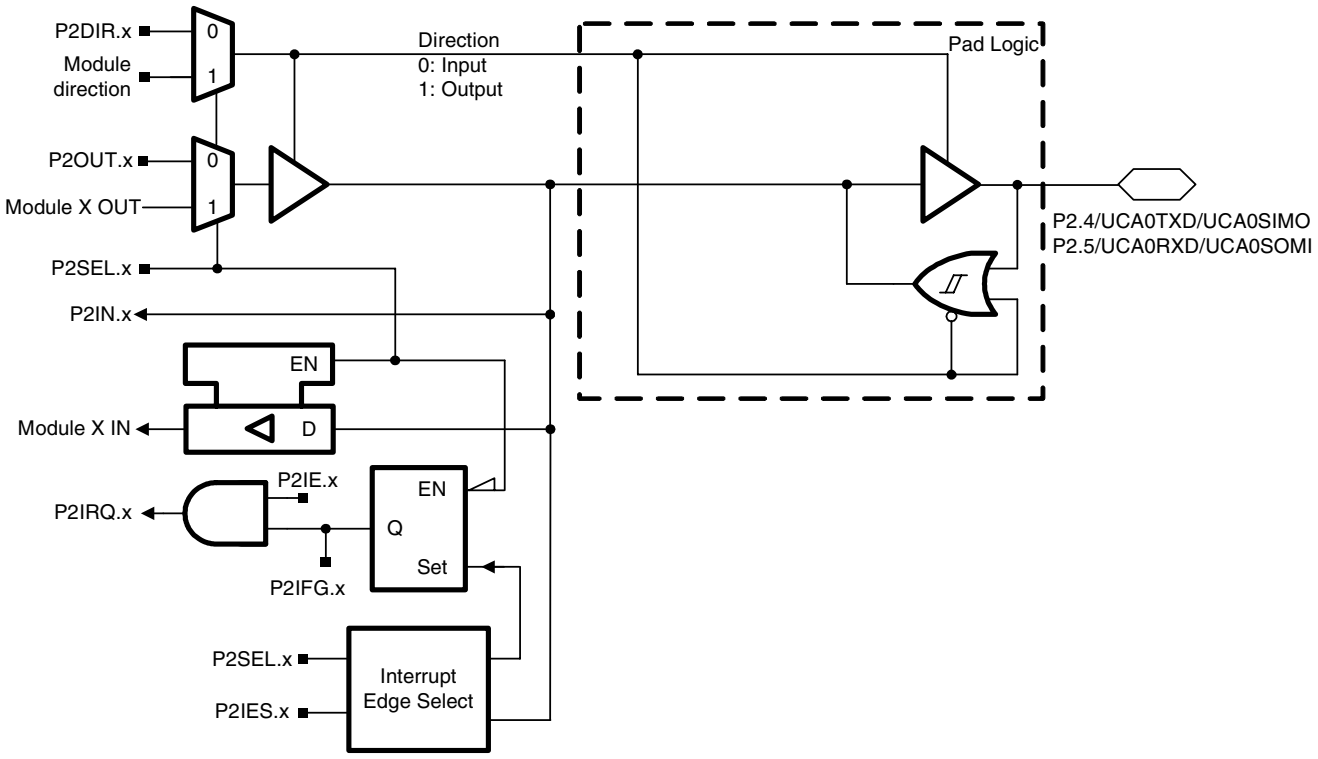
Port P2 (P2.2 to P2.3) pin functions

PIN NAME (P2.X)	X	FUNCTION	CONTROL BITS / SIGNALS	
			P2DIR.x	P2SEL.x
P2.2/TB1	2	P2.x (I/O)	I: 0; O: 1	0
		Timer_B3.CCI1A	0	1
		Timer_B3.TB1	1	1
P2.3/TB2	3	P2.x (I/O)	I: 0; O: 1	0
		Timer_B3.CCI2A	0	1
		Timer_B3.TB2	1	1

PRODUCT PREVIEW

APPLICATION INFORMATION

Port P2 pin schematic: P2.4 and P2.5, input/output with Schmitt trigger



Port P2 (P2.4 and P2.5) pin functions

PIN NAME (P2.X)	X	FUNCTION	CONTROL BITS / SIGNALS	
			P2DIR.x	P2SEL.x
P2.4/UCA0TXD/ UCA0SIMO	4	P2.x (I/O)	I: 0; O: 1	0
		UCA0TXD/UCA0SIMO (see Notes 2)	x	1
P2.5/UCA0RXD/ UCA0SOMI	5	P2.x (I/O)	I: 0; O: 1	0
		UCA0RXD/UCA0SOMI (see Notes 2)	x	1

NOTES: 1. x: Don't care
2. The pin direction is controlled by the USCI module.

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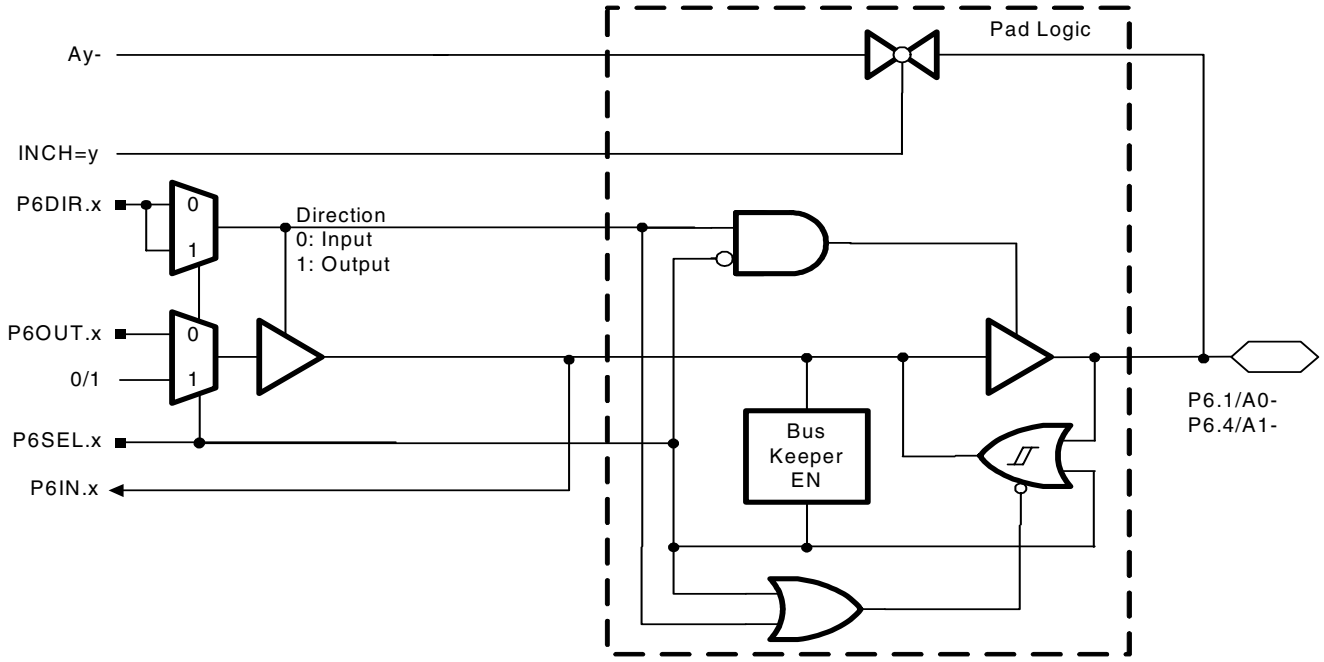
PRODUCT PREVIEW

APPLICATION INFORMATION

Port P6 pin schematic: P6.1 and P6.4, input/output with Schmitt trigger



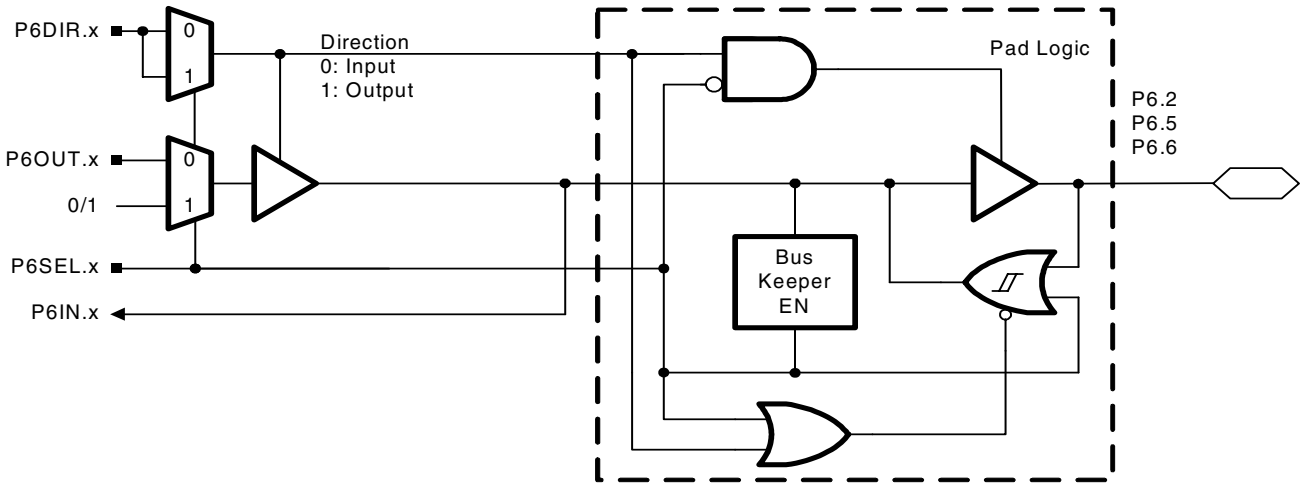
Port P6 (P6.1 and P6.4) pin functions

PIN NAME (P6.X)	X	FUNCTION	CONTROL BITS / SIGNALS	
			P6DIR.x	P6SEL.x
P6.1/A0–	1	P6.x (I/O)	I: 0; O: 1	0
		A0–	x	1
P6.4/A1–	4	P6.x (I/O)	I: 0; O: 1	0
		A1–	x	1

NOTES: 1. x: Don't care

APPLICATION INFORMATION

Port P6 pin schematic: P6.2, P6.5 and P6.6, input/output with Schmitt trigger



Port P6 (P6.2, P6.5 and P6.6) pin functions

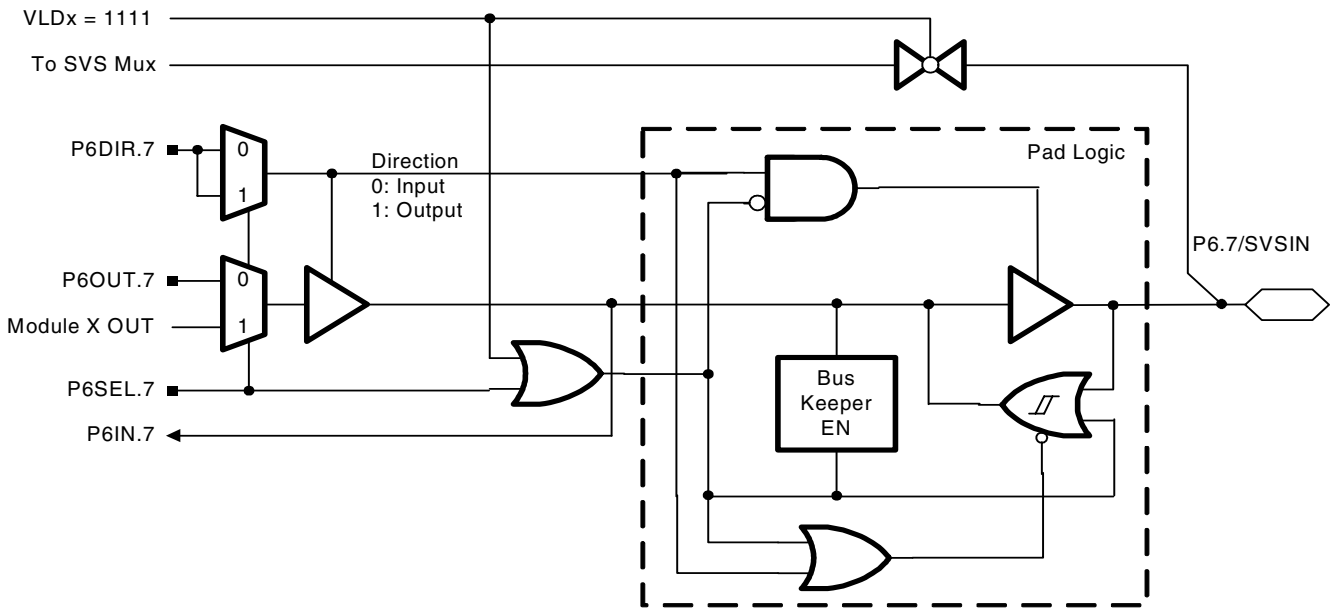
PIN NAME (P6.X)	X	FUNCTION	CONTROL BITS / SIGNALS	
			P6DIR.x	P6SEL.x
P6.2	2	P6.x (I/O)	I: 0; O: 1	0
P6.5	5	P6.x (I/O)	I: 0; O: 1	0
P6.6	6	P6.x (I/O)	I: 0; O: 1	0

NOTES: 1. x: Don't care

PRODUCT PREVIEW

APPLICATION INFORMATION

Port P6 pin schematic: P6.7, input/output with Schmitt trigger



Port P6 (P6.7) pin functions

PIN NAME (P6.X)	X	FUNCTION	CONTROL BITS / SIGNALS		
			P6DIR.x	P6SEL.x	VLDx
P6.7/SVSIN	7	P6.x (I/O)	I: 0; O: 1	0	x
		SVSIN	x	1	1111

NOTES: 1. x: Don't care

PRODUCT PREVIEW

MSP430F47x
MIXED SIGNAL MICROCONTROLLER

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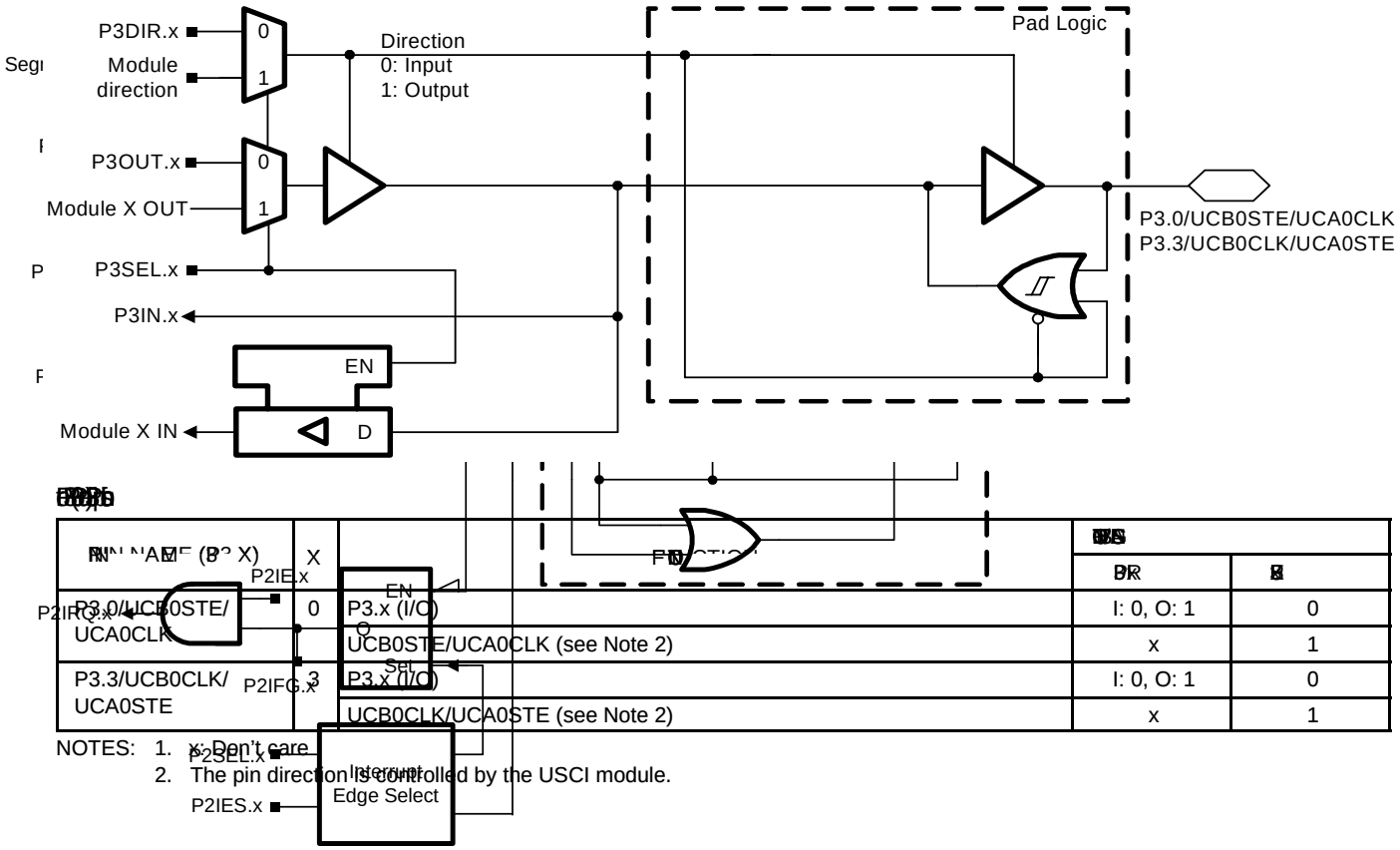

PIN NAME (P3.X)	X	FUNCTION	SELECTION	
			P3DIR	P3SEL
P3.0/UCB0STE/ UCA0CLK	0	P3.x (I/O)	I: 0, O: 1	0
		UCB0STE/UCA0CLK (see Note 2)	x	1
P3.3/UCB0CLK/ UCA0STE	3	P3.x (I/O)	I: 0, O: 1	0
		UCB0CLK/UCA0STE (see Note 2)	x	1

NOTES: 1. x: Don't care
2. The pin direction is controlled by the USCI module.

PIN NAME (P2.X)	X	FUNCTION	SELECTION		
			P2DIR	P2SEL	CAOUT
P2.6/CAOUT/S2	6	P2.x (I/O)	I: 0, O: 1	0	0
		CAOUT	1	1	0
		S2	x	x	1
P2.7/S3	7	P2.x (I/O)	I: 0, O: 1	0	0
		V_{SS}	1	1	0
		S3	x	x	1

NOTES: 1. x: Don't care

AVAILABLE OPTIONS

T_A	PACKAGED DEVICES†‡	
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−40 °C to 85 °C	MSP430F477IZQW MSP430F478IZQW MSP430F479IZQW	MSP430F477IPN MSP430F478IPN MSP430F479IPN

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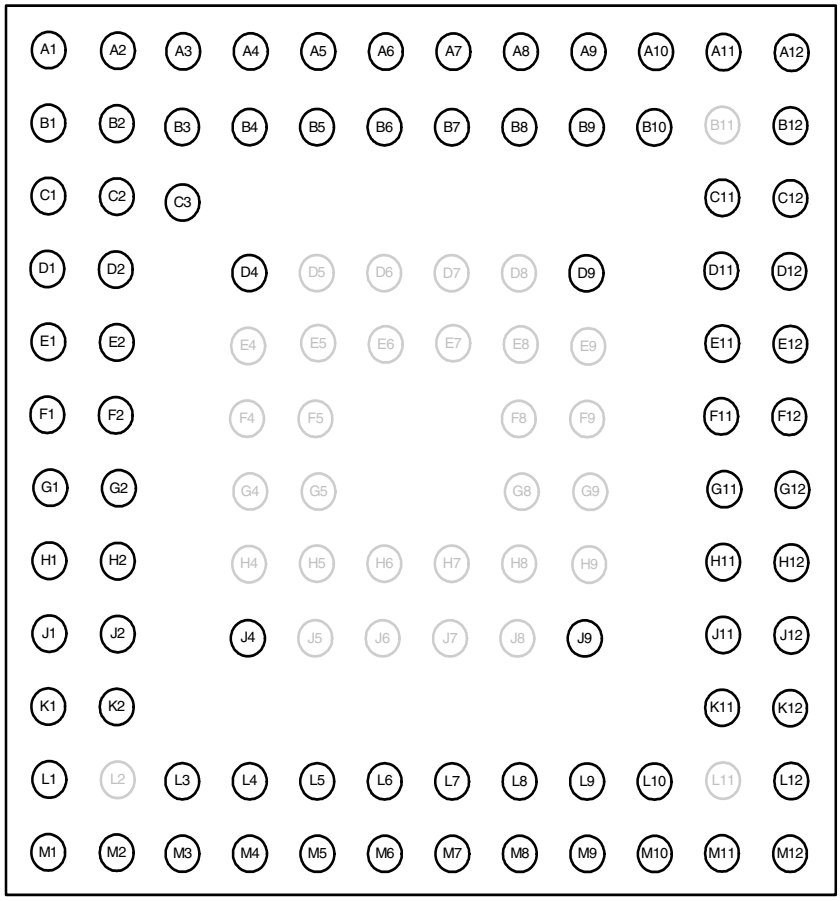
  - MSP−FET430PIF (Parallel Port)
- Debugging and Programming Interface with Target Board
  - MSP−FET430U80
- Production Programmer
  - MSP−GANG430

PRODUCT PREVIEW

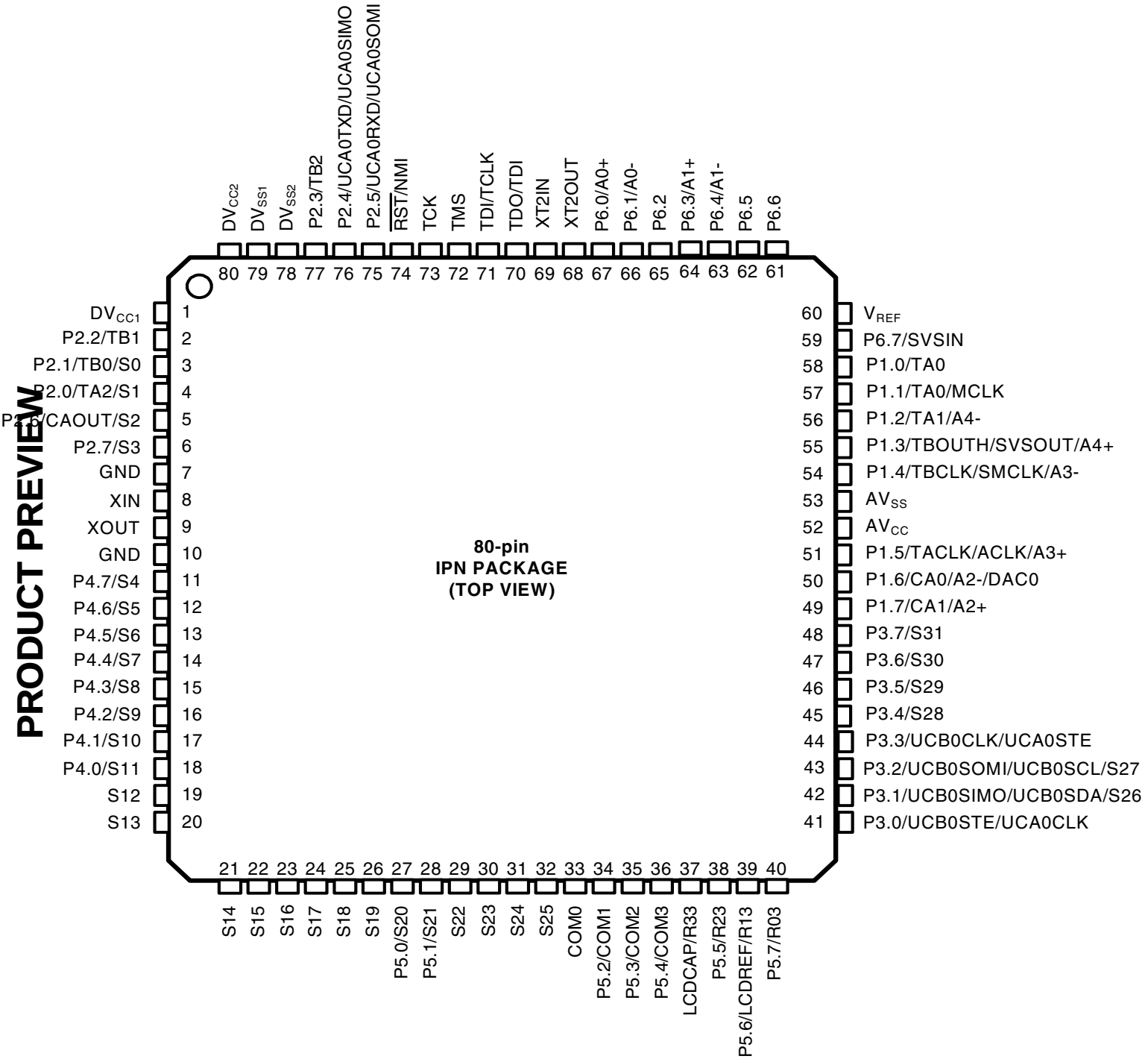
pin designation, MSP430F47xIZQW



Note: For terminal assignments, see the *MSP430x47x Terminal Functions* table.

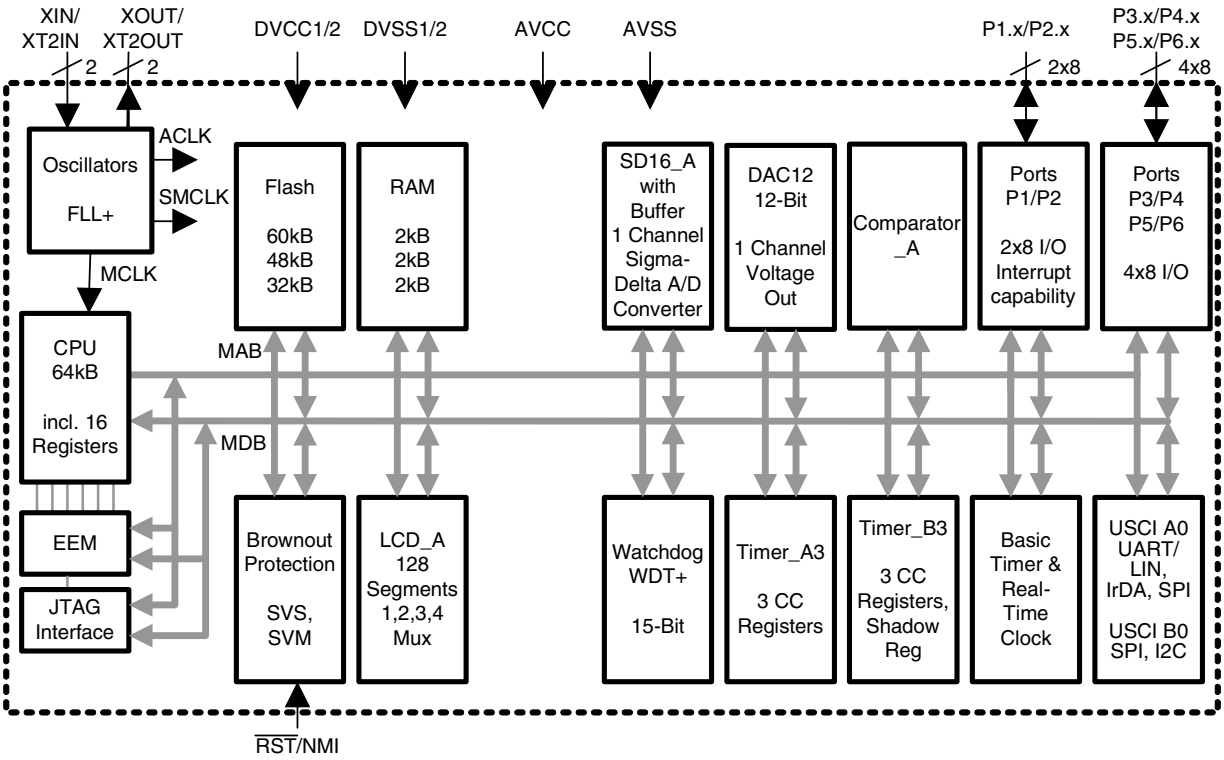
PRODUCT PREVIEW

pin designation, MSP430F47xIPN



PRODUCT PREVIEW

MSP430F47x functional block diagram



PRODUCT PREVIEW

PRODUCT PREVIEW

Terminal Functions

TERMINAL			I/O	DESCRIPTION
NAME	NO.			
	80 PIN	113 PIN		
AV_{CC}	52	F12		Analog supply voltage, positive terminal
AV_{SS}	53	E12		Analog supply voltage, negative terminal
DV_{CC1}	1	A1		Digital supply voltage, positive terminal. Supplies all digital parts.
DV_{SS1}	79	A3		Digital supply voltage, negative terminal. Supplies all digital parts.
DV_{CC2}	80	A2		Digital supply voltage, positive terminal. Supplies all digital parts.
DV_{SS2}	78	B2 B3		Digital supply voltage, negative terminal. Supplies all digital parts.
P1.0/TA0	58	C11	I/O	General-purpose digital I/O pin Timer_A, capture: CCI0A input, compare: Out0 output BSL transmit
P1.1/TA0/MCLK	57	C12	I/O	General-purpose digital I/O pin Timer_A, capture: CCI0B input, compare: Out0 output MCLK signal output BSL receive
P1.2/TA1/A4–	56	D11	I/O	General-purpose digital I/O pin Timer_A, capture: CCI1A input, compare: Out1 output SD16 negative analog input A4
P1.3/TBOUTH/ SVSOUT/A4+)	55	D12	I/O	General-purpose digital I/O pin/Timer_A, capture: CCI2A input, compare: Out2 output switch all PWM digital output ports to high impedance – Timer_B TB0 to TB2 SVS comparator output SD16 positive analog input A4
P1.4/TBCLK/ SMCLK/A3–	54	E11	I/O	General-purpose digital I/O pin/ Timer_B, clock signal TBCLK input SMCLK signal output SD16 negative analog input A3
P1.5/TACLK/ ACLK/A3+	51	F11	I/O	General-purpose digital I/O pin Timer_A, clock signal TACLK input ACLK signal output SD16 positive analog input A3
P1.6/CA0/A2–/ DAC0	50	G12	I/O	General-purpose digital I/O pin Comparator_A input 0 SD16 negative analog input A2 DAC12.0 output
P1.7/CA1/A2+	49	G11	I/O	General-purpose digital I/O pin Comparator_A input 1 SD16 positive analog input A2
P2.0/TA2/S1	4	C2 C3	I/O	General-purpose digital I/O pin Timer_A, capture: CCI2A/B input, compare: Out2 output LCD segment output 1
P2.1/TB0/S0	3	C1	I/O	General-purpose digital I/O pin Timer_B, capture: CCI0A/B input, compare: Out0 output LCD segment output 0

Terminal Functions (continued)

TERMINAL			I/O	DESCRIPTION
NAME	NO.			
	80 PIN	113 PIN		
P2.2/TB1	2	B1	I/O	General-purpose digital I/O pin Timer_B, capture: CCI1A/B input, compare: Out1 output
P2.3/TB2	77	B4	I/O	General-purpose digital I/O pin Timer_B, capture: CCI2A/B input, compare: Out2 output
P2.4/UCA0TXD/ UCA0SIMO	76	A4	I/O	General-purpose digital I/O pin USCIA transmit data output in UART mode, slave data in/master out in SPI mode
P2.5/UCA0RXD/ UCA0SOMI	75	D4	I/O	General-purpose digital I/O pin USCI A0 receive data input in UART mode, slave data out/master in in SPI mode
P2.6/CAOUT/S2	5	D1	I/O	General-purpose digital I/O pin Comparator_A output LCD segment output 2
P2.7/S3	6	D2	I/O	General-purpose digital I/O pin LCD segment output 3
P3.0/UCB0STE/ UCA0CLK	41	M12	I/O	General-purpose digital I/O pin USCI B0 slave transmit enable/USCI A0 clock input/output
P3.1/UCB0SIMO/ UCB0SDA/S26	42	L12	I/O	General-purpose digital I/O pin USCI B0 slave in/master out in SPI mode, SDA I^2C data in I^2C mode LCD segment output 26
P3.2/UCB0SOMI/ UCB0SCL/S27	43	K11	I/O	General-purpose digital I/O pin USCI B0 slave out/master in in SPI mode, SCL I^2C clock in I^2C mode LCD segment output 27
P3.3/UCB0CLK/ UCA0STE	44	K12	I/O	General-purpose digital I/O USCI B0 clock input/output, USCI A0 slave transmit enable
P3.4/S28	45	J11	I/O	General-purpose digital I/O pin LCD segment output 28
P3.5/S29	46	J12	I/O	General-purpose digital I/O pin LCD segment output 29
P3.6/S30	47	H11	I/O	General-purpose digital I/O pin LCD segment output 30
P3.7/S31	48	H12	I/O	General-purpose digital I/O pin LCD segment output 31
P4.0/S11	18	K2	I/O	General-purpose digital I/O pin LCD segment output 11
P4.1/S10	17	K1	I/O	General-purpose digital I/O pin LCD segment output 10
P4.2/S9	16	J2	I/O	General-purpose digital I/O pin LCD segment output 9
P4.3/S8	15	J1	I/O	General-purpose digital I/O pin LCD segment output 8
P4.4/S7	14	H2	I/O	General-purpose digital I/O pin LCD segment output 7
P4.5/S6	13	H1	I/O	General-purpose digital I/O pin LCD segment output 6
P4.6/S5	12	G2	I/O	General-purpose digital I/O pin LCD segment output 5
P4.7/S4	11	G1	I/O	General-purpose digital I/O pin LCD segment output 4

PRODUCT PREVIEW

PRODUCT PREVIEW

Terminal Functions (continued)

TERMINAL			I/O	DESCRIPTION
NAME	NO.			
	80 PIN	113 PIN		
COM0	33	L8	O	Common output, COM0–3 are used for LCD backplanes
P5.0/S20	27	L5	I/O	General-purpose digital I/O pin LCD segment output 20
P5.1/S21	28	M5	I/O	General-purpose digital I/O pin LCD segment output 21
P5.2/COM1	34	M8	I/O	General-purpose digital I/O pin common output, COM0–3 are used for LCD backplanes
P5.3/COM2	35	L9	I/O	General-purpose digital I/O pin common output, COM0–3 are used for LCD backplanes
P5.4/COM3	36	M9	I/O	General-purpose digital I/O pin common output, COM0–3 are used for LCD backplanes
LCDCAP/R33	37	J9	I/O	Capacitor connection for LCD charge pump input port of most positive analog LCD level (V4)
P5.5/R23	38	M10	I/O	General-purpose digital I/O pin input port of the second most positive analog LCD level (V3)
P5.6/LCDREF/ R13	39	L10	I/O	General-purpose digital I/O pin External LCD reference voltage input input port of the third most positive analog LCD level (V3 or V2)
P5.7/R03	40	M11	I/O	General-purpose digital I/O pin input port of the fourth most positive analog LCD level (V1)
P6.0/A0+	67	B8	I/O	General-purpose digital I/O pin SD16 positive analog input A0
P6.1/A0–	66	B9	I/O	General-purpose digital I/O pin SD16 positive negative input A0
P6.2	65	A9	I/O	General-purpose digital I/O pin
P6.3/A1+	64	D9	I/O	General-purpose digital I/O pin SD16 positive analog input A1
P6.4/A1–	63	A10	I/O	General-purpose digital I/O pin SD16 positive negative input A1
P6.5	62	B10	I/O	General-purpose digital I/O pin
P6.6	61	A11	I/O	General-purpose digital I/O pin
P6.7/SVSIN	59	B12	I/O	General-purpose digital I/O pin SVS input
S12	19	L1	O	LCD segment output 12
S13	20	M1	O	LCD segment output 13
S14	21	M2	O	LCD segment output 14
S15	22	M3	O	LCD segment output 15
S16	23	L3	O	LCD segment output 16

Terminal Functions (continued)

TERMINAL			I/O	DESCRIPTION
NAME	NO.			
	80 PIN	113 PIN		
S17	24	L4	O	LCD segment output 17
S18	25	M4	O	LCD segment output 18
S19	26	J4	O	LCD segment output 19
S22	29	L6	O	LCD segment output 22
S23	30	M6	O	LCD segment output 23
S24	31	L7	O	LCD segment output 24
S25	32	M7	O	LCD segment output 25
GND	7	E2		Ground. It is used to shield the oscillator. See Note 1.
XIN	8	E1	I	Input port for crystal oscillator XT1. Standard or watch crystals can be connected.
XOUT	9	F1	O	Output port for crystal oscillator XT1. Standard or watch crystals can be connected.
GND	10	F2		Ground. It is used to shield the oscillator. See Note NO TAG.
V_{REF}	60	A12	O	Input for an external reference voltage/internal reference voltage output
$\overline{RST}$/NMI	74	B5	I	Reset input, nonmaskable interrupt input port, or bootstrap loader start (in flash devices).
TCK	73	A5	I	Test clock (JTAG). TCK is the clock input port for device programming test and bootstrap loader start.
TDI/TCLK	71	A6	I	Test data input or test clock input. The device protection fuse is connected to TDI/TCLK.
TDO/TDI	70	B7	I/O	Test data output port. TDO/TDI data output or programming data input terminal.
TMS	72	B6	I	Test mode select. TMS is used as an input port for device programming and test.
XT2OUT	68	A8	O	Output terminal of crystal oscillator XT2
XT2IN	69	A7	I	Input port for crystal oscillator XT2

NOTE 1: It is recommended to connect GND externally to DVss.

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short-form description

CPU

The MSP430 CPU has a 16−bit RISC architecture that is highly transparent to the application. All operations, other than program-flow instructions, are performed as register operations in conjunction with seven addressing modes for source operand and four addressing modes for destination operand.

The CPU is integrated with 16 registers that provide reduced instruction execution time. The register-to-register operation execution time is one cycle of the CPU clock.

Four of the registers, R0 to R3, are dedicated as program counter, stack pointer, status register, and constant generator, respectively. The remaining registers are general-purpose registers.

Peripherals are connected to the CPU using data, address, and control buses, and can be handled with all instructions.

instruction set

The instruction set consists of 51 instructions with three formats and seven address modes. Each instruction can operate on word and byte data. Table 1 shows examples of the three types of instruction formats, and Table 2 shows the address modes.

Table 1. Instruction Word Formats

Dual operands, source-destination	e.g., ADD R4, R5	R4 + R5 −−−> R5
Single operands, destination only	e.g., CALL R8	PC −−>(TOS), R8−−> PC
Relative jump, un/conditional	e.g., JNE	Jump-on-equal bit = 0

Table 2. Address Mode Descriptions

ADDRESS MODE	S	D	SYNTAX	EXAMPLE	OPERATION
Register	F	F	MOV Rs, Rd	MOV R10, R11	R10 —> R11
Indexed	F	F	MOV X(Rn), Y(Rm)	MOV 2(R5), 6(R6)	M(2+R5)—> M(6+R6)
Symbolic (PC relative)	F	F	MOV EDE, TONI		M(EDE) —> M(TONI)
Absolute	F	F	MOV & MEM, & TCDAT		M(MEM) —> M(TCDAT)
Indirect	F		MOV @Rn, Y(Rm)	MOV @R10, Tab(R6)	M(R10) —> M(Tab+R6)
Indirect autoincrement	F		MOV @Rn+, Rm	MOV @R10+, R11	M(R10) —> R11 R10 + 2—> R10
Immediate	F		MOV #X, TONI	MOV #45, TONI	#45 —> M(TONI)

NOTE: S = source D = destination

operating modes

The MSP430 has one active mode and five software-selectable low-power modes of operation. An interrupt event can wake up the device from any of the five low-power modes, service the request, and restore back to the low-power mode on return from the interrupt program.

The following six operating modes can be configured by software:

- Active mode (AM)
  - All clocks are active
- Low-power mode 0 (LPM0)
  - CPU is disabled
  - ACLK and SMCLK remain active
  - FLL+ loop control remains active
- Low-power mode 1 (LPM1)
  - CPU is disabled
  - ACLK and SMCLK remain active
  - FLL+ loop control is disabled
- Low-power mode 2 (LPM2)
  - CPU is disabled
  - MCLK, FLL+ loop control, and DCOCLK are disabled
  - DCO's dc generator remains enabled
  - ACLK remains active
- Low-power mode 3 (LPM3)
  - CPU is disabled
  - MCLK, FLL+ loop control, and DCOCLK are disabled
  - DCO's dc generator is disabled
  - ACLK remains active
- Low-power mode 4 (LPM4)
  - CPU is disabled
  - ACLK is disabled
  - MCLK, FLL+ loop control, and DCOCLK are disabled
  - DCO's dc generator is disabled
  - Crystal oscillator is stopped

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interrupt vector addresses

The interrupt vectors and the power-up starting address are located in the address range 0xFFFF to 0xFFC0. The vector contains the 16-bit address of the appropriate interrupt-handler instruction sequence.

If the reset vector (located at address 0xFFFE) contains 0xFFFF (e.g., flash is not programmed) the CPU goes into LPM4 immediately after power−up.

INTERRUPT SOURCE	INTERRUPT FLAG	SYSTEM INTERRUPT	WORD ADDRESS	PRIORITY
Power-Up External Reset Watchdog Flash Memory PC Out−of−Range (see Note 4)	PORIFG RSTIFG WDTIFG KEYV (see Note 1)	Reset	0xFFFE	15, highest
NMI Oscillator Fault Flash Memory Access Violation	NMIIFG (see Notes 1 and 3) OFIFG (see Notes 1 and 3) ACCVIFG (see Notes 1, 2 and 4)	(Non)maskable (Non)maskable (Non)maskable	0xFFFC	14
Timer_B3	TBCCR0 CCIFG0 (see Note 2)	Maskable	0xFFFA	13
Timer_B3	TBCCR1 CCIFG1 ... TBCCR3 CCIFG3, TBIFG (see Notes 1 and 2)	Maskable	0xFFF8	12
Comparator_A	CAIFG	Maskable	0xFFF6	11
Watchdog Timer+	WDTIFG	Maskable	0xFFF4	10
USCI_A0/USCI_B0 receive USCI_B0 I2C status	UCA0RXIFG, UCB0RXIFG (see Notes 1 and 5)	Maskable	0xFFF2	9
USCI_A0/USCI_B0 transmit USCI_B0 I2C receive/transmit	UCA0TXIFG, UCB0TXIFG (see Note 1 and 6)	Maskable	0xFFF0	8
SD16_A	SD16CCTLx SD16OVIFG, SD16CCTLx SD16IFG (see Notes 1 and 2)	Maskable	0xFFEE	7
Timer_A3	TACCR0 CCIFG0 (see Note 2)	Maskable	0xFFEC	6
Timer_A3	TACCR1 CCIFG1 and TACCR2 CCIFG2, TAIFG (see Notes 1 and 2)	Maskable	0xFFEA	5
I/O Port P1 (Eight Flags)	P1IFG.0 to P1IFG.7 (see Notes 1 and 2)	Maskable	0xFFE8	4
DAC12	DAC12_0IFG, DAC12_1IFG	Maskable	0xFFE6	3
		Maskable	0xFFE4	2
I/O Port P2 (Eight Flags)	P2IFG.0 to P2IFG.7 (see Notes 1 and 2)	Maskable	0xFFE2	1
Basic Timer1/RTC	BTIFG	Maskable	0xFFE0	0, lowest

NOTES: 1. Multiple source flags
2. Interrupt flags are located in the module.
3. A reset is generated if the CPU tries to fetch instructions from within the module register memory address range (0h to 01FFh). (Non)maskable: the individual interrupt-enable bit can disable an interrupt event, but the general-interrupt enable cannot disable it.
4. Access and key violations, KEYV and ACCVIFG.
5. In SPI mode: UCB0RXIFG. In I2C mode: UCALIFG, UCNACKIFG, ICSTTIFG, UCSTPIFG.
6. In UART/SPI mode: UCB0TXIFG. In I2C mode: UCB0RXIFG, UCB0TXIFG.

special function registers

Most interrupt and module-enable bits are collected in the lowest address space. Special-function register bits not allocated to a functional purpose are not physically present in the device. This arrangement provides simple software access.

interrupt enable 1 and 2

Address	7	6	5	4	3	2	1	0
00h			ACCVIE	NMIIE			OFIE	WDTIE
			rw-0	rw-0			rw-0	rw-0

WDTIE	Watchdog timer interrupt enable. Inactive if watchdog mode is selected. Active if watchdog timer is configured in interval timer mode.
OFIE	Oscillator fault enable
NMIIE	(Non)maskable interrupt enable
ACCVIE	Flash access violation interrupt enable

Address	7	6	5	4	3	2	1	0
01h	BTIE				UCB0TXIE	UCB0RXIE	UCA0TXIE	UCA0RXIE
	rw-0				rw-0	rw-0	rw-0	rw-0

UCA0RXIE	USCI_A0 receive interrupt enable
UCA0TXIE	USCI_A0 transmit interrupt enable
UCB0RXIE	USCI_B0 receive interrupt enable
UCB0TXIE	USCI_B0 transmit interrupt enable
BTIE	Basic timer interrupt enable

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interrupt flag register 1 and 2

Address	7	6	5	4	3	2	1	0
02h				NMIIFG	RSTIFG	PORIFG	OFIFG	WDTIFG
				rw-0	rw-(0)	rw-(1)	rw-1	rw-(0)

WDTIFG Set on watchdog timer overflow (in watchdog mode) or security key violation. Reset on V_{CC} power-up or a reset condition at $\overline{RST}$/NMI pin in reset mode.

OFIFG Flag set on oscillator fault

RSTIFG External reset interrupt flag. Set on a reset condition at $\overline{RST}$/NMI pin in reset mode. Reset on V_{CC} power-up.

PORIFG Power-on interrupt flag. Set on V_{CC} power-up.

NMIIFG Set via $\overline{RST}$/NMI pin.

Address	7	6	5	4	3	2	1	0
03h	BTIFG				UCB0 TXIFG	UCB0 RXIFG	UCA0 TXIFG	UCA0 RXIFG
	rw-0				rw-1	rw-0	rw-1	rw-0

UCA0RXIFG USCI_A0 receive interrupt flag

UCA0TXIFG USCI_A0 transmit interrupt flag

UCB0RXIFG USCI_B0 receive interrupt flag

UCB0TXIFG USCI_B0 transmit interrupt flag

BTIFG Basic Timer1 interrupt flag

Legend		
	rw:	Bit can be read and written.
	rw-0, 1:	Bit can be read and written. It is Reset or Set by PUC.
	rw-(0, 1):	Bit can be read and written. It is Reset or Set by POR.
		SFR bit is not present in device

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memory organization

		MSP430F477	MSP430F478	MSP430F479
Memory Main: interrupt vector Main: code memory	Size Flash Flash	32KB 0FFFFh to 0FFE0h 0FFFFh to 08000h	48KB 0FFFFh to 0FFE0h 0FFFFh to 04000h	60KB 0FFFFh to 0FFE0h 0FFFFh to 01100h
Information memory	Size Flash	256 Byte 010FFh to 01000h	256 Byte 010FFh to 01000h	256 Byte 010FFh to 01000h
Boot memory	Size ROM	1KB 0FFFh to 0C00h	1KB 0FFFh to 0C00h	1KB 0FFFh to 0C00h
RAM	Size	2KB 09FFh to 0200h	2KB 09FFh to 0200h	2KB 09FFh to 0200h
Peripherals	16-bit 8-bit 8-bit SFR	01FFh to 0100h 0FFh to 010h 0Fh to 00h	01FFh to 0100h 0FFh to 010h 0Fh to 00h	01FFh to 0100h 0FFh to 010h 0Fh to 00h

bootstrap loader (BSL)

The MSP430 BSL enables users to program the flash memory or RAM using a UART serial interface. Access to the MSP430 memory via the BSL is protected by user-defined password. For complete description of the features of the BSL and its implementation, see the MSP430 Memory Programming User s Guide, literature number SLAU265.

BSL Function	PN Package Pins	ZQW Package Pins
Data Transmit	58 - P1.0	C11 – P1.0
Data Receive	57 - P1.1	C12 – P1.1

flash memory (Flash)

The flash memory can be programmed via the JTAG port, the bootstrap loader, or in-system by the CPU. The CPU can perform single-byte and single-word writes to the flash memory. Features of the flash memory include:

- Flash memory has n segments of main memory and four segments of information memory (A to D) of 64 bytes each. Each segment in main memory is 512 bytes in size.
- Segments 0 to n may be erased in one step, or each segment may be individually erased.
- Segments A to D can be erased individually, or as a group with segments 0 to n.
  Segments A to D are also called information memory.
- Segment A might contain calibration data. After reset, segment A is protected against programming or erasing. It can be unlocked, but care should be taken not to erase this segment if the calibration data is required.
- Flash content integrity check with marginal read modes.

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watchdog timer (WDT+)

The primary function of the WDT+ module is to perform a controlled system restart after a software problem occurs. If the selected time interval expires, a system reset is generated. If the watchdog function is not needed in an application, the module can be configured as an interval timer and can generate interrupts at selected time intervals.

Basic Timer1 and real-time clock

The Basic Timer1 has two independent 8-bit timers that can be cascaded to form a 16-bit timer/counter. Both timers can be read and written by software. The Basic Timer1 is extended to provide an integrated real-time clock (RTC). An internal calendar compensates for month with less than 31 days and includes leap year correction.

LCD_A driver with regulated charge pump

The LCD_A driver generates the segment and common signals required to drive an LCD display. The LCD_A controller has dedicated data memory to hold segment drive information. Common and segment signals are generated as defined by the mode. Static, 2-MUX, 3-MUX, and 4-MUX LCDs are supported by this peripheral. The module can provide a LCD voltage independent of the supply voltage via an integrated charge pump. Furthermore, it is possible to control the level of the LCD voltage and, thus, contrast in software.

Timer_A3

Timer_A3 is a 16-bit timer/counter with three capture/compare registers. Timer_A3 can support multiple capture/compares, PWM outputs, and interval timing. Timer_A3 also has extensive interrupt capabilities. Interrupts may be generated from the counter on overflow conditions and from each of the capture/compare registers.

TIMER_A3 SIGNAL CONNECTIONS

INPUT PIN NUMBER		DEVICE INPUT SIGNAL	MODULE INPUT NAME	MODULE BLOCK	MODULE OUTPUT SIGNAL	OUTPUT PIN NUMBER	
PN	ZQW					PN	ZQW
P1.5 – 51	F11	TACLK	TACLK	Timer	NA		
		ACLK	ACLK				
		SMCLK	SMCLK				
P1.5 – 51	F11	TAINCLK	INCLK				
P1.0 – 58	C11	TA0	CCI0A	CCR0	TA0	P1.0 – 58	C11
P1.1 – 57	C12	TA0	CCI0B			P1.1 – 57	C12
		DV_{SS}	GND				
		DV_{CC}	V_{CC}				
P1.2 – 56	D11	TA1	CCI1A	CCR1	TA1	P1.2 – 56	D11
		CAOUT (internal)	CCI1B				
		DV_{SS}	GND				
		DV_{CC}	V_{CC}				
P2.0 – 4	C2	TA2	CCI2A	CCR2	TA2	P2.0 – 4	C2
		ACLK (internal)	CCI2B				
		DV_{SS}	GND				
		DV_{CC}	V_{CC}				

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Timer_B3

Timer_B3 is a 16-bit timer/counter with three capture/compare registers. Timer_B3 can support multiple capture/compares, PWM outputs, and interval timing. Timer_B3 also has extensive interrupt capabilities. Interrupts may be generated from the counter on overflow conditions and from each of the capture/compare registers.

TIMER_B3 SIGNAL CONNECTIONS							
INPUT PIN NUMBER		DEVICE INPUT SIGNAL	MODULE INPUT NAME	MODULE BLOCK	MODULE OUTPUT SIGNAL	OUTPUT PIN NUMBER	
PN	ZQW					PN	ZQW
P1.4 – 54	E11	TBCLK	TBCLK	Timer	NA		
		ACLK	ACLK				
		SMCLK	SMCLK				
P1.4 – 54	E11	$\overline{\text{TBCLK}}$ (See Note 1)	INCLK				
P2.1 – 3	C1	TB0	CCI0A	CCR0	TB0	P2.1 – 3	C1
P2.1 – 3	C1	TB0	CCI0B				
		V_{SS}	GND				
		V_{CC}	V_{CC}				
P2.2 – 2	B1	TB1	CCI1A	CCR1	TB1	P2.2 – 2	B1
P2.2 – 2	B1	TB1	CCI1B				
		V_{SS}	GND				
		V_{CC}	V_{CC}				
P2.3 – 77	B4	TB2	CCI2A	CCR2	TB2	P2.3 – 77	B4
		ACLK (internal)	CCI2B				
		V_{SS}	GND				
		V_{CC}	V_{CC}				

NOTE 1: The inversion of TBCLK is done inside the module.

universal serial communication interfaces (USCIs) (USCI_A0, USCI_B0)

The USCI module is used for serial data communication. The USCI module supports synchronous communication protocols such as SPI (3 pin or 4 pin), I2C, and asynchronous communication protocols such as UART, enhanced UART with automatic baudrate detection (LIN), and IrDA.

USCI_A0 provides support for SPI (3 pin or 4 pin), UART, enhanced UART and IrDA.

USCI_B0 provides support for SPI (3 pin or 4 pin) and I2C.

Comparator_A

The primary function of the Comparator_A module is to support precision slope analog-to-digital conversions, battery-voltage supervision, and monitoring of external analog signals.

SD16_A

The SD16_A module supports 16-bit analog-to-digital conversions. The module implements a 16-bit sigma-delta core and a reference generator. In addition to external analog inputs, an internal V_{CC} sense and temperature sensor are also available.

DAC12

The DAC12 module is a 12-bit, R-ladder, voltage-output digital-to-analog converter (DAC). The DAC12 may be used in 8-bit or 12-bit mode.

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peripheral file map

PERIPHERALS WITH WORD ACCESS			
Watchdog	Watchdog timer control	WDTCTL	0120h
Timer_B3	Capture/compare register 2	TBCCR2	0196h
	Capture/compare register 1	TBCCR1	0194h
	Capture/compare register 0	TBCCR0	0192h
	Timer_B register	TBR	0190h
	Capture/compare control 2	TBCCTL2	0186h
	Capture/compare control 1	TBCCTL1	0184h
	Capture/compare control 0	TBCCTL0	0182h
	Timer_B control	TBCTL	0180h
	Timer_B interrupt vector	TBIV	011Eh
Timer_A3	Capture/compare register 2	TACCR2	0176h
	Capture/compare register 1	TACCR1	0174h
	Capture/compare register 0	TACCR0	0172h
	Timer_A register	TAR	0170h
	Capture/compare control 2	TACCTL2	0166h
	Capture/compare control 1	TACCTL1	0164h
	Capture/compare control 0	TACCTL0	0162h
	Timer_A control	TACTL	0160h
	Timer_A interrupt vector	TAIV	012Eh
Flash	Flash control 4	FCTL4	01BEh
	Flash control 3	FCTL3	012Ch
	Flash control 2	FCTL2	012Ah
	Flash control 1	FCTL1	0128h
DAC12	DAC12_0 data	DAC12_0DAT	01C8h
	DAC12_0 control	DAC12_0CTL	01C0h
SD16_A (see also: Peripherals with Byte Access)	General control	SD16CTL	0100h
	Channel 0 control	SD16CCTL0	0102h
	Channel 0 conversion memory	SD16MEM0	0112h
	Interrupt vector word register	SD16IV	0110h
PERIPHERALS WITH BYTE ACCESS			
SD16_A (see also: Peripherals with Word Access)	Channel 0 input control	SD16INCTL0	0B0h
	Analog enable	SD16AE	0B7h

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peripheral file map (continued)

LCD_A	LCD voltage control 1	LCDAVCTL1	0AFh
	LCD voltage control 0	LCDAVCTL0	0AEh
	LCD voltage port control 1	LCDAPCTL1	0ADh
	LCD voltage port control 0	LCDAPCTL0	0ACh
	LCD memory 20	LCDM20	0A4h
	:	:	:
	LCD memory 16	LCDM16	0A0h
	LCD memory 15	LCDM15	09Fh
	:	:	:
	LCD memory 1	LCDM1	091h
	LCD control and mode	LCDACTL	090h
USCI A0/B0	USCI A0 auto-baudrate control	UCA0ABCTL	0x005D
	USCI A0 transmit buffer	UCA0TXBUF	0x0067
	USCI A0 receive buffer	UCA0RXBUF	0x0066
	USCI A0 status	UCA0STAT	0x0065
	USCI A0 modulation control	UCA0MCTL	0x0064
	USCI A0 baud rate control 1	UCA0BR1	0x0063
	USCI A0 baud rate control 0	UCA0BR0	0x0062
	USCI A0 control 1	UCA0CTL1	0x0061
	USCI A0 control 0	UCA0CTL0	0x0060
	USCI A0 IrDA receive control	UCA0IRRCTL	0x005F
	USCI A0 IrDA transmit control	UCA0IRTCTL	0x005E
	USCI B0 transmit buffer	UCB0TXBUF	0x006F
	USCI B0 receive buffer	UCB0RXBUF	0x006E
	USCI B0 status	UCB0STAT	0x006D
	USCI B0 I2C interrupt enable	UCB0CIE	0x006C
	USCI B0 baud rate control 1	UCB0BR1	0x006B
	USCI B0 baud rate control 0	UCB0BR0	0x006A
	USCI B0 control 1	UCB0CTL1	0x0069
	USCI B0 control 0	UCB0CTL0	0x0068
	USCI B0 I2C slave address	UCB0SA	0x011A
	USCI B0 I2C own address	UCB0OA	0x0118
Comparator_A	Comparator_A port disable	CAPD	05Bh
	Comparator_A control2	CACTL2	05Ah
	Comparator_A control1	CACTL1	059h
Brownout, SVS	SVS control register (reset by brownout signal)	SVSCTL	056h
FLL+ Clock	FLL+ control 1	FLL_CTL1	054h
	FLL+ control 0	FLL_CTL0	053h
	System clock frequency control	SCFQCTL	052h
	System clock frequency integrator	SCFI1	051h
	System clock frequency integrator	SCFI0	050h

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peripheral file map (continued)

PERIPHERALS WITH BYTE ACCESS			
RTC (Basic Timer1)	Real-time clock year high byte	RTCYEARH	04Fh
	Real-time clock year low byte	RTCYEARL	04Eh
	Real-time clock month	RTCMON	04Dh
	Real-time clock day of month	RTCDAY	04Ch
	Basic Timer1 counter	BTCNT2	047h
	Basic Timer1 counter	BTCNT1	046h
	Real-time counter 4	RTCNT4	045h
	(Real-time clock day of week)	(RTCDOW)	
	Real-time counter 3	RTCNT3	044h
	(Real-time clock hour)	(RTCHOUR)	
	Real-time counter 2	RTCNT2	043h
	(Real-time clock minute)	(RTCMIN)	
	Real-time counter 1	RTCNT1	042h
	(Real-time clock second)	(RTCSEC)	
	Real-time clock control	RTCCTL	041h
	Basic Timer1 control	BTCTL	040h
Port P6	Port P6 selection	P6SEL	037h
	Port P6 direction	P6DIR	036h
	Port P6 output	P6OUT	035h
	Port P6 input	P6IN	034h
Port P5	Port P5 selection	P5SEL	033h
	Port P5 direction	P5DIR	032h
	Port P5 output	P5OUT	031h
	Port P5 input	P5IN	030h
Port P4	Port P4 selection	P4SEL	01Fh
	Port P4 direction	P4DIR	01Eh
	Port P4 output	P4OUT	01Dh
	Port P4 input	P4IN	01Ch
Port P3	Port P3 selection	P3SEL	01Bh
	Port P3 direction	P3DIR	01Ah
	Port P3 output	P3OUT	019h
	Port P3 input	P3IN	018h
Port P2	Port P2 selection	P2SEL	02Eh
	Port P2 interrupt enable	P2IE	02Dh
	Port P2 interrupt-edge select	P2IES	02Ch
	Port P2 interrupt flag	P2IFG	02Bh
	Port P2 direction	P2DIR	02Ah
	Port P2 output	P2OUT	029h
	Port P2 input	P2IN	028h

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peripheral file map (continued)

PERIPHERALS WITH BYTE ACCESS (CONTINUED)			
Port P1	Port P1 selection 2 register	P1SEL2	057h
	Port P1 selection	P1SEL	026h
	Port P1 interrupt enable	P1IE	025h
	Port P1 interrupt-edge select	P1IES	024h
	Port P1 interrupt flag	P1IFG	023h
	Port P1 direction	P1DIR	022h
	Port P1 output	P1OUT	021h
	Port P1 input	P1IN	020h
Special functions	SFR interrupt flag 2	IFG2	003h
	SFR interrupt flag 1	IFG1	002h
	SFR interrupt enable 2	IE2	001h
	SFR interrupt enable 1	IE1	000h

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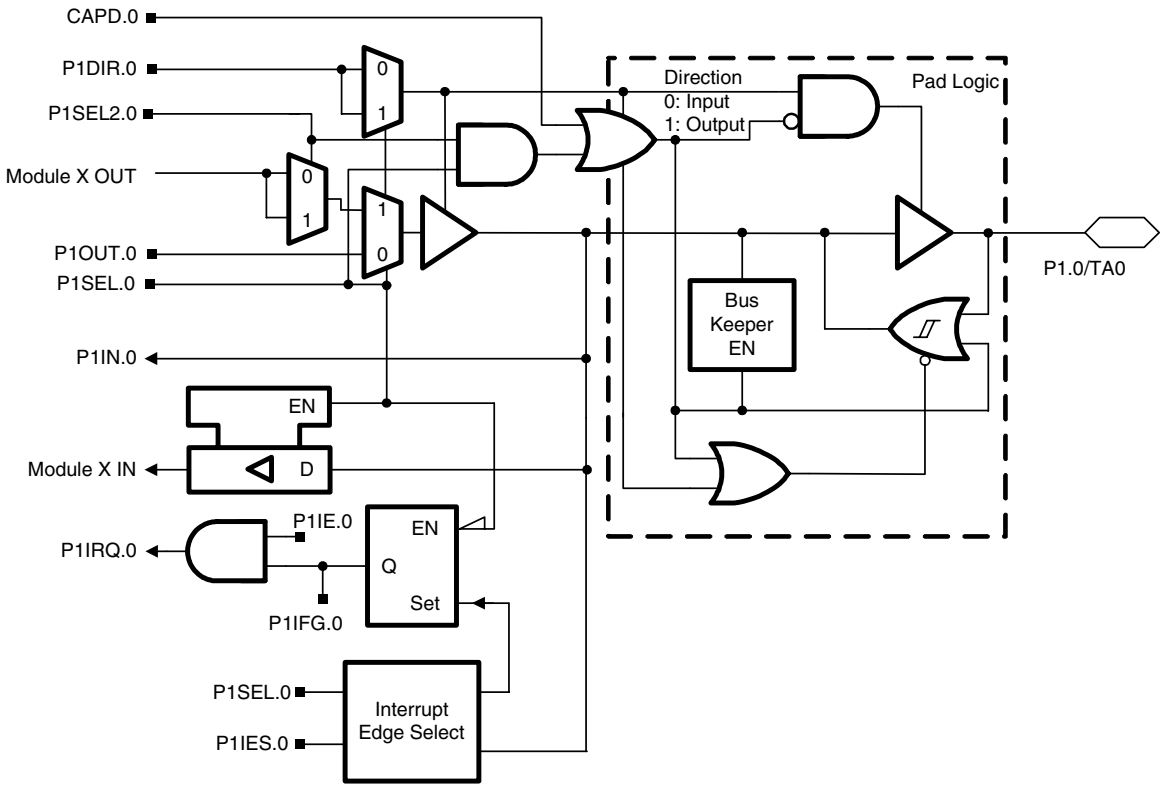
APPLICATION INFORMATION

Port P1 pin schematic: P1.0, input/output with Schmitt trigger

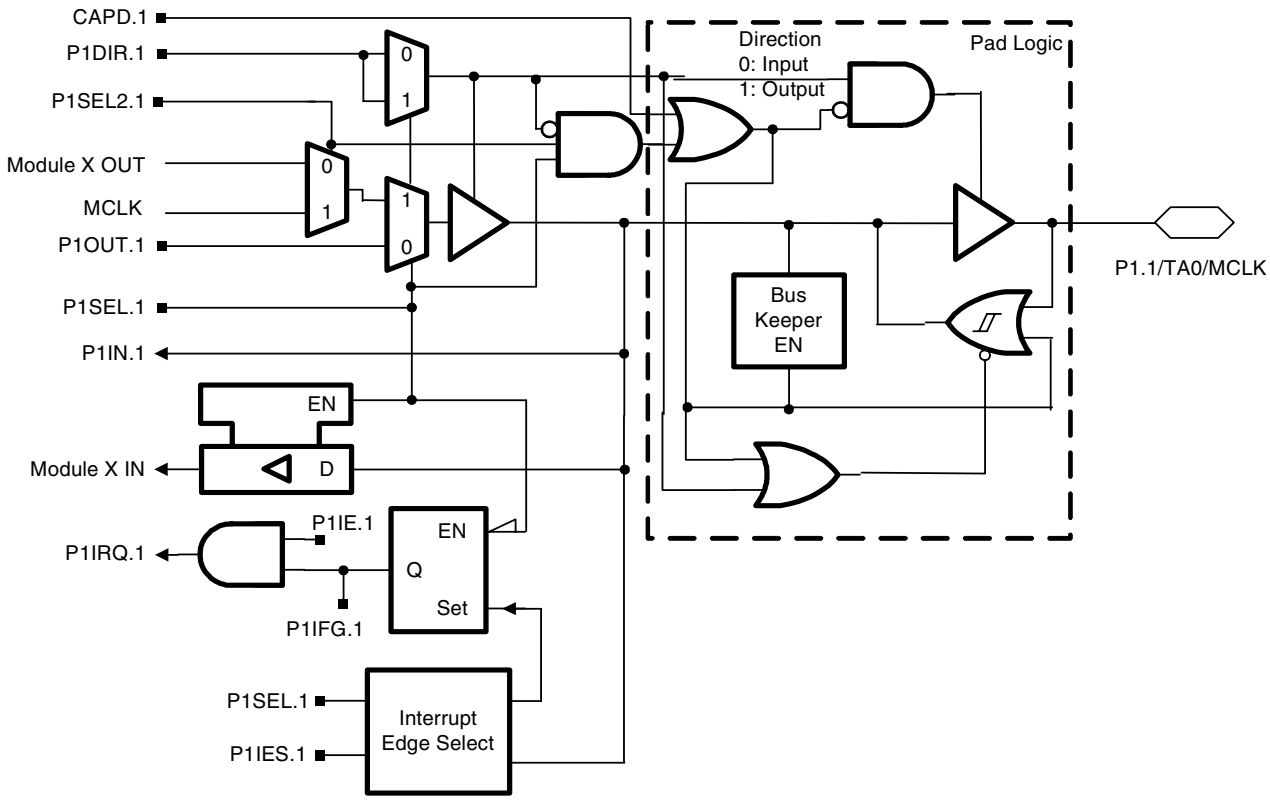


Port P1 (P1.0) pin functions

PIN NAME (P1.X)	X	FUNCTION	CONTROL BITS / SIGNALS			
			CAPD.x	P1DIR.x	P1SEL.x	P1SEL2.x
P1.0/TA0	0	P1.x (I/O)	0	I: 0; O: 1	0	0
		Timer_A3.CCI0A	0	0	1	0
		Timer_A3.TA0	0	1	1	0

APPLICATION INFORMATION

Port P1 pin schematic: P1.1, input/output with Schmitt trigger



Port P1 (P1.1) pin functions

PIN NAME (P1.X)	X	FUNCTION	CONTROL BITS / SIGNALS			
			CAPD.x	P1DIR.x	P1SEL.x	P1SEL2.x
P1.1/TA0/MCLK	1	P1.x (I/O)	0	I: 0; O: 1	0	0
		Timer_A3.CCI0A	0	0	1	0
		Timer_A3.TA0	0	1	1	0
		MCLK	0	1	1	1

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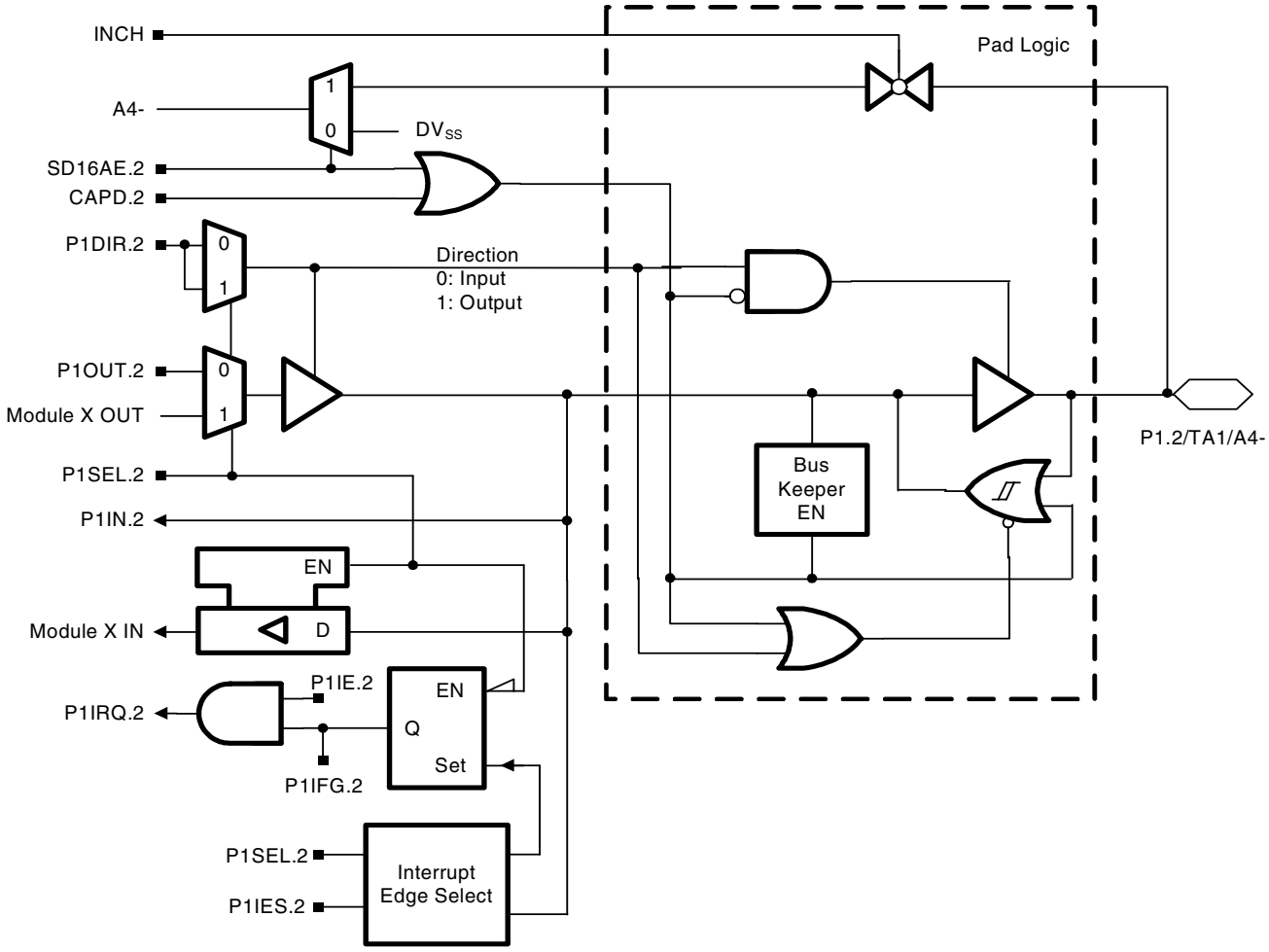
APPLICATION INFORMATION

Port P1 pin schematic: P1.2 input/output with Schmitt trigger



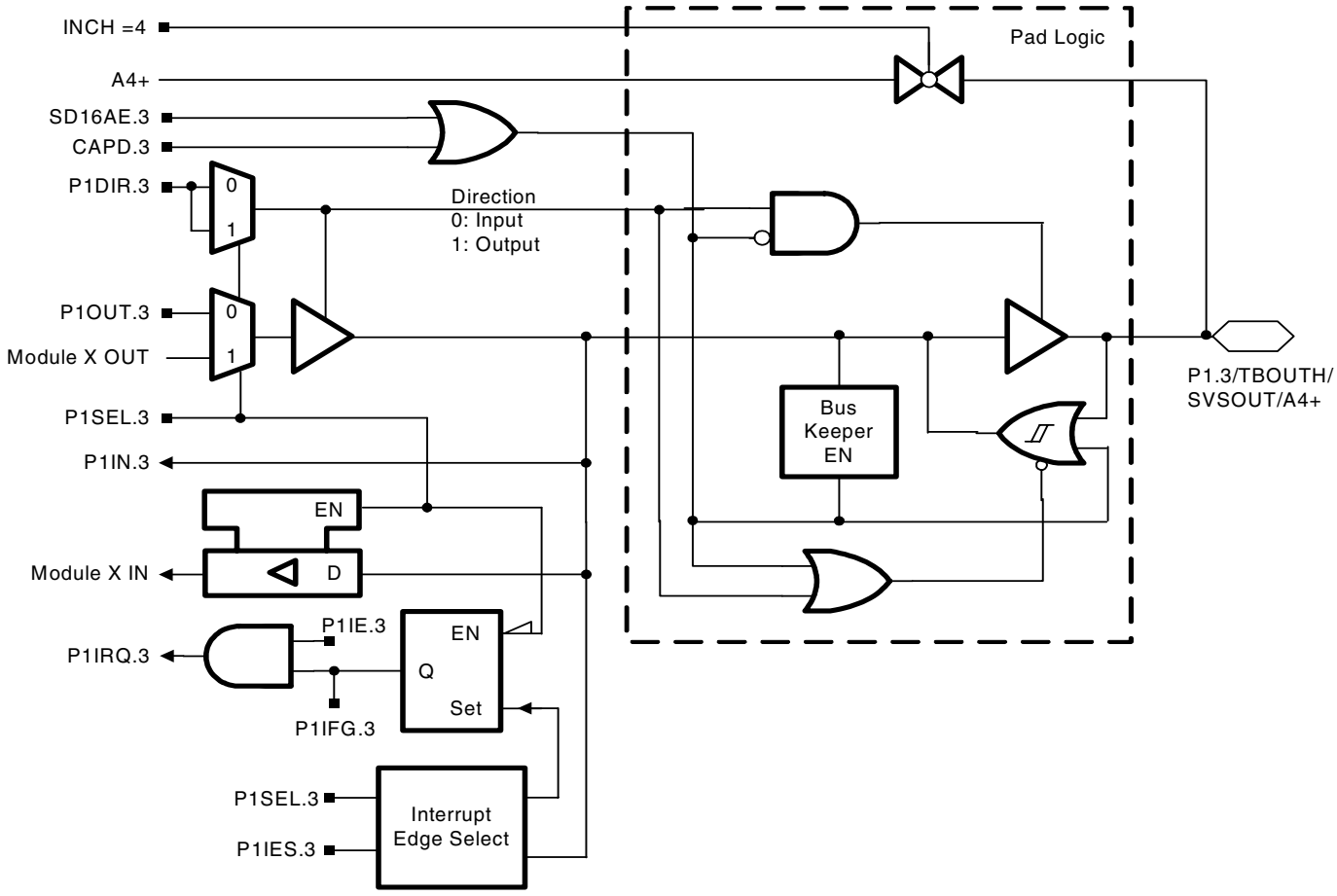
Port P1 (P1.2) pin functions

PIN NAME (P1.X)	X	FUNCTION	CONTROL BITS / SIGNALS			
			CAPD.x	P1DIR.x	P1SEL.x	P1SEL2.x = 0 SD16AE.x
P1.2/TA1/A4–	2	P1.x (I/O)	0	I: 0; O: 1	0	0
		Timer_A3.CCI1A	0	0	1	0
		Timer_A3.TA1	0	1	1	0
		A4–	x	x	x	1

NOTES: 1. x: Don't care

APPLICATION INFORMATION

Port P1 pin schematic: P1.3, input/output with Schmitt trigger



Port P1 (P1.3) pin functions

PIN NAME (P1.X)	X	FUNCTION	CONTROL BITS / SIGNALS			
			CAPD.x	P1DIR.x	P1SEL.x	P1SEL2.x = 0 SD16AE.x
P1.3/TBOUTH/ SVSOUT/A4+	3	P1.x (I/O)	0	I: 0; O: 1	0	0
		TBOUTH	0	0	1	0
		SVSOUT	0	1	1	0
		A4+	x	x	x	1

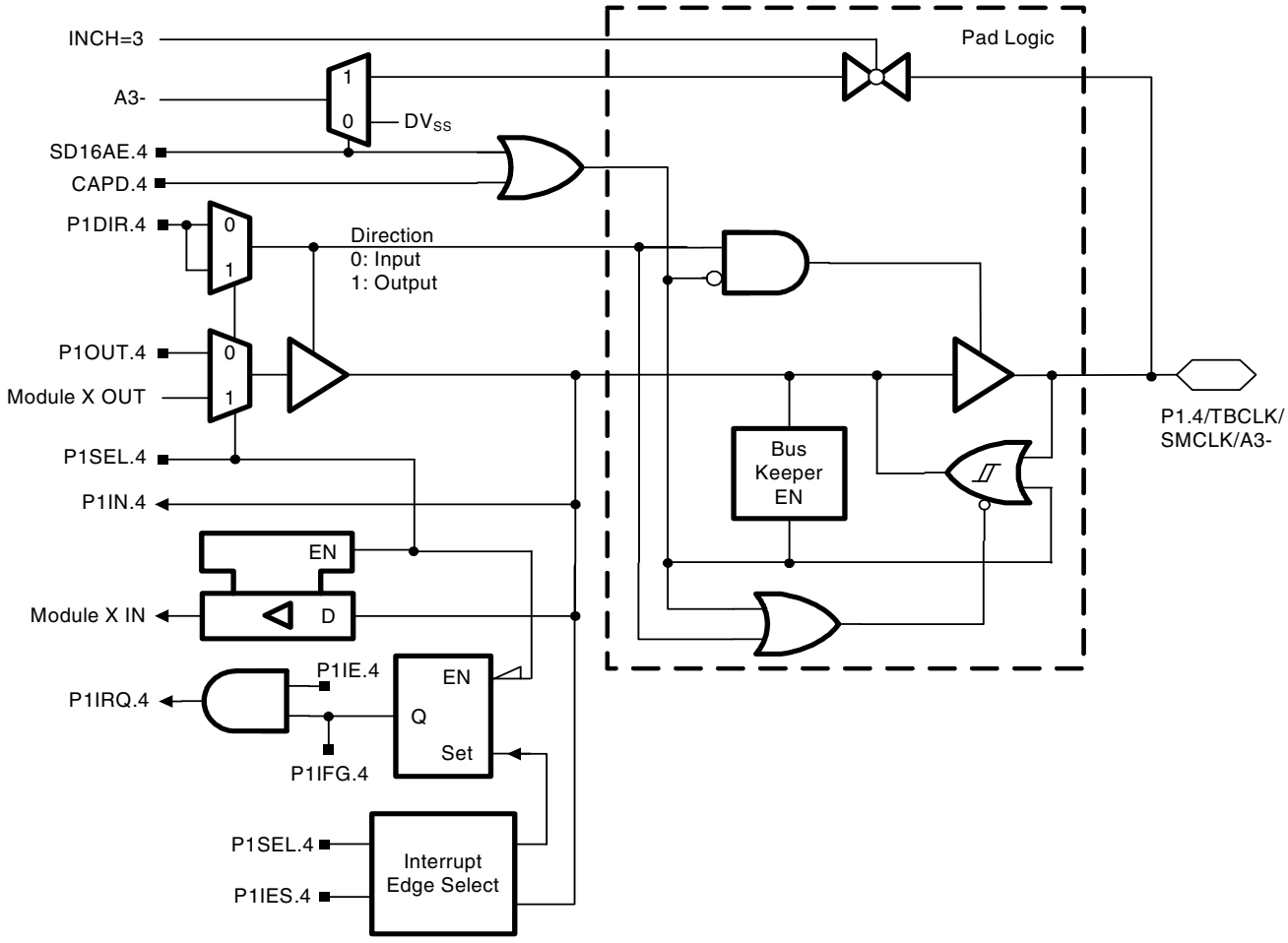
NOTES: 1. x: Don't care

PRODUCT PREVIEW

PRODUCT PREVIEW

APPLICATION INFORMATION

Port P1 pin schematic: P1.4, input/output with Schmitt trigger



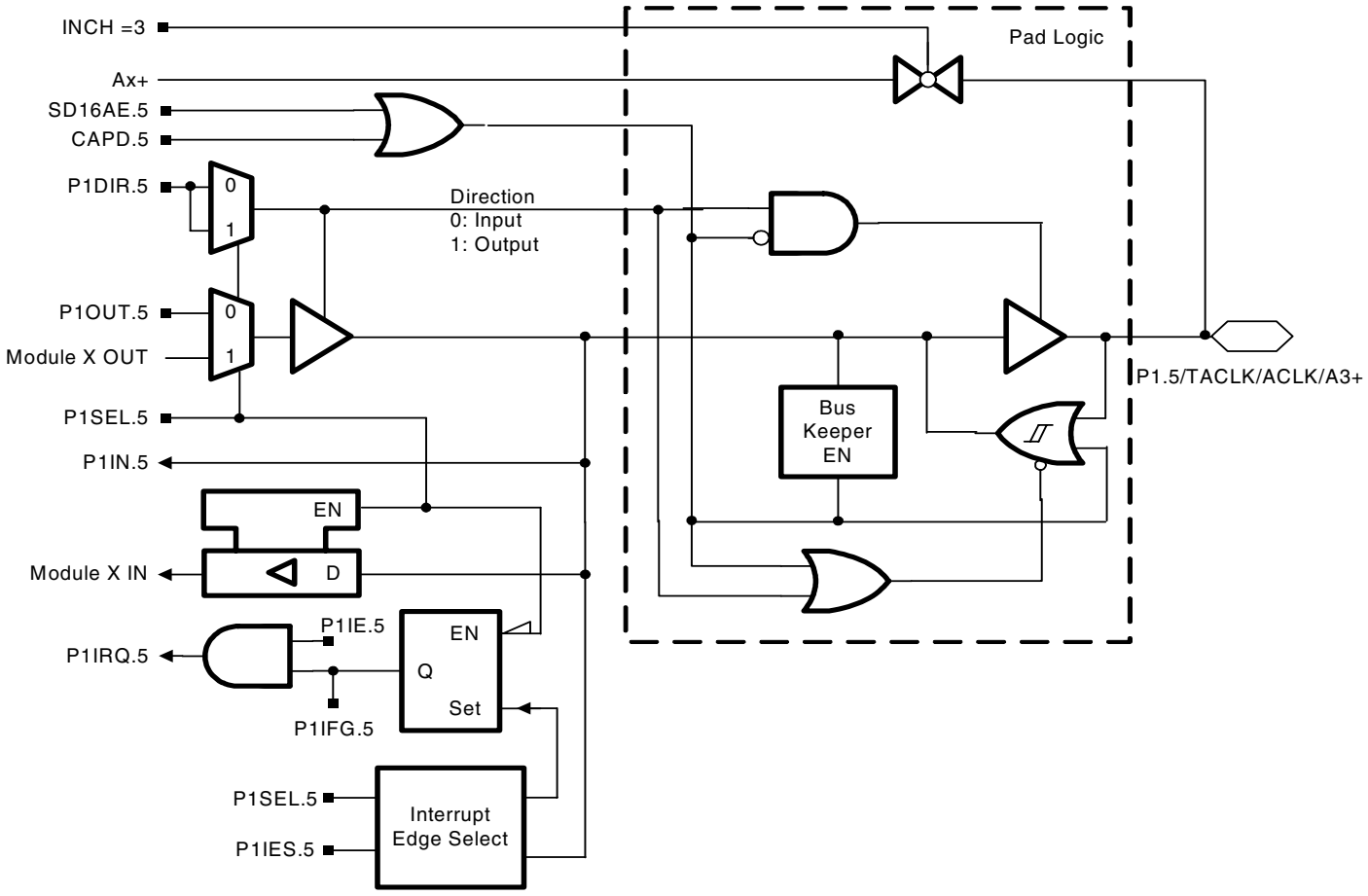
Port P1 (P1.4) pin functions

PIN NAME (P1.X)	X	FUNCTION	CONTROL BITS / SIGNALS			
			CAPD.x	P1DIR.x	P1SEL.x	P1SEL2.x = 0 SD16AE.x
P1.4TBCLK/SMCLK/ A3–	4	P1.x (I/O)		I: 0; O: 1	0	0
		TBCLK		0	1	0
		SMCLK		1	1	0
		A3–		x	x	1

NOTES: 1. x: Don't care

APPLICATION INFORMATION

Port P1 pin schematic: P1.5, input/output with Schmitt trigger



Port P1 (P1.5) pin functions

PIN NAME (P1.X)	X	FUNCTION	CONTROL BITS / SIGNALS			
			CAPD.x	P1DIR.x	P1SEL.x	P1SEL2.x = 0 SD16AE.x
P1.5/TACLK/ACLK/ A3+	5	P1.x (I/O)	0	I: 0; O: 1	0	0
		TACLK	0	0	1	0
		ACLK	0	1	1	0
		A3+	x	x	x	1

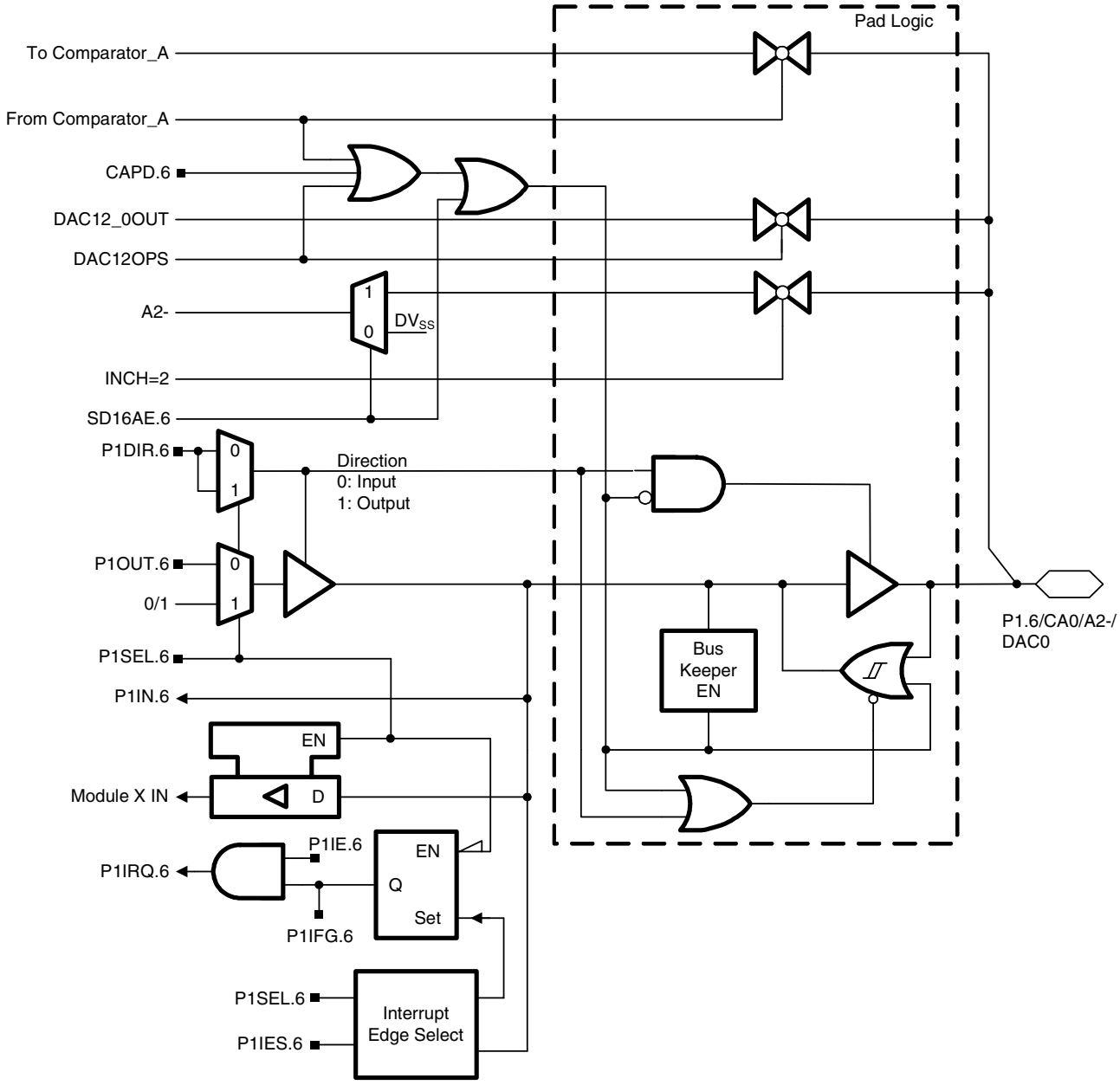
NOTES: 1. x: Don't care

PRODUCT PREVIEW

PRODUCT PREVIEW

APPLICATION INFORMATION

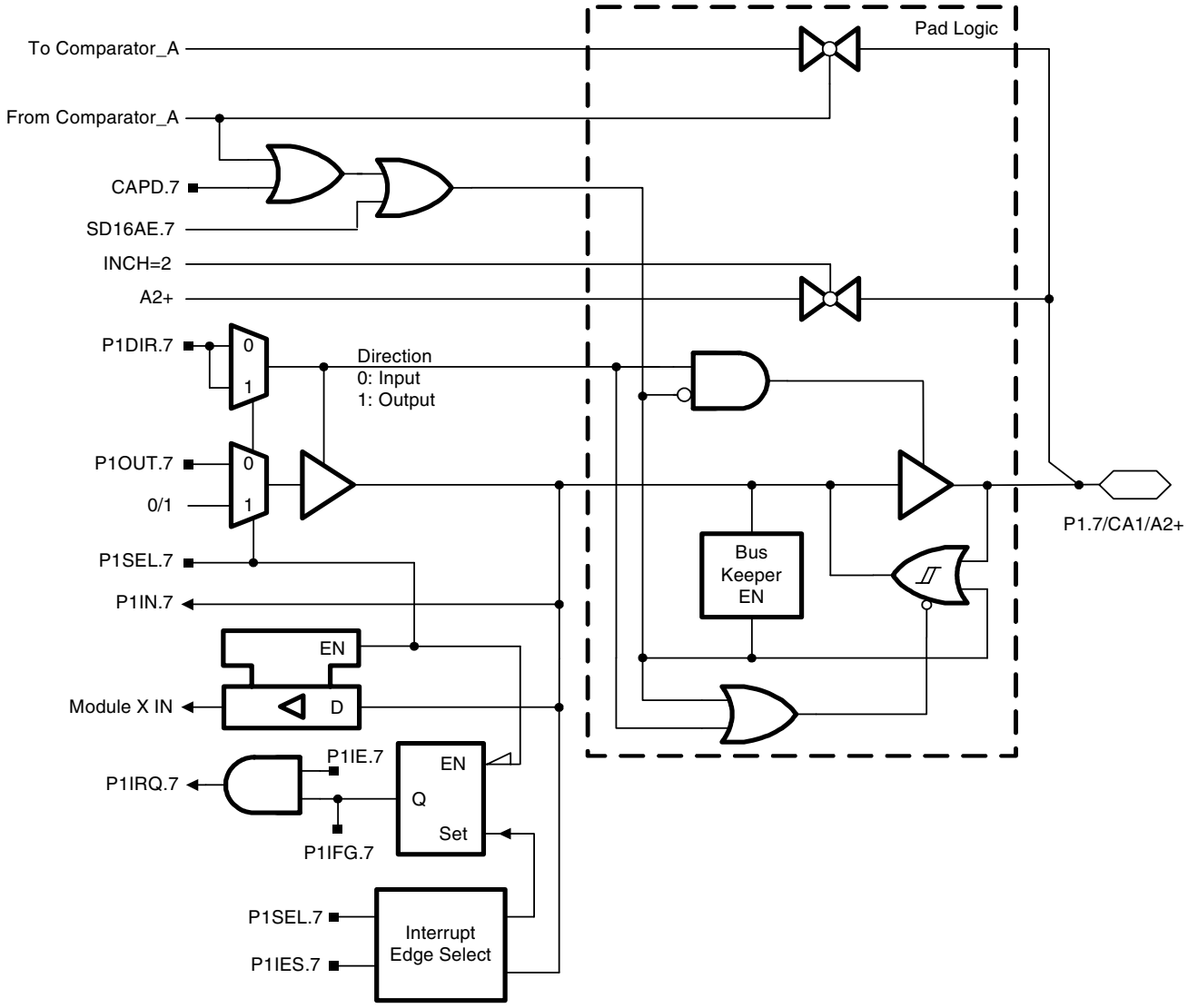
Port P1 pin schematic: P1.6, input/output with Schmitt trigger



PRODUCT PREVIEW

APPLICATION INFORMATION

Port P1 pin schematic: P1.7, input/output with Schmitt trigger



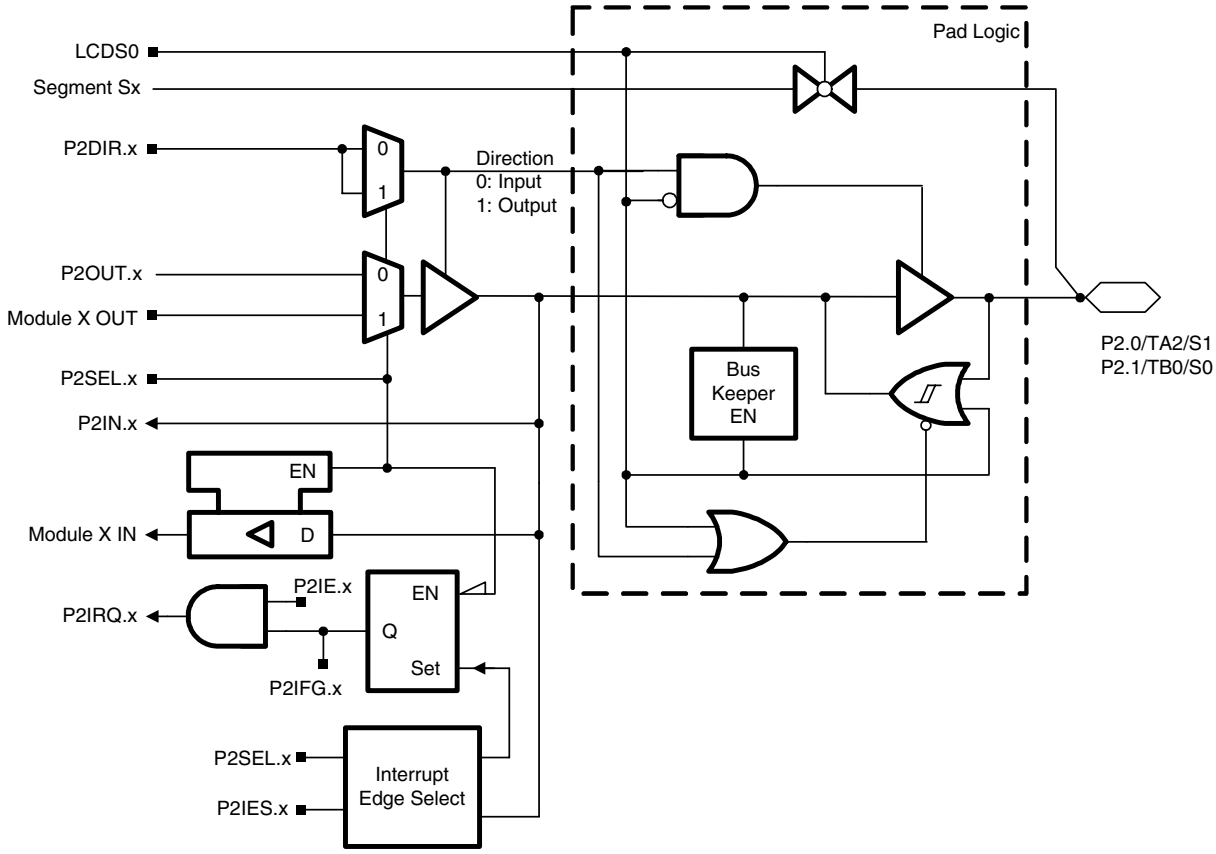
Port P1 (P1.7) pin functions

PIN NAME (P1.X)	X	FUNCTION	CONTROL BITS / SIGNALS			
			P1DIR.x	P1SEL.x	P1SEL2.x = 0 CAPD.x	P1SEL2.x = 0 SD16AE.x
P1.7/CA1/A2+	7	P1.x (I/O)	I: 0; O: 1	0	0	0
		CA1	x	x	1 or selected	x
		A2+	x	x	x	1

NOTES: 1. x: Don't care

APPLICATION INFORMATION

Port P2 pin schematic: P2.0 to P2.1, input/output with Schmitt trigger



Port P2 (P2.0 to P2.1) pin functions

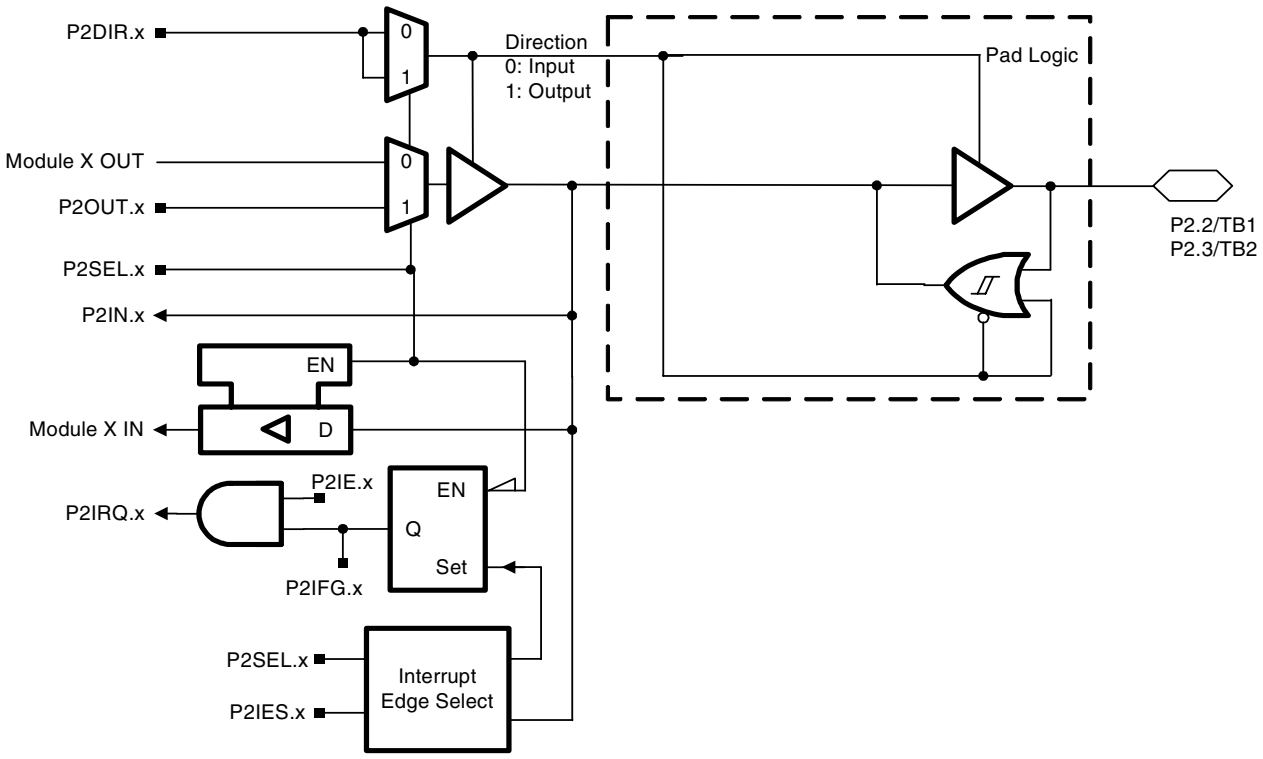
PIN NAME (P2.X)	X	FUNCTION	CONTROL BITS / SIGNALS		
			P2DIR.x	P2SEL.x	LCDS0
P2.0/TA2/S1	0	P2.x (I/O)	I: 0; O: 1	0	0
		Timer_A3.CCI2A	0	1	0
		Timer_A3.TA2	1	1	0
		S1	x	x	1
P2.1/TB0/S0	1	P2.x (I/O)	I: 0; O: 1	0	0
		Timer_B3.CCI0A	0	1	0
		Timer_B3.TB0	1	1	0
		S0	x	x	1

NOTES: 1. x: Don't care

PRODUCT PREVIEW

APPLICATION INFORMATION

Port P2 pin schematic: P2.2 to P2.3, input/output with Schmitt trigger



Port P2 (P2.2 to P2.3) pin functions

PIN NAME (P2.X)	X	FUNCTION	CONTROL BITS / SIGNALS	
			P2DIR.x	P2SEL.x
P2.2/TB1	2	P2.x (I/O)	I: 0; O: 1	0
		Timer_B3.CCI1A	0	1
		Timer_B3.TB1	1	1
P2.3/TB2	3	P2.x (I/O)	I: 0; O: 1	0
		Timer_B3.CCI2A	0	1
		Timer_B3.TB2	1	1

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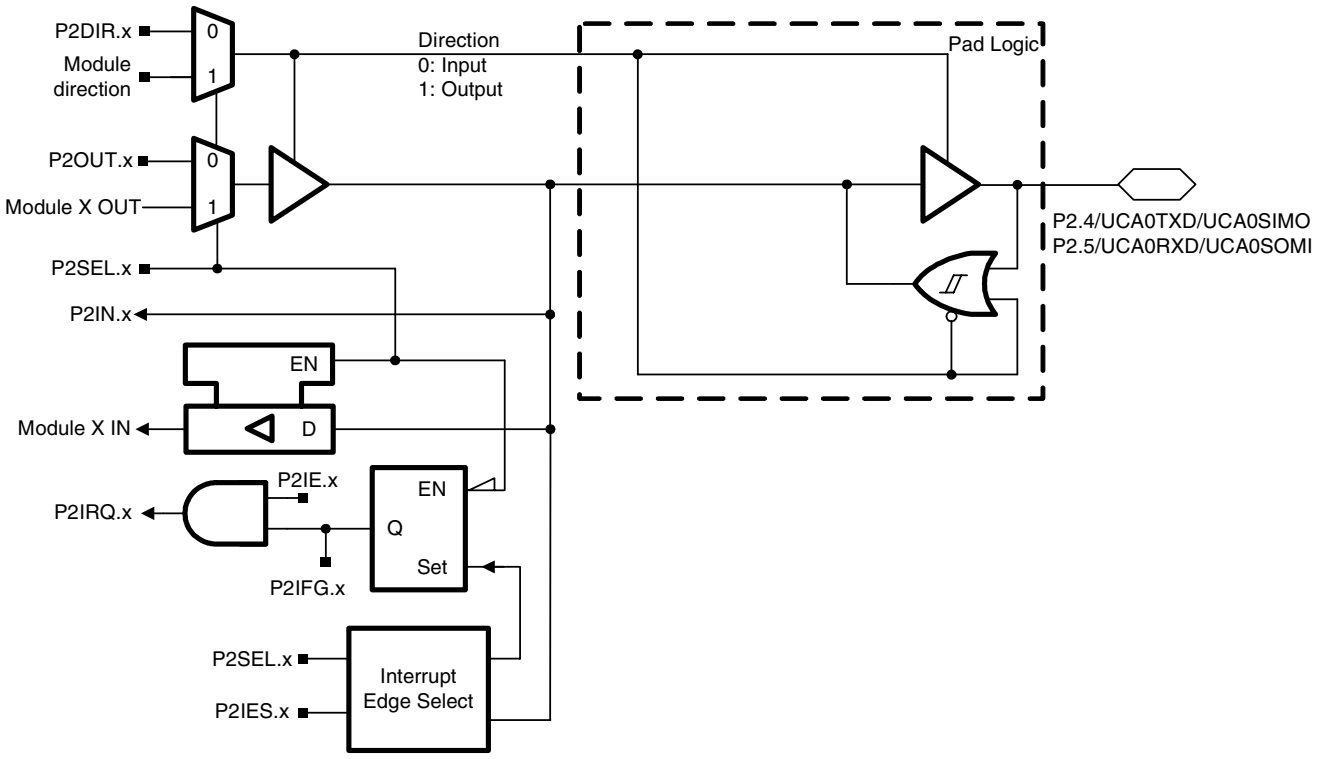
APPLICATION INFORMATION

Port P2 pin schematic: P2.4 and P2.5, input/output with Schmitt trigger



Port P2 (P2.4 and P2.5) pin functions

PIN NAME (P2.X)	X	FUNCTION	CONTROL BITS / SIGNALS	
			P2DIR.x	P2SEL.x
P2.4/UCA0TXD/ UCA0SIMO	4	P2.x (I/O)	I: 0; O: 1	0
		UCA0TXD/UCA0SIMO (see Notes 2)	x	1
P2.5/UCA0RXD/ UCA0SOMI	5	P2.x (I/O)	I: 0; O: 1	0
		UCA0RXD/UCA0SOMI (see Notes 2)	x	1

NOTES: 1. x: Don't care
2. The pin direction is controlled by the USCI module.

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