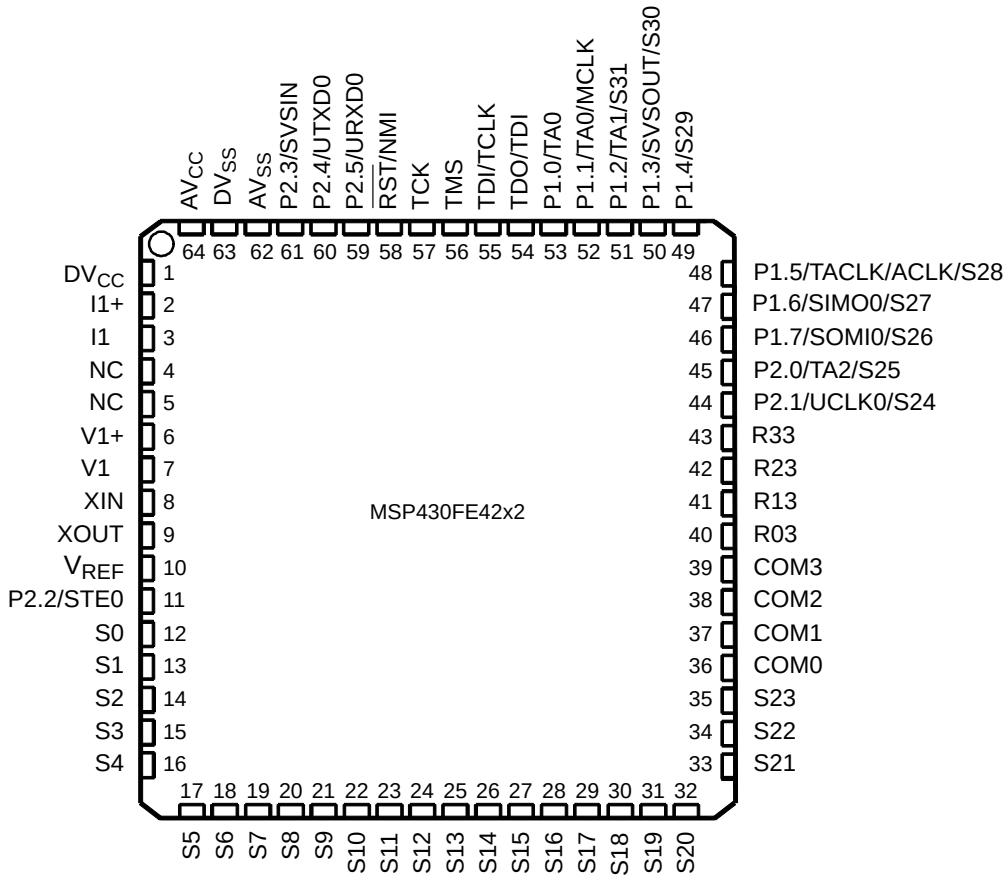
AVAILABLE OPTIONS

T_A	PACKAGED DEVICES
	PLASTIC 64-PIN QFP (PM)
40 °C to 85°C	MSP430FE4232IPM MSP430FE4242IPM MSP430FE4252IPM MSP430FE4272IPM

pin designation



peripheral file map (continued)

PERIPHERALS WITH BYTE ACCESS (CONTINUED)			
USART0	Transmit buffer	U0TXBUF	077h
	Receive buffer	U0RXBUF	076h
	Baud rate	U0BR1	075h
	Baud rate	U0BR0	074h
	Modulation control	U0MCTL	073h
	Receive control	U0RCTL	072h
	Transmit control	U0TCTL	071h
	USART control	U0CTL	070h
Brownout, SVS	SVS control register	SVSCTL	056h
FLL+ Clock	FLL+ control 1	FLL_CTL1	054h
	FLL+ control 0	FLL_CTL0	053h
	System clock frequency control	SCFQCTL	052h
	System clock frequency integrator	SCFI1	051h
	System clock frequency integrator	SCFI0	050h
Basic Timer1	BT counter 2	BTCNT2	047h
	BT counter 1	BTCNT1	046h
	BT control	BTCTL	040h
Port P2	Port P2 selection	P2SEL	02Eh
	Port P2 interrupt enable	P2IE	02Dh
	Port P2 interrupt-edge select	P2IES	02Ch
	Port P2 interrupt flag	P2IFG	02Bh
	Port P2 direction	P2DIR	02Ah
	Port P2 output	P2OUT	029h
	Port P2 input	P2IN	028h
Port P1	Port P1 selection	P1SEL	026h
	Port P1 interrupt enable	P1IE	025h
	Port P1 interrupt-edge select	P1IES	024h
	Port P1 interrupt flag	P1IFG	023h
	Port P1 direction	P1DIR	022h
	Port P1 output	P1OUT	021h
	Port P1 input	P1IN	020h
Special Functions	SFR module enable 2	ME2	005h
	SFR module enable 1	ME1	004h
	SFR interrupt flag 2	IFG2	003h
	SFR interrupt flag 1	IFG1	002h
	SFR interrupt enable 2	IE2	001h
	SFR interrupt enable 1	IE1	000h

electrical characteristics over recommended operating free-air temperature (unless otherwise noted) (continued)

wake-up LPM3

PARAMETER		TEST CONDITIONS		MIN	MAX	UNIT
$t_{d(LPM3)}$	Delay time	f = 1 MHz	V_{CC} = 3 V		6	µs
		f = 2 MHz			6	
		f = 3 MHz			6	

RAM (see Note 1)

PARAMETER	TEST CONDITIONS	MIN	MAX	UNIT
VRAMh	CPU halted (see Note 1)	1.6		V

NOTE 1: This parameter defines the minimum supply voltage when the data in the program memory RAM remain unchanged. No program execution should take place during this supply voltage condition.

LCD

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
$V_{(33)}$	Analog voltage	Voltage at R33	V_{CC} = 3 V	2.5		V_{CC} + 0.2	V
$V_{(23)}$		Voltage at R23			(V_{33} V_{03}) × 2/3 + V_{03}		
$V_{(13)}$		Voltage at R13			($V_{(33)}$ $V_{(03)}$) × 1/3 + $V_{(03)}$		
$V_{(33)}$ $V_{(03)}$		Voltage at R33/R03		2.5		V_{CC} +0.2	
$I_{(R03)}$	Input leakage	R03 = V_{SS}	No load at all segment and common lines, V_{CC} = 3 V			±20	nA
$I_{(R13)}$		R13 = V_{CC}/3				±20	
$I_{(R23)}$		R23 = 2 × V_{CC}/3				±20	
$V_{(Sxx0)}$	Segment line voltage	$I_{(Sxx)}$ = 3 µA, V_{CC} = 3 V		$V_{(03)}$		$V_{(03)}$ 0.1	V
$V_{(Sxx1)}$				$V_{(13)}$		$V_{(13)}$ 0.1	
$V_{(Sxx2)}$				V(23)		$V_{(23)}$ 0.1	
$V_{(Sxx3)}$				V(33)		$V_{(33)}$ + 0.1	

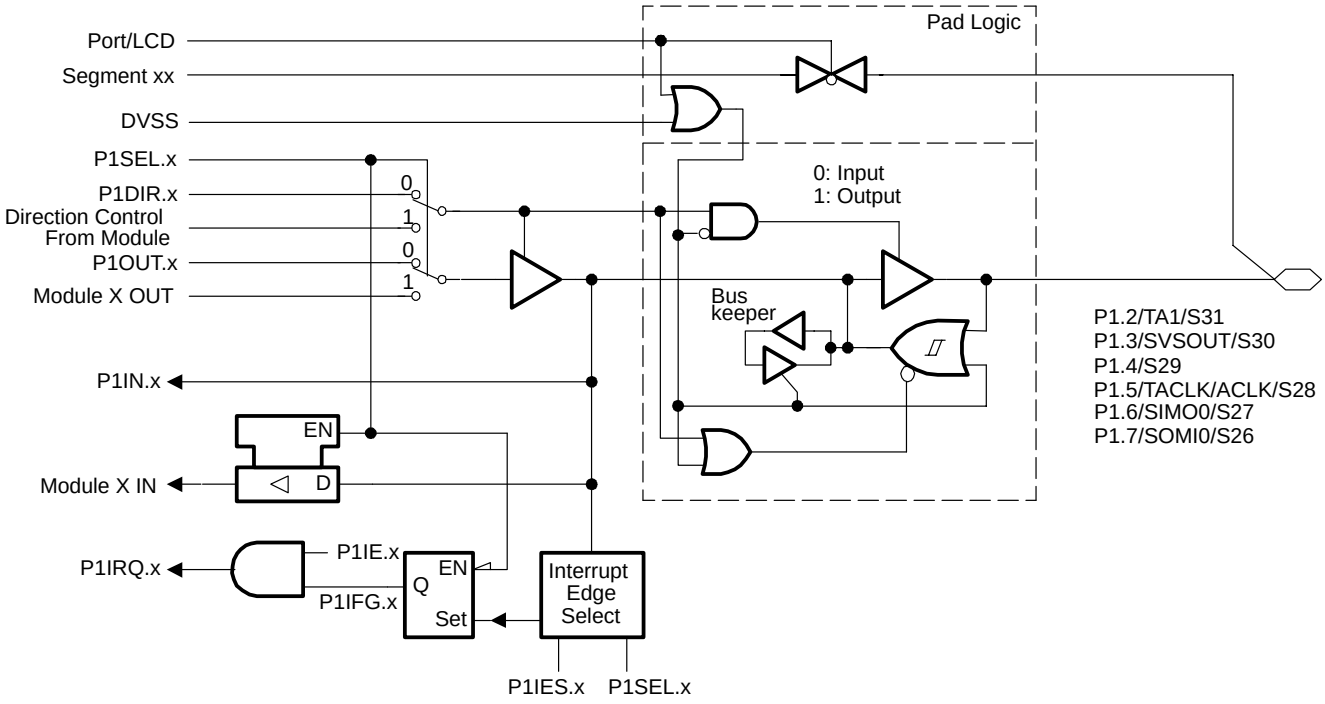
USART0 (see Note 1)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{(\ )}$	USART0: deglitch time	V_{CC} = 3 V, SYNC = 0, UART mode	150	280	500	ns

NOTE 1: The signal applied to the USART0 receive signal/terminal (URXD0) should meet the timing requirements of $t_{(\ )}$ to ensure that the URXS flip-flop is set. The URXS flip-flop is set with negative pulses meeting the minimum-timing condition of $t_{(\ )}$. The operating conditions to set the flag must be met independently from this timing constraint. The deglitch circuitry is active only on negative transitions on the URXD0 line.

APPLICATION INFORMATION

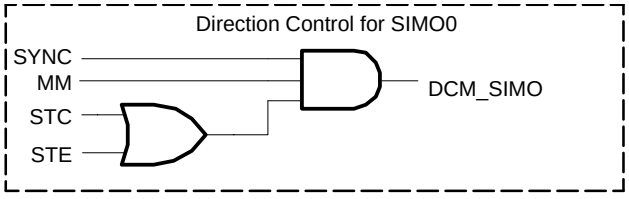
Port P1, P1.2 to P1.7, input/output with Schmitt trigger

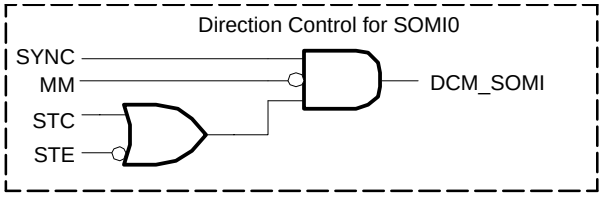


NOTE: 2 x 7.
Port Function is Active if Port/LCD = 0

PnSEL.x	PnDIR.x	Direction Control From Module	PnOUT.x	Module X OUT	PnIN.x	Module X IN	PnIE.x	PnIFG.x	PnIES.x	Port/LCD	Segment
P1SEL.2	P1DIR.2	P1DIR.2	P1OUT.2	Out1 Sig.	P1IN.2	CCI1A	P1IE.2	P1IFG.2	P1IES.2	0: LCDM < 0E0h 1: LCDM 0E0h	S31
P1SEL.3	P1DIR.3	P1DIR.3	P1OUT.3	SVSOUT	P1IN.3	unused	P1IE.3	P1IFG.3	P1IES.3		S30
P1SEL.4	P1DIR.4	P1DIR.4	P1OUT.4	DVSS	P1IN.4	unused	P1IE.4	P1IFG.4	P1IES.4		S29
P1SEL.5	P1DIR.5	P1DIR.5	P1OUT.5	ACLK	P1IN.5	TACLK	P1IE.5	P1IFG.5	P1IES.5		S28
P1SEL.6	P1DIR.6	DCM_SIMO	P1OUT.6	SIMO0(o)	P1IN.6	SIMO0(i)	P1IE.6	P1IFG.6	P1IES.6	0: LCDM < 0C0h 1: LCDM 0C0h	S27
P1SEL.7	P1DIR.7	DCM_SOMI	P1OUT.7	SOMI0(o)	P1IN.7	SOMI0(i)	P1IE.7	P1IFG.7	P1IES.7		S26

Timer_A3
USART0





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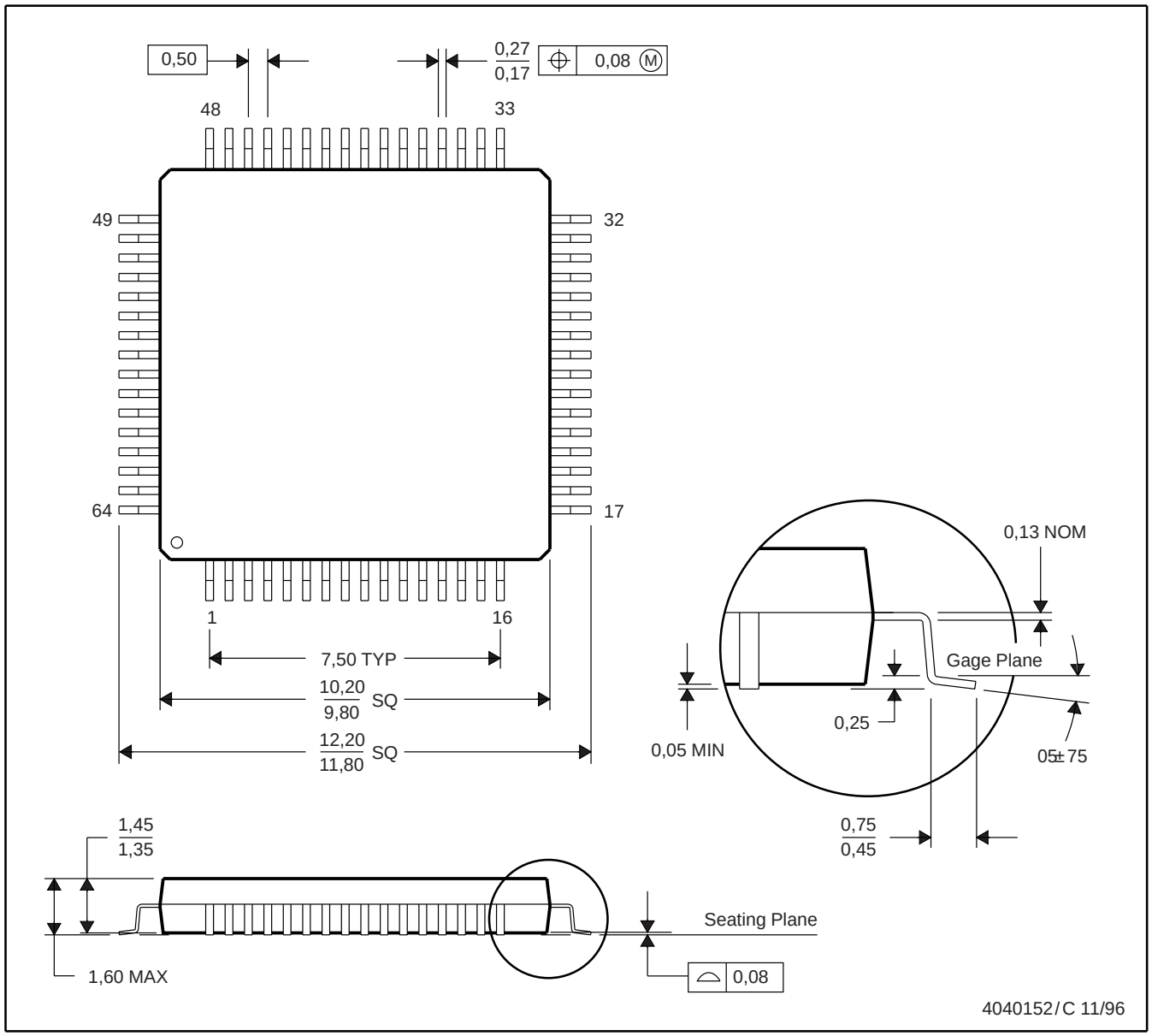
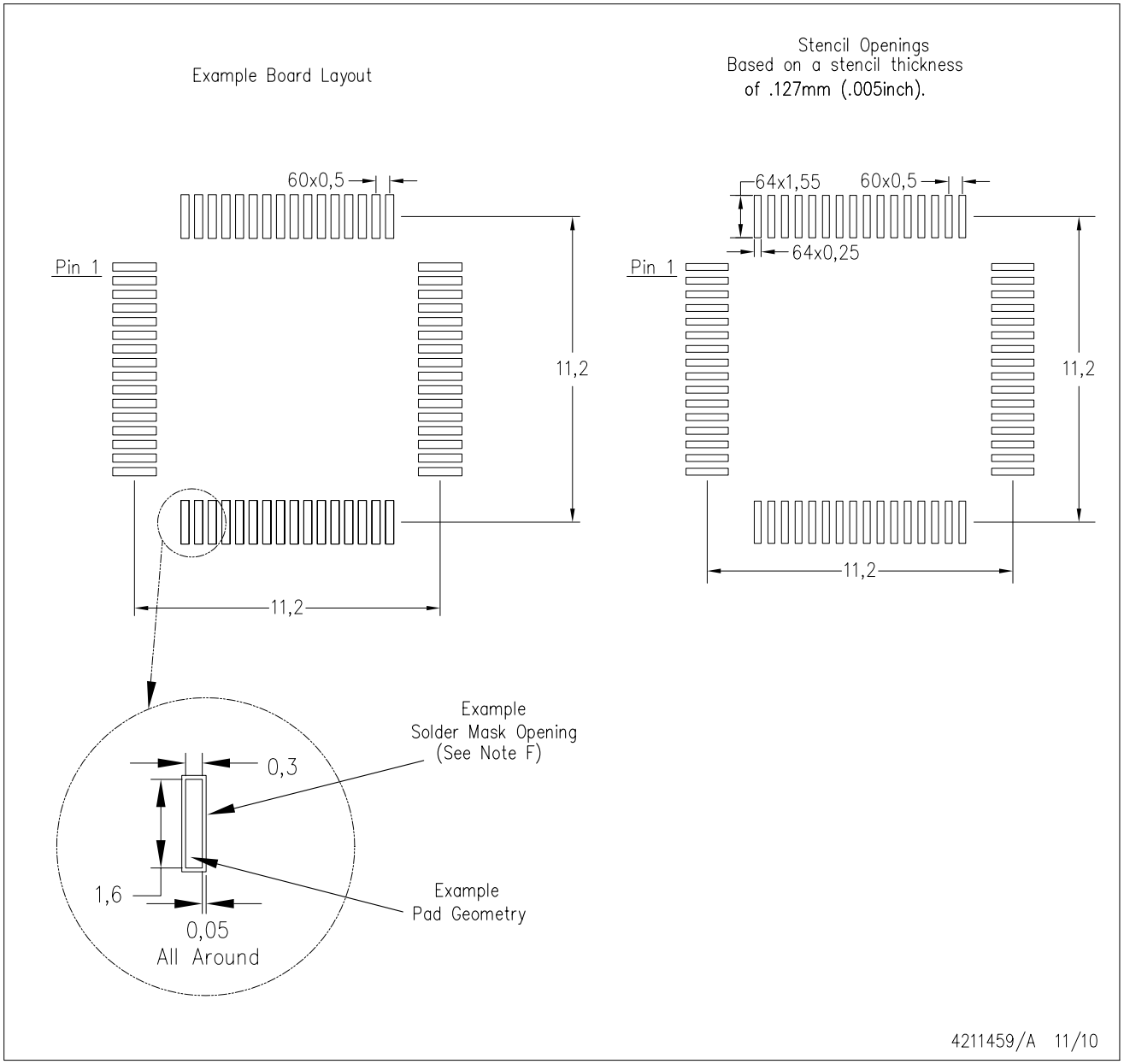
PM (S-PQFP-G64) PLASTIC QUAD FLATPACK



NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS-026
D. May also be thermally enhanced plastic with leads connected to the die pads.

PM (S–PQFP–G64) PLASTIC QUAD FLATPACK



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.
D. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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