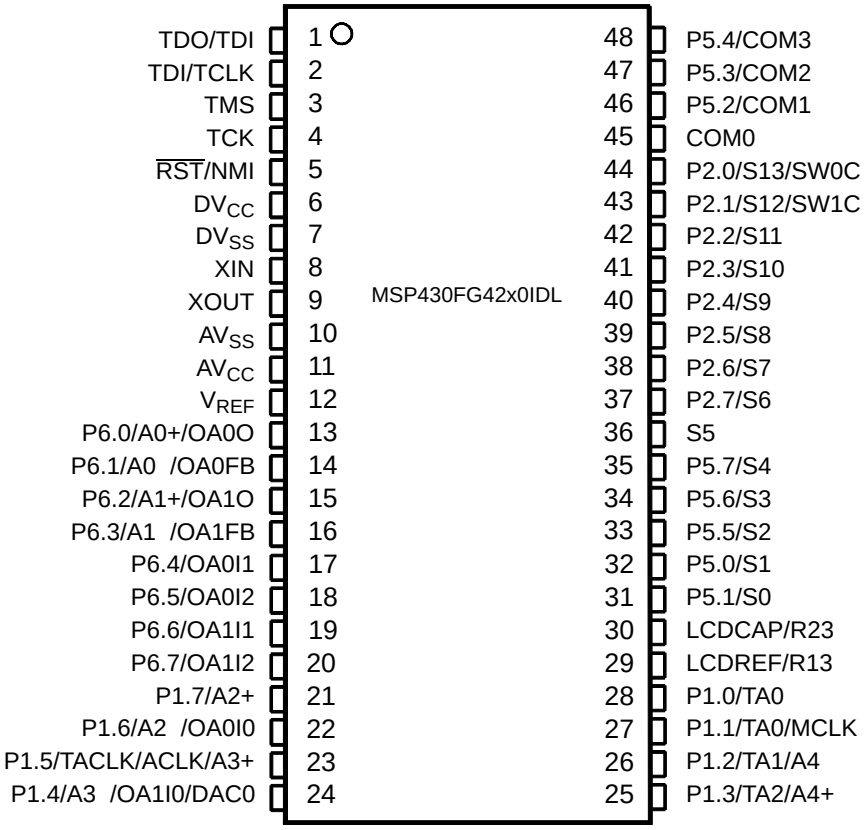
pin designation, DL package

DL PACKAGE
(TOP VIEW)



electrical characteristics over recommended operating free-air temperature (unless otherwise noted) (continued)

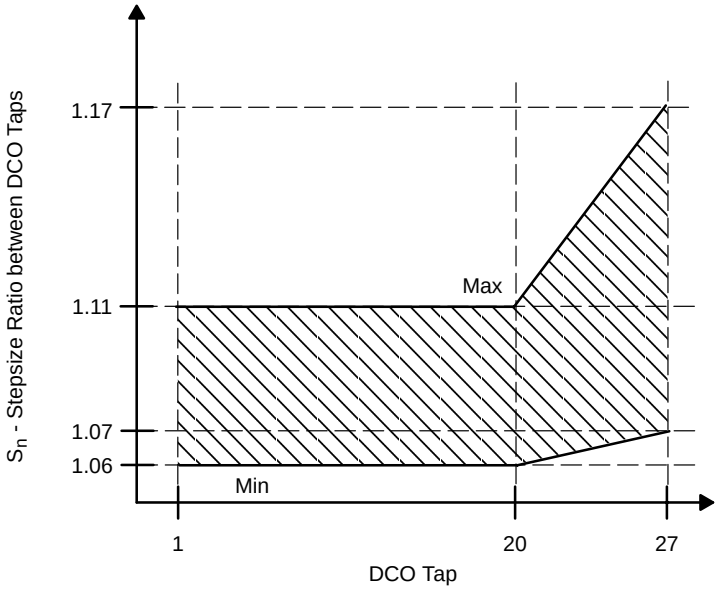


Figure 10. DCO Tap Step Size

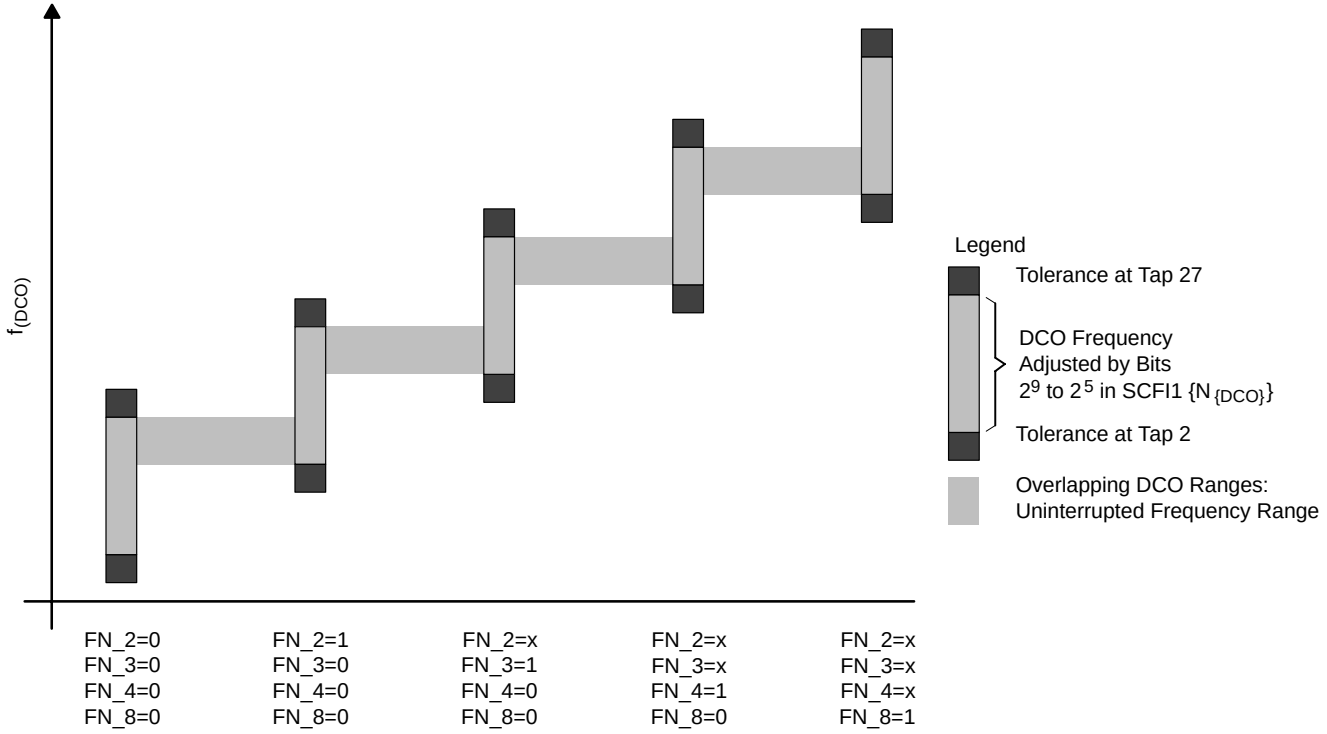


Figure 11. Five Overlapping DCO Ranges Controlled by FN_x Bits

electrical characteristics over recommended operating free-air temperature (unless otherwise noted)

crystal oscillator, LFXT1 oscillator (see Notes 1 and 2)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
C_{XIN}	Integrated input capacitance (see Note 4)	OSCCAPx = 0h, V_{CC} = 2.2 V / 3 V		0		pF
		OSCCAPx = 1h, V_{CC} = 2.2 V / 3 V		10		
		OSCCAPx = 2h, V_{CC} = 2.2 V / 3 V		14		
		OSCCAPx = 3h, V_{CC} = 2.2 V / 3 V		18		
C_{XOUT}	Integrated output capacitance (see Note 4)	OSCCAPx = 0h, V_{CC} = 2.2 V / 3 V		0		pF
		OSCCAPx = 1h, V_{CC} = 2.2 V / 3 V		10		
		OSCCAPx = 2h, V_{CC} = 2.2 V / 3 V		14		
		OSCCAPx = 3h, V_{CC} = 2.2 V / 3 V		18		
V_{IL}	Input levels at XIN	V_{CC} = 2.2 V/3 V (see Note 3)	V_{SS}		$0.2\times V_{CC}$	V
V_{IH}			$0.8\times V_{CC}$		V_{CC}	

NOTES:
1. The parasitic capacitance from the package and board may be estimated to be 2 pF. The effective load capacitor for the crystal is $(C_{XIN} \times C_{XOUT}) / (C_{XIN} + C_{XOUT})$. This is independent of XTS_FLL.
2. To improve EMI on the low-power LFXT1 oscillator, particularly in the LF mode (32 kHz), the following guidelines should be observed.
   Keep as short of a trace as possible between the FG42x0 and the crystal.
   Design a good ground plane around the oscillator pins.
   Prevent crosstalk from other clock or data lines into oscillator pins XIN and XOUT.
   Avoid running PCB traces underneath or adjacent to the XIN and XOUT pins.
   Use assembly materials and praxis to avoid any parasitic load on the oscillator XIN and XOUT pins.
   If conformal coating is used, ensure that it does not induce capacitive/resistive leakage between the oscillator pins.
   Do not route the XOUT line to the JTAG header to support the serial programming adapter as shown in other documentation. This signal is no longer required for the serial programming adapter.
3. Applies only when using an external logic-level clock source. XTS_FLL must be set. Not applicable when using a crystal or resonator.
4. External capacitance is recommended for precision real-time clock applications, OSCCAPx = 0h.

electrical characteristics over recommended operating free-air temperature (unless otherwise noted) (continued)

SD16_A, power supply and recommended operating conditions

PARAMETER		TEST CONDITIONS		V_{CC}	MIN	TYP	MAX	UNIT
AV_{CC}	Analog supply voltage	$AV_{CC} = DV_{CC}$ $AV_{SS} = DV_{SS} = 0V$			2.5		3.6	V
I_{SD16}	Analog supply current including internal reference	SD16LP = 0, f_{SD16} = 1 MHz, SD16OSR = 256	SD16BUFx = 00, GAIN: 1,2	3 V		650	950	µA
			SD16BUFx = 00, GAIN: 4,8,16			730	1100	
			SD16BUFx = 00, GAIN: 32			1050	1550	
		SD16LP = 1, f_{SD16} = 0.5 MHz, SD16OSR = 256	SD16BUFx = 00, GAIN: 1			620	930	
			SD16BUFx = 00, GAIN: 32			700	1060	
		SD16LP = 0, f_{SD16} = 1 MHz, SD16OSR = 256	SD16BUFx = 01, GAIN: 1			850		
			SD16BUFx = 10, GAIN: 1			1130		
			SD16BUFx = 11, GAIN: 1			1130		
f_{SD16}	Analog front-end input clock frequency	SD16LP = 0 (Low power mode disabled)		3 V	0.03	1	1.1	MHz
		SD16LP = 1 (Low power mode enabled)			0.03	0.5		

SD16_A, input range

PARAMETER		TEST CONDITIONS		V_{CC}	MIN	TYP	MAX	UNIT
$V_{ID,FSR}$	Differential full scale input voltage range	Bipolar mode, SD16UNI = 0			V_{REF}/2GAIN		$+V_{REF}$/2GAIN	mV
		Unipolar mode, SD16UNI = 1			0		$+V_{REF}$/2GAIN	
V_{ID}	Differential input voltage range for specified performance (see Note 1)	SD16REFON=1	SD16GAINx = 1			–500		mV
			SD16GAINx = 2			–250		
			SD16GAINx = 4			–125		
			SD16GAINx = 8			–62		
			SD16GAINx = 16			–31		
			SD16GAINx = 32			–15		
Z_I	Input impedance (one input pin to AV_{SS})	f_{SD16} = 1MHz, SD16BUFx = 00	SD16GAINx = 1	3 V		200		k
			SD16GAINx = 32			75		
		f_{SD16} = 1MHz, SD16BUFx = 01	SD16GAINx = 1			>10		M
Z_{ID}	Differential Input impedance (IN+ to IN)	f_{SD16} = 1MHz, SD16BUFx = 00	SD16GAINx = 1	3 V	300	400		k
			SD16GAINx = 32		100	150		
		f_{SD16} = 1MHz, SD16BUFx > 00	SD16GAINx = 1			>10		M
V_I	Absolute input voltage range	SD16BUFx = 00			AV_{SS} 0.1V		AV_{CC}	V
		SD16BUFx > 00			AV_{SS}		AV_{CC} 1.2V	
V_{IC}	Common-mode input voltage range	SD16BUFx = 00			AV_{SS} 0.1V		AV_{CC}	V
		SD16BUFx > 00			AV_{SS}		AV_{CC} 1.2V	

NOTES: 1. The analog input range depends on the reference voltage applied to V_{REF}. If V_{REF} is sourced externally, the full-scale range is defined by $V_{FSR+} = +(V_{REF}/2)/GAIN$ and $V_{FSR} = (V_{REF}/2)/GAIN$. The analog input range should not exceed 80% of V_{FSR+} or V_{FSR} .

electrical characteristics over recommended operating free-air temperature (unless otherwise noted) (continued)

SD16_A, performance (f $_{SD16}$ = 30kHz, SD16REFON = 1, SD16BUFx = 01)

PARAMETER		TEST CONDITIONS		V_{CC}	MIN	TYP	MAX	UNIT
SINAD	Signal-to-noise + distortion ratio	SD16GAINx = 1,Signal Amplitude = 500mV SD16OSRx = 256	f_{IN} = 2.8Hz	3 V		84		dB
		SD16GAINx = 1,Signal Amplitude = 500mV SD16OSRx = 512				84		
		SD16GAINx = 1,Signal Amplitude = 500mV SD16OSRx = 1024				84		
	Nominal gain	SD16GAINx = 1, SD16OSRx = 1024		3 V	0.97	1.00	1.02	
dG/dT	Gain temperature drift	SD16GAINx = 1, SD16OSRx = 1024 (see Note 1)		3 V		15		ppm/ C
dG/dV_{CC}	Gain supply voltage drift	SD16GAINx = 1, SD16OSRx = 1024, V_{CC} = 2.5 V to 3.6 V (see Note 2)				0.35		%/V

NOTES: 1. Calculated using the box method: (MAX(40...85 C) MIN(40...85 C))/MIN(40...85 C)/(85C (40 C))
2. Calculated using the box method: (MAX(2.5...3.6V) MIN(2.5...3.6V))/MIN(2.5...3.6V)/(3.6V 2.5V)

SD16_A, performance (f $_{SD16}$ = 1MHz, SD16OSRx = 256, SD16REFON = 1, SD16BUFx = 00)

PARAMETER		TEST CONDITIONS		V_{CC}	MIN	TYP	MAX	UNIT
SINAD	Signal-to-noise + distortion ratio	SD16GAINx = 1,Signal Amplitude = 500mV	f_{IN} = 50 Hz, 100 Hz	3 V	83.5	85		dB
		SD16GAINx = 2,Signal Amplitude = 250mV			81.5	84		
		SD16GAINx = 4,Signal Amplitude = 125mV			76	79.5		
		SD16GAINx = 8,Signal Amplitude = 62mV			73	76.5		
		SD16GAINx = 16,Signal Amplitude = 31mV			69	73		
		SD16GAINx = 32,Signal Amplitude = 15mV			62	69		
G	Nominal gain	SD16GAINx = 1		3 V	0.97	1.00	1.02	
		SD16GAINx = 2			1.90	1.96	2.02	
		SD16GAINx = 4			3.76	3.86	3.96	
		SD16GAINx = 8			7.36	7.62	7.84	
		SD16GAINx = 16			14.56	15.04	15.52	
		SD16GAINx = 32			27.20	28.35	29.76	
E_{OS}	Offset error	SD16GAINx = 1		3 V			–0.2	%FSR
		SD16GAINx = 32					–1.5	
dE_{OS}/dT	Offset error temperature coefficient	SD16GAINx = 1		3 V		–4	–20	ppm FSR/ C
		SD16GAINx = 32				–20	–100	
CMRR	Common-mode rejection ratio	SD16GAINx = 1, Common-mode input signal: V_{ID} = 500 mV, f_{IN} = 50 Hz, 100 Hz		3 V		>90		dB
		SD16GAINx = 32, Common-mode input signal: V_{ID} = 16 mV, f_{IN} = 50 Hz, 100 Hz				>75		
AC PSRR	AC power supply rejection ratio	SD16GAINx = 1, V_{CC} = 3 V – 100 mV, f_{VCC} = 50 Hz		3 V		>80		dB

electrical characteristics over recommended operating free-air temperature (unless otherwise noted) (continued)

SD16_A, temperature sensor

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
TC_{Sensor}	Sensor temperature coefficient			1.18	1.32	1.46	mV/K
$V_{Offset,sensor}$	Sensor offset voltage			100		100	mV
V_{Sensor}	Sensor output voltage (see Note 2)	Temperature sensor voltage at T_A = 85°C	3 V	435	475	515	mV
		Temperature sensor voltage at T_A = 25°C		355	395	435	
		Temperature sensor voltage at T_A = 0°C		320	360	400	

NOTES: 1. The following formula can be used to calculate the temperature sensor output voltage:
$V_{Sensor,typ} = TC_{Sensor} (273 + T [°C]) + V_{Offset,sensor}$ [mV]
2. Results based on characterization and/or production test, not TC_{Sensor} or $V_{Offset,sensor}$.

SD16_A, built-in voltage reference

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
V_{REF}	Internal reference voltage	SD16REFON = 1, SD16VMIDON = 0	3 V	1.14	1.20	1.26	V
I_{REF}	Reference supply current	SD16REFON = 1, SD16VMIDON = 0	3 V		175	260	µA
TC	Temperature coefficient	SD16REFON = 1, SD16VMIDON = 0	3 V		18	50	ppm/K
C_{REF}	V_{REF} load capacitance	SD16REFON = 1, SD16VMIDON = 0 (see Note 1)			100		nF
I_{LOAD}	$V_{REF(I)}$ maximum load current	SD16REFON = 1, SD16VMIDON = 0	3 V			–200	nA
t_{ON}	Turn-on time	SD16REFON = 0 >1, SD16VMIDON = 0, C_{REF} = 100 nF	3 V		5		ms
DC PSR	DC power-supply rejection, V_{REF}/ V_{CC}	SD16REFON = 1, SD16VMIDON = 0, V_{CC} = 2.5 V to 3.6 V			100		µV/V

NOTES: 1. There is no capacitance required on V_{REF}. However, a capacitance of at least 100nF is recommended to reduce any reference voltage noise.

SD16_A, reference output buffer

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
$V_{REF,BUF}$	Reference buffer output voltage	SD16REFON = 1, SD16VMIDON = 1	3 V		1.2		V
$I_{REF,BUF}$	Reference supply + reference output buffer quiescent current	SD16REFON = 1, SD16VMIDON = 1	3 V		385	600	µA
$C_{REF(O)}$	Required load capacitance on V_{REF}	SD16REFON = 1, SD16VMIDON = 1		470			nF
$I_{LOAD,Max}$	Maximum load current on V_{REF}	SD16REFON = 1, SD16VMIDON = 1	3 V			–1	mA
	Maximum voltage variation vs load current	$\|I_{LOAD}\|$ = 0 to 1 mA	3 V	15		+15	mV
t_{ON}	Turn-on time	SD16REFON = 0 >1, SD16VMIDON = 1, C_{REF} = 470 nF	3 V		100		µs

SD16_A, external reference input

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
$V_{REF(I)}$	Input voltage range	SD16REFON = 0	3 V	1.0	1.25	1.5	V
$I_{REF(I)}$	Input current	SD16REFON = 0	3 V			50	nA

electrical characteristics over recommended operating free-air temperature (unless otherwise noted) (continued)

12-bit DAC, supply specifications

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
AV_{CC}	Analog supply voltage	$AV_{CC} = DV_{CC}$, $AV_{SS} = DV_{SS} = 0$ V		2.20		3.60	V
I_{DD}	Supply current (see Notes 1 and 2)	DAC12AMPx = 2, DAC12IR=0, DAC12_xDAT=0800h	2.2V/3V		50	110	µA
		DAC12AMPx = 2, DAC12IR=1, DAC12_xDAT = 0800h, $V_{REF,DAC12} = AV_{CC}$			50	110	
		DAC12AMPx = 5, DAC12IR = 1, DAC12_xDAT = 0800h, $V_{REF,DAC12} = AV_{CC}$			200	440	
		DAC12AMPx=7, DAC12IR = 1, DAC12_xDAT = 0800h, $V_{REF,DAC12} = AV_{CC}$			700	1500	
PSRR	Power supply rejection ratio (see Notes 3 and 4)	DAC12_xDAT = 800h, $V_{REF,DAC12}$ = 1.2V AV_{CC} = 100 mV	2.7V		70		dB

NOTES: 1. No load at the output pin assuming that the control bits for the shared pins are set properly.
2. Current into reference terminals not included. If DAC12IR = 1 current flows through the input divider; see Reference Input specifications.
3. PSRR = $20 \times \log\{ AV_{CC} / V_{DAC12_xOUT}\}$.
4. V_{REF} is applied externally. The internal reference is not used.

electrical characteristics over recommended operating free-air temperature (unless otherwise noted) (continued)

12-bit DAC, linearity specifications (see Figure 12)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
	Resolution	12-bit monotonic		12			bits
INL	Integral nonlinearity (see Note 1)	$V_{REF,DAC12}$ = 1.2 V, DAC12AMPx = 7, DAC12IR = 1	2.7 V		–2.0	–8.0	LSB
DNL	Differential nonlinearity (see Note 1)	$V_{REF,DAC12}$ = 1.2 V, DAC12AMPx = 7, DAC12IR = 1	2.7 V		–0.4	–1.0	LSB
E_O	Offset voltage w/o calibration (see Notes 1, 2)	$V_{REF,DAC12}$ = 1.2 V, DAC12AMPx = 7, DAC12IR = 1	2.7 V			–20	mV
	Offset voltage with calibration (see Notes 1, 2)	$V_{REF,DAC12}$ = 1.2 V, DAC12AMPx = 7, DAC12IR = 1	2.7 V			–2.5	
$d_{E(O)}/d_T$	Offset error temperature coefficient (see Note 1)		2.7 V		–30		µV/C
E_G	Gain error (see Note 1)	$V_{REF,DAC12}$ = 1.2 V	2.7 V			–3.50	% FSR
$d_{E(G)}/d_T$	Gain temperature coefficient (see Note 1)		2.7 V		10		ppm of FSR/°C
t_{Offset_Cal}	Time for offset calibration (see Note 3)	DAC12AMPx = 2	2.7 V			100	ms
		DAC12AMPx = 3, 5	2.7 V			32	
		DAC12AMPx = 4, 6, 7	2.7 V			6	

NOTES: 1. Parameters calculated from the best-fit curve from 0x0A to 0xFFF. The best-fit curve method is used to deliver coefficients a and b of the first order equation: y = a + b*x. $V_{DAC12_xOUT} = E_O + (1 + E_G) * (V_{REF,DAC12}/4095) *$ DAC12_xDAT, DAC12IR = 1.
2. The offset calibration works on the output operational amplifier. Offset calibration is triggered setting bit DAC12CALON.
3. The offset calibration can be done if DAC12AMPx = {2, 3, 4, 5, 6, 7}. The output operational amplifier is switched off with DAC12AMPx = {0, 1}. It is recommended that the DAC12 module be configured prior to initiating calibration. Port activity during calibration may effect accuracy and is not recommended.

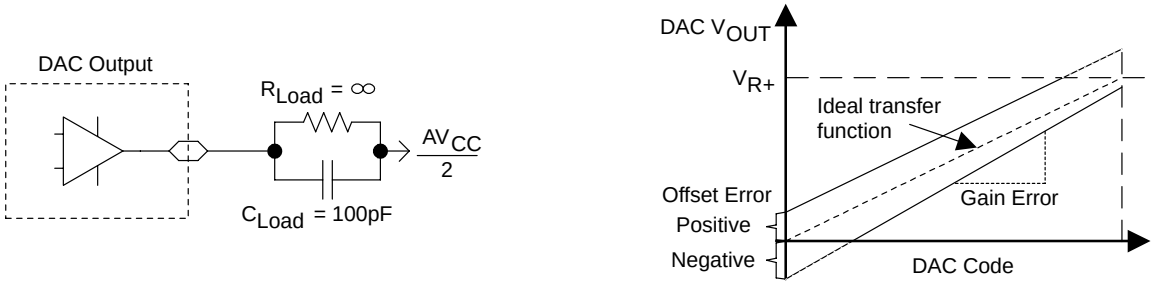


Figure 12. Linearity Test Load Conditions and Gain/Offset Definition

electrical characteristics over recommended operating free-air temperature (unless otherwise noted)

operational amplifier OA, dynamic specifications

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
SR	Slew rate	Fast Mode			1.2		V/µs
		Medium Mode			0.8		
		Slow Mode			0.3		
	Open-loop voltage gain				100		dB
$_m$	Phase margin	C_L = 50 pF			60		deg
	Gain margin	C_L = 50 pF			20		dB
GBW	Gain-bandwidth product (see Figure 19 and Figure 20)	Noninverting, Fast Mode, R_L = 47k , C_L = 50pF	2.2 V/3 V		2.2		MHz
		Noninverting, Medium Mode, R_L =300k , C_L = 50pF			1.4		
		Noninverting, Slow Mode, R_L =300k , C_L = 50pF			0.5		
$t_{en(on)}$	Enable time on	t_{on}, noninverting, Gain = 1	2.2 V/3 V		10	20	µs
$t_{en(off)}$	Enable time off		2.2 V/3 V			1	µs

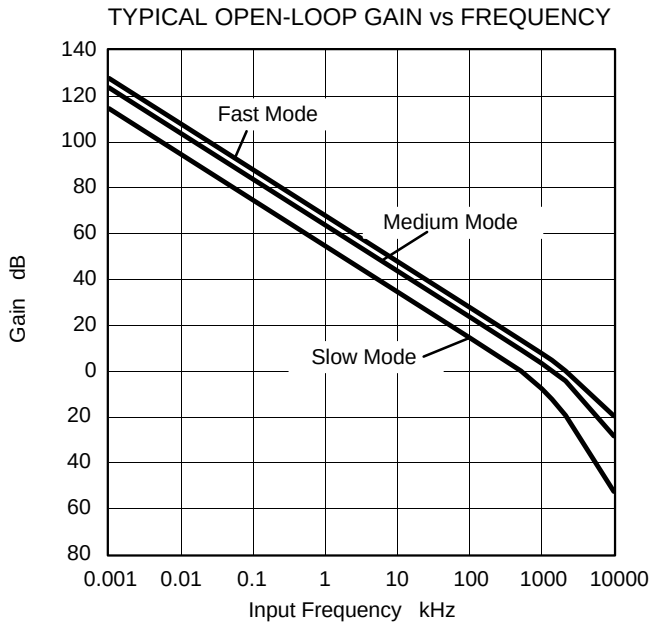


Figure 19

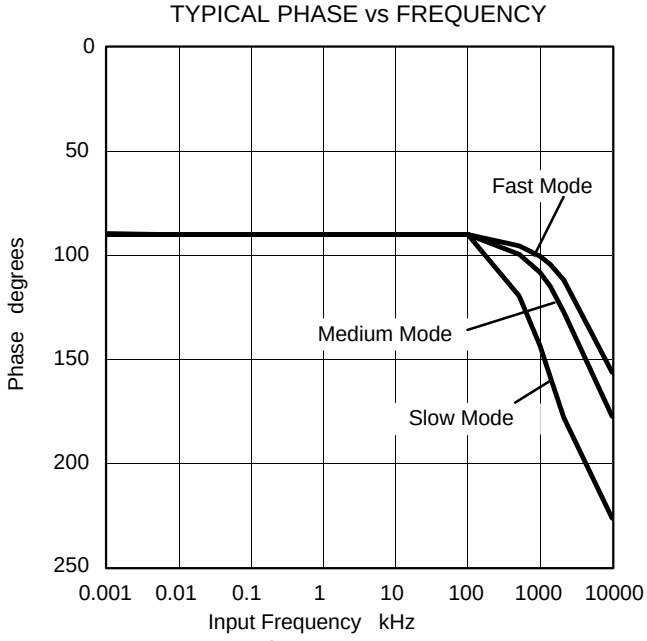


Figure 20

switches to ground

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
V_{CC}	Supply voltage			2.5		3.6	V
I_{lkg}	Input leakage current (see Note 1)	T_A = 40 C to + 55 C			–1	–10	nA
		T_A = 55 C to 85 C				–50	
I_{IN}	Input current	Input switched to Ground.		0		100	µA
R_{ON}	On resistance	I_{IN}=100 µA, T_A= 40°C to 85°C				10	

NOTES: 1. ESD damage can degrade input current leakage.

electrical characteristics over recommended operating free-air temperature (unless otherwise noted)

flash memory

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
$V_{CC(PGM/ERASE)}$	Program and erase supply voltage			2.5		3.6	V
f_{FTG}	Flash timing generator frequency			257		476	kHz
I_{PGM}	Supply current from DV_{CC} during program		2.5V/3.6V		3	5	mA
I_{ERASE}	Supply current from DV_{CC} during erase		2.5V/3.6V		3	7	mA
t_{CPT}	Cumulative program time	see Note 1	2.5V/3.6V			10	ms
$t_{CMErase}$	Cumulative mass erase time	see Note 2	2.5V/3.6V	200			ms
	Program/erase endurance			10^4	10^5		cycles
$t_{Retention}$	Data retention duration	T_J = 25°C		100			years
t_{Word}	Word or byte program time	see Note 3			35		t_{FTG}
$t_{Block, 0}$	Block program time for 1st byte or word				30		
$t_{Block, 1-63}$	Block program time for each additional byte or word				21		
$t_{Block, End}$	Block program end-sequence wait time				6		
$t_{Mass Erase}$	Mass erase time				5297		
$t_{Seg Erase}$	Segment erase time				4819		

NOTES: 1. The cumulative program time must not be exceeded when writing to a 64 byte flash block. This parameter applies to all programming methods: individual word/byte write and block write modes.
2. The mass erase duration generated by the flash timing generator is at least 11.1ms (= 5297x1/f_{FTG},max = 5297x1/476kHz). To achieve the required cumulative mass erase time the Flash Controller s mass erase operation can be repeated until this time is met. (A worst case minimum of 19 cycles are required).
3. These values are hardwired into the Flash Controller s state machine (t_{FTG} = 1/f_{FTG}).

JTAG interface

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
f_{TCK}	TCK input frequency	see Note 1	2.2 V	0		5	MHz
			3 V	0		10	MHz
$R_{Internal}$	Internal pull-up resistance on TMS, TCK, TDI/TCLK	see Note 2	2.2 V/ 3 V	25	60	90	k

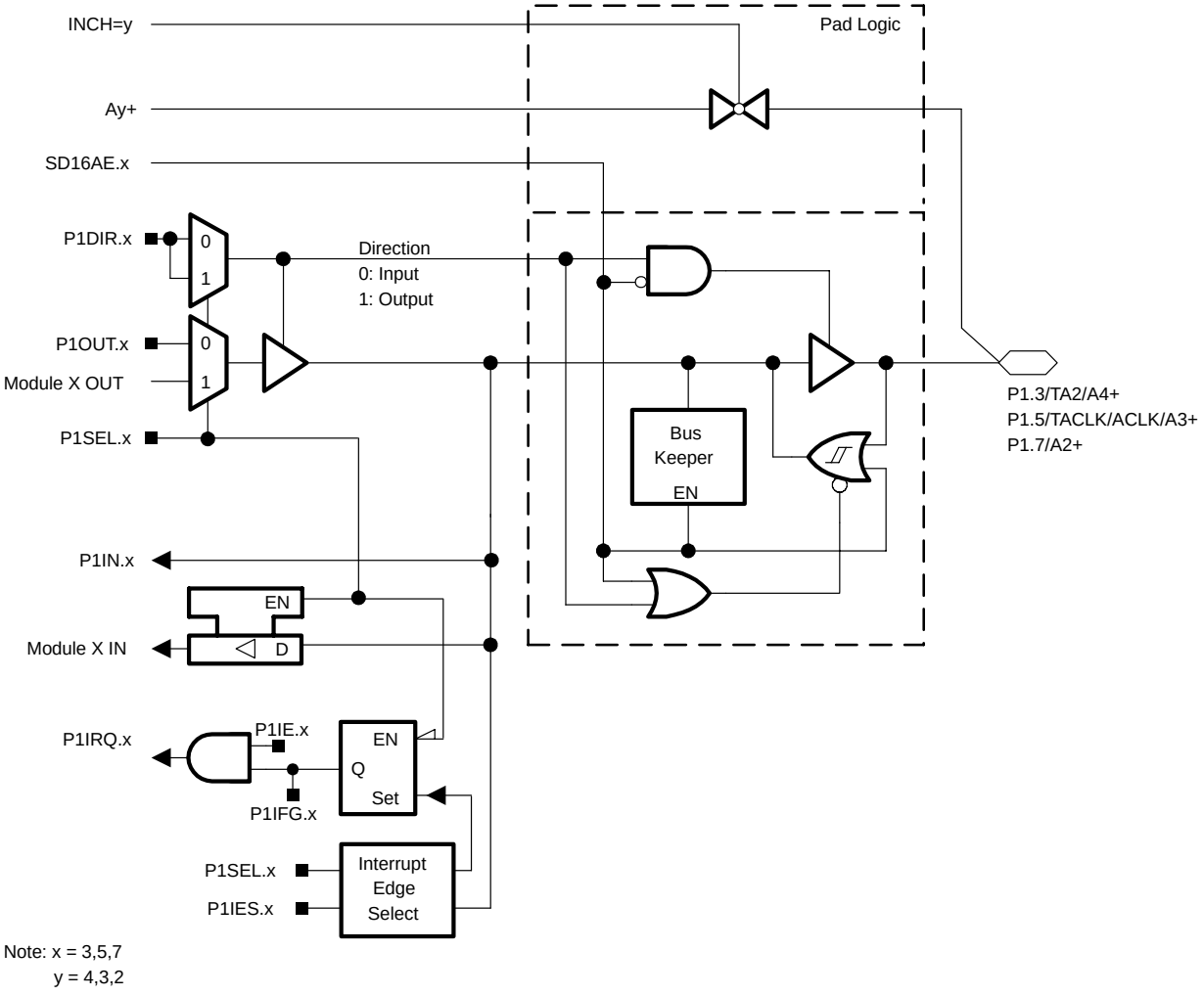
NOTES: 1. f_{TCK} may be restricted to meet the timing requirements of the module selected.
2. TMS, TDI/TCLK, and TCK pull-up resistors are implemented in all versions.

JTAG fuse (see Note 1)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
$V_{CC(FB)}$	Supply voltage during fuse-blow condition	T_A = 25°C		2.5			V
V_{FB}	Voltage level on TDI/TCLK for fuse-blow: F versions			6		7	V
I_{FB}	Supply current into TDI/TCLK during fuse blow					100	mA
t_{FB}	Time to blow fuse					1	ms

NOTES: 1. Once the fuse is blown, no further access to the MSP430 JTAG/Test and emulation features is possible. The JTAG block is switched to bypass mode.

Port P1 pin schematic: P1.3, P1.5, P1.7, input/output with Schmitt trigger and analog functions



Note: x = 3,5,7
y = 4,3,2

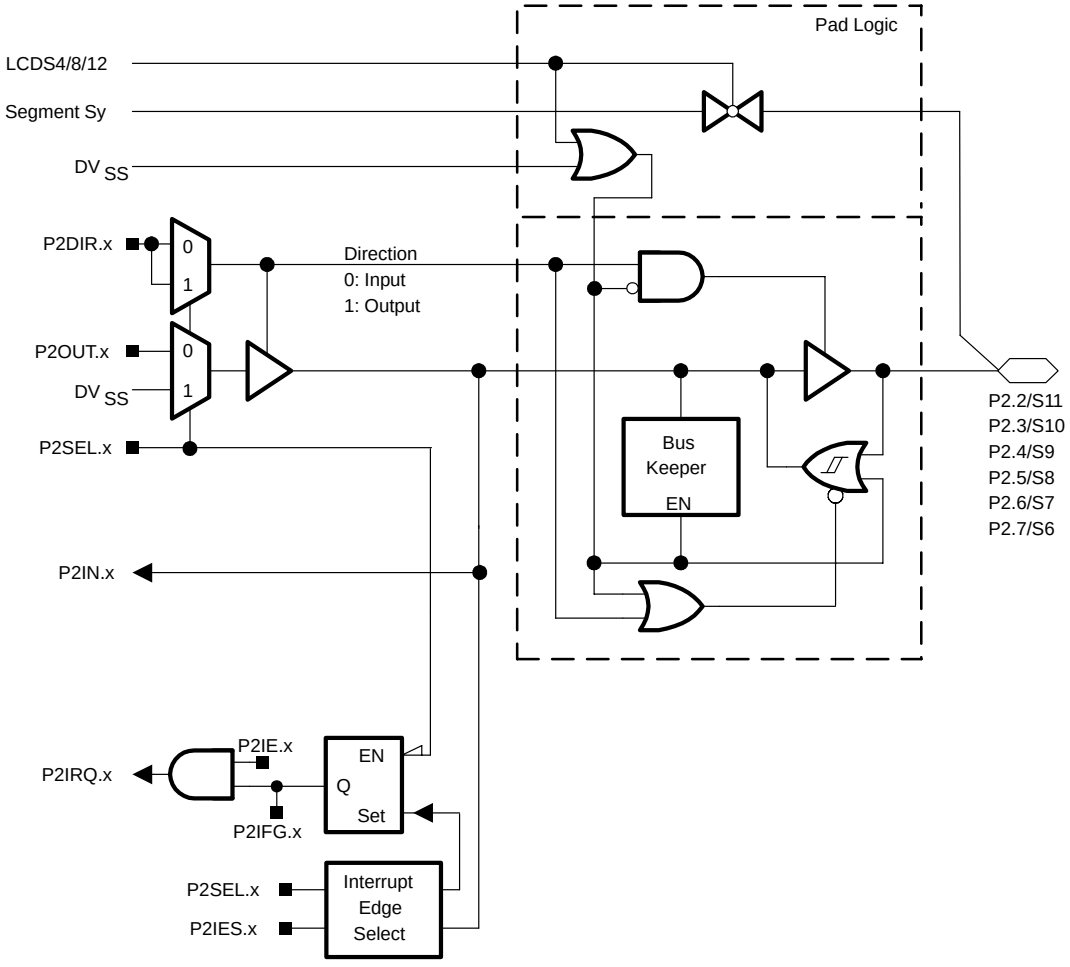
Port P1 (P1.3, P1.5, P1.7) pin functions

PIN NAME (P1.X)	X	FUNCTION	CONTROL BITS / SIGNALS		
			P1DIR.x	P1SEL.x	SD16AE.x
P1.3/TA2/A4+	3	P1.3 Input/Output	0/1	0	0
		Timer_A3.CCI2A	0	1	0
		Timer_A3.TA2	1	1	0
		A4+ (see Note 3)	X	X	1
P1.5/TACLK/ACLK/A3+	5	P1.5 Input/Output	0/1	0	0
		Timer_A3.TACLK/$\overline{\text{INCLK}}$	0	1	0
		ACLK	1	1	0
		A3+ (see Note 3)	X	X	1
P1.7/A2+	7	P1.5 Input/Output	0/1	0	0
		N/A	0	1	0
		DVSS	1	1	0
		A2+ (see Note 3)	X	X	1

Default after reset (PUC/POR)

NOTES: 1. N/A: Not available or not applicable.
2. X: Don t care.
3. Setting the SD16AE.x bit disables the output driver as well as the input Schmitt trigger to prevent parasitic cross currents when applying analog signals.

Port P2 pin schematic: P2.2 to P2.7, input/output with Schmitt trigger, LCD and analog functions



Note: x = 2 to 7
y = 11 to 6

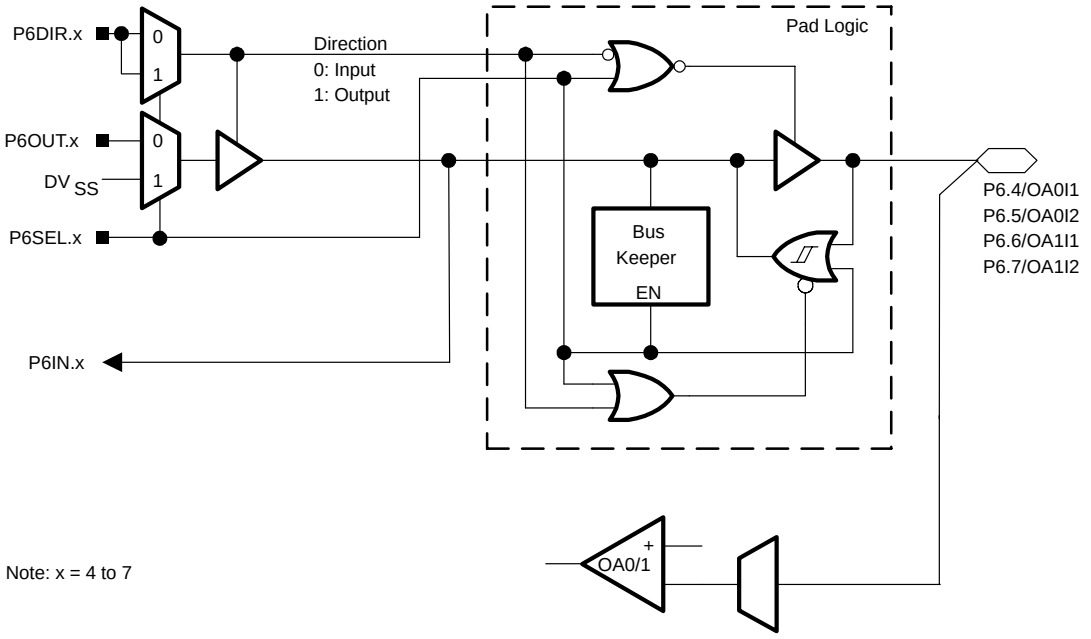
Port P2 (P2.0 to P2.7) pin functions

PIN NAME (P2.X)	X	FUNCTION	CONTROL BITS / SIGNALS		
			P2DIR.x	P2SEL.x	LCDS12
P2.2/S11	2	P2.2 Input/Output	0/1	0	0
		N/A	0	1	0
		DVSS	1	1	0
		S11	X	X	1
P2.3/S10	3	P2.3 Input/Output	0/1	0	0
		N/A	0	1	0
		DVSS	1	1	0
		S10	X	X	1
P2.4/S9	4	P2.4 Input/Output	0/1	0	0
		N/A	0	1	0
		DVSS	1	1	0
		S9	X	X	1
P2.5/S8	5	P2.5 Input/Output	0/1	0	0
		N/A	0	1	0
		DVSS	1	1	0
		S8	X	X	1
P2.6/S7	6	P2.6 Input/Output	0/1	0	0
		N/A	0	1	0
		DVSS	1	1	0
		S7	X	X	1
P2.7/S6	7	P2.7 Input/Output	0/1	0	0
		N/A	0	1	0
		DVSS	1	1	0
		S6	X	X	1

Default after reset (PUC/POR)

NOTES: 1. N/A: Not available or not applicable.
2. X: Don t care.

Port P6 pin schematic: P6.4 to P6.7, input/output with Schmitt trigger and analog functions



Port P6 (P6.4 to P6.7) pin functions

PIN NAME (P6.X)	X	FUNCTION	CONTROL BITS / SIGNALS	
			P6DIR.x	P6SEL.x
P6.4/OA0I1	4	P6.4 Input/Output	0/1	0
		OA0I1 (see Note 3)	X	1
P6.5/OA0I2	5	P6.5 Input/Output	0/1	0
		OA0I2 (see Note 3)	X	1
P6.6/OA1I1	6	P6.6 Input/Output	0/1	0
		OA1I1 (see Note 3)	X	1
P6.7/OA1I2	7	P6.7 Input/Output	0/1	0
		OA1I2 (see Note 3)	X	1

Default after reset (PUC/POR)

NOTES: 1. N/A: Not available or not applicable.
2. X: Don t care.
3. Setting the P6SEL.x bit disables the output driver as well as the input Schmitt trigger to prevent parasitic cross currents when applying analog signals.

Data Sheet Revision History

Literature Number	Summary
SLAS556	Product Preview data sheet release
SLAS556A	Production Data data sheet release

NOTE: Page and figure numbers refer to the respective document revision.

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