AVAILABLE OPTIONS

T_A	PACKAGED DEVICES†‡	
	PLASTIC 113-BALL BGA (ZQW)	PLASTIC 80-PIN QFP (PN)§
–40°C to 85°C	MSP430FG477IZQW MSP430FG478IZQW MSP430FG479IZQW	MSP430FG477IPN MSP430FG478IPN MSP430FG479IPN

† For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.
‡ Package drawings, thermal data, and symbolization are available at www.ti.com/packaging.
§ Product Preview

DEVELOPMENT TOOL SUPPORT

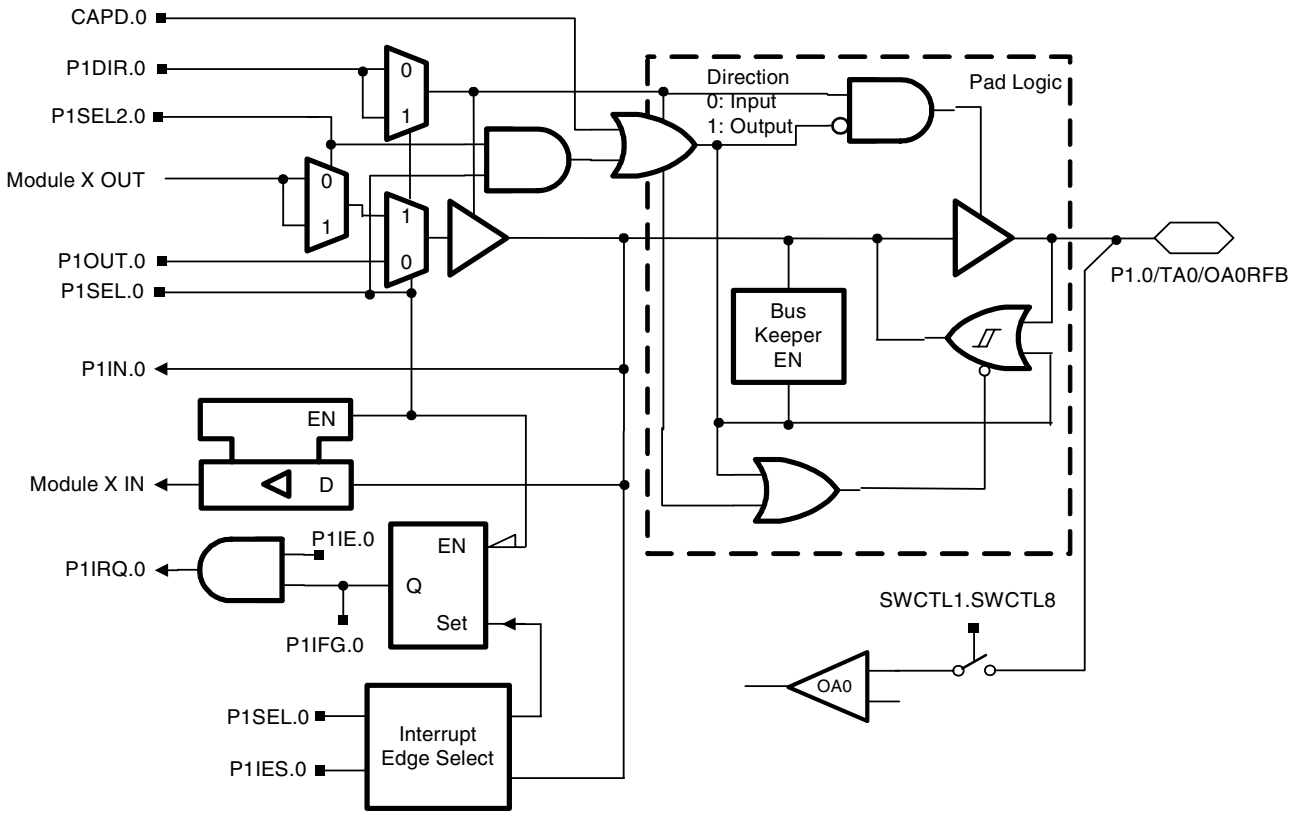
All MSP430 microcontrollers include an Embedded Emulation Module (EEM) allowing advanced debugging and programming through easy to use development tools. Recommended hardware options include the following:

- Debugging and Programming Interface
  - MSP–FET430UIF (USB)
  - MSP–FET430PIF (Parallel Port)
- Debugging and Programming Interface with Target Board
  - MSP–FET430U80
- Production Programmer
  - MSP–GANG430

PRODUCT PREVIEW

APPLICATION INFORMATION

Port P1 pin schematic: P1.0, input/output with Schmitt trigger



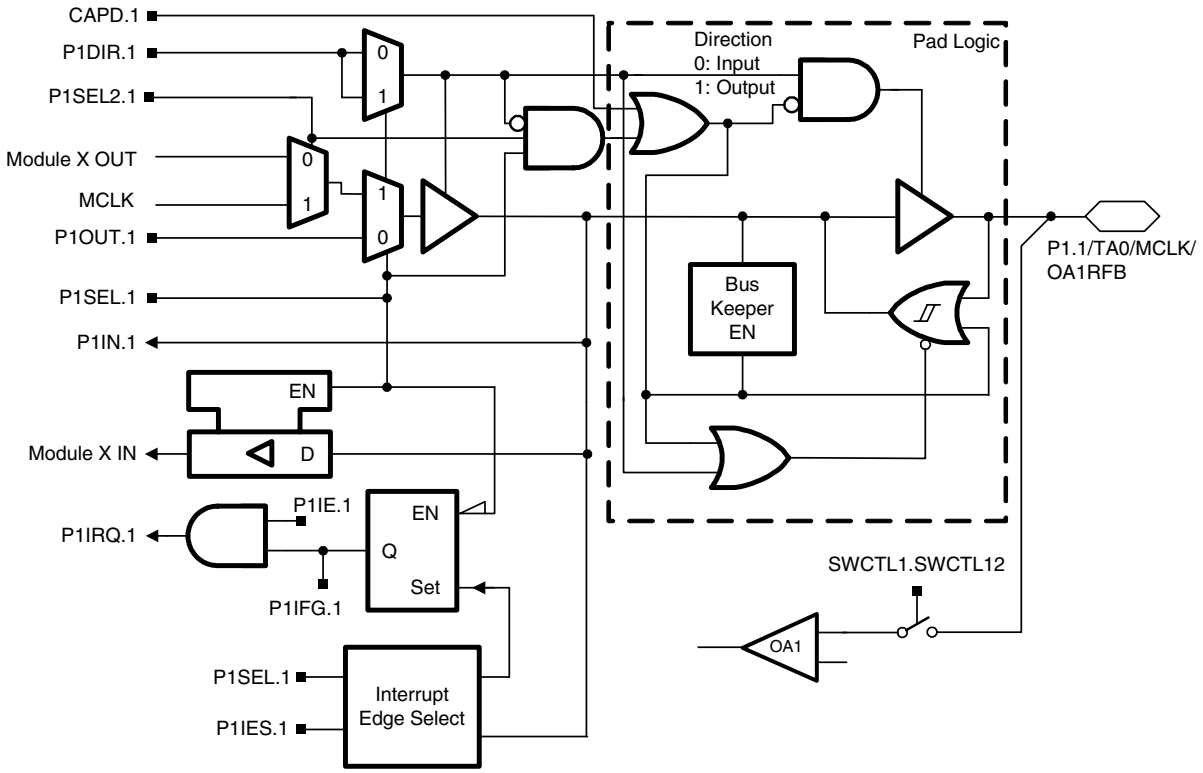
Port P1 (P1.0) pin functions

PIN NAME (P1.X)	X	FUNCTION	CONTROL BITS / SIGNALS			
			CAPD.x	P1DIR.x	P1SEL.x	P1SEL2.x
P1.0/TA0/OA0RFB	0	P1.x (I/O)	0	I: 0; O: 1	0	0
		Timer_A3.CCI0A	0	0	1	0
		Timer_A3.TA0	0	1	1	0
		OA0RFB	x	x	1	1

PRODUCT PREVIEW

APPLICATION INFORMATION

Port P1 pin schematic: P1.1, input/output with Schmitt trigger



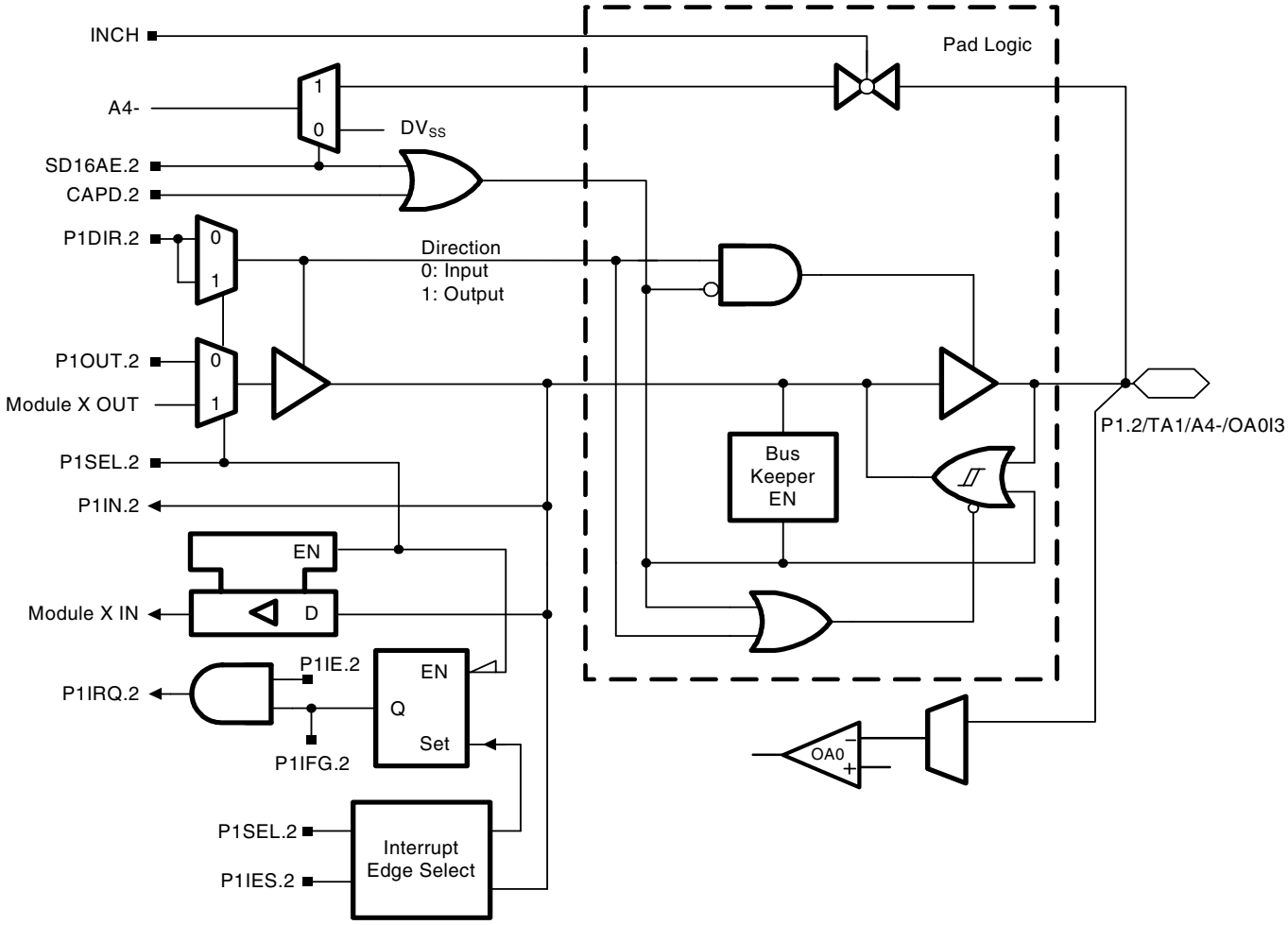
Port P1 (P1.1) pin functions

PIN NAME (P1.X)	X	FUNCTION	CONTROL BITS / SIGNALS			
			CAPD.x	P1DIR.x	P1SEL.x	P1SEL2.x
P1.1/TA0/MCLK OA1RFB	1	P1.x (I/O)	0	I: 0; O: 1	0	0
		Timer_A3.CCI0A	0	0	1	0
		Timer_A3.TA0	0	1	1	0
		OA1RFB	x	0	1	1
		MCLK	0	1	1	1

PRODUCT PREVIEW

APPLICATION INFORMATION

Port P1 pin schematic: P1.2 input/output with Schmitt trigger



Port P1 (P1.2) pin functions

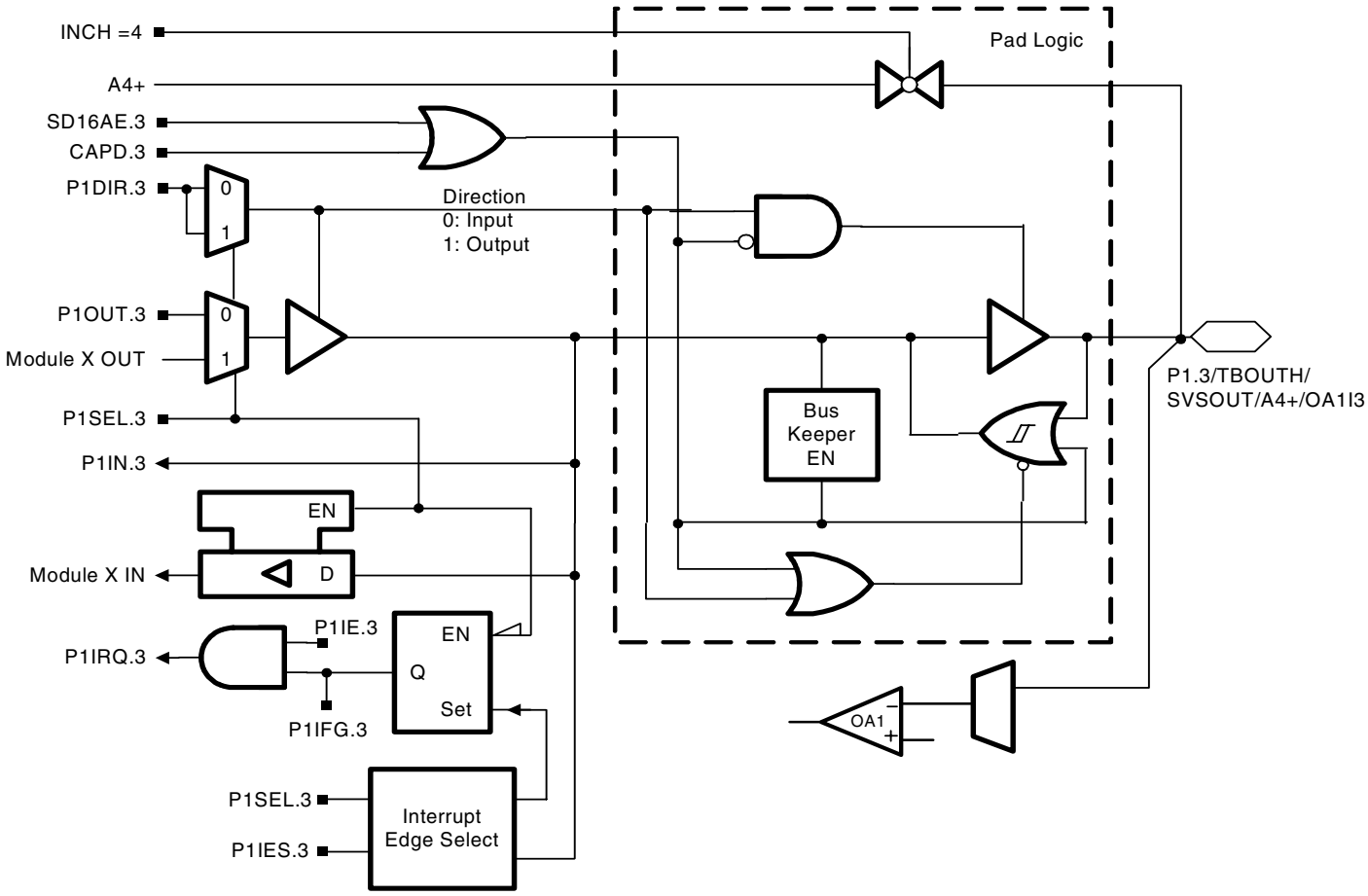
PIN NAME (P1.X)	X	FUNCTION	CONTROL BITS / SIGNALS				
			CAPD.x	P1DIR.x	P1SEL.x	P1SEL2.x=0 OAN (OA0)	P1SEL2.x=0 SD16AE.x
P1.2/TA1/A4-/OA0I3	2	P1.x (I/O)	0	I: 0; O: 1	0	xx	0
		Timer_A3.CCI1A	0	0	1	xx	0
		Timer_A3.TA1	0	1	1	xx	0
		A4-	x	x	x	xx	1
		OA0I3	x	x	x	10	1

NOTES: 1. x: Don't care

PRODUCT PREVIEW

APPLICATION INFORMATION

Port P1 pin schematic: P1.3, input/output with Schmitt trigger



Port P1 (P1.3) pin functions

PIN NAME (P1.X)	X	FUNCTION	CONTROL BITS / SIGNALS				
			CAPD.x	P1DIR.x	P1SEL.x	P1SEL2.x=0 OAN (OA1)	P1SEL2.x=0 SD16AE.x
P1.3/TBOUTH/ SVSOUT/A4+/OA1I3	3	P1.x (I/O)	0	I: 0; O: 1	0	xx	0
		TBOUTH	0	0	1	xx	0
		SVSOUT	0	1	1	xx	0
		A4+	x	x	x	xx	1
		OA1I3	x	x	x	10	1

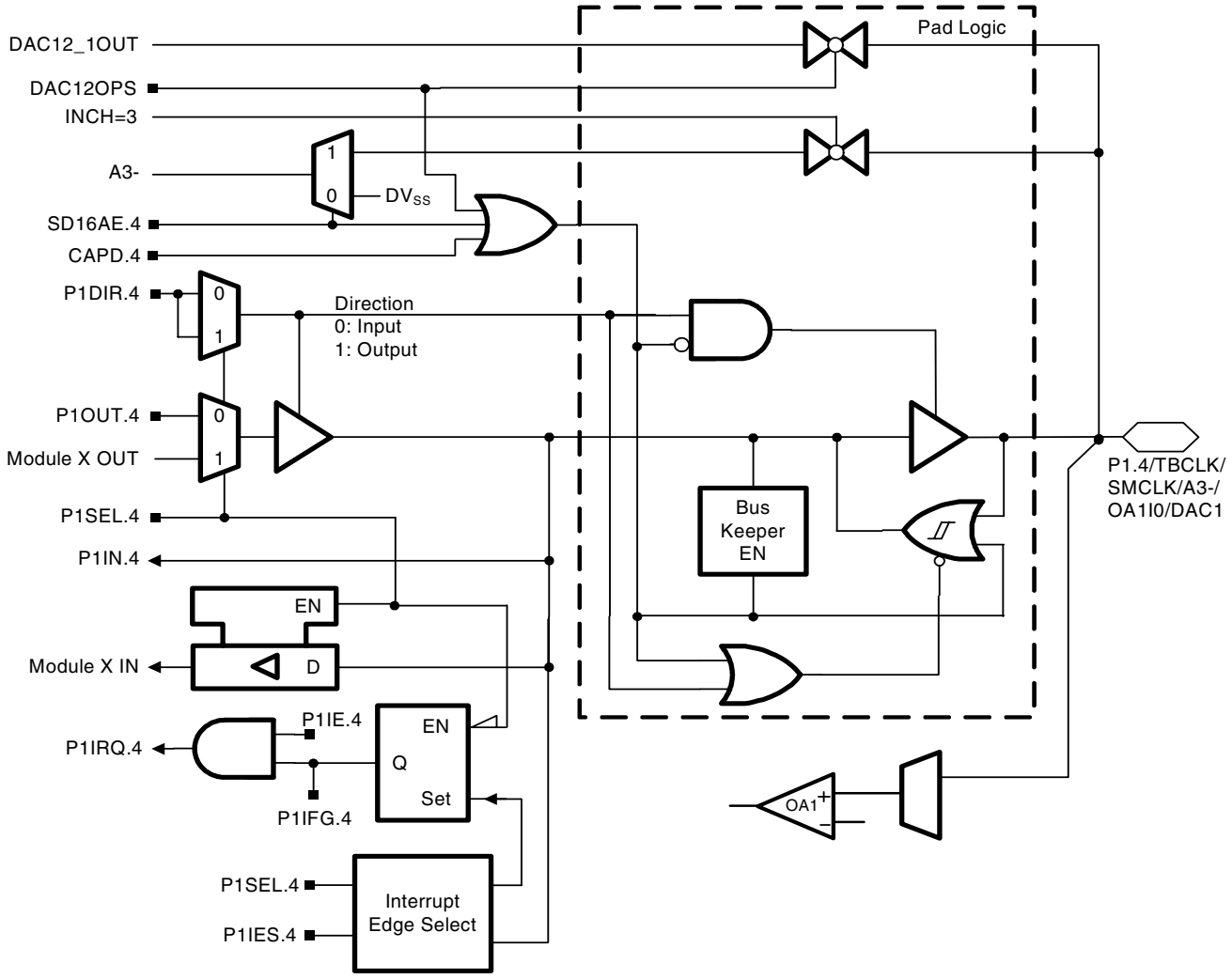
NOTES: 1. x: Don't care

PRODUCT PREVIEW

PRODUCT PREVIEW

APPLICATION INFORMATION

Port P1 pin schematic: P1.4, input/output with Schmitt trigger



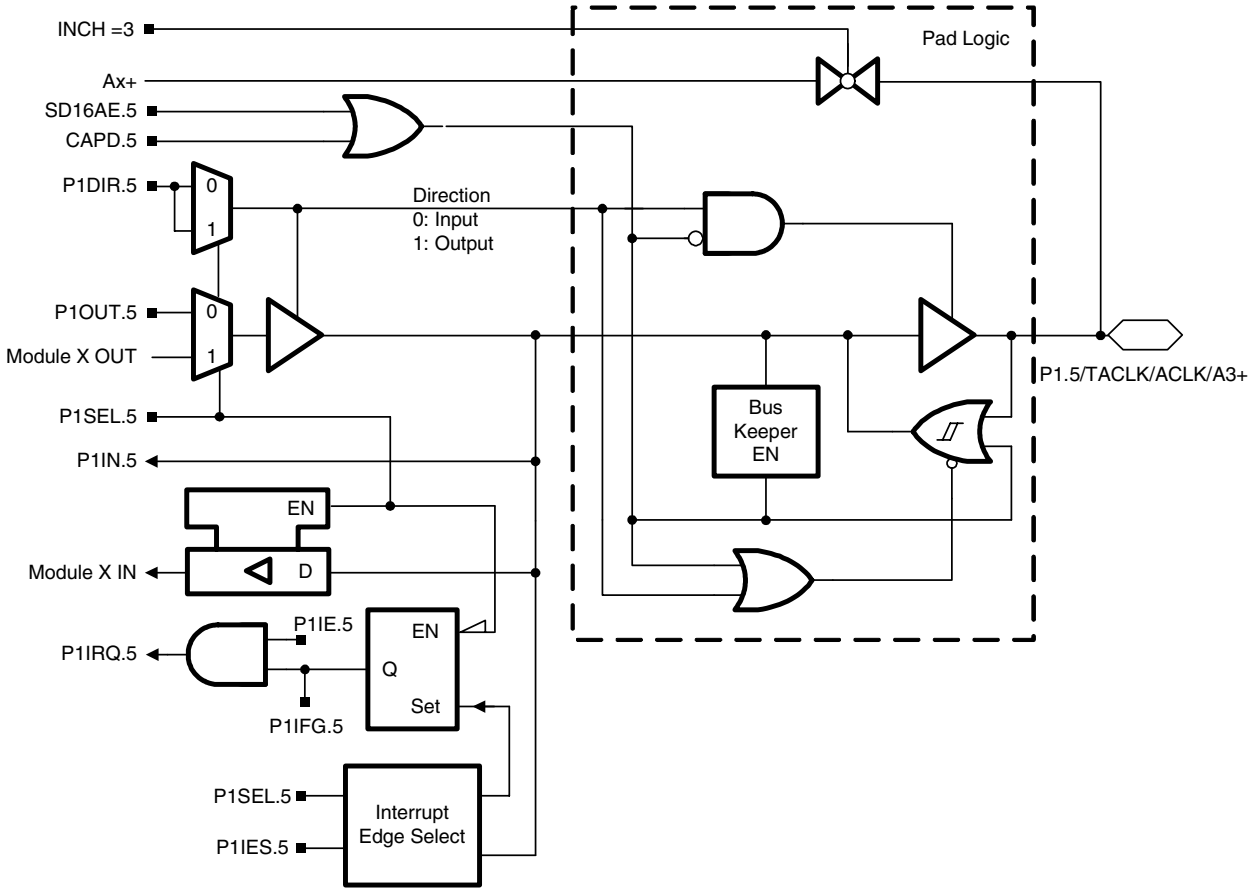
Port P1 (P1.4) pin functions

PIN NAME (P1.X)	X	FUNCTION	CONTROL BITS / SIGNALS					
			CAPD.x	P1DIR.x	P1SEL.x	P1SEL2.x=0 SD16AE.x	P1SEL2.x=0 OAP (OA1)	P1SEL2.x=0 DAC12OPS (DAC12_1)
P1.4TBCLK/SMCLK/ A3-/OA1I0/DAC1	4	P1.x (I/O)		I: 0; O: 1	0	0	xx	0
		TBCLK		0	1	0	xx	0
		SMCLK		1	1	0	xx	0
		A3-		x	x	1	xx	0
		OA1I0		x	x	1	00	0
		DAC1		x	x	x	xx	1

NOTES: 1. x: Don't care

APPLICATION INFORMATION

Port P1 pin schematic: P1.5, input/output with Schmitt trigger



Port P1 (P1.5) pin functions

PIN NAME (P1.X)	X	FUNCTION	CONTROL BITS / SIGNALS			
			CAPD.x	P1DIR.x	P1SEL.x	P1SEL2.x=0 SD16AE.x
P1.5/TACLK/ACLK/ A3+	5	P1.x (I/O)	0	I: 0; O: 1	0	0
		TACLK	0	0	1	0
		ACLK	0	1	1	0
		A3+	x	x	x	1

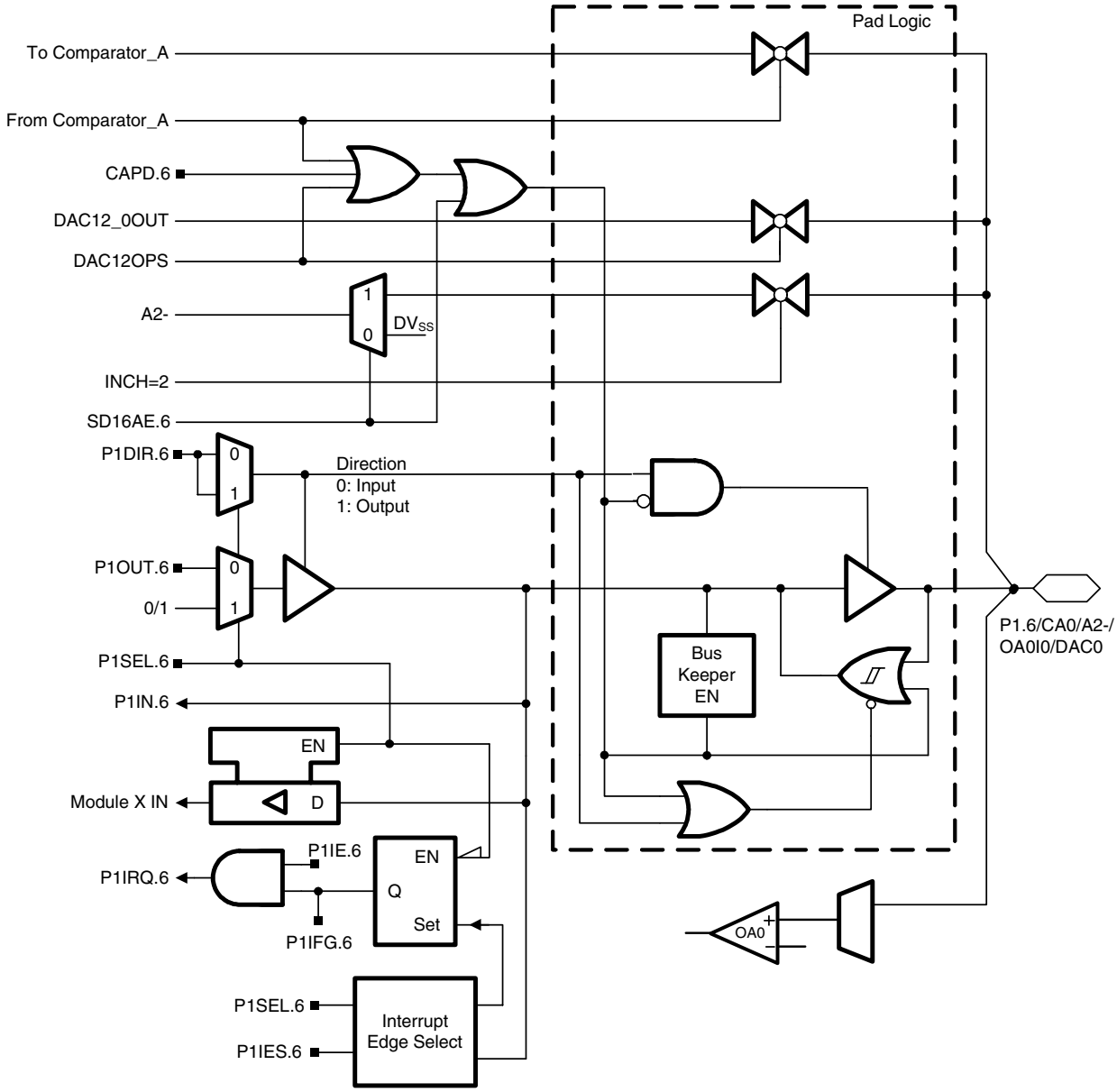
NOTES: 1. x: Don't care

PRODUCT PREVIEW

PRODUCT PREVIEW

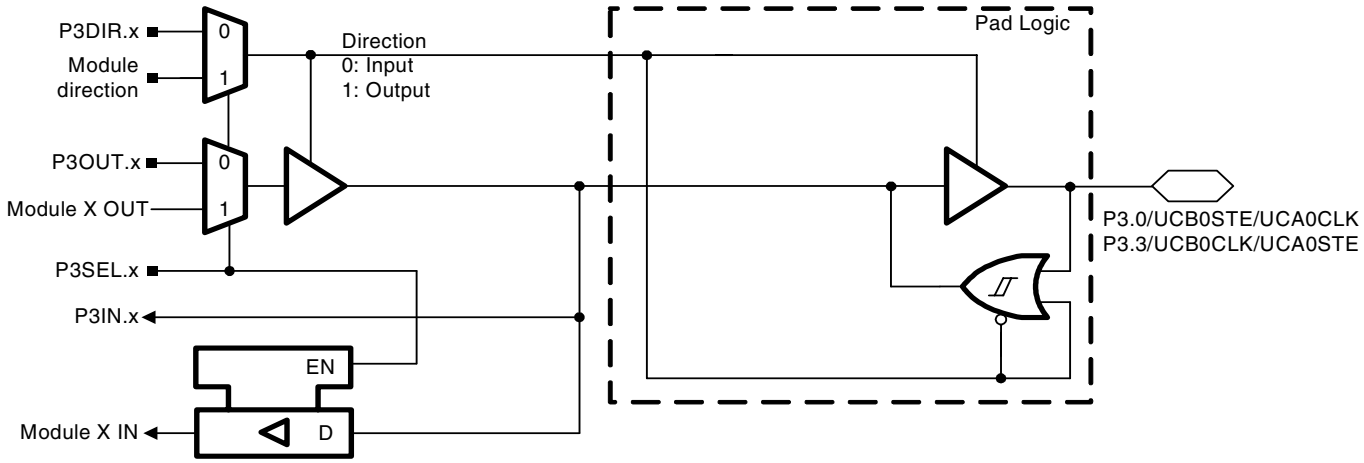
APPLICATION INFORMATION

Port P1 pin schematic: P1.6, input/output with Schmitt trigger



APPLICATION INFORMATION

Port P3 pin schematic: P3.0 and P3.3, input/output with Schmitt trigger



Port P3 (P3.0 and P3.3) pin functions

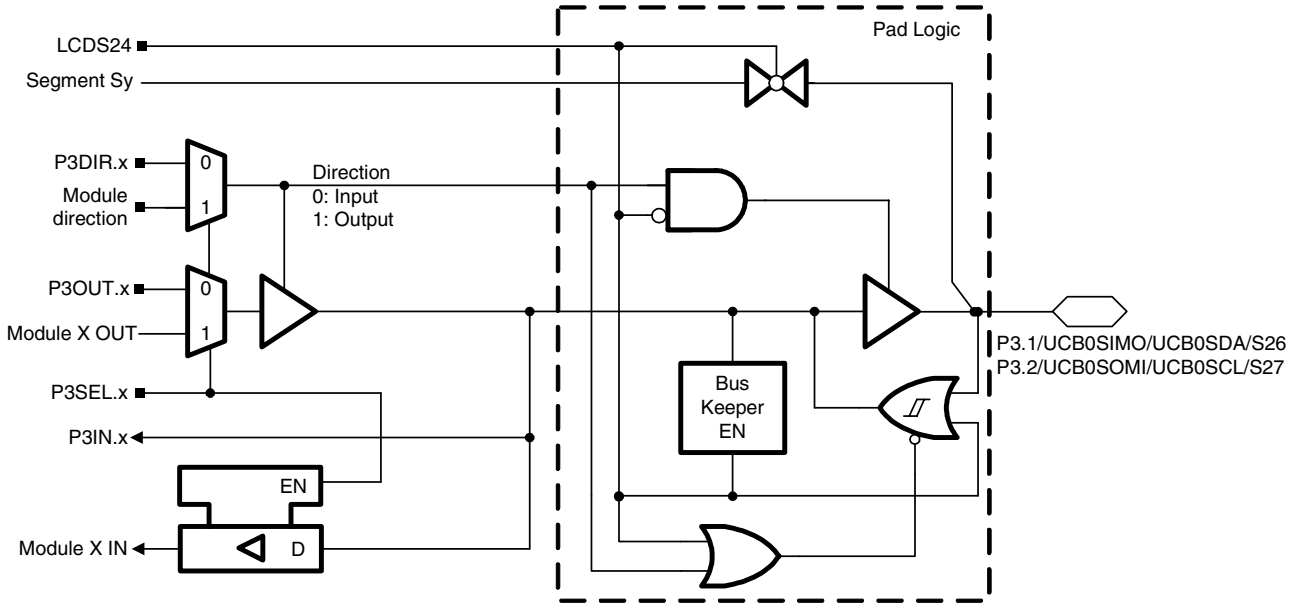
PIN NAME (P3.X)	X	FUNCTION	CONTROL BITS / SIGNALS	
			P3DIR.x	P3SEL.x
P3.0/UCB0STE/ UCA0CLK	0	P3.x (I/O)	I: 0; O: 1	0
		UCB0STE/UCA0CLK (see Note 2)	x	1
P3.3/UCB0CLK/ UCA0STE	3	P3.x (I/O)	I: 0; O: 1	0
		UCB0CLK/UCA0STE (see Note 2)	x	1

NOTES: 1. x: Don't care
2. The pin direction is controlled by the USCI module.

PRODUCT PREVIEW

APPLICATION INFORMATION

Port P3 pin schematic: P3.1 and P3.2, input/output with Schmitt trigger



Port P3 (P3.1 and P3.2) pin functions

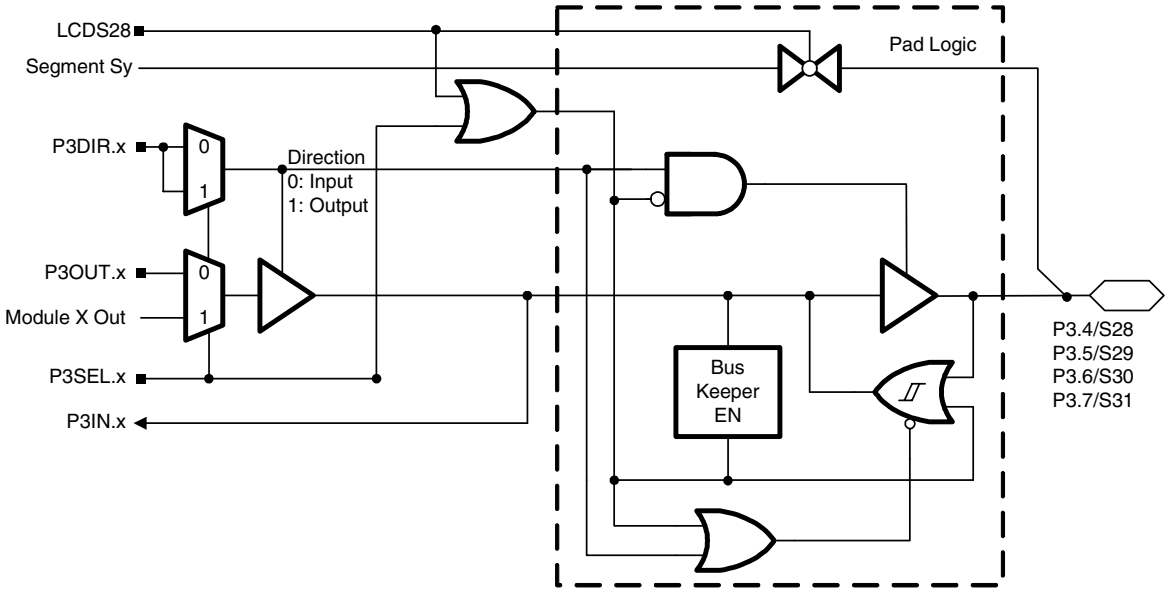
PIN NAME (P3.X)	X	FUNCTION	CONTROL BITS / SIGNALS		
			P3DIR.x	P3SEL.x	LCDS24
P3.1/UCB0SIMO/ UCB0SDA/S26	1	P3.x (I/O)	I: 0; O: 1	0	0
		UCB0SIMO/UCB0SDA (see Notes 2 and 3)	x	1	0
		S26	x	x	1
P3.2/UCB00SOMI/ UCB0SCL/S27	2	P3.x (I/O)	I: 0; O: 1	0	0
		UCB0SOMI/UCB0SCL (see Notes 2 and 3)	x	1	0
		S27	x	x	1

NOTES: 1. x: Don't care
2. The pin direction is controlled by the USCI module.
3. In case the I2C functionality is selected the output drives only the logical 0 to V_{SS} level.

PRODUCT PREVIEW

APPLICATION INFORMATION

Port P3 pin schematic: P3.4 to P3.7, input/output with Schmitt trigger



Port P3 (P3.4 to P3.7) pin functions

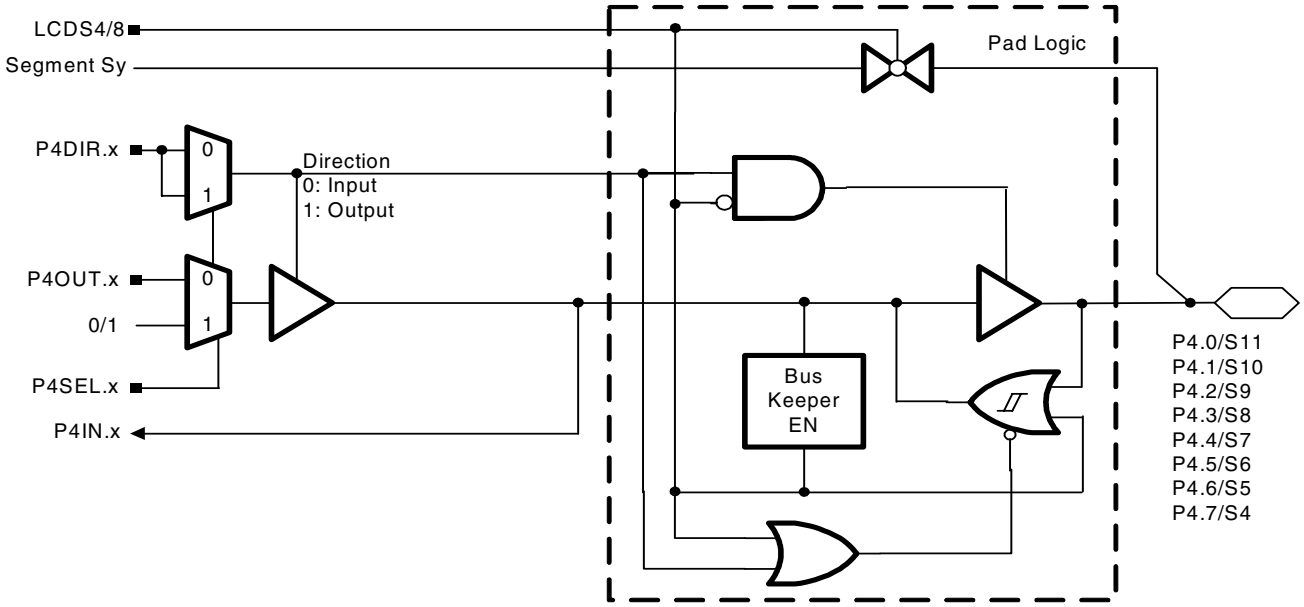
PIN NAME (P3.X)	X	FUNCTION	CONTROL BITS / SIGNALS		
			P3DIR.x	P3SEL.x	LCDS28
P3.4/S28	4	P3.x (I/O)	I: 0; O: 1	0	0
		S28	x	x	1
P3.5/S29	5	P3.x (I/O)	I: 0; O: 1	0	0
		S29	x	x	1
P3.6/S30	6	P3.x (I/O)	I: 0; O: 1	0	0
		S30	x	x	1
P3.7/S31	7	P3.x (I/O)	I: 0; O: 1	0	0
		S31	x	x	1

NOTES: 1. x: Don't care

PRODUCT PREVIEW

APPLICATION INFORMATION

Port P4 pin schematic: P4.0 to P4.7, input/output with Schmitt trigger



Port P4 (P4.0 and P4.7) pin functions

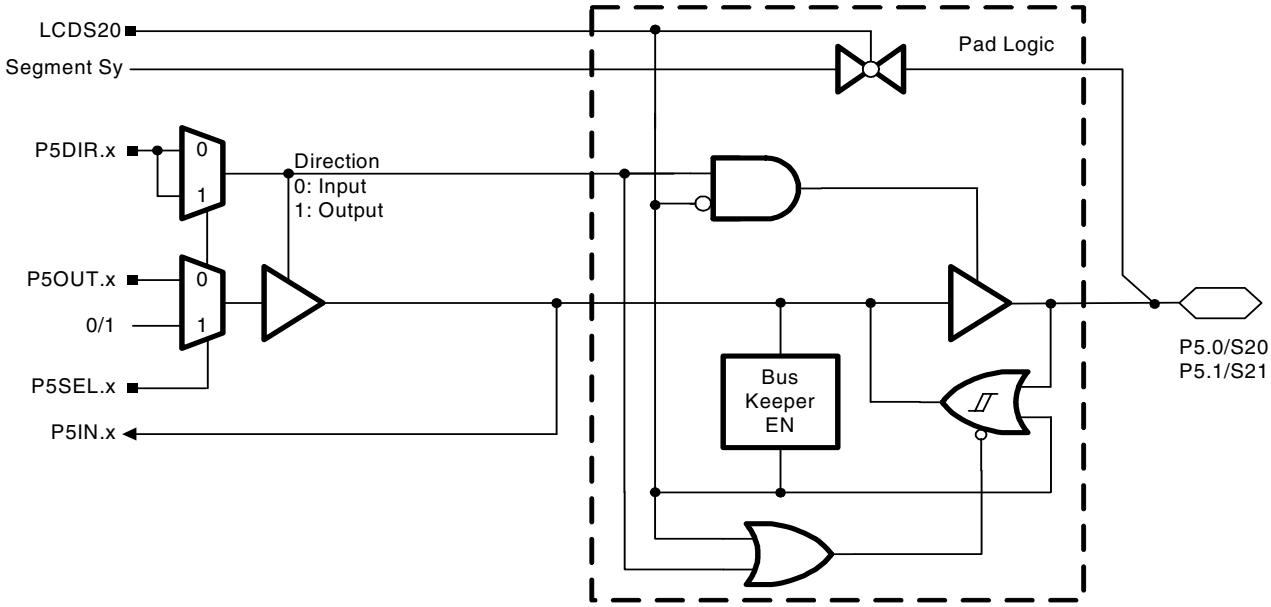
PIN NAME (P4.X)	X	FUNCTION	CONTROL BITS / SIGNALS		
			P4DIR.x	P4SEL.x	LCDS4/8
P4.0/S11	0	P4.x (I/O)	I: 0; O: 1	0	0 (LCDS8)
		S11	x	x	1 (LCDS8)
P4.1/S10	1	P4.x (I/O)	I: 0; O: 1	0	0 (LCDS8)
		S10	x	x	1 (LCDS8)
P4.2/S9	2	P4.x (I/O)	I: 0; O: 1	0	0 (LCDS8)
		S9	x	x	1 (LCDS8)
P4.3/S8	3	P4.x (I/O)	I: 0; O: 1	0	0 (LCDS8)
		S8	x	x	1 (LCDS8)
P4.4/S7	4	P4.x (I/O)	I: 0; O: 1	0	0 (LCDS4)
		S7	x	x	1 (LCDS4)
P4.5/S6	5	P4.x (I/O)	I: 0; O: 1	0	0 (LCDS4)
		S6	x	x	1 (LCDS4)
P4.6/S5	6	P4.x (I/O)	I: 0; O: 1	0	0 (LCDS4)
		S5	x	x	1 (LCDS4)
P4.7/S4	7	P4.x (I/O)	I: 0; O: 1	0	0 (LCDS4)
		S4	x	x	1 (LCDS4)

NOTES: 1. x: Don't care

PRODUCT PREVIEW

APPLICATION INFORMATION

Port P5 pin schematic: P5.0 and P5.1, input/output with Schmitt trigger



Port P5 (P5.0 and P5.1) pin functions

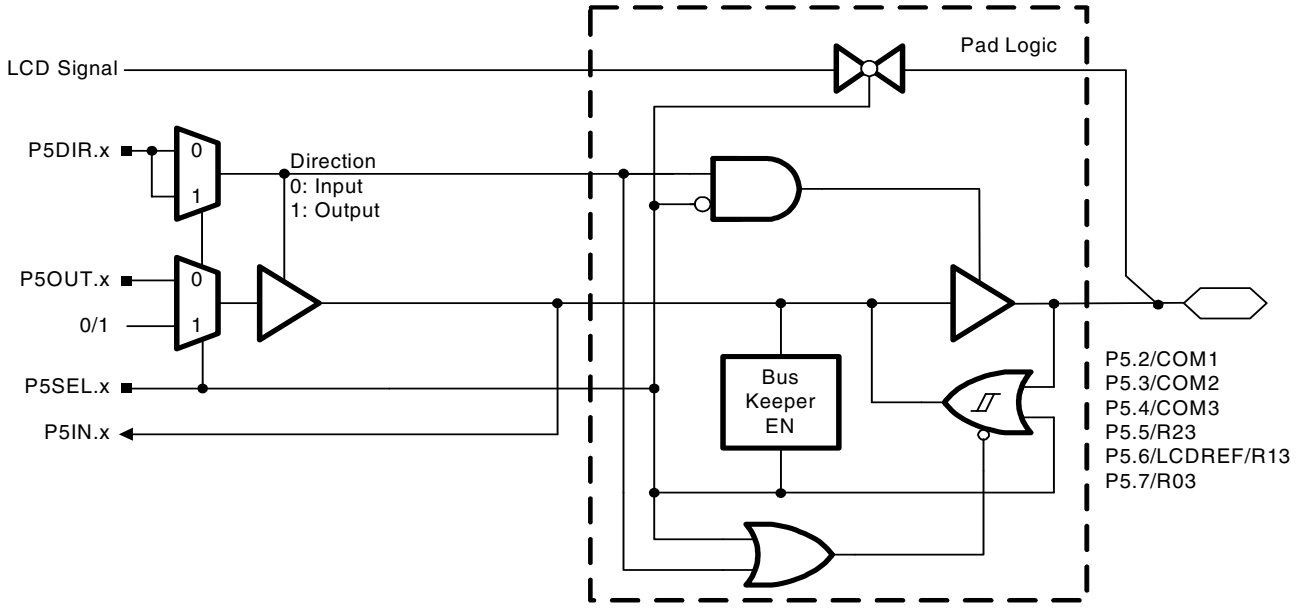
PIN NAME (P5.X)	X	FUNCTION	CONTROL BITS / SIGNALS		
			P5DIR.x	P5SEL.x	LCDS20
P5.0/S20	0	P5.x (I/O)	I: 0; O: 1	0	0
		S20	x	x	1
P5.1/S21	1	P5.x (I/O)	I: 0; O: 1	0	0
		S21	x	x	1

NOTES: 1. x: Don't care

PRODUCT PREVIEW

APPLICATION INFORMATION

Port P5 pin schematic: P5.2 to P5.7, input/output with Schmitt trigger



Port P5 (P5.2 to P5.7) pin functions

PIN NAME (P5.X)	X	FUNCTION	CONTROL BITS / SIGNALS	
			P5DIR.x	P5SEL.x
P5.2/COM1	2	P5.x (I/O)	I: 0; O: 1	0
		COM1	x	1
P5.3/COM2	3	P5.x (I/O)	I: 0; O: 1	0
		COM2	x	1
P5.4/COM3	4	P5.x (I/O)	I: 0; O: 1	0
		COM3	x	1
P5.5/R23	5	P5.x (I/O)	I: 0; O: 1	0
		R23	x	1
P5.6/LCDREF/R13	6	P5.x (I/O)	I: 0; O: 1	0
		R13 or LCDREF	x	1
P5.7/R03	7	P5.x (I/O)	I: 0; O: 1	0
		R03	x	1

NOTES: 1. x: Don't care

PRODUCT PREVIEW

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)
MSP430FG477IPNR	PREVIEW	LQFP	PN	80	1000	TBD	Call TI	Call TI
MSP430FG477IZQWR	PREVIEW	BGA MICROSTAR JUNIOR	ZQW	113	2500	TBD	Call TI	Call TI
MSP430FG478IPNR	PREVIEW	LQFP	PN	80	1000	TBD	Call TI	Call TI
MSP430FG478IZQWR	PREVIEW	BGA MICROSTAR JUNIOR	ZQW	113	2500	TBD	Call TI	Call TI
MSP430FG479IPNR	PREVIEW	LQFP	PN	80	1000	TBD	Call TI	Call TI
MSP430FG479IZQWR	PREVIEW	BGA MICROSTAR JUNIOR	ZQW	113	2500	TBD	Call TI	Call TI

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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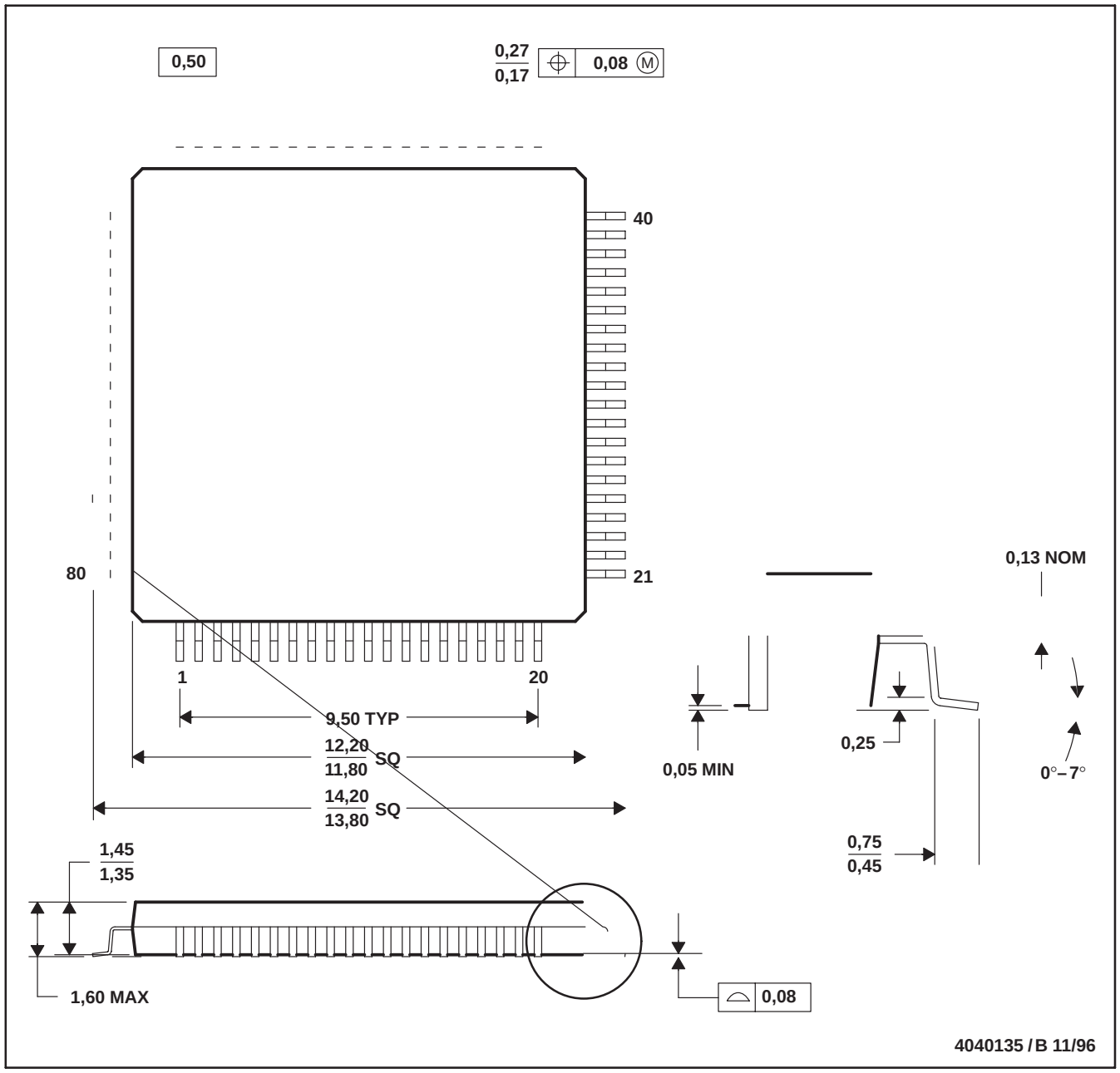
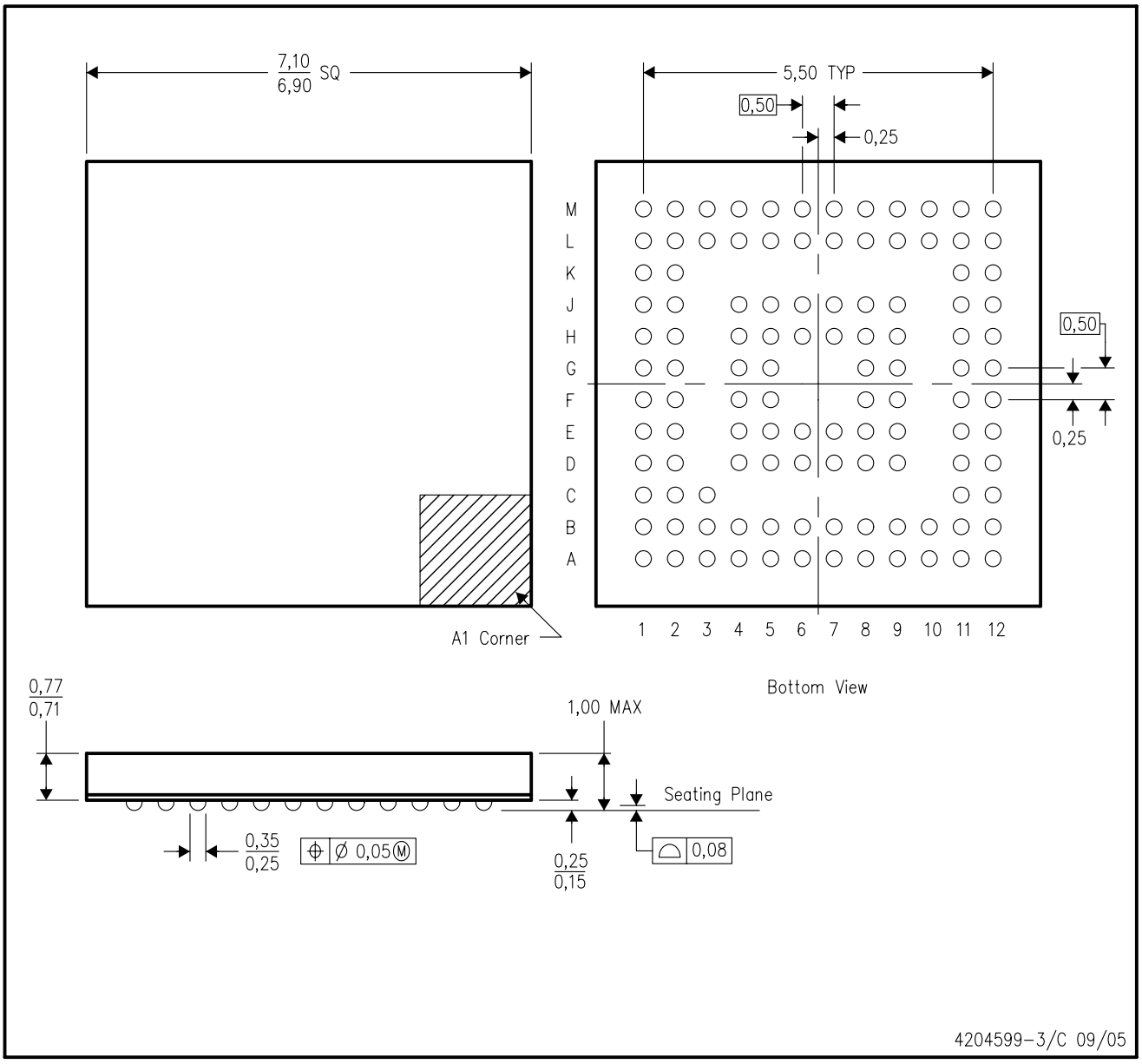
MTQF010A – JANUARY 1995 – REVISED DECEMBER 1996

PN (S-PQFP-G80) **PLASTIC QUAD FLATPACK**



NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS-026

ZQW (S–PBGA–N113) PLASTIC BALL GRID ARRAY



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Falls within JEDEC MO–225
D. This is a lead–free solder ball design.

- **Low Supply-Voltage Range: 1.8 V to 3.6 V**
- **Ultra-Low Power Consumption:**
  Active Mode: 262 μA at 1 MHz, 2.2 V
  Standby Mode: 1.1 μA
  Off Mode (RAM Retention): 0.1 μA
- **Five Power-Saving Modes**
- **Wake-Up From Standby Mode in Less Than 6 μs**
- **16-Bit RISC Architecture, 125-ns Instruction Cycle Time**
- **16-Bit Sigma-Delta Analog-to-Digital (A/D) Converter With Internal Reference and Five Differential Analog Inputs**
- **Dual 12-Bit Digital-to-Analog (D/A) Converter**
- **Dual Configurable Operational Amplifiers**
- **16-Bit Timer_A With Three Capture/Compare Registers**
- **16-Bit Timer_B With Three Capture/Compare-With-Shadow Registers**
- **Two Universal Serial Communication Interfaces (USCI)**
  USCI_A0
  - **Enhanced UART Supporting Auto-Baudrate Detection**
  - **IrDA Encoder and Decoder**
  - **Synchronous SPI**

  USCI_B0
  - **I^2C™**
  - **Synchronous SPI**
- **Integrated LCD Driver With Contrast Control for Up to 128 Segments**
- **Brownout Detector**
- **Basic Timer With Real-Time Clock Feature**
- **Supply Voltage Supervisor/Monitor With Programmable Level Detection**
- **On-Chip Comparator**
- **Serial Onboard Programming, No External Programming Voltage Needed Programmable Code Protection by Security Fuse**
- **Bootstrap Loader**
- **On-Chip Emulation Module**
- **Family Members Include**
  MSP430FG477: 32KB+256B Flash Memory 2KB RAM
  MSP430FG478: 48KB+256B Flash Memory 2KB RAM
  MSP430FG479: 60KB+256B Flash Memory 2KB RAM
- **Available in 113-Ball BGA (see Available Options) and 80-Pin QFP Package**
- **For Complete Module Descriptions, See the *MSP430x4xx Family User's Guide*, Literature Number SLAU056**

PRODUCT PREVIEW

description

The Texas Instruments MSP430 family of ultralow-power microcontrollers consists of several devices featuring different sets of peripherals targeted for various applications. The architecture, combined with five low-power modes, is optimized to achieve extended battery life in portable measurement applications. The device features a powerful 16-bit RISC CPU, 16-bit registers, and constant generators that contribute to maximum code efficiency. The digitally controlled oscillator (DCO) allows wake-up from low-power modes to active mode in less than 6 μs.

The MSP430FG47x is a microcontroller configuration with two 16-bit timers, a basic timer with a real-time clock, a high performance 16-bit sigma-delta A/D converter, dual 12-bit D/A converters, two configurable operational amplifiers, two universal serial communication interface, 48 I/O pins, and a liquid crystal display driver.

Typical applications for this device include analog and digital sensor systems, digital motor control, remote controls, thermostats, digital timers, hand-held meters, etc.

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage. ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications. These devices have limited built-in ESD protection.

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

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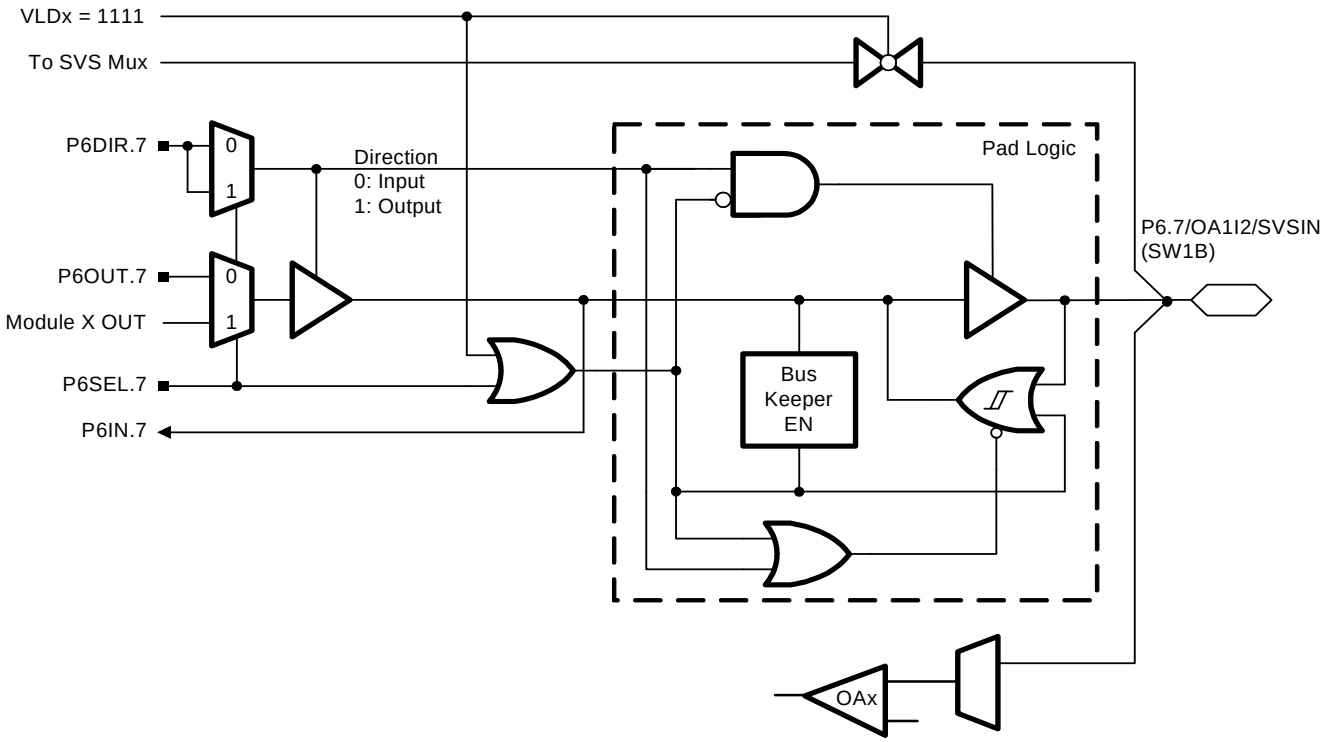
APPLICATION INFORMATION

Port P6 pin schematic: P6.7, input/output with Schmitt trigger



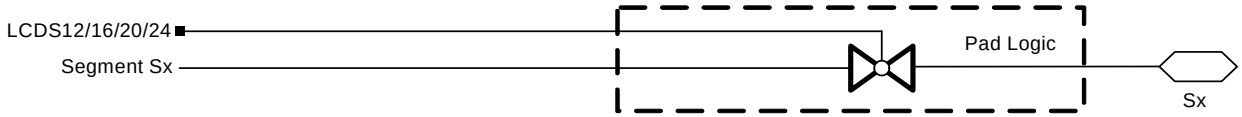
Port P6 (P6.7) pin functions

PIN NAME (P6.X)	X	FUNCTION	CONTROL BITS / SIGNALS		
			P6DIR.x	P6SEL.x	VLDx
P6.7/OA1I2/SVSIN	7	P6.x (I/O)	I: 0, O: 1	0	x
		OA1I2	x	1	x
		SVSIN	x	1	1111

NOTES: 1. x: Don t care.

APPLICATION INFORMATION

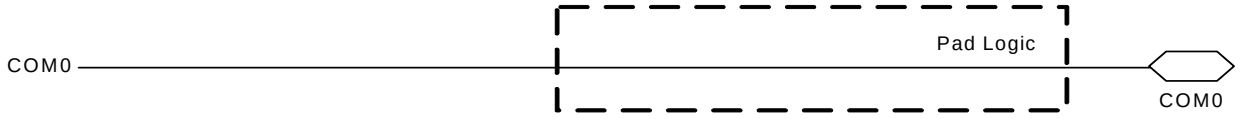
Segment pin schematic: Sx, dedicated Segment Pins



Sx pin functions

PIN NAME	X	FUNCTION	CONTROL BITS / SIGNALS
			LCDSy
Sx	12	Sx	1 (LCDS12)
		3-state	0 (LCDS12)
Sx	13	Sx	1 (LCDS12)
		3-state	0 (LCDS12)
Sx	14	Sx	1 (LCDS12)
		3-state	0 (LCDS12)
Sx	15	Sx	1 (LCDS12)
		3-state	0 (LCDS12)
Sx	16	Sx	1 (LCD16)
		3-state	0 (LCD16)
Sx	17	Sx	1 (LCD16)
		3-state	0 (LCD16)
Sx	18	Sx	1 (LCD16)
		3-state	0 (LCD16)
Sx	19	Sx	1 (LCDS16)
		3-state	0 (LCDS16)
Sx	22	Sx	1 (LCDS20)
		3-state	0 (LCDS20)
Sx	23	Sx	1 (LCDS20)
		3-state	0 (LCDS20)
Sx	24	Sx	1 (LCDS24)
		3-state	0 (LCDS24)
Sx	25	Sx	1 (LCDS24)
		3-state	0 (LCDS24)

Segment pin schematic: COM0, dedicated COM0 pin

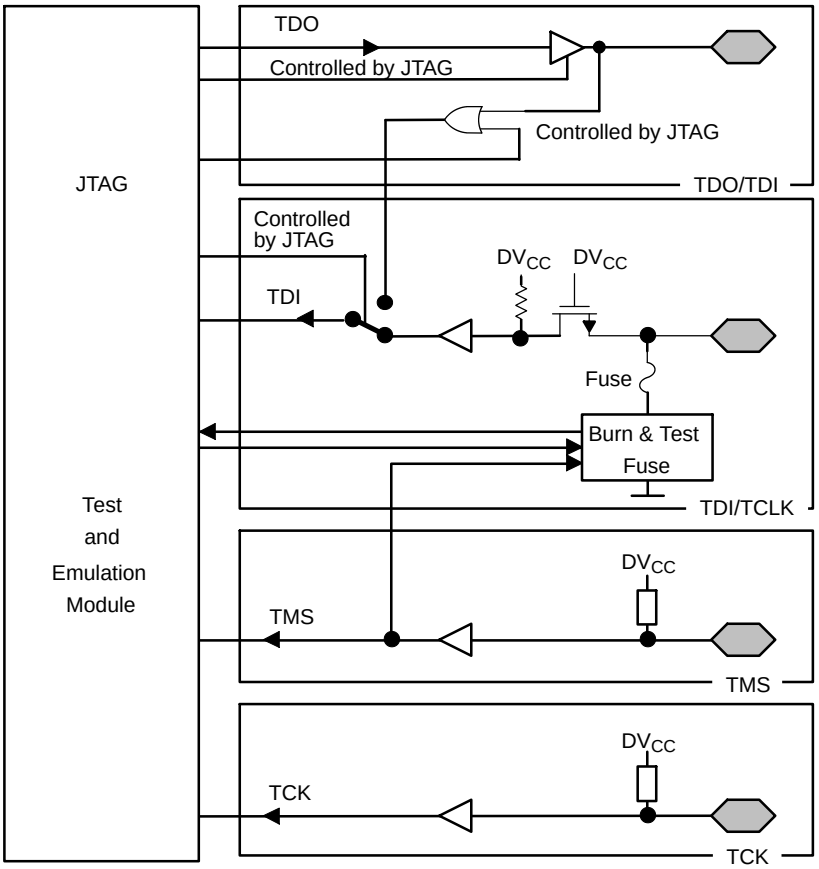


Sx pin functions

PIN NAME	X	FUNCTION
COM0	–	COM0

APPLICATION INFORMATION

JTAG pins: TMS, TCK, TDI/TCLK, TDO/TD I, input/output with Schmitt trigger



During Programming Activity and During Blowing of the Fuse, Pin TDO/TDI Is Used to Apply the Test Input Data for JTAG Circuitry

JTAG fuse check mode

For details on the JTAG fuse check mode, see the MSP430 Memory Programming User's Guide (SLAU265) chapter Fuse Check and Reset of the JTAG State Machine (TAP Controller) .

Data Sheet Revision History

LITERATURE NUMBER	SUMMARY
SLAS580	Product Preview release
SLAS580A	Changes throughout to update Product Preview
SLAS580B	Production Data release
SLAS580C	In recommended operating conditions table, changed maximum LFXT1 crystal frequency, $f_{(LFXT1)}$, with XT1 selected from 8 MHz to 6 MHz (page 24)
SLAS580D	Changed limits on $t_{d(SVSon)}$ parameter (page 32) Corrected measurement pin name for Duty cycle, LF mode parameter (page 37)

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/ Ball Finish	MSL Peak Temp (3)	Samples (Requires Login)
MSP430FG477IPN	ACTIVE	LQFP	PN	80	119	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	
MSP430FG477IPNR	ACTIVE	LQFP	PN	80	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	
MSP430FG477IZQW	ACTIVE	BGA MICROSTAR JUNIOR	ZQW	113	250	Green (RoHS & no Sb/Br)	SNAGCU	Level-3-260C-168 HR	
MSP430FG477IZQWR	ACTIVE	BGA MICROSTAR JUNIOR	ZQW	113	2500	Green (RoHS & no Sb/Br)	SNAGCU	Level-3-260C-168 HR	
MSP430FG478IPN	ACTIVE	LQFP	PN	80	119	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	
MSP430FG478IPNR	ACTIVE	LQFP	PN	80	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	
MSP430FG478IZQW	ACTIVE	BGA MICROSTAR JUNIOR	ZQW	113	250	Green (RoHS & no Sb/Br)	SNAGCU	Level-3-260C-168 HR	
MSP430FG478IZQWR	ACTIVE	BGA MICROSTAR JUNIOR	ZQW	113	2500	Green (RoHS & no Sb/Br)	SNAGCU	Level-3-260C-168 HR	
MSP430FG479IPN	ACTIVE	LQFP	PN	80	119	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	
MSP430FG479IPNR	ACTIVE	LQFP	PN	80	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	
MSP430FG479IZQW	ACTIVE	BGA MICROSTAR JUNIOR	ZQW	113	250	Green (RoHS & no Sb/Br)	SNAGCU	Level-3-260C-168 HR	
MSP430FG479IZQWR	ACTIVE	BGA MICROSTAR JUNIOR	ZQW	113	2500	Green (RoHS & no Sb/Br)	SNAGCU	Level-3-260C-168 HR	

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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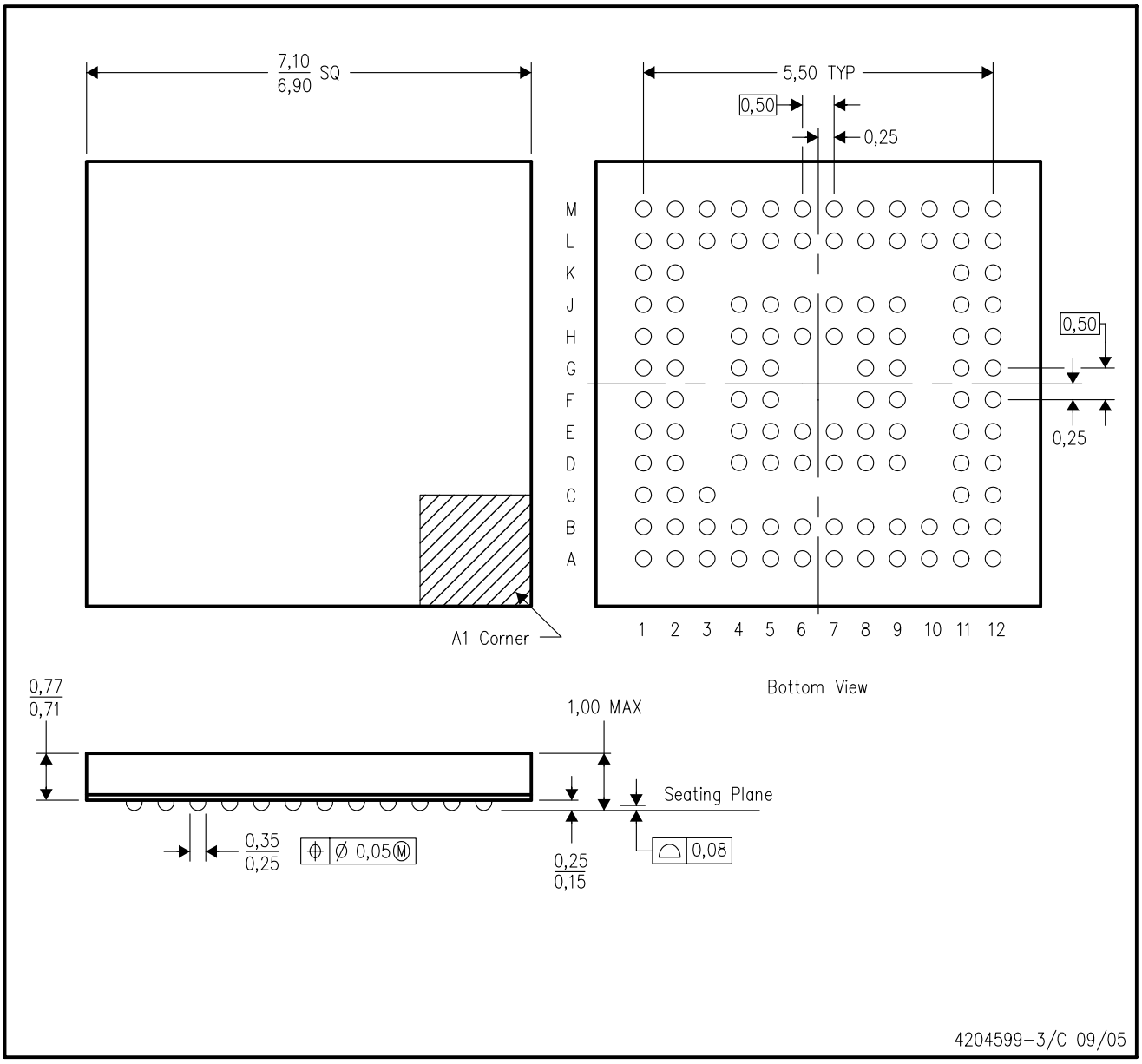
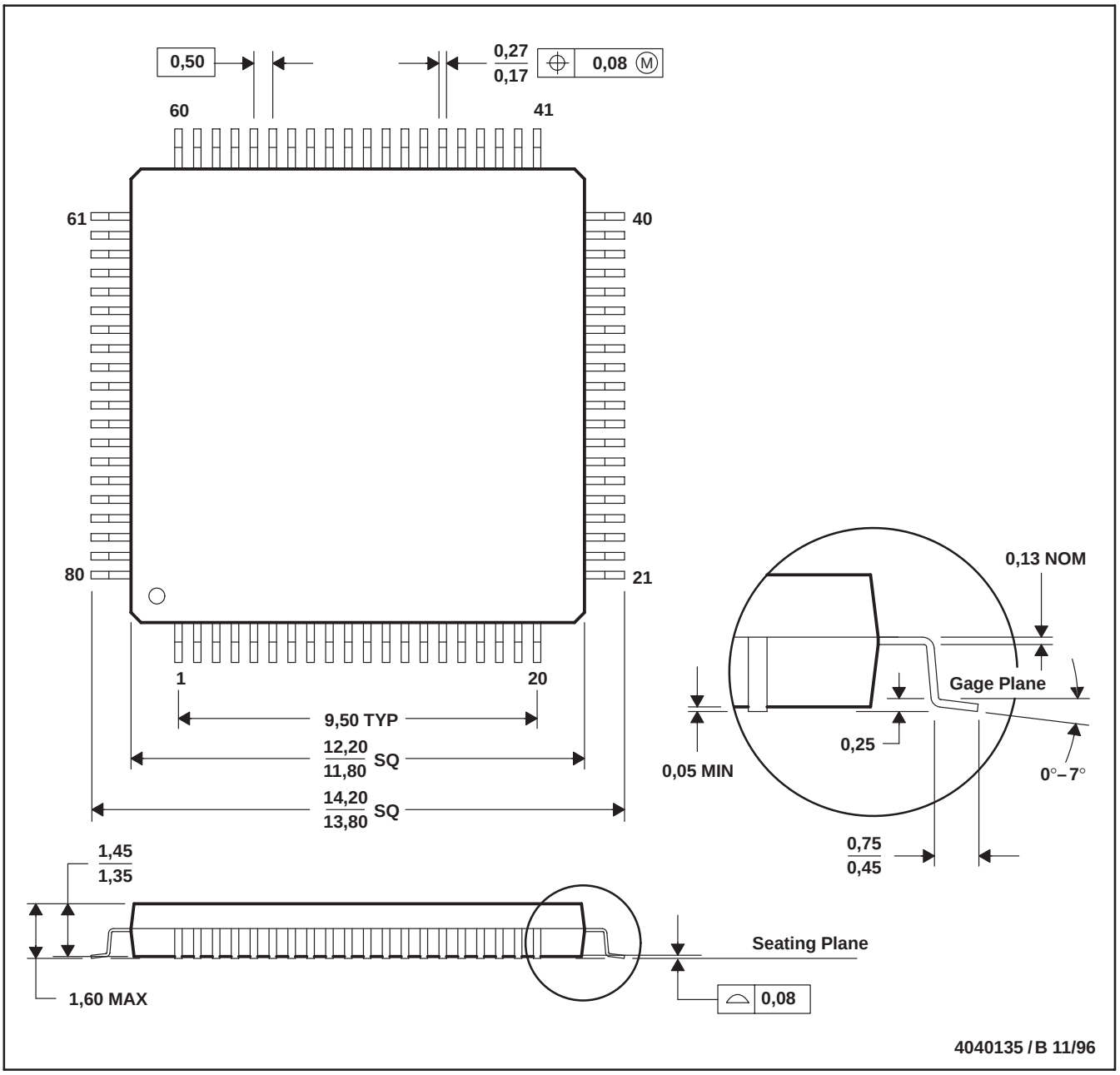
ZQW (S–PBGA–N113) PLASTIC BALL GRID ARRAY



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Falls within JEDEC MO–225
D. This is a lead–free solder ball design.

MTQF010A – JANUARY 1995 – REVISED DECEMBER 1996

PN (S-PQFP-G80) **PLASTIC QUAD FLATPACK**



NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS-026

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