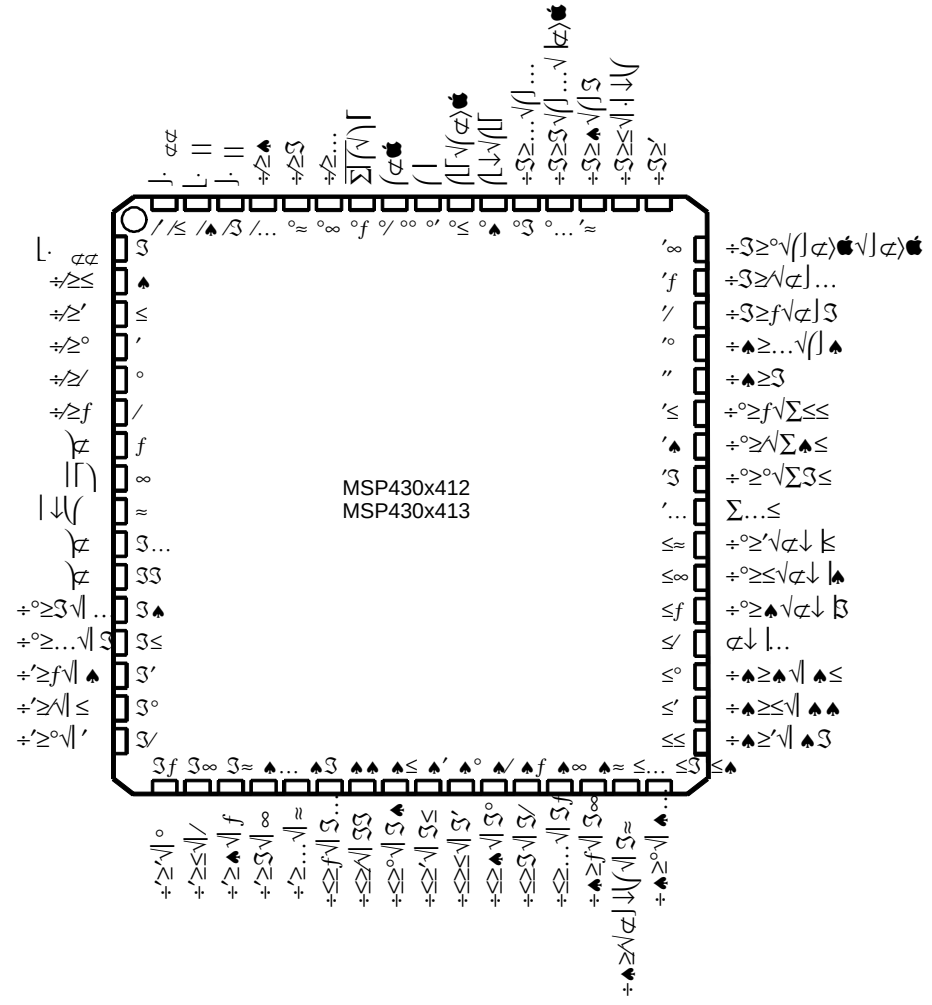
AVAILABLE OPTIONS

T_A	PACKAGED DEVICES	
	PLASTIC 64-PIN QFP (PM)	PLASTIC 64-PIN QFN (RTD/RGC)

pin designation MSP430x412, MSP430x413



electrical characteristics over recommended operating free-air temperature (unless otherwise noted) (continued)

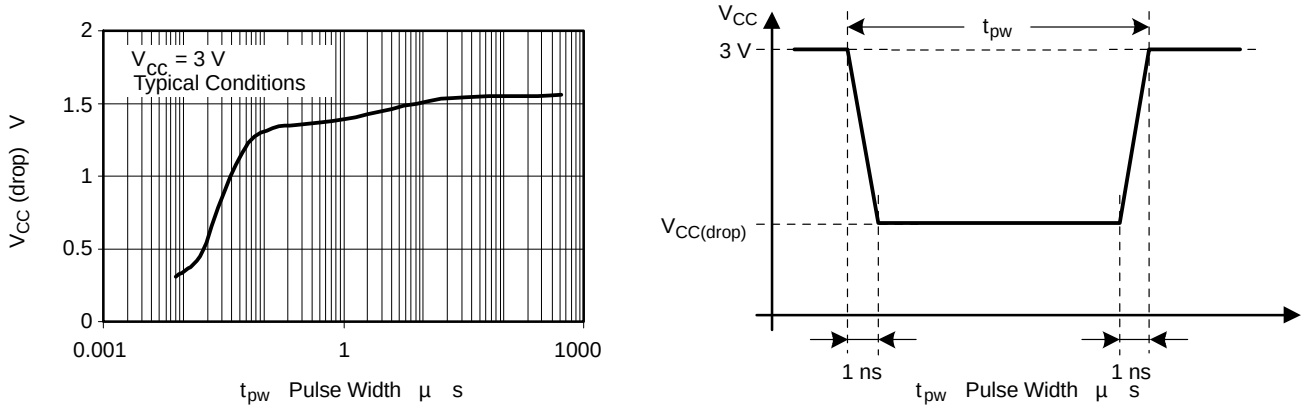


Figure 15. $V_{CC(drop)}$ Level With a Square Voltage Drop to Generate a POR/Brownout Signal

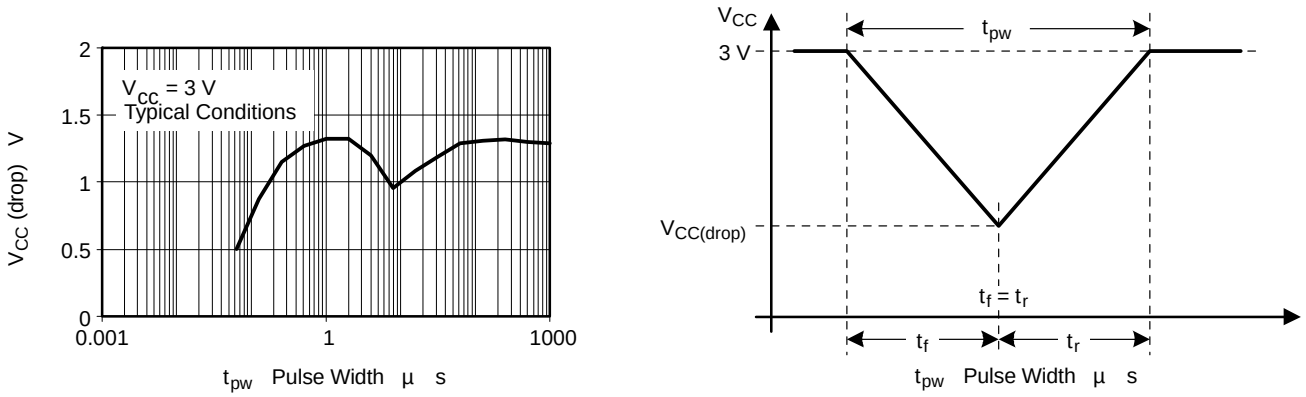


Figure 16. $V_{CC(drop)}$ Level With a Triangle Voltage Drop to Generate a POR/Brownout Signal

SVS (supply voltage supervisor/monitor) (MSP430x412, MSP430x413 only) (see Notes 1 and 2)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
⌠∂⟨⌡·⌡Σ®	⌡·⌡	∂· ⊄⊄√∂⌡ ⌈≤… ·√∝♣ ⟨♣↔↔ ⟩↵⌡↔ ♠®	°		ℑ°…	µ♣
		∂· ⊄⊄√∂⌡ ≤… ·√∝♣ ⟨♣↔↔ ⟩↵⌡↔ ♠®			♠……	µ♣
⌠∂⟨⌡·⌡⊂↵®		⌡·⌡↵⊇″ ♣•}⌡⊂⌡⊗♦↵∝ … ⌡↵ ℑ″⊄⊄ ↑ ≤ · ⟨♣↔↔ ⟩↵⌡↔ ♠®	♠…		ℑ°…	µ♣
· ⟨⌡·⌡♣⌡⊆♦⌡®		∂· ⊄⊄√∂⌡ ≤ ·√♣ ⟨♣↔↔ ⌈}♥←♦↔ ℑƒ®		ℑ≥°°	ℑ≥ƒ	·
· ⟨⌡·⌡∇⌈⟨ ®		∂· ⊄⊄√∂⌡ ≤ ·√♣ ⟨♣↔↔ ⌈}♥←♦↔ ℑƒ®	ℑ≥∞	ℑ≥≈°	♠≥♠	·
· ⟨×♣⟨⌡·⌡∇⌈⟨ ®		∂· ⊄⊄√∂⌡ ≤ ·√♣ ⟨♣↔↔ ⌈}♥←♦↔ ℑƒ®	ƒ…	ℑ……	ℑ°°	∝·
⌈⊄⊄⟨⌡·⌡® ⟨♣↔↔ ⟩↵⌡↔ ℑ®		·⟩⌊ … ⟨·⟩⌊ ≡}⌡♣ ⊆♦↔ }⊇⌡·⌡⊄⟨⟩ ♦↔♥}♣⌡↔♠♠℗″♠≥♠ ·√≤ ·		ℑ…	ℑ°	µ⌡

⟩⌠⟨™⌡∫ ℑ≥ ⟨ ⌡↔ ⊂←♦♦↔⊇⌡ ⊂↵⊇♣←∝≠⌡}↵⊇ ↵⊗⌡↔⌡· ∝↵∂←ℜ↔ }♣ ⊇↵⌡ }⊇⊄ℜ↔∂♦ℵ⊇⌡ ⌡↔↵⊇♣←∝≠⌡}↵⊇ ∂⊂⌡⊂≥
♠≥ ⟨ ⌡↔⌡·⌡ }♣ ⊇↵⌡ ⊂⊂⌡}℘↔⊆⌡ ≠↵•↔♦ ←≠≥

electrical characteristics over recommended operating free-air temperature (unless otherwise noted) (continued)

SVS (supply voltage supervisor/monitor) (MSP430x415, MSP430x417 only) (see Notes 1 and 2)

PARAMETER	TEST CONDITIONS		MIN	NOM	MAX	UNIT

electrical characteristics over recommended operating free-air temperature (unless otherwise noted) (continued)

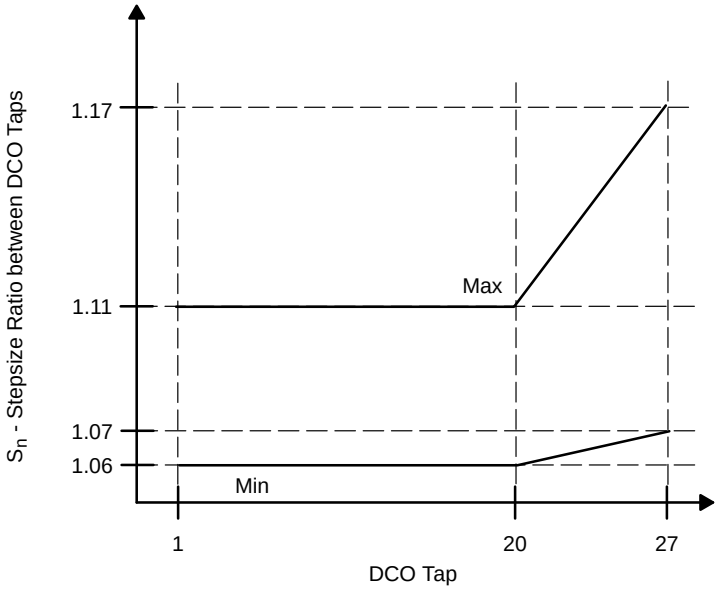


Figure 20. DCO Tap Step Size

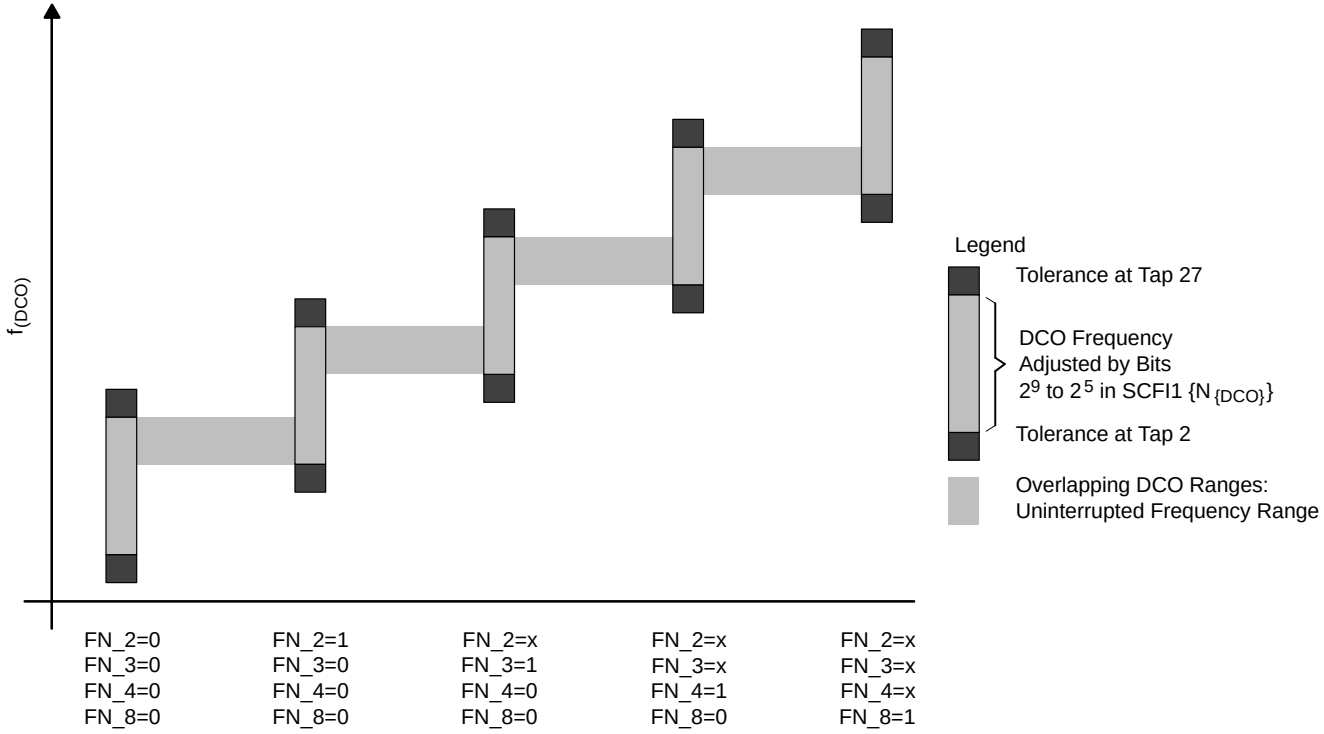


Figure 21. Five Overlapping DCO Ranges Controlled by FN_x Bits

electrical characteristics over recommended operating free-air temperature (unless otherwise noted) (continued)

crystal oscillator, LFXT1 oscillator (see Notes 1 and 2)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
f_{LFXT1}	LFXT1: 32768-Hz crystal	XTS = 0, LFXT1Sx = 0	1.8 V to 3.6 V		32768		Hz
	LFXT1: 32768-Hz crystal	XTS = 0, LFXT1Sx = 0	2.2 V to 3.6 V		32768		Hz
	LFXT1: 32768-Hz crystal	XTS = 0, LFXT1Sx = 0	3 V		32768		Hz
	LFXT1: 32768-Hz crystal	XTS = 0, LFXT1Sx = 0	3.6 V		32768		Hz
$f_{LFXT1,LF}$	LFXT1: 32768-Hz crystal	XTS = 0, LFXT1Sx = 0	1.8 V to 3.6 V		32768		Hz
	LFXT1: 32768-Hz crystal	XTS = 0, LFXT1Sx = 0	2.2 V to 3.6 V		32768		Hz
	LFXT1: 32768-Hz crystal	XTS = 0, LFXT1Sx = 0	3 V		32768		Hz
	LFXT1: 32768-Hz crystal	XTS = 0, LFXT1Sx = 0	3.6 V		32768		Hz
$f_{LFXT1,VLO}$	LFXT1: Ultra-low-power 32768-Hz crystal	XTS = 0, LFXT1Sx = 0	1.8 V to 3.6 V		32768		Hz
	LFXT1: Ultra-low-power 32768-Hz crystal	XTS = 0, LFXT1Sx = 0	2.2 V to 3.6 V		32768		Hz
	LFXT1: Ultra-low-power 32768-Hz crystal	XTS = 0, LFXT1Sx = 0	3 V		32768		Hz
	LFXT1: Ultra-low-power 32768-Hz crystal	XTS = 0, LFXT1Sx = 0	3.6 V		32768		Hz
$f_{LFXT1,HF}$	LFXT1: 32768-Hz crystal	XTS = 0, LFXT1Sx = 0	1.8 V to 3.6 V		32768		Hz
	LFXT1: 32768-Hz crystal	XTS = 0, LFXT1Sx = 0	2.2 V to 3.6 V		32768		Hz
	LFXT1: 32768-Hz crystal	XTS = 0, LFXT1Sx = 0	3 V		32768		Hz
	LFXT1: 32768-Hz crystal	XTS = 0, LFXT1Sx = 0	3.6 V		32768		Hz
$f_{LFXT1,HF,logic}$	LFXT1: 32768-Hz crystal	XTS = 0, LFXT1Sx = 0	1.8 V to 3.6 V		32768		Hz
	LFXT1: 32768-Hz crystal	XTS = 0, LFXT1Sx = 0	2.2 V to 3.6 V		32768		Hz
	LFXT1: 32768-Hz crystal	XTS = 0, LFXT1Sx = 0	3 V		32768		Hz
	LFXT1: 32768-Hz crystal	XTS = 0, LFXT1Sx = 0	3.6 V		32768		Hz
$f_{LFXT1,HF0}$	LFXT1: 32768-Hz crystal	XTS = 0, LFXT1Sx = 0	1.8 V to 3.6 V		32768		Hz
	LFXT1: 32768-Hz crystal	XTS = 0, LFXT1Sx = 0	2.2 V to 3.6 V		32768		Hz
	LFXT1: 32768-Hz crystal	XTS = 0, LFXT1Sx = 0	3 V		32768		Hz
	LFXT1: 32768-Hz crystal	XTS = 0, LFXT1Sx = 0	3.6 V		32768		Hz
$f_{LFXT1,HF1}$	LFXT1: 32768-Hz crystal	XTS = 0, LFXT1Sx = 0	1.8 V to 3.6 V		32768		Hz
	LFXT1: 32768-Hz crystal	XTS = 0, LFXT1Sx = 0	2.2 V to 3.6 V		32768		Hz
	LFXT1: 32768-Hz crystal	XTS = 0, LFXT1Sx = 0	3 V		32768		Hz
	LFXT1: 32768-Hz crystal	XTS = 0, LFXT1Sx = 0	3.6 V		32768		Hz
$f_{LFXT1,HF2}$	LFXT1: 32768-Hz crystal	XTS = 0, LFXT1Sx = 0	1.8 V to 3.6 V		32768		Hz
	LFXT1: 32768-Hz crystal	XTS = 0, LFXT1Sx = 0	2.2 V to 3.6 V		32768		Hz
	LFXT1: 32768-Hz crystal	XTS = 0, LFXT1Sx = 0	3 V		32768		Hz
	LFXT1: 32768-Hz crystal	XTS = 0, LFXT1Sx = 0	3.6 V		32768		Hz
$f_{LFXT1,HF3

electrical characteristics over recommended operating free-air temperature (unless otherwise noted) (continued)

flash memory

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT

JTAG interface

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT

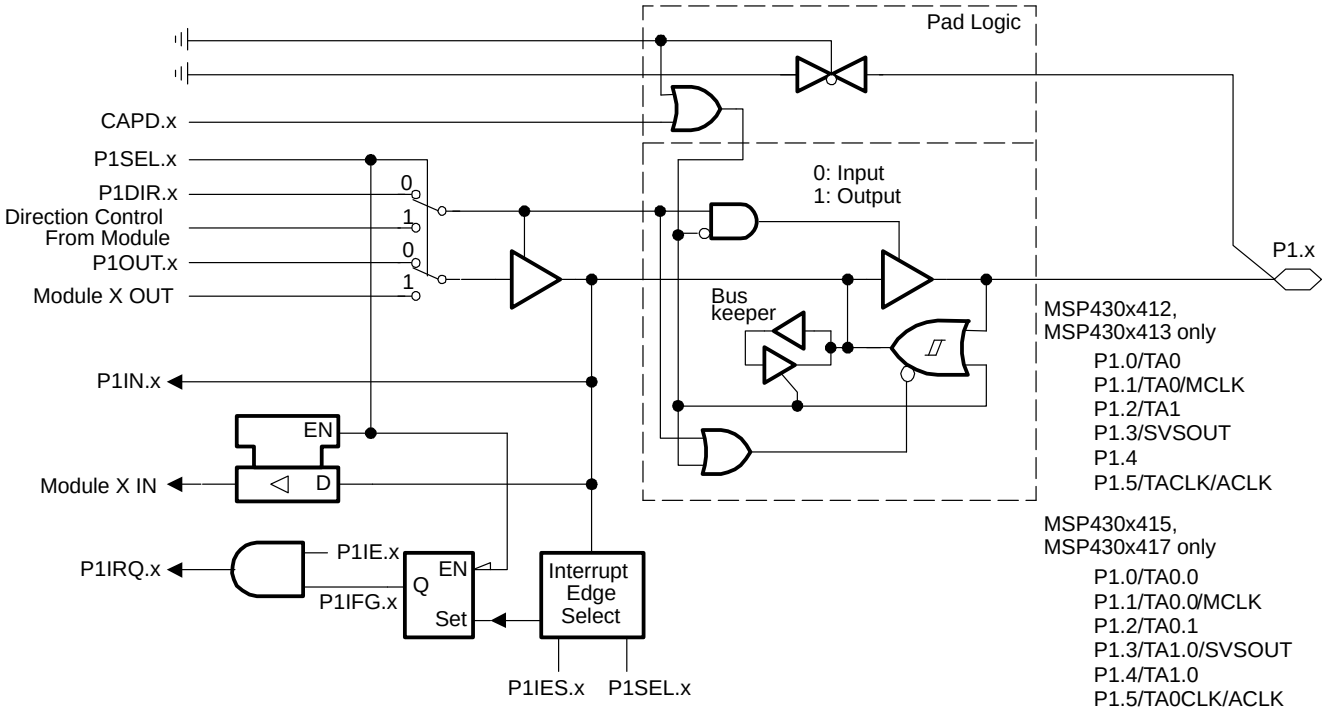
JTAG fuse (see Note 1)

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT

APPLICATION INFORMATION

input/output schematics

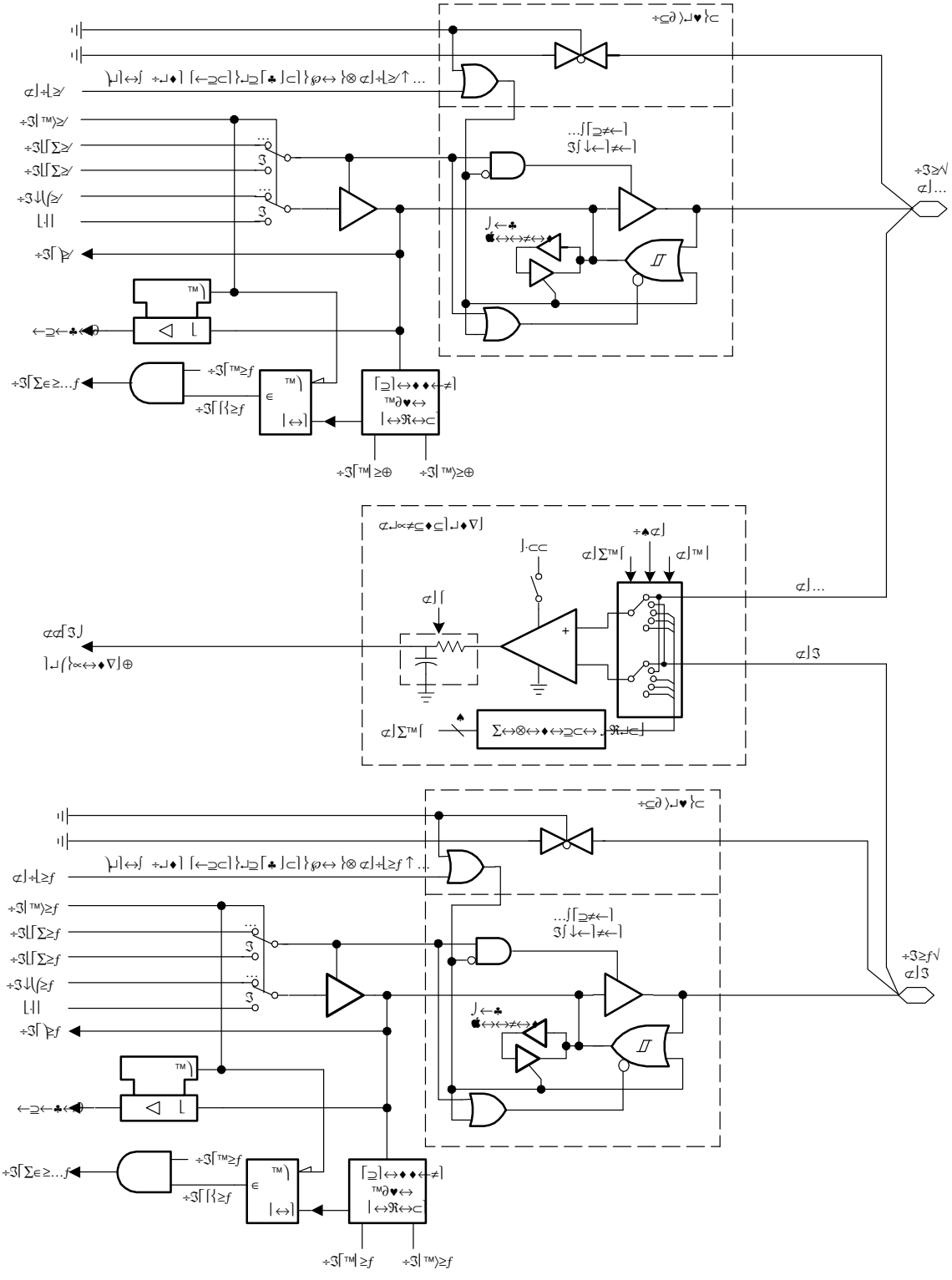
Port P1, P1.0 to P1.5, input/output with Schmitt trigger



PnSEL.x	PnDIR.x	Direction Control From Module	PnOUT.x	Module X OUT	PnIN.x	Module X IN	PnIE.x	PnIFG.x	PnIES.x
0	0	0	0	0	0	0	0	0	0
0	0	0	1	1	0	0	0	0	1
0	1	1	0	0	0	0	0	0	0
0	1	1	1	1	0	0	0	0	1
1	0	0	0	0	1	1	1	1	0
1	0	0	1	1	1	1	1	1	1
1	1	1	0	0	1	1	1	1	0
1	1	1	1	1	1	1	1	1	1

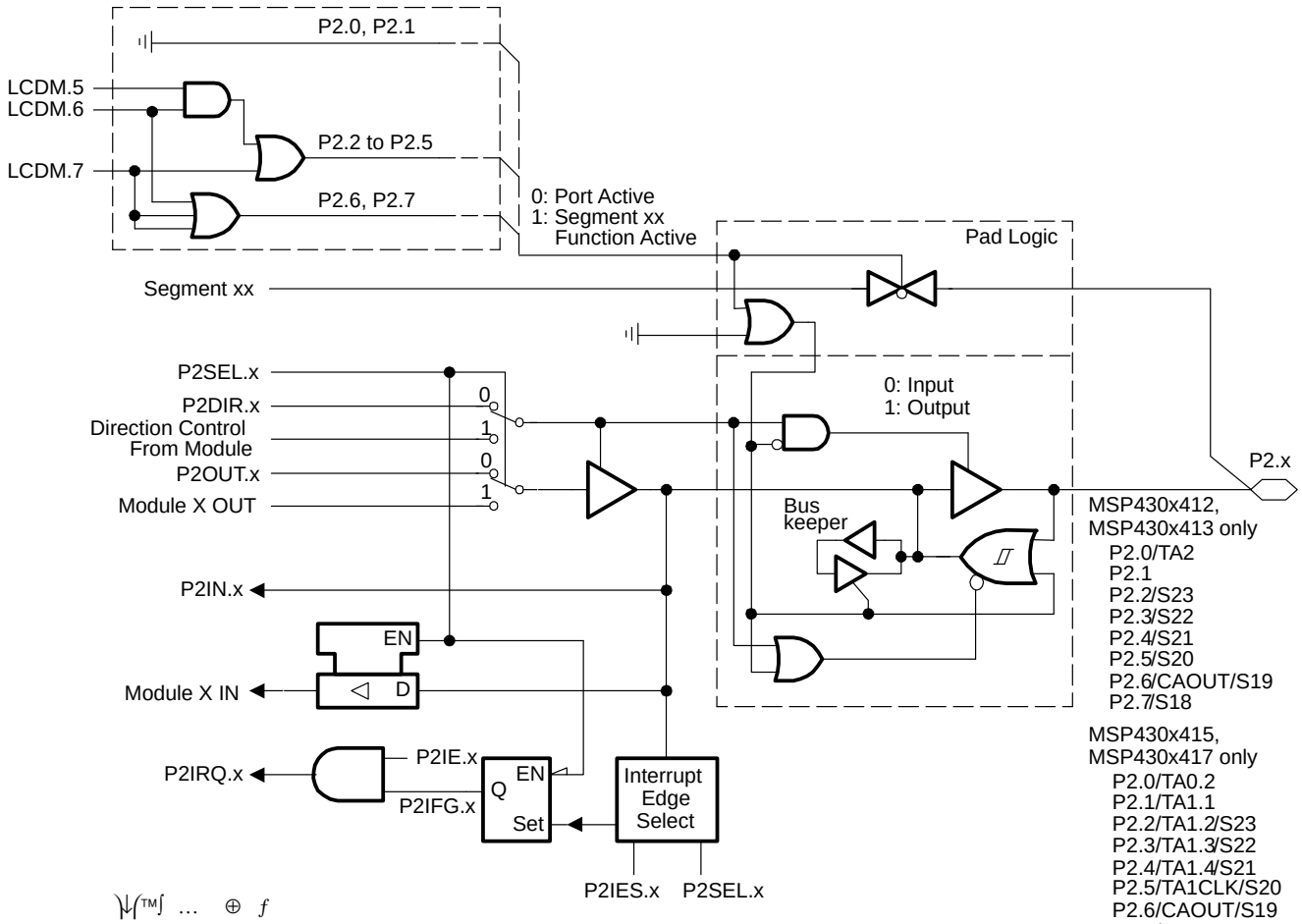
APPLICATION INFORMATION

Port P1, P1.6, P1.7 input/output with Schmitt trigger



APPLICATION INFORMATION

port P2, P2.0 to P2.7, input/output with Schmitt trigger



PnSEL.x	PnDIR.x	Direction Control From Module	PnOUT.x	Module X OUT	PnIN.x	Module X IN	PnIE.x	PnIFG.x	PnIES.x
0	0	0	0	0	P2IN.0	0	P2IE.0	P2IFG.0	P2IES.0
0	0	0	1	1	P2IN.1	0	P2IE.1	P2IFG.1	P2IES.1
0	0	1	0	0	P2IN.2	1	P2IE.2	P2IFG.2	P2IES.2
0	0	1	1	1	P2IN.3	1	P2IE.3	P2IFG.3	P2IES.3
0	1	0	0	0	P2IN.4	0	P2IE.4	P2IFG.4	P2IES.4
0	1	0	1	1	P2IN.5	0	P2IE.5	P2IFG.5	P2IES.5
0	1	1	0	0	P2IN.6	1	P2IE.6	P2IFG.6	P2IES.6
0	1	1	1	1	P2IN.7	1	P2IE.7	P2IFG.7	P2IES.7
1	0	0	0	0	P2IN.0	P2SEL.0	P2IE.0	P2IFG.0	P2IES.0
1	0	0	1	1	P2IN.1	P2SEL.1	P2IE.1	P2IFG.1	P2IES.1
1	0	1	0	0	P2IN.2	P2SEL.2	P2IE.2	P2IFG.2	P2IES.2
1	0	1	1	1	P2IN.3	P2SEL.3	P2IE.3	P2IFG.3	P2IES.3
1	1	0	0	0	P2IN.4	P2SEL.4	P2IE.4	P2IFG.4	P2IES.4
1	1	0	1	1	P2IN.5	P2SEL.5	P2IE.5	P2IFG.5	P2IES.5
1	1	1	0	0	P2IN.6	P2SEL.6	P2IE.6	P2IFG.6	P2IES.6
1	1	1	1	1	P2IN.7	P2SEL.7	P2IE.7	P2IFG.7	P2IES.7

for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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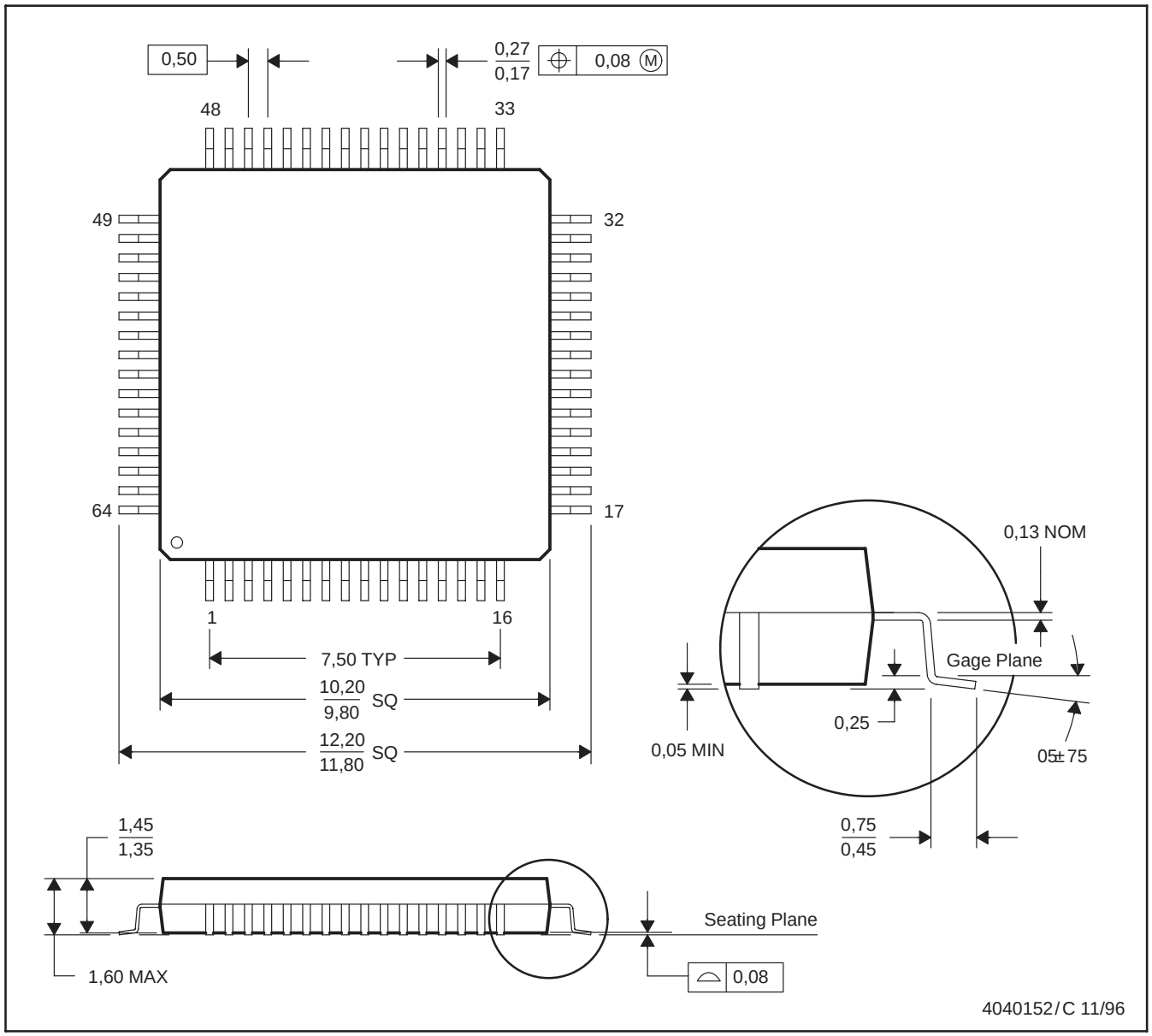
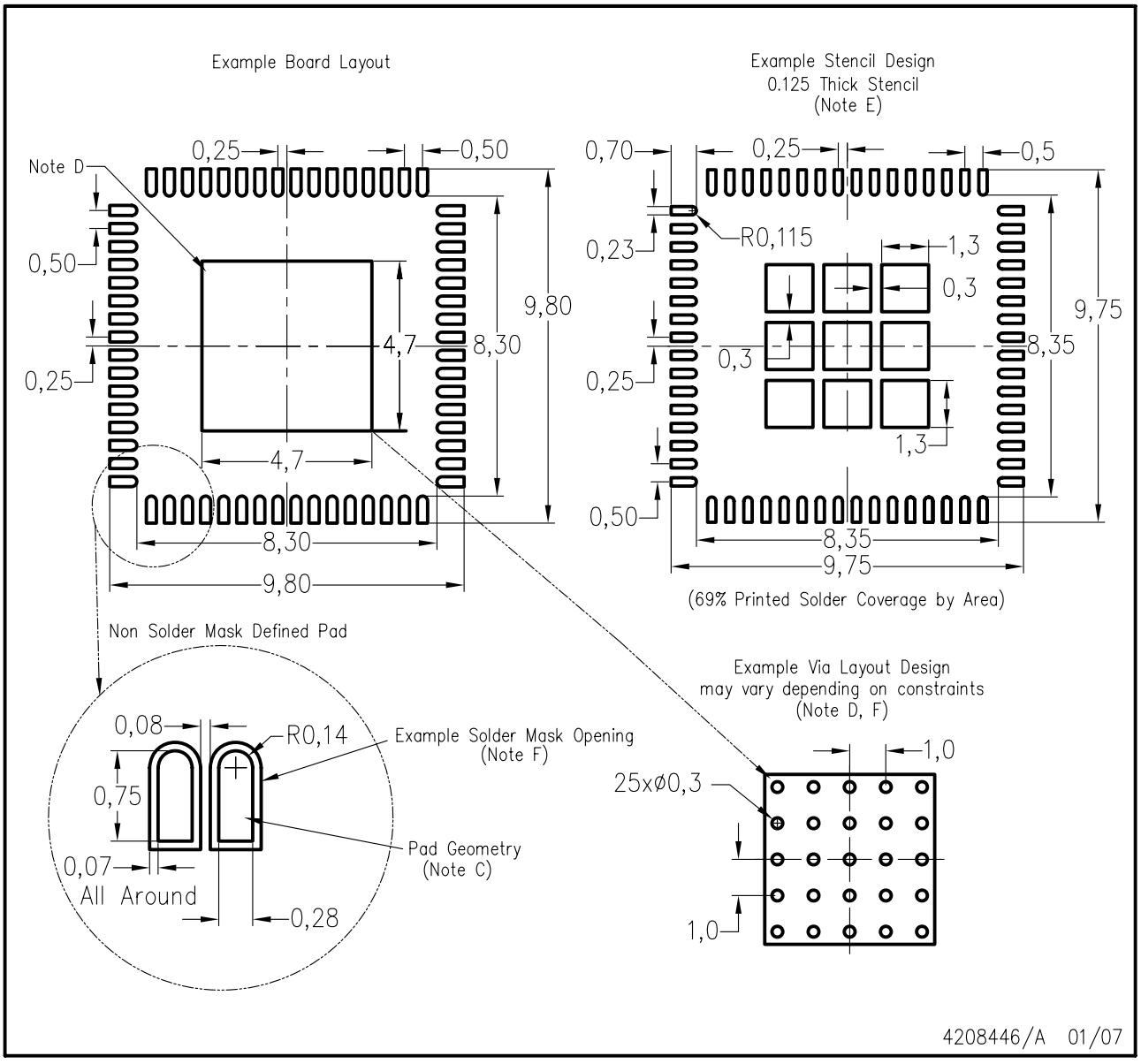
MTQF008A ± JANUARY 1995 ± REVISED DECEMBER 1996

PM (S-PQFP-G64) PLASTIC QUAD FLATPACK



NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS-026
D. May also be thermally enhanced plastic with leads connected to the die pads.

RTD (S–PQFP–N64)



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat–Pack Package, Texas Instruments Literature No. SCBA017 and SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>.
E. Laser cutting apertures with electropolish and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
F. Customer should contact their board fabrication site for recommended solder mask tolerances and vias tenting recommendations for vias placed int the thermal pad.

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Logic	logic.ti.com	Optical Networking	www.ti.com/opticalnetwork
Power Mgmt	power.ti.com	Security	www.ti.com/security
Microcontrollers	microcontroller.ti.com	Telephony	www.ti.com/telephony
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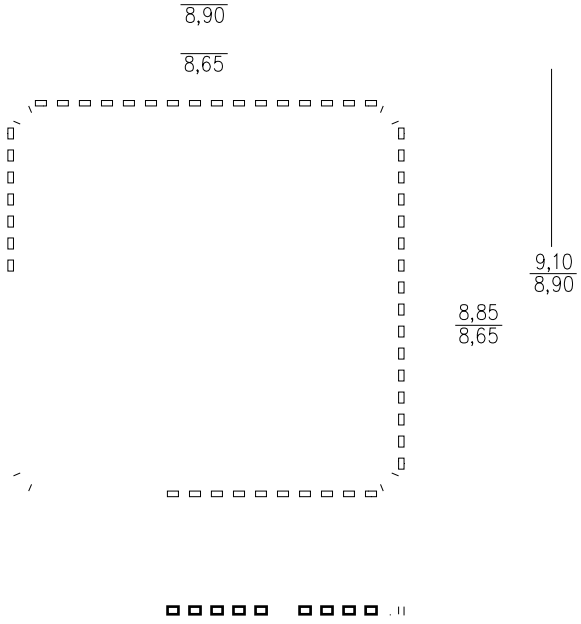


D The package thermal pad must be soldered to the board for thermal and mechanical performance. See the Product Data Sheet for details regarding the exposed thermal pad dimensions.

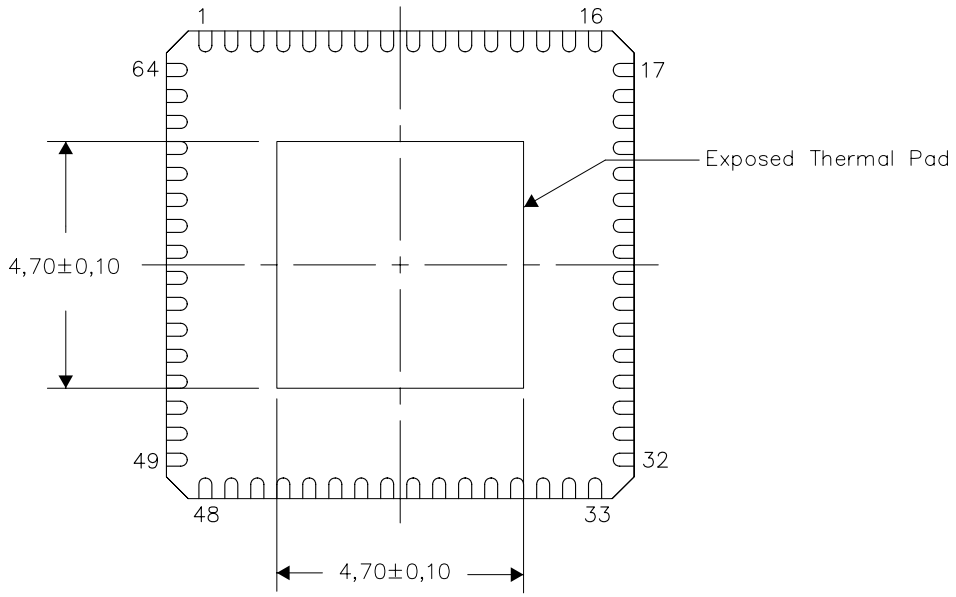
RTD (S–PVQFN–N64) PLASTIC QUAD FLATPACK NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



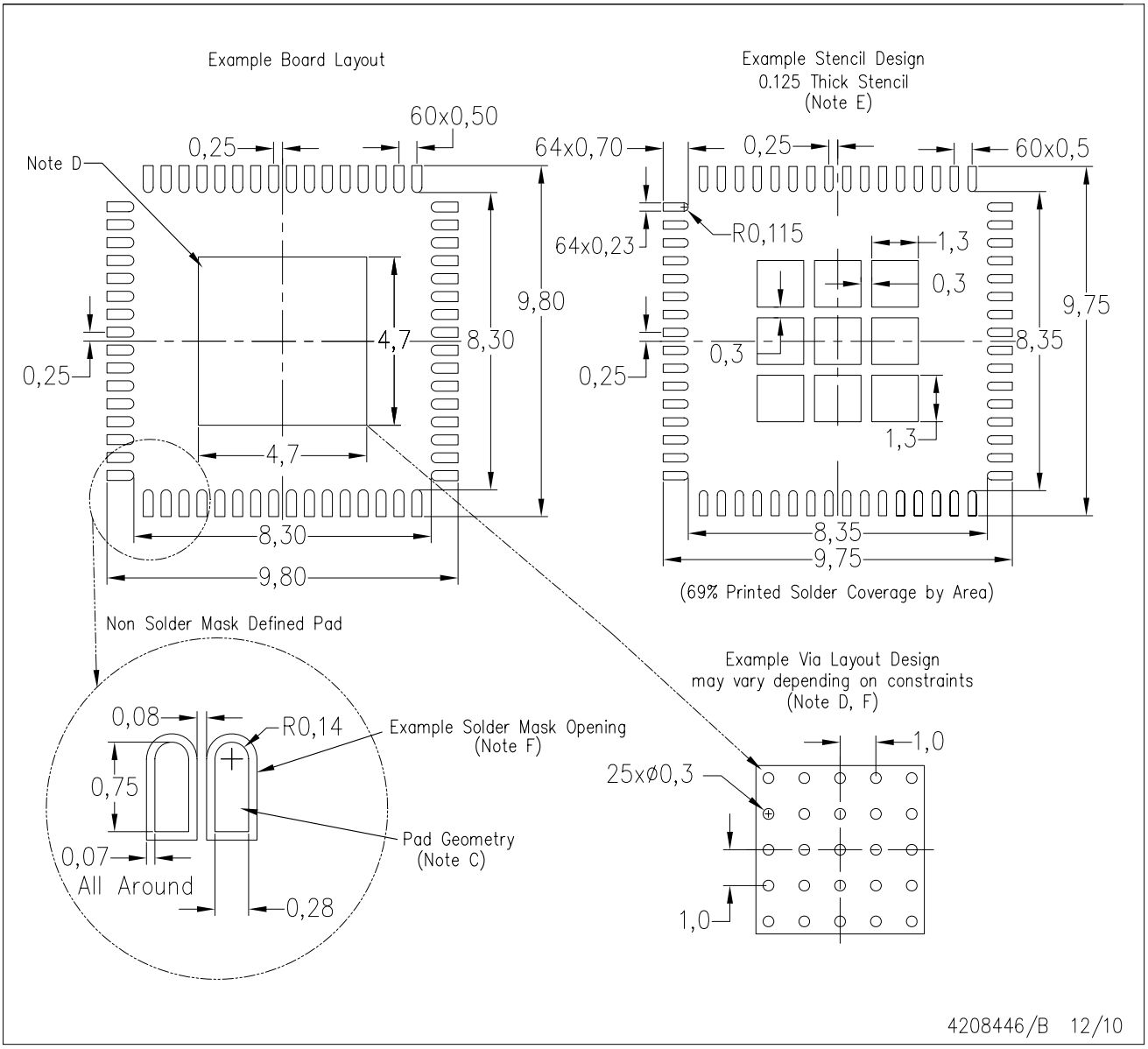
Bottom View

Exposed Thermal Pad Dimensions

4206338–3/E 12/10

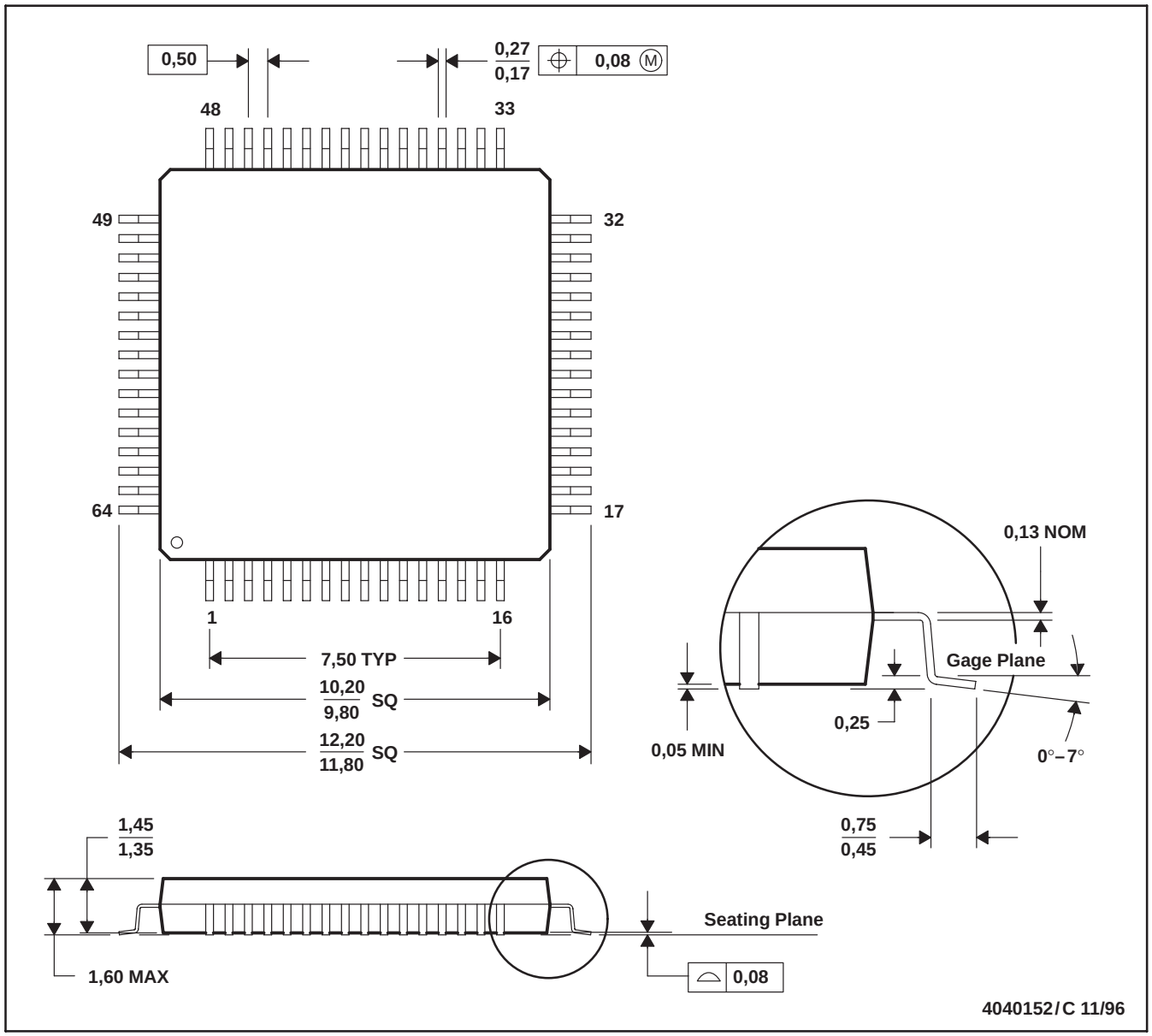
NOTE: A. All linear dimensions are in millimeters

RTD (S–PVQFN–N64) PLASTIC QUAD FLATPACK NO–LEAD



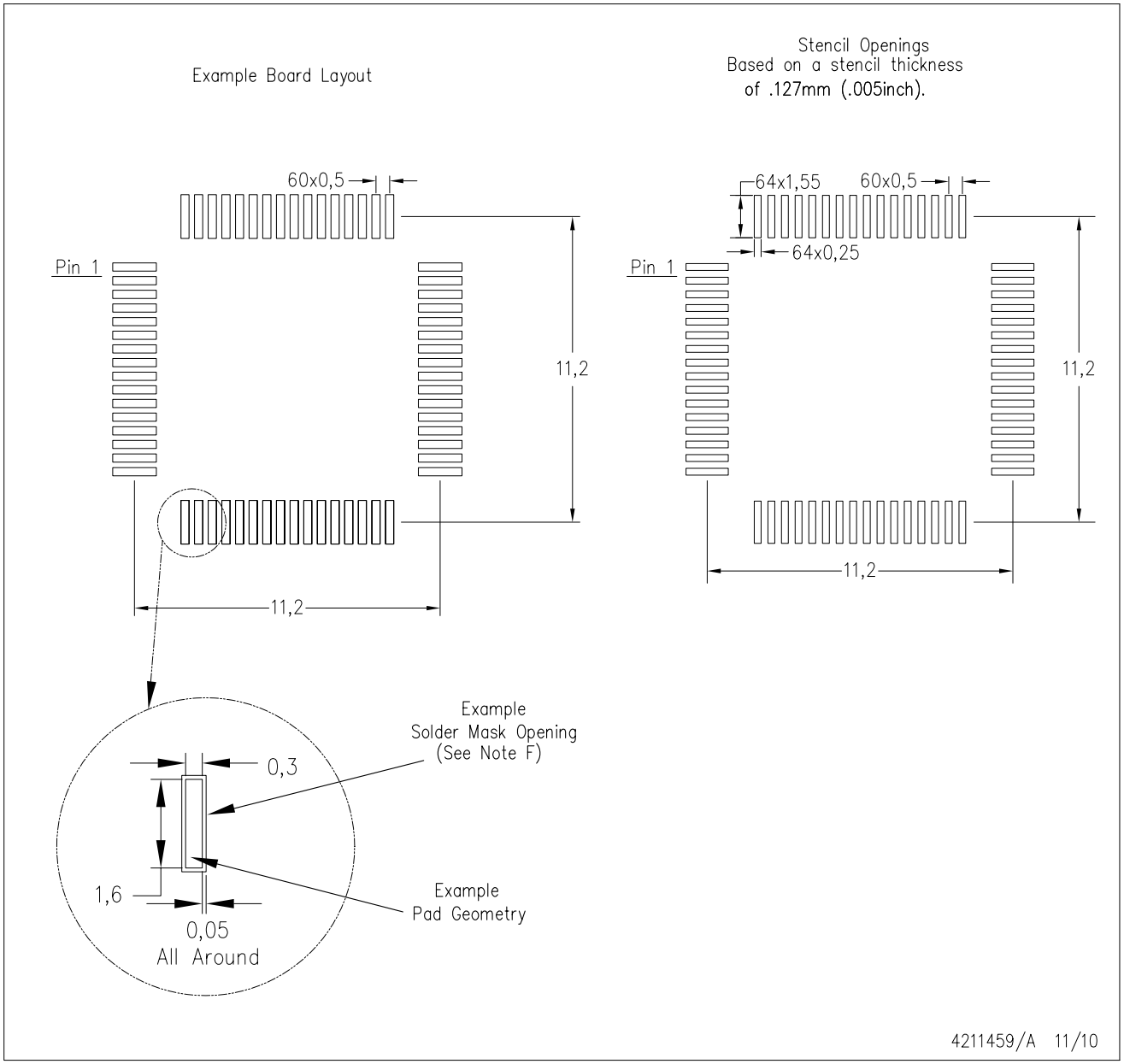
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat–Pack Package, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>.
E. Laser cutting apertures with electropolish and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
F. Customer should contact their board fabrication site for recommended solder mask tolerances and vias tenting recommendations for vias placed int the thermal pad.

PM (S-PQFP-G64) **PLASTIC QUAD FLATPACK**



NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS-026
D. May also be thermally enhanced plastic with leads connected to the die pads.

PM (S–PQFP–G64) PLASTIC QUAD FLATPACK



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.
D. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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