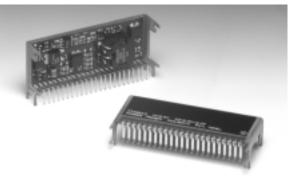
(Revised 7/20/2001)



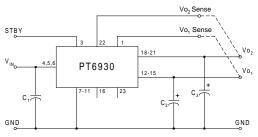
### **Features**

- Dual Outputs:
  - +3.3V/2.5V
  - +3.3V/1.5V
  - +3.3V/1.8V
- Adjustable Output Voltages
- Remote Sense (both outputs)
- Standby Function
- Over-Temperature Protection
- Soft-Start
- Internal Sequencing
- 23-pin Excalibur<sup>TM</sup> Package

## **Description**

The PT6930 Excalibur™ series of 8-A dual-output ISRs are designed to power DSP ICs. Both output voltages are independently adjustable with external resistors. The second output may also be set to an alternate lower bus voltage with a simple pin strap. Internal power sequencing of both outputs, during both power-up and power-down, meets the requirements of most DSP chipsets.

# **Standard Application**



 $C_1/C_2$  =Req'd 330µF electrolytic (See table footnotes)  $C_3$  =Optional 100µF electrolytic

### **Pin-Out Information**

Pin	Function	_ Piı	ı Func	tion
1	$\mathrm{Vo}_1$ Sense	13	$Vo_1$	
2	No Connect	14	· Vo <sub>1</sub>	
3	STBY	15	Vo <sub>1</sub>	
4	$V_{IN}$	16	Vo <sub>1</sub> A	djust
5	$V_{\rm IN}$	17	No Co	onnect
6	$V_{\rm IN}$	18	Vo <sub>2</sub>	
7	GND	19	Vo <sub>2</sub>	
8	GND	20	Vo <sub>2</sub>	
9	GND	21	Vo <sub>2</sub>	
10	GND	22	Vo <sub>2</sub> S	ense
11	GND	23	Vo <sub>2</sub> A	Adjust*
12	Vo <sub>1</sub>			

<sup>\*</sup> Note:Vo<sub>1</sub> & Vo<sub>2</sub> Adjust can be pin-strapped to an alternative lower bus voltage. Consult the voltage adjustment application note for more information.

## **Ordering Information**

**PT6931** = +3.3 Volts

+2.5/1.8 Volts

**PT6932**  $\Box$  = +3.3 Volts

+1.5/1.2 Volts **PT6933**□ = +3.3 Volts

+1.8/1.2 Volts

## PT Series Suffix (PT1234X)

#### Case/Pin Configuration

Comiguration	
Vertical Through-Hole	N
Horizontal Through-Hole	Α
Horizontal Surface Mount	C

(For dimensions and PC board layout, see Package Styles 1320 and 1330).

### **Specifications**

Characteristics				PT6930 SERIES				
(T <sub>a</sub> = 25°C unless noted)	Symbols	Conditions	Min	Тур	Max	Units		
Output Current	${ m Io_1, Io_2}$	T <sub>a</sub> =+60°C, 200 LFM, pkg N	Vo <sub>1</sub> =3.3 V Vo <sub>2</sub> =2.5 V Vo <sub>2</sub> =1.8 V Vo <sub>2</sub> =1.5 V Vo <sub>1</sub> =1.2 V	0.1 (1) 0 0 0 0	_ _ _ _	5.5 (2) 2.2 (2) 1.75 (2) 1.45 (2) 1.2 (2)	A	
		$T_a = +25$ °C, natural convection	Vo <sub>1</sub> =3.3V Vo <sub>2</sub> =2.5V Vo <sub>2</sub> =1.8V Vo <sub>2</sub> =1.5V Vo <sub>1</sub> =1.2V	0.1 (1) 0 0 0 0	_ _ _ _	6.0 (2) 2.2 (2) 1.75 (2) 1.45 (2) 1.2 (2)	A A	
Input Voltage Range	$V_{in}$	$0.1A \le I_o \le I_{typ}$		4.5	_	5.5	V	
Output Voltage Tolerance	$\Delta { m V_o}$	$V_{\text{in}}$ = +5V, $I_{\text{o}}$ = $I_{\text{typ}}$ , both outputs $0^{\circ}\text{C} \leq T_{\text{a}} \leq +65^{\circ}\text{C}$		Vo-0.1	_	Vo+0.1	V	
Line Regulation	Reg <sub>line</sub>	$4.5$ V $\leq$ V $_{in}$ $\leq$ $5.5$ V, $I_{o}$ = $I_{typ}$	$V_{0_1} V_{0_2}$	_	±7 ±7	±17 ±13	V	
Load Regulation	$Reg_{load}$	$V_{\rm in}$ = +5V, $0.1 \le I_{\rm o} \le I_{\rm typ}$	$\begin{matrix} V_{O_1} \\ V_{O_2} \end{matrix}$	_	±17 ±4	±33 ±10	mV	
V <sub>o</sub> Ripple/Noise	$V_n$	$V_{\rm in}$ = +5V, $I_{\rm o}$ = $I_{\rm typ}$	$\begin{matrix} V_{O_1} \\ V_{O_2} \end{matrix}$	_	50 25	_	mV	
Transient Response with $C_2 = 330 \mu F$	${ m t_{tr} \over V_{os}}$	$I_{o}$ step between $0.5xI_{typ}$ and $I_{typ}$ $V_{o}$ over/undershoot	$V_{o_1}$ $V_{o_2}$	_	25 60 60	Ξ	μSec mV	
Efficiency	η	$V_{\rm in}$ = +5V, $I_{\rm o}$ =4A total			75	_	%	
Switching Frequency	$f_{\mathrm{o}}$	$4.5V \le V_{in} \le 5.5V$ $0.1A \le I_0 \le I_{typ}$		475	600	725	kHz	

(Continued)

# 8-A 5V-Input Dual-Output Integrated Switching Regulator

## **Specifications** (From previous page)

Characteristics			PT6930 SERIES				
(T <sub>a</sub> = 25°C unless noted)	Symbols	Conditions	Min	Тур	Max	Units	
Absolute Maximum Operating Temperature Range	$T_a$	_	-40 (3)	_	+85 (4)	°C	
Storage Temperature	$T_s$	_	-40	_	+125	°C	
Weight	_	Vertical/Horizontal	_	29	_	grams	

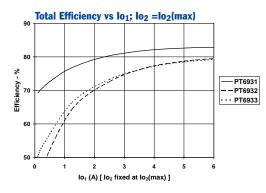
Notes: (1) I<sub>o</sub>min current of 0.1A can be divided btween both outputs; Vo<sub>1</sub>, or Vo<sub>2</sub>. The ISR will operate down to no-load with reduced specifications.

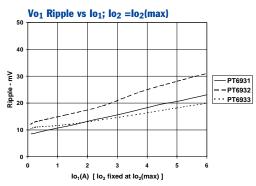
- (2) Iomax listed for each output assumes the maximum current drawn simultaneously on both outputs. Consult the factory for the absolute maximum.
- (3) For operating temperatures below 0°C, use tantalum type capacitors at both the input and output.
- (4) See Safe Operating Area curves for appropriate derating.

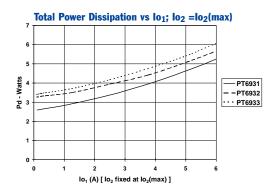
Input/Output Capacitors: The PT6930 series requires a minimumm capacitance of 330 $\mu$ F at both the input and  $Vo_1$  output for proper operation in all applications. In addition, the input capacitor,  $C_1$ , must be rated for a minimum of 1.0Arms ripple current. For transient or dynamic dynamic loads, additional capacitance may be required.

# TYPICAL CHARACTERISTICS

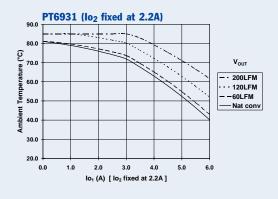
# PT6930 Series Performance (See Note A)







# Safe Operating Area @V<sub>IN</sub> =5V (See Note B)



**Note A:** All characteristic data in the above graphs has been developed from actual products tested at 25°C. This data is considered typical data for the ISR. **Note B:** SOA curves represent operating conditions at which internal components are at or below the manufactuer's maximum rated operating temperatures.

## PT6920/PT6930 Series

# Adjusting the Output Voltage of the PT6920 and PT6930 Dual Output Voltage ISRs

Each output voltage from the PT6920 and PT6930 series of ISRs can be independantly adjusted higher or lower than the factory trimmed pre-set voltage.  $Vo_1$  or  $Vo_2$  may each be adjusted either up or down using a single external resistor  $^2$ . Table 1 gives the adjustment range for both  $Vo_1$  and  $Vo_2$  for each model in the series as  $V_a(\text{min})$  and  $V_a(\text{max})$ . Note that  $Vo_2$  must always be lower than  $Vo_1$   $^3$ .

**Vo<sub>1</sub> Adjust Up:** To increase the output, add a resistor R4 between pin 16 ( $V_1$  Adjust) and pins 7-11 (GND) <sup>2</sup>.

**Vo<sub>1</sub> Adjust Down:** Add a resistor (R3), between pin 16 (Vo<sub>1</sub> Adjust) and pin 1 (Vo<sub>1</sub> Sense) 2.

**Vo<sub>2</sub> Adjust Up:** Add a resistor R2 between pin 23 (Vo<sub>2</sub> Adjust) and pins 7-11 (GND) <sup>2</sup>.

**Vo<sub>2</sub> Adjust Down:** Add a resistor (R1) between pin 23 (Vo<sub>2</sub> Adjust) and pin 22 (Vo<sub>2</sub> Sense) <sup>2</sup>.

Refer to Figure 1 and Table 2 for both the placement and value of the required resistor.

#### Notes:

- 1. The output voltages, Vo<sub>1</sub> and Vo<sub>2</sub>, may be adjusted independently.
- Use only a single 1% resistor in either the (R3) or R4 location to adjust Vo<sub>1</sub>, and in the (R1) or R2 location to adjust Vo<sub>2</sub>. Place the resistor as close to the ISR as possible.
- 3. Vo<sub>2</sub> must always be at least 0.2V lower than Vo<sub>1</sub>.
- 4. Vo<sub>2</sub> on both the PT6921 and PT6931 models may be adjusted from 2.5V to 1.8V by simply connecting pin 22 (Vo<sub>2</sub> Sense) to pin 23 (Vo<sub>2</sub> Adjust). For more details, consult the data sheet.

- If Vo<sub>1</sub> is increased above 3.3V, the minimum input voltage to the ISR must also be increased. The minimum required input voltage must be (Vo<sub>1</sub> + 1.2)V or 4.5V, whichever is greater. Do not exceed 5.5V
- 6. Never connect capacitors to either the Vo<sub>1</sub> Adjust or Vo<sub>2</sub> Adjust pins. Any capacitance added to these control pins will affect the stability of the respective regulated output.
- 7. Adjusting either voltage (Vo<sub>1</sub> or Vo<sub>2</sub>) may increase the power dissipation in the regulator, and correspondingly change the maximum current available at either output. Consult the factory for application assistance.

The adjust up and adjust down resistor values can also be calculated using the following formulas. Be sure to select the correct formula parameter from Table 1 for the output and model being adjusted.

$$(R1)$$
 or  $(R3)$  =  $\frac{R_o(V_a - V_r)}{V_o - V_a}$   $-R_s$   $k\Omega$ 

R2 or R4 = 
$$\frac{V_r \cdot R_o}{V_a - V_o} - R_s$$
  $k\Omega$ 

Where: V<sub>o</sub> = Original output voltage, (Vo<sub>1</sub> or Vo<sub>2</sub>)

V<sub>a</sub> = Adjusted output voltage

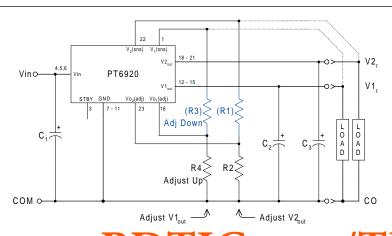
 $V_r$  = The reference voltage from Table 1  $R_o$  = The resistance value from Table 1

 $R_{\rm s}$  = The resistance value from Table 1

Table 1

PT6920 ADJUSTMENT RANGE AND FORMULA PARAMETERS							
Output Bus	Vo <sub>1</sub>		Vo <sub>2</sub>				
Series Pt #							
Standard Case	PT6921/22	PT6921	PT6922				
Excalibur Case	PT6931/32	PT6931	PT6932	PT6933			
Adj. Resistor	(R3)/R4	(R1)/R2	(R1)/R2	(R1)/R2			
V <sub>O</sub> (nom)	3.3V	2.5V	1.5V	1.8V			
Va(min)	2.3V	1.8V	1.2V	1.2V			
Va(max)	3.6V	3.0V	3.0V	3.0V			
Vr	1.02V	1.0V	1.0V	1.0V			
R <sub>0</sub> (kΩ)	12.1	10.0	9.76	10.0			
R <sub>S</sub> (kΩ)	12.1	11.5	6.49	3.32			

Figure 1



## PT6920/PT6930 Series

Table 2

Output Bus	Vo <sub>1</sub>		Vo <sub>2</sub>	
Series Pt#		-		
Standard Case	PT6921/6922	PT6921	PT6922	
Excalibur Case	PT6931/6932	PT6931	PT6932	PT6933
Adj Resistor	(R3)/R4	(R1)/R2	(R1)/R2	(R1)/R2
V <sub>o</sub> (nom)	3.3Vdc	2.5Vdc	1.5Vdc	1.8Vdc
Va(req'd)				
1.2			$(0.0)$ k $\Omega$	$(0.0)$ k $\Omega$
1.25		-	$(3.3)$ k $\Omega$	$(1.2)$ k $\Omega$
1.3			$(8.2)$ k $\Omega$	$(2.7)$ k $\Omega$
1.35		-	$(16.3)$ k $\Omega$	$(4.5)$ k $\Omega$
1.4			$(32.6)$ k $\Omega$	$(6.7)$ k $\Omega$
1.45			$(81.4)$ k $\Omega$	$(9.5)$ k $\Omega$
1.5				(13.3)kΩ
1.55			189.0kΩ	$(18.7)$ k $\Omega$
1.6			91.1kΩ	(26.7)kΩ
1.65			58.6kΩ	(40.0)kΩ
1.7			42.3kΩ	(66.7)kΩ
1.75			32.6kΩ	(147.0)kΩ
1.8		$(0.0)$ k $\Omega$	26.0kΩ	
1.85		(1.6)kΩ	21.4kΩ	197.0kΩ
1.9		(3.5)kΩ	17.9kΩ	96.7kΩ
1.95		(5.8)kΩ	15.2kΩ	63.3kΩ
2.0		(8.5)kΩ	13.0kΩ	46.7kΩ
2.05		(11.8)kΩ	11.3kΩ	36.7kΩ
2.1		(16.0)kΩ	9.8kΩ	30.0kΩ
2.15		(21.4)kΩ	8.5kΩ	25.3kΩ
2.2		(28.5)kΩ	7.5kΩ	21.7kΩ
2.25		(38.5)kΩ	6.5kΩ	18.9kΩ
2.3	(3.4)kΩ	(53.5)kΩ	5.7kΩ	16.7kΩ
2.35	(4.8)kΩ	(78.5)kΩ	5.0kΩ	14.9kΩ
2.4	(6.5)kΩ	(129.0)kΩ	4.4kΩ	13.3kΩ
2.45	(8.3)kΩ	$(279.0)$ k $\Omega$	3.8kΩ	12.1kΩ
2.5	(10.3)kΩ	(=,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,	3.3kΩ	11.0kΩ
2.55	(12.6)kΩ	189.0kΩ	2.8kΩ	10.0kΩ
2.6	(15.2)kΩ	88.5kΩ	2.4kΩ	9.2kΩ
2.65	(18.2)kΩ	55.2kΩ	2.0kΩ	8.4kΩ
2.7	$(21.8)$ k $\Omega$ See Note 3	38.5kΩ	1.6kΩ	7.8kΩ
2.75	(26.0)kΩ	28.5kΩ	1.3kΩ	7.2kΩ
2.8	(31.0)kΩ	21.8kΩ	1.0kΩ	6.7kΩ
2.85	(37.1)kΩ	17.1kΩ	0.7kΩ	6.2kΩ
2.9	(44.8)kΩ	13.5kΩ	0.5kΩ	5.8kΩ
2.95	(54.6)kΩ	10.7kΩ	0.2kΩ	5.4kΩ
3.0	(67.8)kΩ	8.5kΩ	0.0kΩ	5.0kΩ
3.05	(86.2)kΩ	0.5 100	3,0100	JIJNAE
3.1	(114.0)kΩ	-		
3.15	(160.0)kΩ	-		
3.2	(252.0)kΩ			
3.25	(528.0)kΩ			
3.3	(J20.0)R22			
3.4	111 0kO Saa Nata 5			
	111.0kΩ See Note 5	-		
3.5	49.6kΩ 29.0kΩ			

R1/R3 = (Blue) R2/R4 = Black

#### PT6920/PT6930 Series

# Using the Standby Function on the PT6920 and PT6930 Dual Output Voltage Converters

Both output voltages of the 23-pin PT6920/6930 dual output converter may be disabled using the regulator's standby function. This function may be used in applications that require power-up/shutdown sequencing, or wherever there is a requirement to control the output voltage On/Off status with external circuitry.

The standby function is provided by the  $STBY^*$  control (pin 3). If pin 3 is left open-circuit the regulator operates normally, and provides a regulated output at both  $Vo_1$  (pins 12–15) and  $Vo_2$  (pins 18–21) whenever a valid supply voltage is applied to  $V_{in}$  (pins 4, 5, & 6) with respect to GND (pins 7–11). If a low voltage  $^2$  is then applied to pin 3, both regulator outputs will be simultaneously disabled and the input current drawn by the ISR will typically drop to less than 30mA (50mA max). The standby control may also be used to hold-off both regulator outputs during the period that input power is applied.

The standby pin is ideally controlled using an open-collector (or open-drain) discrete transistor (See Figure 1). It may also be driven directly from a dedicated TTL<sup>3</sup> compatible gate. Table 1 provides details of the threshold requirements.

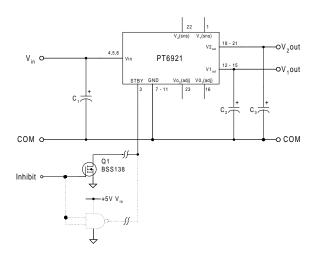
Table 1 Inhibit Control Thresholds 2,3

Parameter	Min	Max	
Enable (VIH)	1.8V	Vin	
Disable (VIL)	-0.1V	0.8V	

#### Notes:

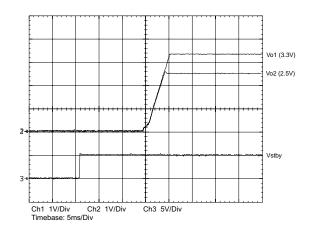
- The Standby/Inhibit control logic is similar for all Power Trends' modules, but the flexibility and threshold tolerances will be different. For specific information on this function for other regulator models, consult the applicable application note.
- 2. The Standby control pin is ideally controlled using an open-collector (or open-drain) discrete transistor and requires no external pull-up resistor. To disable the regulator output, the control pin must be pulled to less than 0.8Vdc with a low-level 0.5mA sink to ground.
- 3. The Standby input on the PT6920/6930 series may be driven by a differential output device, making it directly compatible with TTL logic. The control input has an internal pull-up to the input voltage  $V_{\rm in}$ . A voltage of 1.8V or greater ensures that the regulator is enabled. <u>Do not</u> use devices that can drive the Standby control input above 5.5V or  $V_{\rm in}$ .

Figure 1



**Turn-On Time:** Turning  $Q_1$  in Figure 1 off removes the low-voltage signal at pin 3 and enables both outputs from the PT6920/6930 regulator. Following a delay of about 10–20ms,  $Vo_1$  and  $Vo_2$  rise together until the lower voltage,  $Vo_2$ , reaches its set output.  $Vo_1$  then continues to rise until both outputs reach full regulation voltage. The total power-up time is less than 25ms, and is relatively independant of load, temperature, and output capacitance. Figure 2 shows waveforms of the output voltages  $Vo_1$  and  $Vo_2$ , for a PT6931 (3.3 $VV_2$ .5 $VV_2$ ). The turn-off of  $VV_3$  corresponds to the rise in  $VV_3$  stby. The waveforms were measured with a 5 $VV_3$  decinput voltage, and with resistive loads of 5A and 2A at the  $Vo_3$  and  $Vo_4$  outputs respectively.

Figure 2



# Capacitor Recommendations for the Dual-Output PT6920/30 Regulator Series

#### **Input Capacitors:**

The recommended input capacitance is determined by 1.0 ampere minimum ripple current rating and 330µF minimum capacitance (300µF for Oscon® or low ESR tantalum). Ripple current and <100m $\Omega$  equivalent series resistance (ESR) values are the major considerations, along with temperature, when designing with different types of capacitors. Tantalum capacitors have a recommended minimum voltage rating of 2 × the maximum DC voltage + AC ripple. This is necessary to insure reliability for input voltage bus applications.

# Output Capacitors: C2(Required), C3(Optional)

The ESR of the required capacitor (C<sub>2</sub>) must not be greater than  $150 \text{m}\Omega$ . Electrolytic capacitors have poor ripple performance at frequencies greater than 400 kHz but excellent low frequency transient response. Above the ripple frequency, ceramic capacitors are necessary to improve the transient response and reduce any high frequency noise components apparent during higher current excursions. Preferred low ESR type capacitor part numbers are identified in Table 1. The optional  $100 \mu\text{F}$  capacitor (C<sub>3</sub>) for Vo<sub>2</sub> can have an ESR of up to  $200 \text{m}\Omega$  for optimum performance and ripple reduction. (Note: Vendor part numbers for the optional capacitor, C<sub>3</sub>, are not identified in the table. Use the same series selected for C<sub>2</sub>)

#### **Tantalum Capacitors**

Tantalum type capacitors can be used for the output but only the AVX TPS series, Sprague 593D/594/595 series or Kemet T495/T510 series. The AVX TPS series, Kemet or Sprague series tantalums are recommended over many other types due to their higher rated surge, power dissipation, and ripple current capability. As a caution the TAJ series by AVX is not recommended. This series has considerably higher ESR, reduced power dissipation and lower ripple current capability. The TAJ Series is a less reliable when compared to the AVX TPS series when determining power dissipation capability. Tantalum types are recommended for applications where ambient temperatures fall below 0°C.

#### **Capacitor Table**

Table 1 identifies the characteristics of capacitors from a number of vendors with acceptable ESR and ripple current (rms) ratings. The number of capacitors required at both the input and output buses is identified for each capacitor type.

This is not an extensive capacitor list. Capacitors from other vendors are available with comparable specifications. Those listed are for guidance. The RMS ripple current rating and ESR (Equivalent Series Resistance at 100kHz) are critical parameters necessary to insure both optimum regulator performance and long capacitor life.

Table 1: Input/Output Capacitors

Capacitor Vendor/			Capacitor (	Characteristics		Qua	entity	
Component Series	Worlding Voltage	Value(μF)	(ESR) Equivalent Series Resistance	85°C Maximum Ripple Current(Irms)	Physical Size(mm)	Input Bus	Output Bus	Vendor Number
Panasonic FC	25V 35V 35V	560µF 390µF 330µF	0.0065W 0.065W 0.117W	1205mA 1205mA 555mA	12.5x15 12.5x15 8x11.5	1 2 (a)	1 1 1	EEUFC1E561S EEUFC1V391S EEUFC1C331
United Chemi -con LXV/FS/ LXZ	16V 35V 10V 20V	330µF 470µF 330µF 150µF	0.120W 0.052W 0.025W 0.030/2W	555mA 1220mA 3500mA 3200mA	8x12 10x20 10x10.5 10x10.5	(a) 1 1 2	1 (N/R) (N/R)	LXZ16VB331M8X12LL LXZ35VB471M10X20LL 10FS330M 20FS150M
Nichicon PL PM	35V 35V 50V	560µF 330µF 470µF	0.048W 0.065/2W 0.046W	1360mA 1020mA 1470mA	16x15 12.5x15 18x15	1 1 1	1 1 1	UPL1V561MHH6 UPL1V331MHH6 UPM1H4711MHH6
Panasonic FC Surface Mtg	10V 35V 16V	1000μF 330μF 330μF	0.043W 0.065W 0.150W	1205mA 1205mA 670mA	12x16.5 12.5x16 10x10.2	1 1 (a)	1 1 1	EEVFC1A102LQ EEVFC1V331LQ EEVFC1C331P
Oscon- SS SV	10V 10V 20V	330µF 330µF 150µF	0.025W 0.025W 0.024/2W	>3500mA >3800mA 3600mA	10.0x10.5 10.3x10.3 10.3x10.3	1 1 2	(N/R) (N/R) (N/R)	10SS330M 10SV300M 20SV150M SV= Surface Mount
AVX Tantalum TPS	10V 10V 10V	330µF 330µF 220µF	0.100/2W 0.100/2W 0.095W	>2500mA >3000mA >2000mA	7.3Lx 4.3Wx 4.1H	2 2 2	1 1 2	TPSV337M010R0100 TPSV337M010R0060 TPSV227M0105R0100
Kemet T510 T495	10V 10V	330μF 220μF	0.033W 0.070W/2=0.035W	1400mA >2000mA	7.3Lx5.7W x 4.0H	2 2	1 2	T510X337M010AS T495X227M010AS
Sprague 594D	10V 10V	330µF 220µF	0.0450W 0.065W	2350mA >2000mA	7.3Lx 6.0Wx 4.1H	2 2	1 2	4D337X0010R2T 594D227X0010D2T

(a) -Not recommended. The maximum ripple current rating of these capacitors does not meet the operating limits. (N/R) -Oscon Type Capcitors are not recommended for this application due to extremely low equivatlent series resistance (ESR)



# PACKAGE OPTION ADDENDUM

www.ti.com 26-Aug-2009

#### PACKAGING INFORMATION

Orderable Device	Status <sup>(1)</sup>	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp <sup>(3)</sup>
PT6931A	ACTIVE	SIP MOD ULE	ELG	23	10	Pb-Free (RoHS)	Call TI	N / A for Pkg Type
PT6931C	ACTIVE	SIP MOD ULE	ELH	23	10	Pb-Free (RoHS)	Call TI	Level-3-215C-168HRS
PT6931N	ACTIVE	SIP MOD ULE	ELF	23	10	Pb-Free (RoHS)	Call TI	N / A for Pkg Type
PT6932A	ACTIVE	SIP MOD ULE	ELG	23	10	Pb-Free (RoHS)	Call TI	N / A for Pkg Type
PT6932C	ACTIVE	SIP MOD ULE	ELH	23	10	Pb-Free (RoHS)	Call TI	Level-3-215C-168HRS
PT6932N	ACTIVE	SIP MOD ULE	ELF	23	10	Pb-Free (RoHS)	Call TI	N / A for Pkg Type
PT6933A	ACTIVE	SIP MOD ULE	ELG	23	10	Pb-Free (RoHS)	Call TI	N / A for Pkg Type
PT6933C	ACTIVE	SIP MOD ULE	ELH	23	10	Pb-Free (RoHS)	Call TI	Level-3-215C-168HRS

<sup>(1)</sup> The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

**Pb-Free** (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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