# LOW NOISE, VERY LOW DRIFT, PRECISION VOLTAGE REFERENCE

**Check for Samples: REF5025-HT**

## FEATURES

- **Low Temperature Drift: 20 ppm/°C**
- **Low Noise: 3 μV$_{PP}$/V**
- **High Output Current: ±7 mA**

## APPLICATIONS

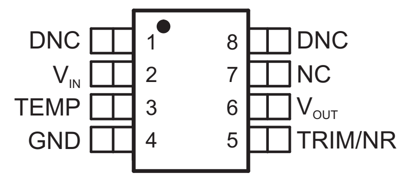
- **Down-Hole Drilling**
- **High Temperature Environments**

## SUPPORTS EXTREME TEMPERATURE APPLICATIONS

- **Controlled Baseline**
- **One Assembly/Test Site**
- **One Fabrication Site**
- **Available in Extreme (–55°C/210°C) Temperature Range**(1)
- **Extended Product Life Cycle**
- **Extended Product-Change Notification**
- **Product Traceability**
- **Texas Instruments high temperature products utilize highly optimized silicon (die) solutions with design and process enhancements to maximize performance over extended temperatures.**

(1) Custom temperature ranges available

**HKJ PACKAGE**
**(TOP VIEW)**

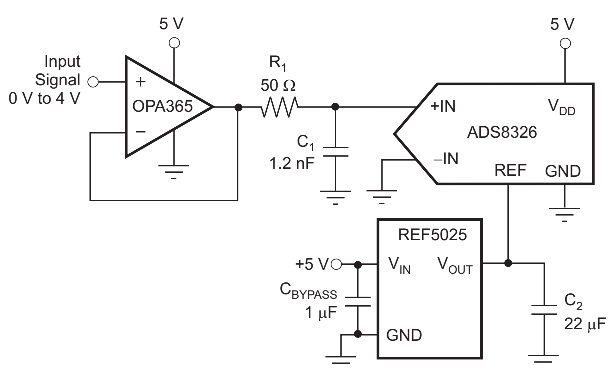



DNC = Do not connect
NC = No internal connection

## DESCRIPTION

The REF5025 is a low-noise, low-drift, very high precision voltage reference. This reference is capable of both sinking and sourcing, and is very robust with regard to line and load changes.

Temperature drift (20 ppm/°C) from –55°C to 210°C is achieved using proprietary design techniques. These features combined with very low noise make the REF5025 ideal for use in down-hole drilling applications.

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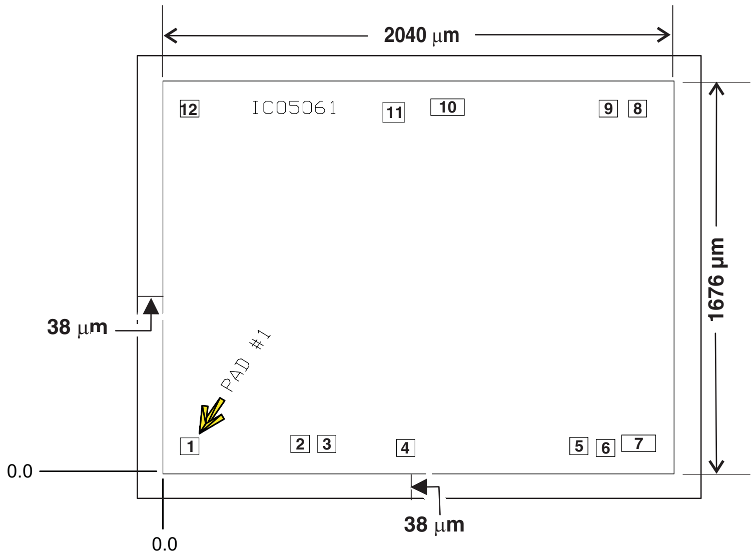
This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

## BARE DIE INFORMATION

| DIE THICKNESS | BACKSIDE FINISH | BACKSIDE POTENTIAL | BOND PAD METALLIZATION COMPOSITION | BOND PAD THICKNESS |
|---|---|---|---|---|
| 15 mils. | Silicon with backgrind | GND | Al-Cu (0.5%) | 598 nm |




### Table 1. Bond Pad Coordinates in Microns

| DISCRIPTION | PAD NUMBER | X min | Y min | X max | Y max |
|---|---|---|---|---|---|
| NC | 1 | 35.45 | 46.55 | 111.45 | 122.55 |
| NC | 2 | 496.75 | 56.55 | 572.75 | 132.55 |
| VIN | 3 | 607.45 | 56.55 | 683.45 | 132.55 |
| NC | 4 | 937.9 | 39.4 | 1013.9 | 115.4 |
| TEMP | 5 | 1660.1 | 47.2 | 1736.1 | 123.2 |
| GND | 6 | 1770.9 | 38.85 | 1847.05 | 115 |
| GND | 7 | 1877.1 | 59.6 | 2016.8 | 135.6 |
| TRIM/NR | 8 | 1904.65 | 1553.4 | 1980.65 | 1629.4 |
| NC | 9 | 1782.15 | 1553.4 | 1858.15 | 1629.4 |
| VOUT | 10 | 1080.2 | 1559.85 | 1219.9 | 1636 |
| VOUT | 11 | 880.25 | 1543.55 | 956.25 | 1619.55 |
| NC | 12 | 35.45 | 1553.45 | 111.45 | 1629.45 |

## ORDERING INFORMATION(1)

| $T_A$ | PACKAGE(2) | ORDERABLE PART NUMBER | TOP-SIDE MARKING |
|---|---|---|---|
| –55°C to 210°C | KGD (bare die) | REF5025SKGD1 | NA |
| | HKJ | REF5025SHKJ | REF5025SHKJ |

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.
(2) Package drawings, thermal data, and symbolization are available at www.ti.com/packaging.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## ABSOLUTE MAXIMUM RATINGS(1)

| | | | UNIT |
|---|---|---|---|
| Input Voltage | | 18 | V |
| Output Short-Circuit | | 30 | mA |
| Operating Temperature Range | | –55 to 210 | °C |
| Storage Temperature Range | | –65 to 210 | °C |
| Junction Temperature ($T_J$ max) | | 210 | °C |
| ESD Rating | Human Body Model (HBM) | 3000 | V |
| | Charged Device Model (CDM) | 1000 | V |

(1) Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those specified is not implied.

## THERMAL CHARACTERISTICS FOR HKJ PACKAGE

over operating free-air temperature range (unless otherwise noted)

| PARAMETER | | | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $\theta_{JC}$ | Junction-to-case thermal resistance | to bottom of case | | | 5.7 | °C/W |
| | | to top of case lid - as if formed dead bug | | | 13.7 | |

## ELECTRICAL CHARACTERISTICS

$T_A$ = 25°C, $I_{LOAD}$ = 0, $C_L$ = 1 µF, $V_{IN}$ = 3.25 V to 18 V (unless otherwise noted).

| PARAMETER | | CONDITIONS | $T_A$ = –55 to 125°C | | | $T_A$ = 210°C | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | MIN | TYP | MAX | MIN | TYP | MAX | |
| **OUTPUT VOLTAGE (2.5 V)** | | | | | | | | | |
| Output voltage | $V_{OUT}$ | | | 2.5 | | | 2.5 | | V |
| Initial accuracy(1) | | $V_{IN}$ = 3.25 V | 0 | | 0.9 | | 0.14 | | % |
| **NOISE** | | | | | | | | | |
| Output voltage noise | | f = 0.1 Hz to 10 Hz | | 7.5 | | | | | $\mu V_{PP}$ |
| **OUTPUT VOLTAGE TEMPERATURE DRIFT** | | | | | | | | | |
| Output voltage temperature drift(2) | $dV_{OUT}/dT$ | Calculated from –55°C to 210°C | | | | | 20 | | ppm/°C |
| **LINE REGULATION** | | | | | | | | | |
| Line regulation | $dV_{OUT}/dV_{IN}$ | From $V_{IN}$ = 3.25 V to $V_{IN}$ = 18 V | | 1 | 2.2 | | 63 | 215 | ppm/V |
| **LOAD REGULATION** | | | | | | | | | |
| Load regulation | $dV_{OUT}/dI_{LOAD}$ | –7 mA < $I_{LOAD}$ < 10 mA, $V_{IN}$ = 3.25 V | | 20 | 50 | | 20 | 75 | ppm/mA |
| **SHORT-CIRCUIT CURRENT** | | | | | | | | | |
| Short-circuit current | $I_{SC}$ | $V_{OUT}$ = 0 V | | 25 | | | 11 | | mA |
| **TEMP PIN** | | | | | | | | | |
| Voltage output | | At $T_A$ = 25°C | | 575 | | | | | mV |
| Temperature sensitivity(3) | | | | 2.64 | | | | | mV/°C |
| **TURN-ON SETTLING TIME** | | | | | | | | | |
| Turn-on settling time | | To 0.1% with $C_L$ = 1 µF | | 200 | | | | | µs |
| **POWER SUPPLY** | | | | | | | | | |
| Supply voltage | $V_S$ | | 3.25 | | 18 | 3.25 | | 18 | V |
| Quiescent current | | | | 0.8 | 1.2 | | | 1.5 | mA |
| **TEMPERATURE RANGE** | | | | | | | | | |
| Specified range | | –55°C to 210°C | | | | | | | |

(1) Refer to Figure 5 of the TYPICAL CHARACTERISTICS.
(2) Refer to Figure 4 of the TYPICAL CHARACTERISTICS.
(3) Refer to Figure 10 of the TYPICAL CHARACTERISTICS.

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## ELECTRICAL CHARACTERISTICS (continued)

$T_A$ = 25°C, $I_{LOAD}$ = 0, $C_L$ = 1 µF, $V_{IN}$ = 3.25 V to 18 V (unless otherwise noted).

| PARAMETER | CONDITIONS | $T_A$ = –55 to 125°C | | | $T_A$ = 210°C | | | UNIT |
|---|---|---|---|---|---|---|---|---|
| | | MIN | TYP | MAX | MIN | TYP | MAX | |
| Operating range | –55°C to 210°C | | | | | | | |


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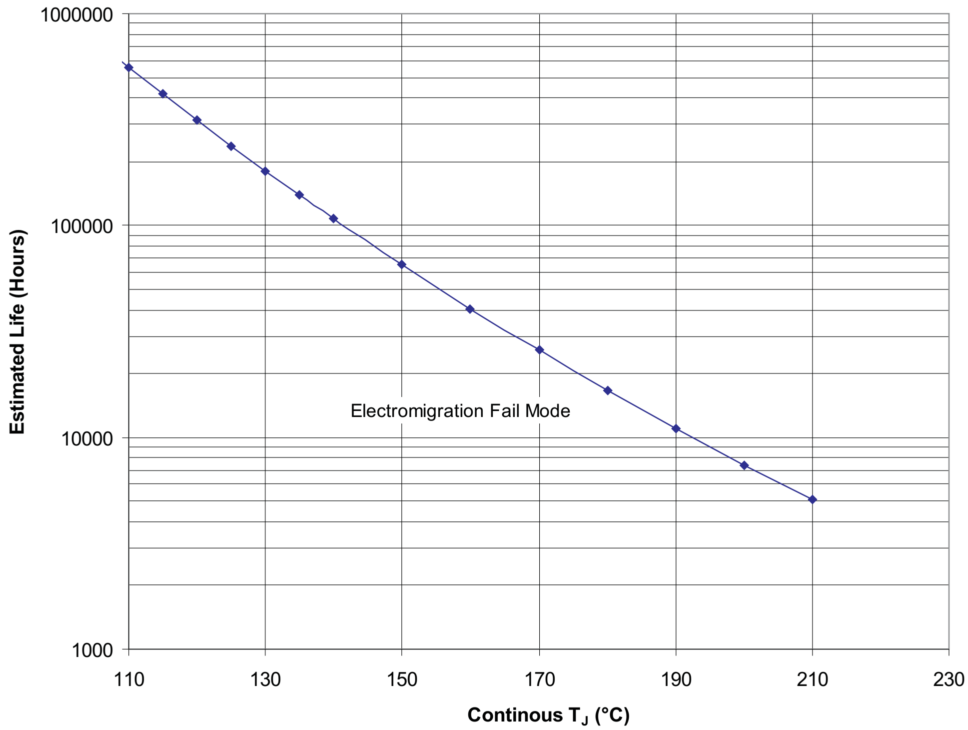


**Figure 1. REF5025SKGD1 Operating Life Derating Chart**

Notes:

1. See datasheet for Absolute Maximum and minimum Recommended Operating Conditions.
2. Silicon operating life design goal is 10 years at 105°C junction temperature ( does not include package interconnect life).

## TYPICAL CHARACTERISTICS

$T_A$ = 25°C, $I_{LOAD}$ = 0, $V_S$ = 3.25 V (unless otherwise noted).

**TEMPERATURE DRIFT (0°C to 85°C)**

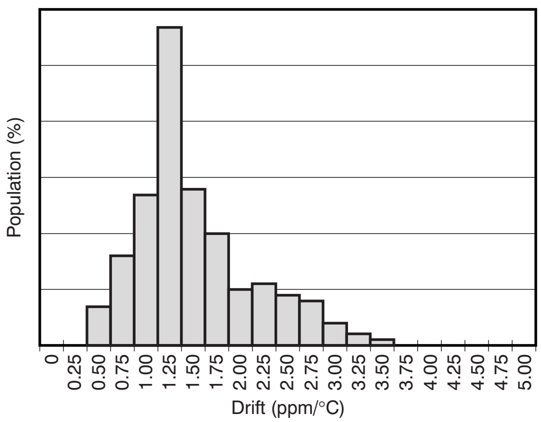


**Figure 2.**

**TEMPERATURE DRIFT (–40°C to 125°C)**

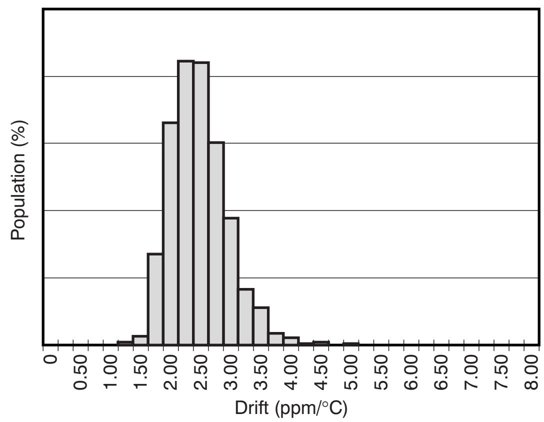


**Figure 3.**


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## TYPICAL CHARACTERISTICS (continued)

$T_A$ = 25°C, $I_{LOAD}$ = 0, $V_S$ = 3.25 V (unless otherwise noted).

**TEMPERATURE DRIFT**
**(–55°C to 210°C)**

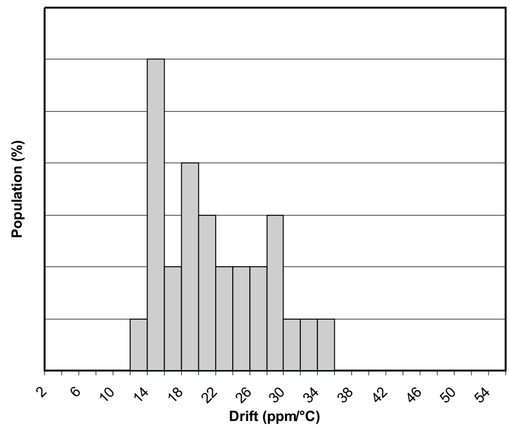


**Figure 4.**

**OUTPUT VOLTAGE**
**INITIAL ACCURACY**
**(AT 210°C)**

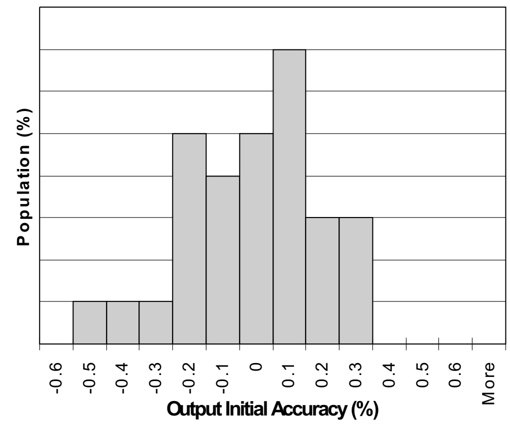


**Figure 5.**

**OUTPUT VOLTAGE ACCURACY**
**vs**
**TEMPERATURE**

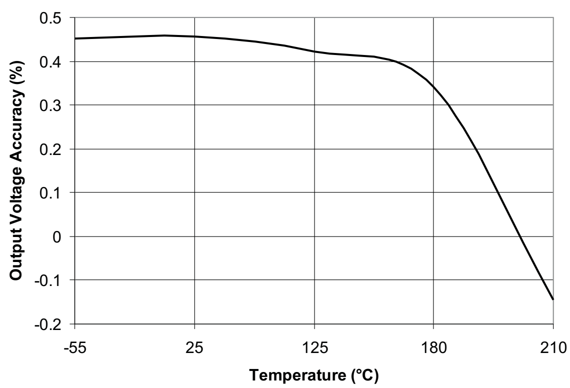


**Figure 6.**

**POWER-SUPPLY REJECTION RATIO**
**vs**
**FREQUENCY**

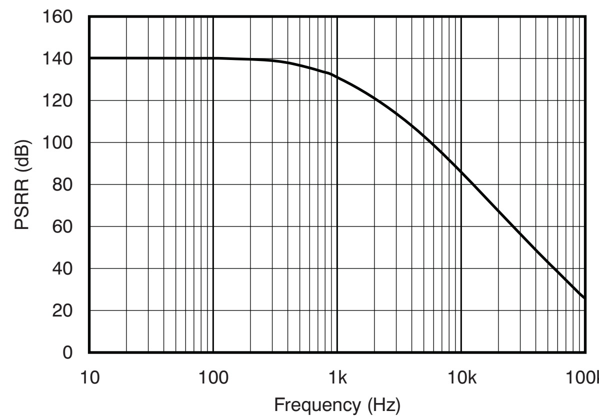


**Figure 7.**


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## TYPICAL CHARACTERISTICS (continued)

$T_A$ = 25°C, $I_{LOAD}$ = 0, $V_S$ = 3.25 V (unless otherwise noted).

**DROPOUT VOLTAGE vs LOAD CURRENT**

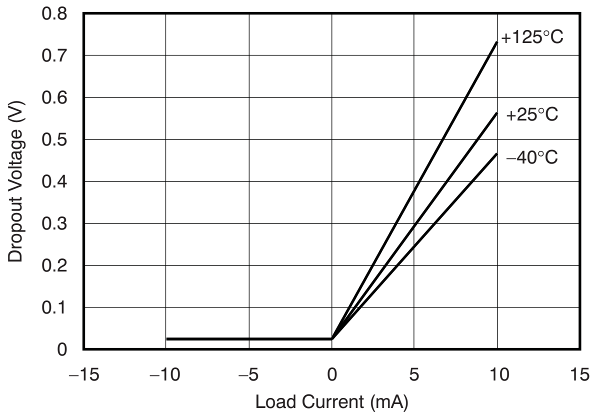


**Figure 8.**

**OUTPUT VOLTAGE vs LOAD CURRENT**

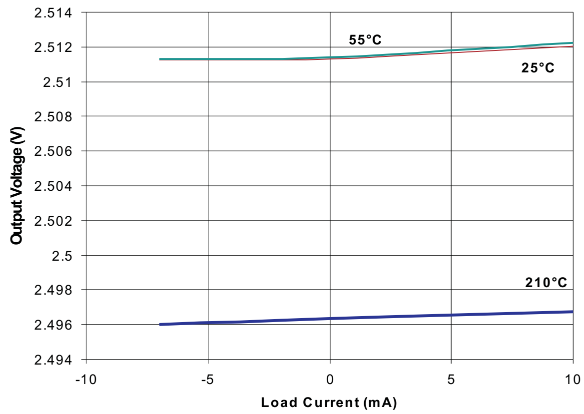


**Figure 9.**

**TEMP PIN OUTPUT VOLTAGE vs TEMPERATURE**

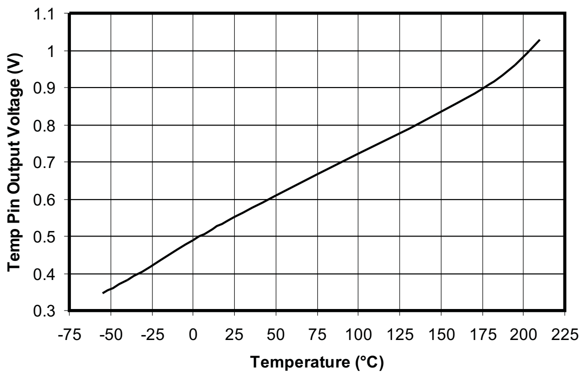


**Figure 10.**

**QUIESCENT CURRENT vs TEMPERATURE**

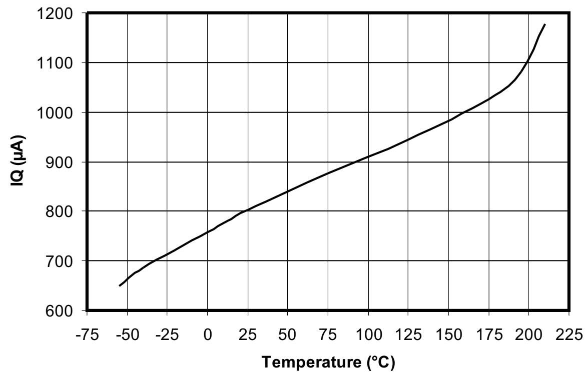


**Figure 11.**


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## TYPICAL CHARACTERISTICS (continued)

$T_A$ = 25°C, $I_{LOAD}$ = 0, $V_S$ = 3.25 V (unless otherwise noted).

**QUIESCENT CURRENT vs INPUT VOLTAGE**

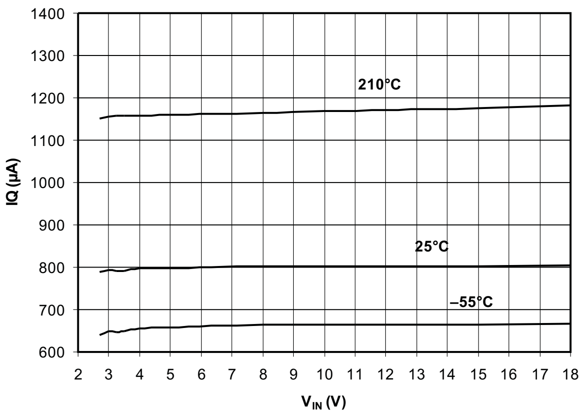


**Figure 12.**

**LINE REGULATION vs TEMPERATURE**

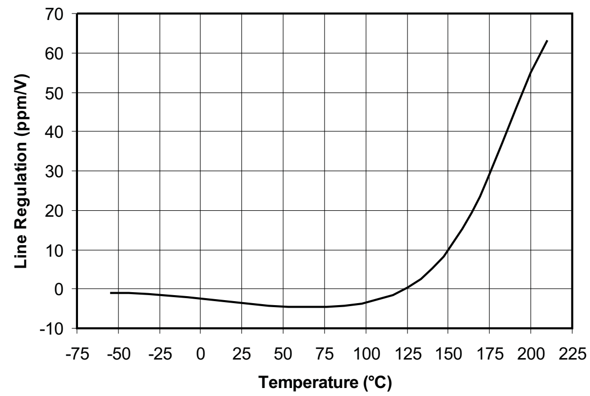


**Figure 13.**

**SHORT-CIRCUIT CURRENT vs TEMPERATURE**

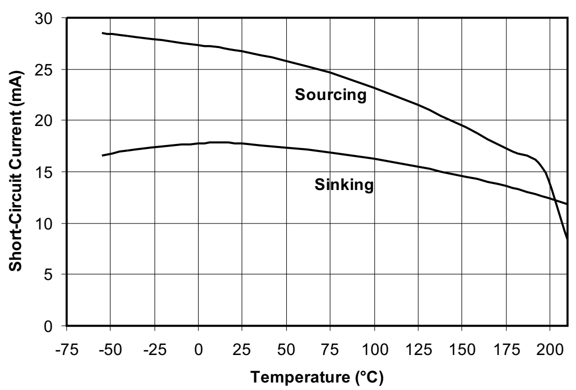


**Figure 14.**

**NOISE**

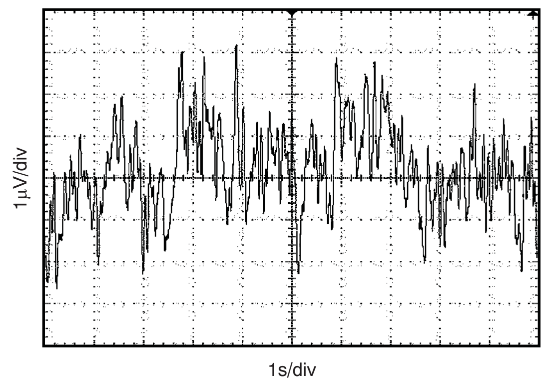


**Figure 15.**

**STARTUP (REF5025, $C_L$ = 1 µF)**

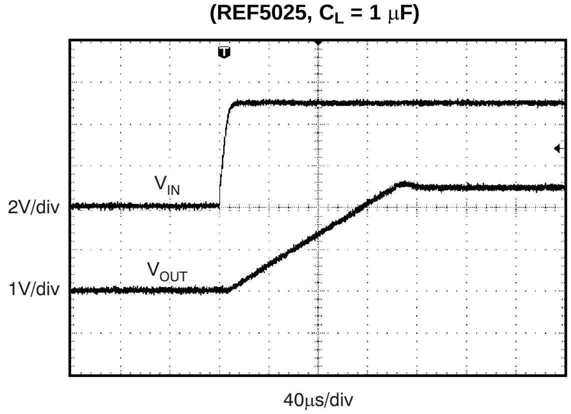


**Figure 16.**

**STARTUP (REF5025, $C_L$ = 10 µF)**

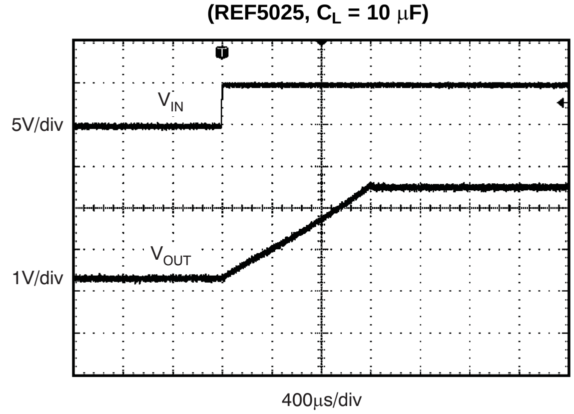


**Figure 17.**


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## TYPICAL CHARACTERISTICS (continued)

$T_A$ = 25°C, $I_{LOAD}$ = 0, $V_S$ = 3.25 V (unless otherwise noted).

**LOAD TRANSIENT ($C_L$ = 1 μF, $I_{OUT}$ = 1 mA)**

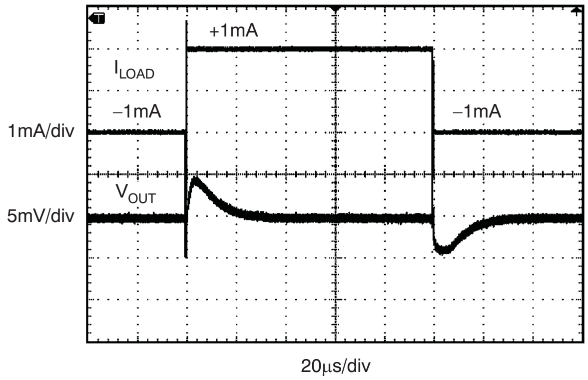


**Figure 18.**

**LOAD TRANSIENT ($C_L$ = 1 μF, $I_{OUT}$ = 10 mA)**

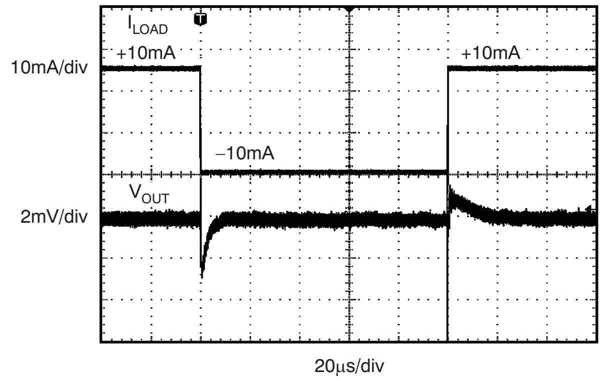


**Figure 19.**

**LOAD TRANSIENT ($C_L$ = 10 μF, $I_{OUT}$ = 1 mA)**

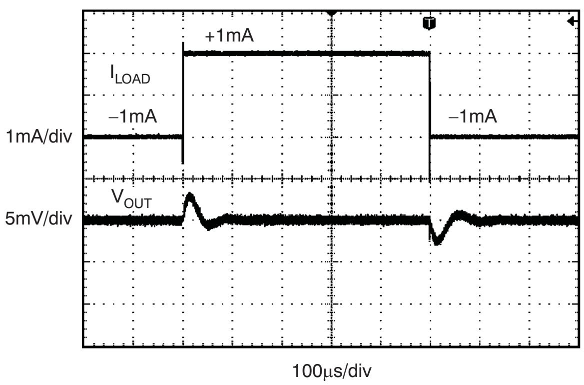


**Figure 20.**

**LOAD TRANSIENT ($C_L$ = 10 μF, $I_{OUT}$ = 10 mA)**

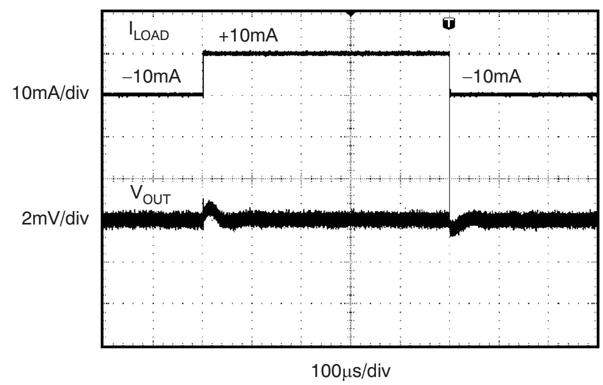


**Figure 21.**

**LINE TRANSIENT ($C_L$ = 1 μF)**

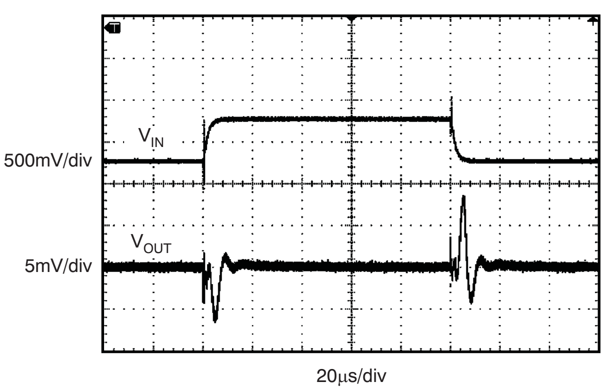


**Figure 22.**

**LINE TRANSIENT ($C_L$ = 10 μF)**

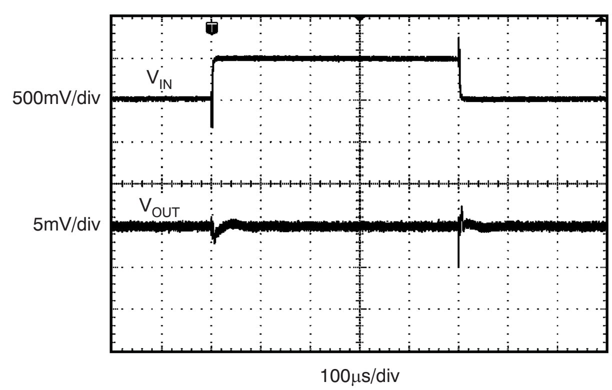


**Figure 23.**


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## APPLICATION INFORMATION

The REF5025 is a low-noise, precision bandgap voltage reference that is specifically designed for excellent initial voltage accuracy and drift. Figure 24 shows a simplified block diagram of the REF5025.

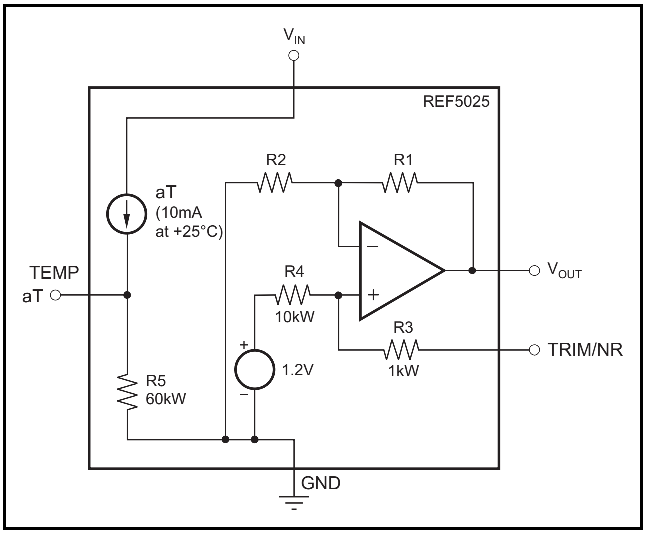


**Figure 24. REF5025 Simplified Block Diagram**

## BASIC CONNECTIONS

Figure 25 shows the typical connections for the REF5025. A supply bypass capacitor ranging between 1 μF to 10 μF is recommended. A 1-μF to 50-μF, low-ESR output capacitor ($C_L$) must be connected from $V_{OUT}$ to GND. The ESR value should be less than or equal to 1.5 Ω. The ESR minimizes gain peaking of the internal 1.2-V reference and thus reduces noise at the $V_{OUT}$ pin.

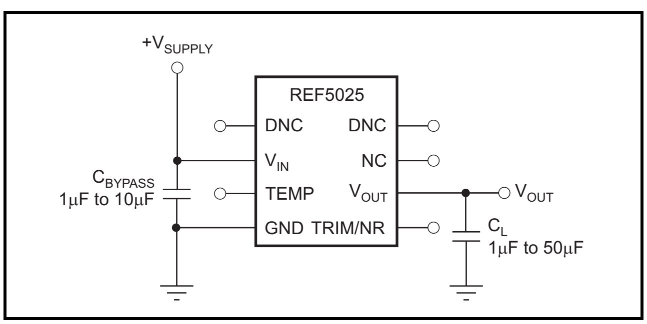


**Figure 25. Basic Connections**

## SUPPLY VOLTAGE

The REF5025 features extremely low dropout voltage. For loaded conditions, a typical dropout voltage versus load plot is shown in Figure 8 of *Typical Characteristics*.

## USING THE TRIM/NR PIN

The REF5025 provides a very accurate voltage output. However, $V_{OUT}$ can be adjusted to reduce noise and shift the output voltage from the nominal value by configuring the trim and noise reduction pin (TRIM/NR, pin 5). The TRIM/NR pin provides a ±15-mV adjustment of the device bandgap, which produces a ±15-mV change on the $V_{OUT}$ pin. Figure 26 shows a typical circuit using the TRIM/NR pin to adjust $V_{OUT}$. When using this technique, the temperature coefficients of the resistors can degrade the temperature drift at the output.

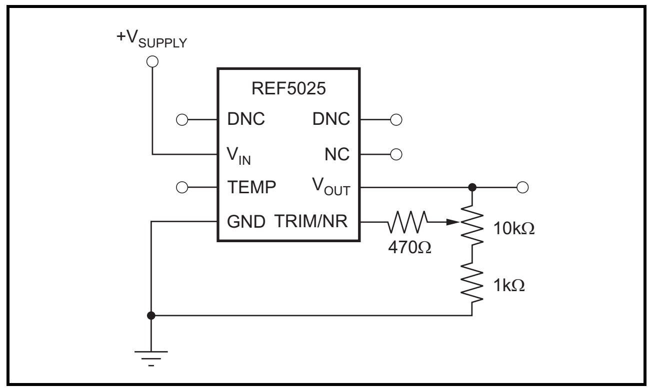


**Figure 26. $V_{OUT}$ Adjustment Using TRIM/NR Pin**

The REF5025 allows access to the bandgap through the TRIM/NR pin. Placing a capacitor from the TRIM/NR pin to GND (as Figure 27 illustrates) in combination with the internal 1-kΩ resistor creates a low-pass filter that lowers the overall noise measured on the $V_{OUT}$ pin. A capacitance of 1 μF is suggested for a low-pass filter with a corner frequency of 14.5 Hz. Higher capacitance results in a lower cutoff frequency.

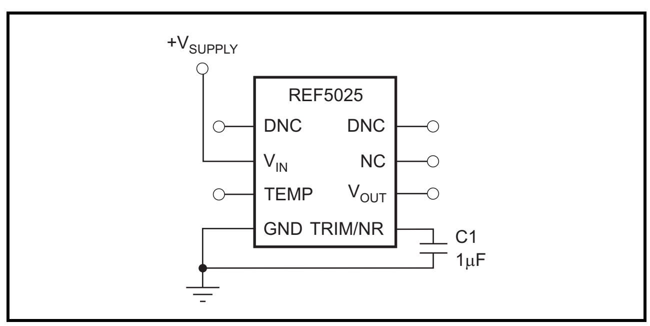


**Figure 27. Noise Reduction Using TRIM/NR Pin**

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## TEMPERATURE DRIFT

The REF5025 is designed for minimal drift error, which is defined as the change in output voltage over temperature. The drift is calculated using the box method, as described by the following equation:

$$\text{Drift} = \left(\frac{V_{OUTMAX} - V_{OUTMIN}}{V_{OUT} \times \text{Temp Range}}\right) \times 10^6 (\text{ppm}) \quad (1)$$

## TEMPERATURE MONITORING

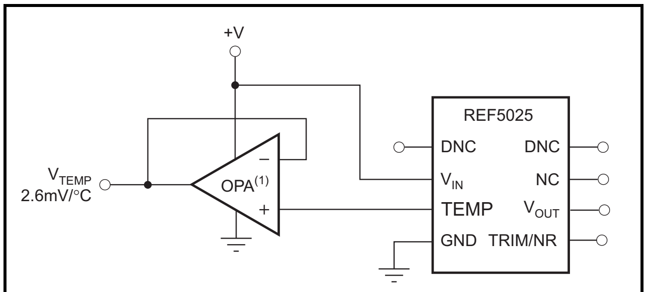
The temperature output terminal (TEMP, pin 3) provides a temperature-dependent voltage output with approximately 60-kΩ source impedance. As seen in Figure 10, the output voltage follows the nominal relationship:

$$V_{TEMP\ PIN} = 509\text{ mV} + 2.64 \times T(°C) \quad (2) \quad (2)$$

(For –55°C to 125°C only. Refer to Figure 10 of the TYPICAL CHARACTERISTICS for 125°C to 210°C.)

This pin indicates general chip temperature, accurate to approximately ±15°C. Although it is not generally suitable for accurate temperature measurements, it can be used to indicate temperature changes or for temperature compensation of analog circuitry. A temperature change of 30°C corresponds to an approximate 79-mV change in voltage at the TEMP pin.

The TEMP pin has high output impedance (see Figure 24). Loading this pin with a low-impedance circuit induces a measurement error; however, it does not have any effect on $V_{OUT}$ accuracy. To avoid errors caused by low-impedance loading, buffer the TEMP pin output with a suitable low-temperature drift op amp, such as the OPA333, OPA335, or OPA376, as shown in Figure 28.




NOTE: (1) Low drift op amp, such as the OPA333, OPA335, or OPA376.

**Figure 28. Buffering the TEMP Pin Output**

## POWER DISSIPATION

The REF5025 is specified to deliver current loads of ±10 mA over the specified input voltage range. The temperature of the device increases according to the equation:

$$T_J = T_A + P_D \times \theta_{JA} \quad (3) \quad (3)$$

Where:

$T_J$ = Junction temperature (°C)

$T_A$ = Ambient temperature (°C)

$P_D$ = Power dissipated (W)

$\theta_{JA}$ = Junction-to-ambient thermal resistance (°C/W)

The REF5025 junction temperature must not exceed the absolute maximum rating of 210°C.

## NOISE PERFORMANCE

Typical 0.1-Hz to 10-Hz voltage noise for each member of the REF5025 is specified in the Electrical Characterisitics table. The noise voltage increases with output voltage and operating temperature. Additional filtering can be used to improve output noise levels, although care should be taken to ensure the output impedance does not degrade performance.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## APPLICATION CIRCUITS

### NEGATIVE REFERENCE VOLTAGE

For applications requiring a negative and positive reference voltage, the REF5025 and OPA735 can be used to provide a dual-supply reference from a 5-V supply. Figure 29 shows the REF5025 used to provide a 2.5-V supply reference voltage. The low drift performance of the REF5025 complements the low offset voltage and zero drift of the OPA735 to provide an accurate solution for split-supply applications. Care must be taken to match the temperature coefficients of $R_1$ and $R_2$.

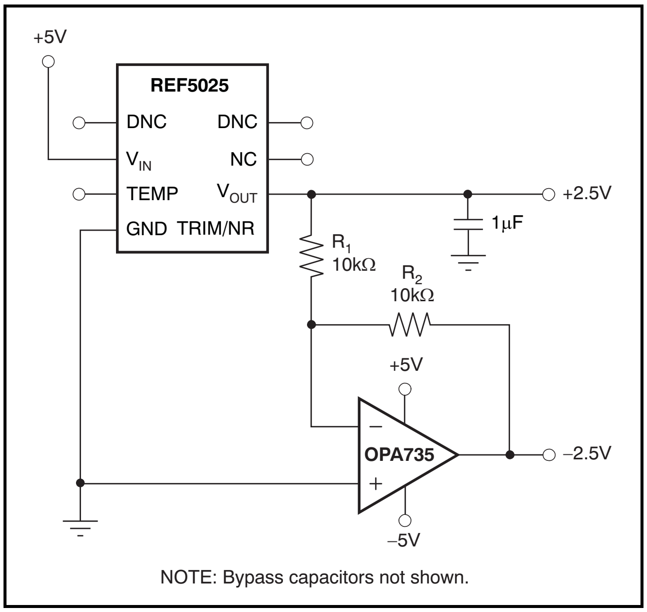


**Figure 29. The REF5025 and OPA735 Create Positive and Negative Reference Voltages**

### DATA ACQUISITION

Data acquisition systems often require stable voltage references to maintain accuracy. The REF5025 features low noise, very low drift, and high initial accuracy for high-performance data converters. Figure 30 shows the REF5025 in a basic data acquisition system.

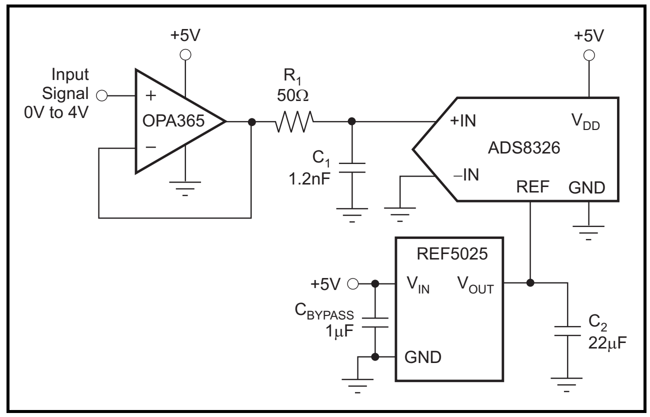


**Figure 30. Basic Data Acquisition System**


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## PACKAGING INFORMATION

| Orderable Device | Status [1] | Package Type | Package Drawing | Pins | Package Qty | Eco Plan [2] | Lead/Ball Finish | MSL Peak Temp [3] |
|---|---|---|---|---|---|---|---|---|
| REF5025SHKJ | ACTIVE | CFP | HKJ | 8 | 1 | TBD | Call TI | N / A for Pkg Type |
| REF5025SKGD1 | ACTIVE | XCEPT | KGD | 0 | 195 | TBD | Call TI | N / A for Pkg Type |

[1] The marketing status values are defined as follows:
**ACTIVE:** Product device recommended for new designs.
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
**OBSOLETE:** TI has discontinued the production of the device.

[2] Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
**TBD:** The Pb-Free/Green conversion plan has not been defined.
**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

[3] MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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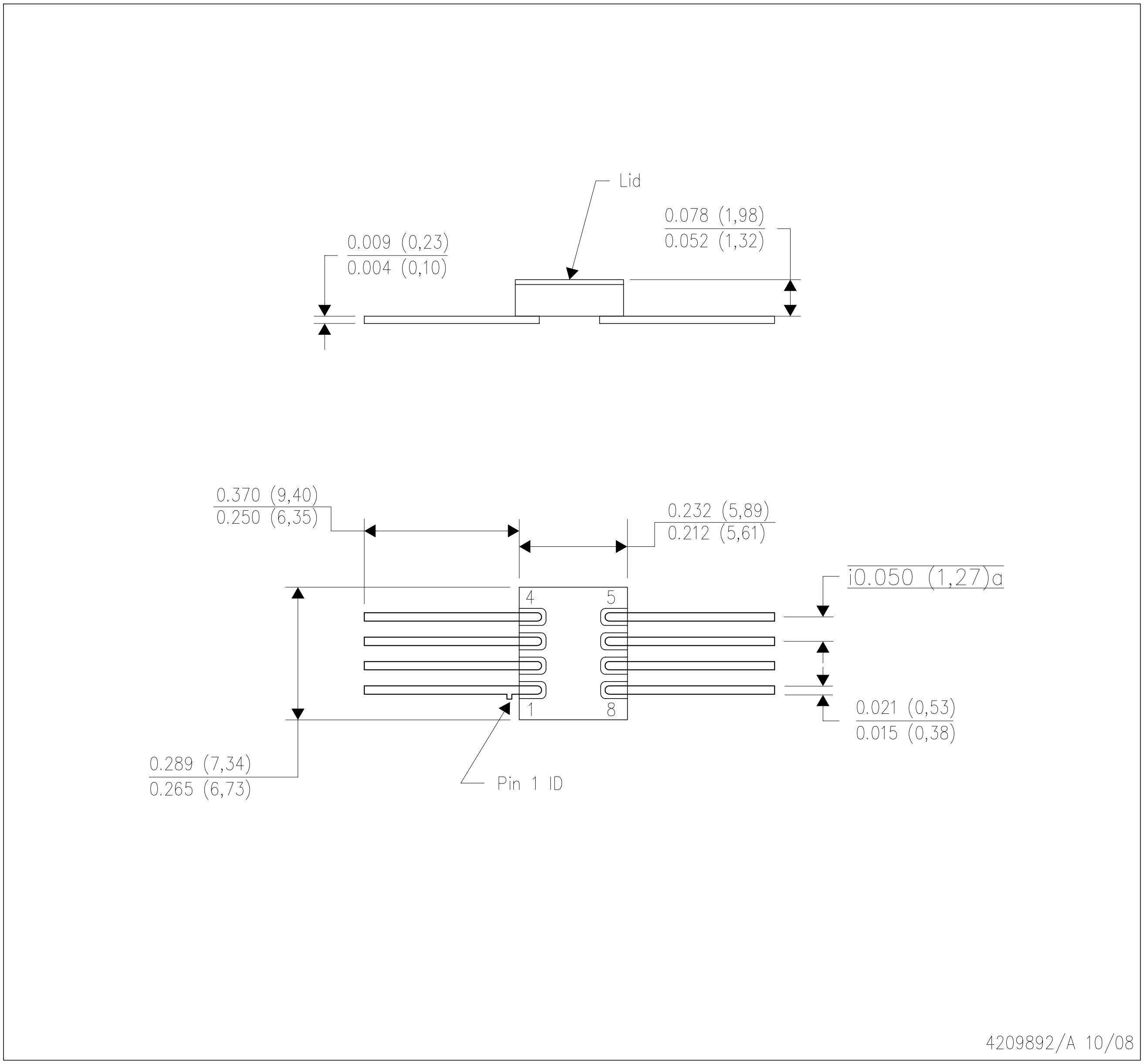
HKJ (R–CDFP–F8) CERAMIC DUAL FLATPACK




NOTES:
- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. This package can be hermetically sealed with a metal lid.
- D. The terminals will be gold plated.



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