- **Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Plastic and Ceramic DIPs**
- **Dependable Texas Instruments Quality and Reliability**

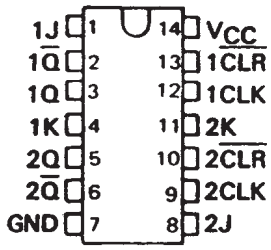
## description

The '107 contain two independent J-K flip-flops with individual J-K, clock, and direct clear inputs. The '107 is a positive pulse-triggered flip-flop. The J-K input data is loaded into the master while the clock is high and transferred to the slave and the outputs on the high-to-low clock transistion. For these devices the J and K inputs must be stable while the clock is high.

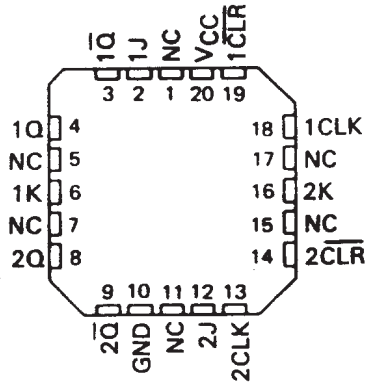
The 'LS107A contain two independent negative-edge-triggered flip-flops. The J and K inputs must be stable prior to the high-to-low clock transition for predictable operation. When the clear is low, it overrides the clock and data inputs forcing the Q output low and the $\overline{Q}$ output high.

The SN54107 and the SN54LS107A are characterized for operation over the full military temperature range of −55°C to 125°C. The SN74107 and the SN74LS107A are characterized for operation from 0°C to 70°C.

**SN54107, SN54LS107A . . . J PACKAGE**
**SN74107 . . . N PACKAGE**
**SN74LS107A . . . D OR N PACKAGE**
**(TOP VIEW)**




**SN54LS107A . . . FK PACKAGE**
**(TOP VIEW)**




NC – No internal connection

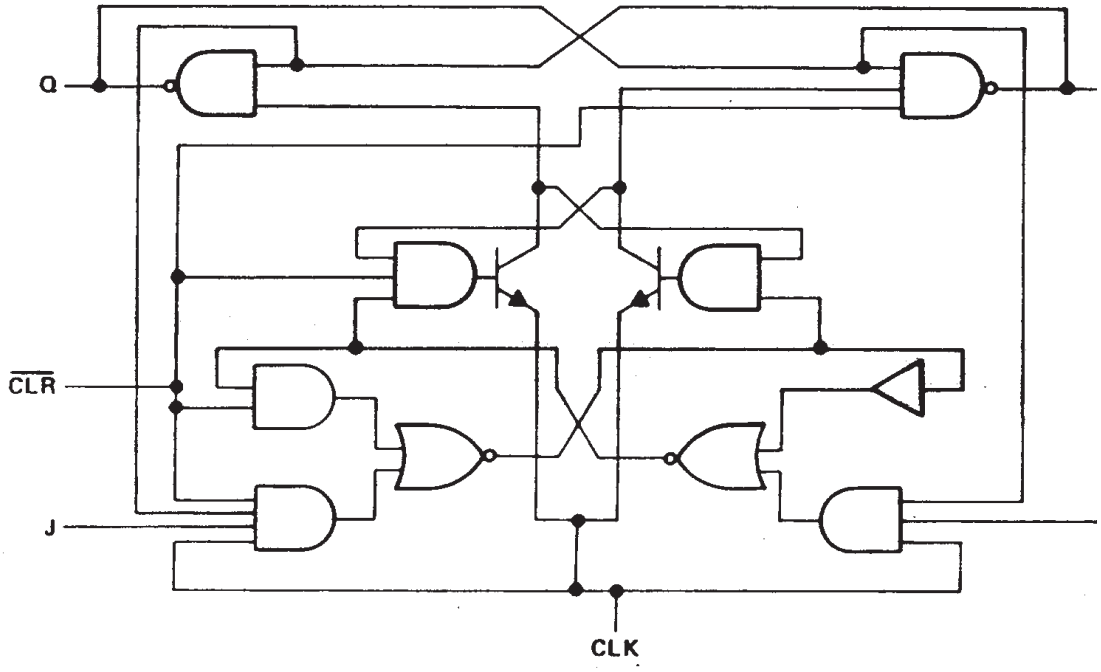
**'107**
**FUNCTION TABLE**

| INPUTS | | | | OUTPUTS | |
|---|---|---|---|---|---|
| $\overline{CLR}$ | CLK | J | K | Q | $\overline{Q}$ |
| L | X | X | X | L | H |
| H | ⊓ | L | L | $Q_0$ | $\overline{Q}_0$ |
| H | ⊓ | H | L | H | L |
| H | ⊓ | L | H | L | H |
| H | ⊓ | H | H | TOGGLE | |

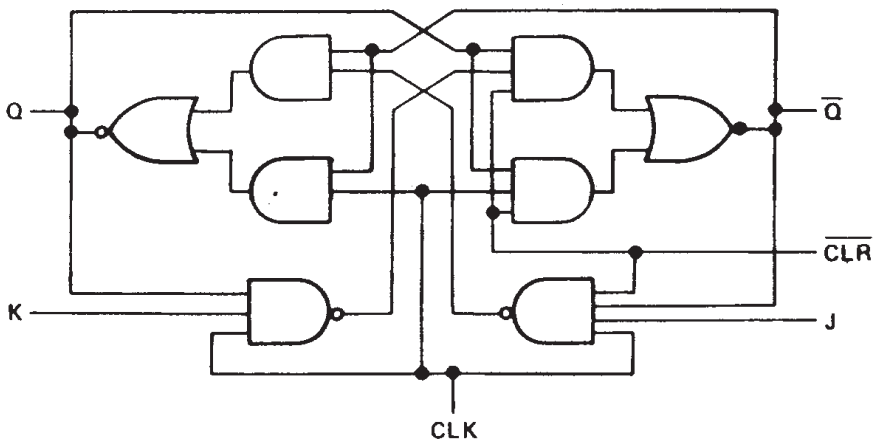
**'LS107A**
**FUNCTION TABLE**

| INPUTS | | | | OUTPUTS | |
|---|---|---|---|---|---|
| $\overline{CLR}$ | CLK | J | K | Q | $\overline{Q}$ |
| L | X | X | X | L | H |
| H | ↓ | L | L | $Q_0$ | $\overline{Q}_0$ |
| H | ↓ | H | L | H | L |
| H | ↓ | L | H | L | H |
| H | ↓ | H | H | TOGGLE | |
| H | H | X | X | $Q_0$ | $\overline{Q}_0$ |

## logic diagrams (positive logic)

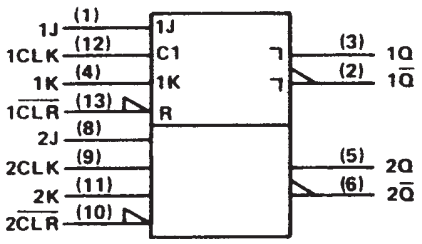



'LS107A

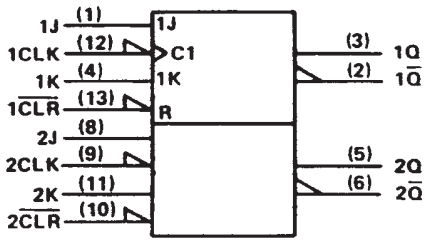


## logic symbols†

'107




'LS107A

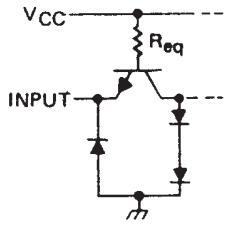



†These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for D, J, and N packages.

## schematic of inputs and outputs

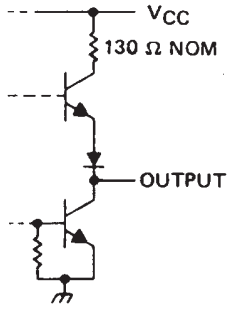
'107

EQUIVALENT OF EACH INPUT



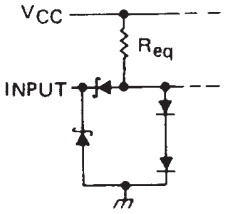

| $I_{IL}$ MAX | $R_{eq}$ NOM |
|---|---|
| – 1.6 mA | 4 kΩ |
| – 3.2 mA | 2 kΩ |

TYPICAL OF ALL INPUTS



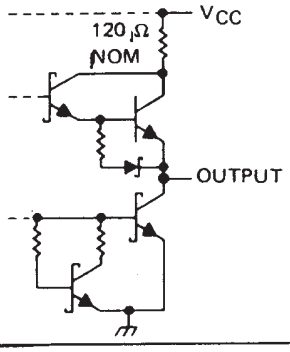

'LS107A

EQUIVALENT OF EACH INPUT




| $I_{IL}$ MAX | $R_{eq}$ NOM |
|---|---|
| – 0.4 mA | 30 kΩ |
| – 0.8 mA | 8.25 kΩ |

TYPICAL OF ALL OUTPUTS




## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, $V_{CC}$ (see Note 1) . . . . . 7 V
Input voltage: '107 . . . . . 5.5 V
'LS107A . . . . . 7 V
Operating free-air temperature range: SN54' . . . . . – 55°C to 125°C
SN74' . . . . . 0°C to 70°C
Storage temperature range . . . . . – 65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

## recommended operating conditions

| | | | SN54107 | | | SN74107 | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | MIN | NOM | MAX | MIN | NOM | MAX | |
| $V_{CC}$ | Supply voltage | | 4.5 | 5 | 5.5 | 4.75 | 5 | 5.25 | V |
| $V_{IH}$ | High-level input voltage | | 2 | | | 2 | | | V |
| $V_{IL}$ | Low-level input voltage | | | | 0.8 | | | 0.8 | V |
| $I_{OH}$ | High-level output current | | | | – 0.4 | | | – 0.4 | mA |
| $I_{OL}$ | Low-level output current | | | | 16 | | | 16 | mA |
| $t_w$ | Pulse duration | CLK high | 20 | | | 20 | | | ns |
| | | CLK low | 47 | | | 47 | | | |
| | | $\overline{CLR}$ low | 25 | | | 25 | | | |
| $t_{su}$ | Input setup time before CLK↑ | | 0 | | | 0 | | | ns |
| $t_h$ | Input hold time-data after CLK↑ | | 0 | | | 0 | | | ns |
| $T_A$ | Operating free-air temperature | | – 55 | | 125 | 0 | | 70 | °C |

## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS† | | | SN54107 | | | SN74107 | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | MIN | TYP‡ | MAX | MIN | TYP‡ | MAX | |
| $V_{IK}$ | | $V_{CC}$ = MIN, | $I_I$ = – 12 mA | | | | – 1.5 | | | – 1.5 | V |
| $V_{OH}$ | | $V_{CC}$ = MIN, $I_{OH}$ = – 0.4 mA | $V_{IH}$ = 2 V, | $V_{IL}$ = 0.8 V, | 2.4 | 3.4 | | 2.4 | 3.4 | | V |
| $V_{OL}$ | | $V_{CC}$ = MIN, $I_{OL}$ = 16 mA | $V_{IH}$ = 2 V, | $V_{IL}$ = 0.8 V, | | 0.2 | 0.4 | | 0.2 | 0.4 | V |
| $I_I$ | | $V_{CC}$ = MAX, | $V_I$ = 5.5 V | | | | 1 | | | 1 | mA |
| $I_{IH}$ | J or K | $V_{CC}$ = MAX, | $V_I$ = 2.4 V | | | | 40 | | | 40 | μA |
| | All other | | | | | | 80 | | | 80 | |
| $I_{IL}$ | J or K | $V_{CC}$ = MAX, | $V_I$ = 0.4 V | | | | – 1.6 | | | – 1.6 | mA |
| | All other | | | | | | – 3.2 | | | – 3.2 | |
| $I_{OS}$§ | | $V_{CC}$ = MAX | | | – 20 | | – 57 | – 18 | | – 57 | mA |
| $I_{CC}$¶ | | $V_{CC}$ = MAX, | See Note 2 | | | 10 | 20 | | 10 | 20 | mA |

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡All typical values are at $V_{CC}$ = 5 V, $T_A$ = 25° C.
§Not more than one output should be shorted at a time.
¶Average per flip-flop.
NOTE 2: With all outputs open, $I_{CC}$ is measured with the Q and $\overline{Q}$ outputs high in turn. At the time of measurement, the clock input is grounded.

## switching characteristics, $V_{CC}$ = 5 V, $T_A$ = 25°C (see note 3)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $f_{max}$ | | | $R_L$ = 400 Ω, $C_L$ = 15 pF | 15 | 20 | | MHz |
| $t_{PLH}$ | $\overline{CLR}$ | $\overline{Q}$ | | | 16 | 25 | ns |
| $t_{PHL}$ | | Q | | | 25 | 40 | ns |
| $t_{PLH}$ | CLK | Q or $\overline{Q}$ | | | 16 | 25 | ns |
| $t_{PHL}$ | | | | | 25 | 40 | ns |

NOTE 3: Load circuits and voltage waveforms are shown in Section 1.

## recommended operating conditions

| | | | SN54LS107A | | | SN74LS107A | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | MIN | NOM | MAX | MIN | NOM | MAX | |
| $V_{CC}$ | Supply voltage | | 4.5 | 5 | 5.5 | 4.75 | 5 | 5.25 | V |
| $V_{IH}$ | High-level input voltage | | 2 | | | 2 | | | V |
| $V_{IL}$ | Low-level input voltage | | | | 0.7 | | | 0.8 | V |
| $I_{OH}$ | High-level output current | | | | – 0.4 | | | – 0.4 | mA |
| $I_{OL}$ | Low-level output current | | | | 4 | | | 8 | mA |
| $f_{clock}$ | Clock frequency | | 0 | | 30 | 0 | | 30 | MHz |
| $t_w$ | Pulse duration | CLK high | 20 | | | 20 | | | ns |
| | | $\overline{CLR}$ low | 25 | | | 25 | | | |
| $t_{su}$ | Setup time before CLK↓ | data high or low | 20 | | | 20 | | | ns |
| | | $\overline{CLR}$ inactive | 25 | | | 25 | | | |
| $t_h$ | Hold time-data after CLK↓ | | 0 | | | 0 | | | ns |
| $T_A$ | Operating free-air temperature | | – 55 | | 125 | 0 | | 70 | °C |

## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS† | | | SN54LS107A | | | SN74LS107A | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | MIN | TYP‡ | MAX | MIN | TYP‡ | MAX | |
| $V_{IK}$ | | $V_{CC}$ = MIN, | $I_I$ = – 18 mA | | | | – 1.5 | | | – 1.5 | V |
| $V_{OH}$ | | $V_{CC}$ = MIN, $I_{OH}$ = – 0.4 mA | $V_{IH}$ = 2 V, | $V_{IL}$ = MAX, | 2.5 | 3.4 | | 2.7 | 3.4 | | V |
| $V_{OL}$ | | $V_{CC}$ = MIN, $I_{OL}$ = 4 mA | $V_{IL}$ = MAX, | $V_{IH}$ = 2 V, | | 0.25 | 0.4 | | 0.25 | 0.4 | V |
| | | $V_{CC}$ = MIN, $I_{OL}$ = 8 mA | $V_{IL}$ = MAX, | $V_{IH}$ = 2 V, | | | | | 0.35 | 0.5 | |
| $I_I$ | J or K | $V_{CC}$ = MAX, | $V_I$ = 7 V | | | | 0.1 | | | 0.1 | mA |
| | CLR | | | | | | 0.3 | | | 0.3 | |
| | CLK | | | | | | 0.4 | | | 0.4 | |
| $I_{IH}$ | J or K | $V_{CC}$ = MAX, | $V_I$ = 2.7 V | | | | 20 | | | 20 | μA |
| | CLR | | | | | | 60 | | | 60 | |
| | CLK | | | | | | 80 | | | 80 | |
| $I_{IL}$ | J or K | $V_{CC}$ = MAX, | $V_I$ = 0.4 V | | | | – 0.4 | | | – 0.4 | mA |
| | CLR or CLK | | | | | | – 0.8 | | | – 0.8 | |
| $I_{OS}$§ | | $V_{CC}$ = MAX, | See Note 4 | | – 20 | | – 100 | – 20 | | – 100 | mA |
| $I_{CC}$ (Total) | | $V_{CC}$ = MAX, | See Note 2 | | | 4 | 6 | | 4 | 6 | mA |

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡All typical values are at $V_{CC}$ = 5 V, $T_A$ = 25°C.
§Not more than one output should be shorted at a time, and the duration of the short circuit should not exceed one second.
NOTE 2: With all outputs open, $I_{CC}$ is measured with the Q and $\overline{Q}$, outputs high in turn. At the time of measurement, the clock input is grounded.
NOTE 4: For certain devices where state commutation can be caused by shorting an output to ground, an equivalent test may be performed with $V_O$ = 2.25 V and 2.125 V for the 54 family and the 74 family, respectively, with the minimum and maximum limits reduced to one half of their stated values.

## switching characteristics, $V_{CC}$ = 5 V, $T_A$ = 25°C (see note 3)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | TEST CONDITIONS | | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|---|
| $f_{max}$ | | | $R_L$ = 2 kΩ, | $C_L$ = 15 pF | 30 | 45 | | MHz |
| $t_{PLH}$ | $\overline{CLR}$ or CLK | Q or $\overline{Q}$ | | | | 15 | 20 | ns |
| $t_{PHL}$ | | | | | | 15 | 20 | ns |

NOTE 3: Load circuits and voltage waveforms are shown in Section 1.

## PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish | MSL Peak Temp (3) |
|---|---|---|---|---|---|---|---|---|
| JM38510/00203BCA | ACTIVE | CDIP | J | 14 | 1 | TBD | A42 | N / A for Pkg Type |
| SN54107J | ACTIVE | CDIP | J | 14 | 1 | TBD | A42 | N / A for Pkg Type |
| SN54107J | ACTIVE | CDIP | J | 14 | 1 | TBD | A42 | N / A for Pkg Type |
| SN74107N | NRND | PDIP | N | 14 | 25 | Pb-Free (RoHS) | CU NIPDAU | N / A for Pkg Type |
| SN74107N | NRND | PDIP | N | 14 | 25 | Pb-Free (RoHS) | CU NIPDAU | N / A for Pkg Type |
| SN74107N3 | OBSOLETE | PDIP | N | 14 | | TBD | Call TI | Call TI |
| SN74107N3 | OBSOLETE | PDIP | N | 14 | | TBD | Call TI | Call TI |
| SN74107NE4 | NRND | PDIP | N | 14 | 25 | Pb-Free (RoHS) | CU NIPDAU | N / A for Pkg Type |
| SN74107NE4 | NRND | PDIP | N | 14 | 25 | Pb-Free (RoHS) | CU NIPDAU | N / A for Pkg Type |
| SN74LS107AD | ACTIVE | SOIC | D | 14 | 50 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN74LS107AD | ACTIVE | SOIC | D | 14 | 50 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN74LS107ADE4 | ACTIVE | SOIC | D | 14 | 50 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN74LS107ADE4 | ACTIVE | SOIC | D | 14 | 50 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN74LS107ADG4 | ACTIVE | SOIC | D | 14 | 50 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN74LS107ADG4 | ACTIVE | SOIC | D | 14 | 50 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN74LS107ADR | ACTIVE | SOIC | D | 14 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN74LS107ADR | ACTIVE | SOIC | D | 14 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN74LS107ADRE4 | ACTIVE | SOIC | D | 14 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN74LS107ADRE4 | ACTIVE | SOIC | D | 14 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN74LS107ADRG4 | ACTIVE | SOIC | D | 14 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN74LS107ADRG4 | ACTIVE | SOIC | D | 14 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN74LS107AN | ACTIVE | PDIP | N | 14 | 25 | Pb-Free (RoHS) | CU NIPDAU | N / A for Pkg Type |
| SN74LS107AN | ACTIVE | PDIP | N | 14 | 25 | Pb-Free (RoHS) | CU NIPDAU | N / A for Pkg Type |
| SN74LS107AN3 | OBSOLETE | PDIP | N | 14 | | TBD | Call TI | Call TI |
| SN74LS107AN3 | OBSOLETE | PDIP | N | 14 | | TBD | Call TI | Call TI |
| SN74LS107ANE4 | ACTIVE | PDIP | N | 14 | 25 | Pb-Free (RoHS) | CU NIPDAU | N / A for Pkg Type |
| SN74LS107ANE4 | ACTIVE | PDIP | N | 14 | 25 | Pb-Free (RoHS) | CU NIPDAU | N / A for Pkg Type |
| SN74LS107ANSR | ACTIVE | SO | NS | 14 | 2000 | Green (RoHS & | CU NIPDAU | Level-1-260C-UNLIM |

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish | MSL Peak Temp (3) |
|---|---|---|---|---|---|---|---|---|
| | | | | | | no Sb/Br) | | |
| SN74LS107ANSR | ACTIVE | SO | NS | 14 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN74LS107ANSRE4 | ACTIVE | SO | NS | 14 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN74LS107ANSRE4 | ACTIVE | SO | NS | 14 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN74LS107ANSRG4 | ACTIVE | SO | NS | 14 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN74LS107ANSRG4 | ACTIVE | SO | NS | 14 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SNJ54107J | ACTIVE | CDIP | J | 14 | 1 | TBD | A42 | N / A for Pkg Type |
| SNJ54107J | ACTIVE | CDIP | J | 14 | 1 | TBD | A42 | N / A for Pkg Type |

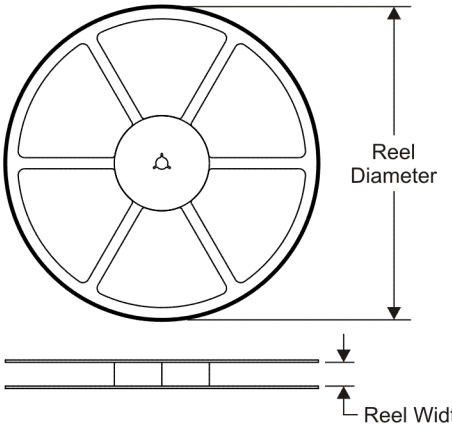
(1) The marketing status values are defined as follows:
**ACTIVE:** Product device recommended for new designs.
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
**OBSOLETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
**TBD:** The Pb-Free/Green conversion plan has not been defined.
**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

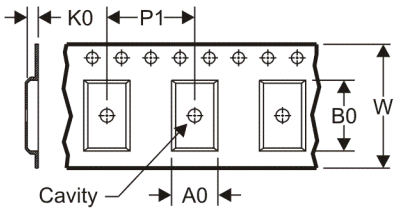
(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

## TAPE AND REEL INFORMATION

**REEL DIMENSIONS**

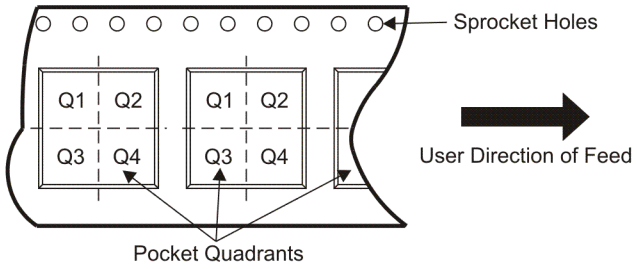



**TAPE DIMENSIONS**




| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

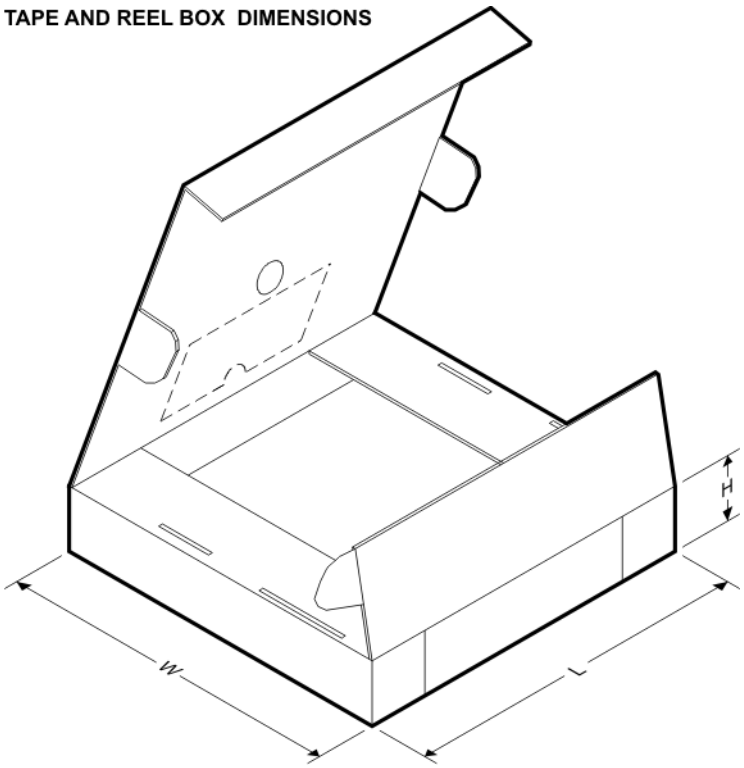
**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| SN74LS107ADR | SOIC | D | 14 | 2500 | 330.0 | 16.4 | 6.5 | 9.0 | 2.1 | 8.0 | 16.0 | Q1 |
| SN74LS107ANSR | SO | NS | 14 | 2000 | 330.0 | 16.4 | 8.2 | 10.5 | 2.5 | 12.0 | 16.0 | Q1 |

TAPE AND REEL BOX DIMENSIONS



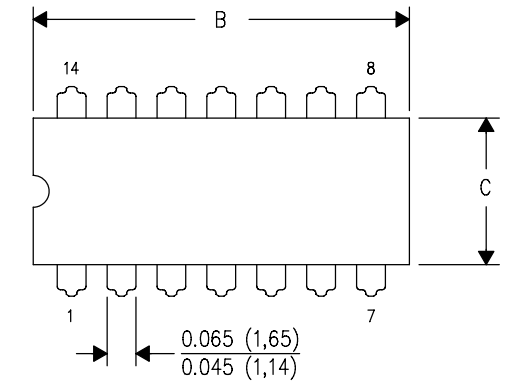

*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| SN74LS107ADR | SOIC | D | 14 | 2500 | 346.0 | 346.0 | 33.0 |
| SN74LS107ANSR | SO | NS | 14 | 2000 | 346.0 | 346.0 | 33.0 |

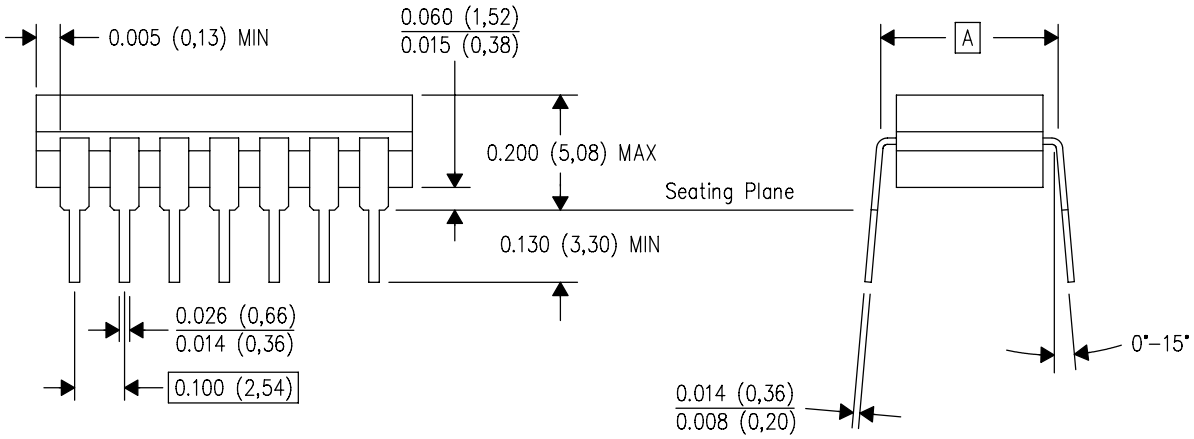
J (R–GDIP–T**)

14 LEADS SHOWN

# CERAMIC DUAL IN–LINE PACKAGE




| DIM \ PINS ** | 14 | 16 | 18 | 20 |
|---|---|---|---|---|
| A | 0.300 (7,62) BSC | 0.300 (7,62) BSC | 0.300 (7,62) BSC | 0.300 (7,62) BSC |
| B MAX | 0.785 (19,94) | .840 (21,34) | 0.960 (24,38) | 1.060 (26,92) |
| B MIN | — | — | — | — |
| C MAX | 0.300 (7,62) | 0.300 (7,62) | 0.310 (7,87) | 0.300 (7,62) |
| C MIN | 0.245 (6,22) | 0.245 (6,22) | 0.220 (5,59) | 0.245 (6,22) |



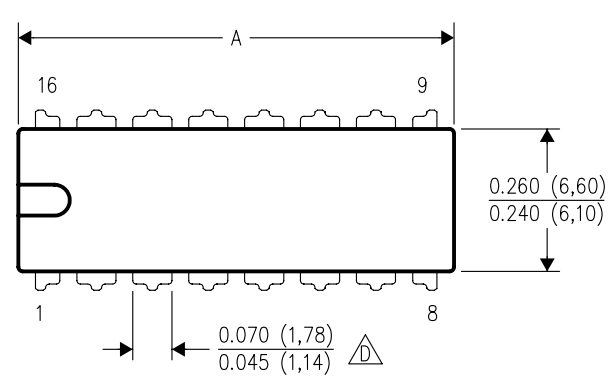

4040083/F 03/03

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package is hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
E. Falls within MIL STD 1835 GDIP1–T14, GDIP1–T16, GDIP1–T18 and GDIP1–T20.

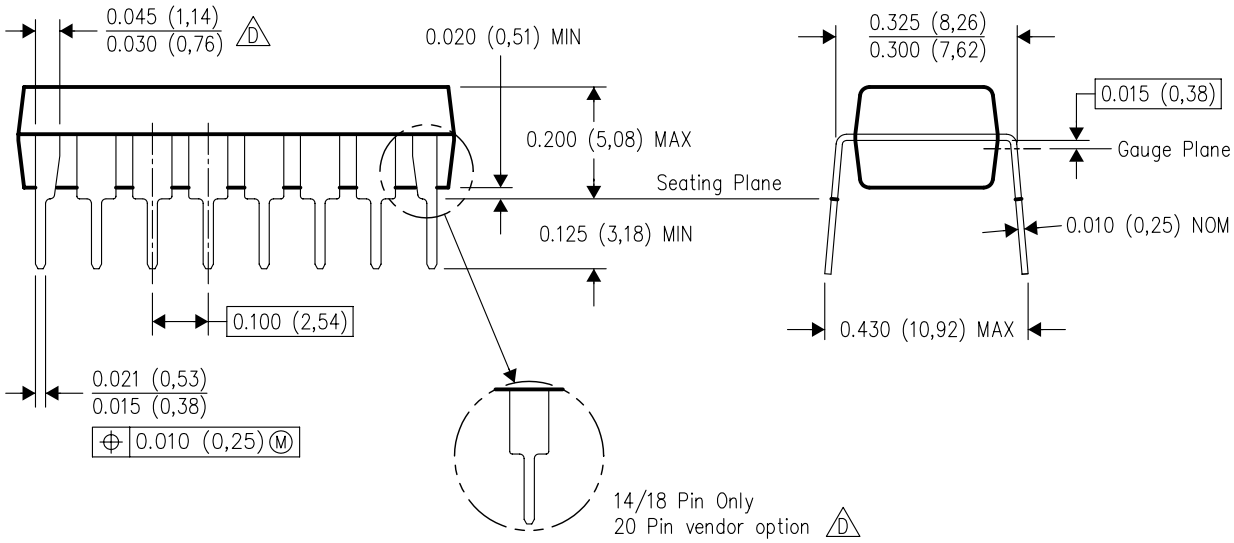
## N (R–PDIP–T**)

## PLASTIC DUAL–IN–LINE PACKAGE

16 PINS SHOWN



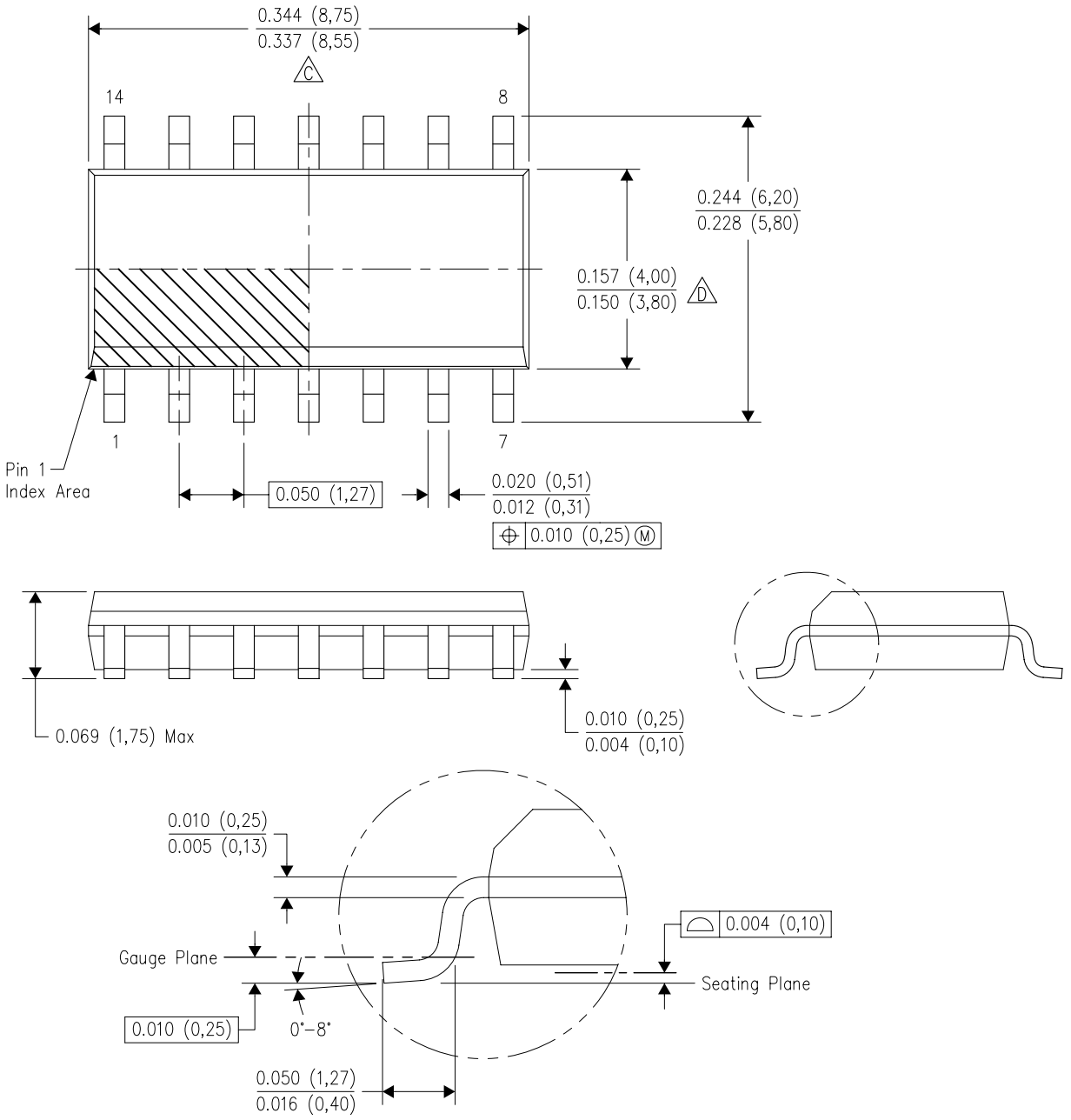

| DIM \ PINS ** | 14 | 16 | 18 | 20 |
|---|---|---|---|---|
| A MAX | 0.775 (19,69) | 0.775 (19,69) | 0.920 (23,37) | 1.060 (26,92) |
| A MIN | 0.745 (18,92) | 0.745 (18,92) | 0.850 (21,59) | 0.940 (23,88) |
| MS–001 VARIATION (C) | AA | BB | AC | AD |




4040049/E 12/2002

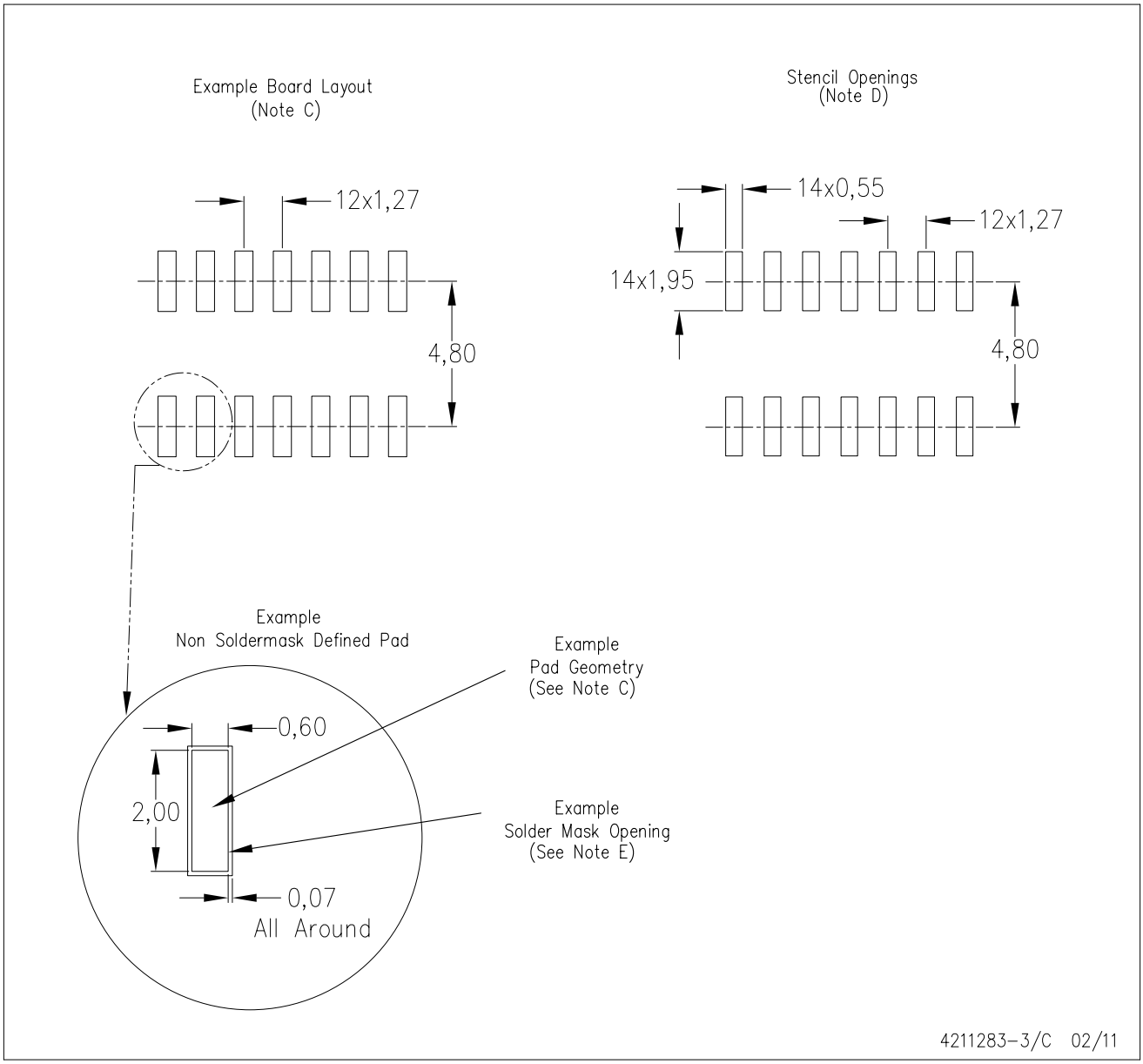
NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001, except 18 and 20 pin minimum body length (Dim A).
D. The 20 pin end lead shoulder width is a vendor option, either half or full width.

D (R–PDSO–G14) PLASTIC SMALL OUTLINE




NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AB.

D (R–PDSO–G14) PLASTIC SMALL OUTLINE

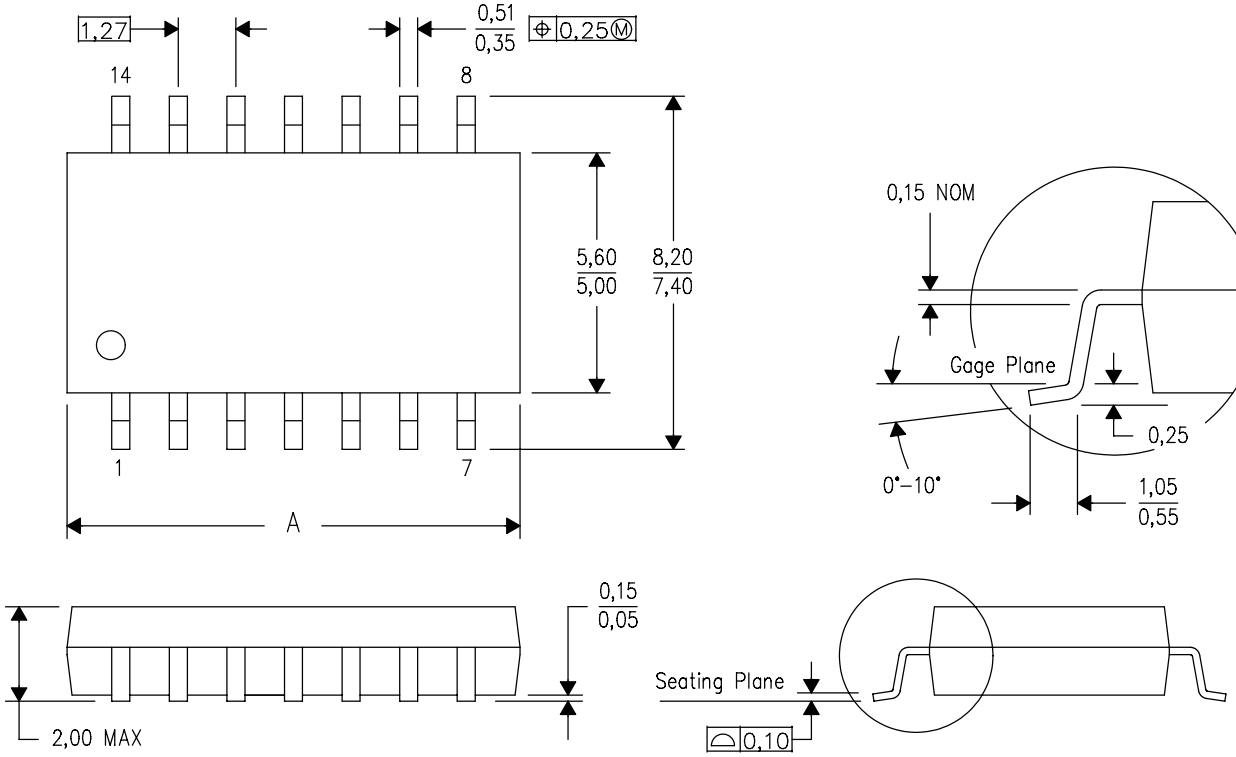



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

## MECHANICAL DATA

**NS (R-PDSO-G**)** **PLASTIC SMALL-OUTLINE PACKAGE**

**14-PINS SHOWN**




| DIM \ PINS ** | 14 | 16 | 20 | 24 |
|---|---|---|---|---|
| A MAX | 10,50 | 10,50 | 12,90 | 15,30 |
| A MIN | 9,90 | 9,90 | 12,30 | 14,70 |

4040062/C 03/03

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

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