

# SN54LS670, SN74LS670 4-BY-4 REGISTER FILES WITH 3-STATE OUTPUTS

SDLS193 – MARCH 1974 – REVISED MARCH 1988

- Separate Read/Write Addressing Permits Simultaneous Reading and Writing
- Fast Access Times . . . Typically 20 ns
- Organized as 4 Words of 4 Bits
- Expandable to 512 Words of n-Bits
- For Use as:
  - Scratch-Pad Memory
  - Buffer Storage between Processors
  - Bit Storage in Fast Multiplication Designs
- 3-State Outputs
- SN54LS170 and SN74LS170 Are Similar But Have Open-Collector Outputs

## description

The SN54LS670 and SN74LS670 MSI 16-bit TTL register files incorporate the equivalent of 98 gates. The register file is organized as 4 words of 4 bits each and separate on-chip decoding is provided for addressing the four word locations to either write-in or retrieve data. This permits simultaneous writing into one location and reading from another word location.

Four data inputs are available which are used to supply the 4-bit word to be stored. Location of the word is determined by the write-address inputs A and B in conjunction with a write-enable signal. Data applied at the inputs should be in its true form. That is, if a high-level signal is desired from the output, a high-level is applied at the data input for that particular bit location. The latch inputs are arranged so that new data will be accepted only if both internal address gate inputs are high. When this condition exists, data at the D input is transferred to the latch output. When the write-enable input,  $\overline{G}_W$ , is high, the data inputs are inhibited and their levels can cause no change in the information stored in the internal latches. When the read-enable input,  $\overline{G}_R$ , is high, the data outputs are inhibited and go into the high-impedance state.

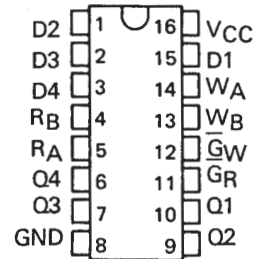
The individual address lines permit direct acquisition of data stored in any four of the latches. Four individual decoding gates are used to complete the address for reading a word. When the read address is made in conjunction with the read-enable signal, the word appears at the four outputs.

This arrangement—data-entry addressing separate from data-read addressing and individual sense line—eliminates recovery times, permits simultaneous reading and writing, and is limited in speed only by the write time (27 nanoseconds typical) and the read time (24 nanoseconds typical). The register file has a nondestructive readout in that data is not lost when addressed.

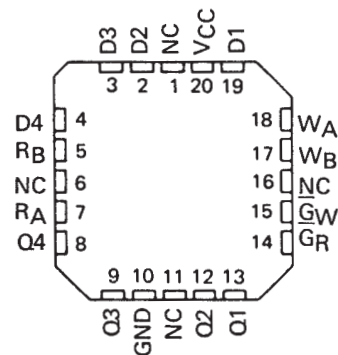
All inputs except read enable and write enable are buffered to lower the drive requirements to one Series 54LS/74LS standard load, and input-clamping diodes minimize switching transients to simplify system design. High-speed, double-ended AND-OR-INVERT gates are employed for the read-address function and have high-sink-current, three-state outputs. Up to 128 of these outputs may be bus connected for increasing the capacity up to 512 words. Any number of these registers may be paralleled to provide n-bit word length.

The SN54LS670 is characterized for operation over the full military temperature range of  $-55^{\circ}\text{C}$  to  $125^{\circ}\text{C}$ ; the SN74LS670 is characterized for operation from  $0^{\circ}\text{C}$  to  $70^{\circ}\text{C}$ .

SN54LS670 . . . J OR W PACKAGE  
SN74LS670 . . . D OR N PACKAGE  
(TOP VIEW)



SN54LS670 . . . FK PACKAGE  
(TOP VIEW)

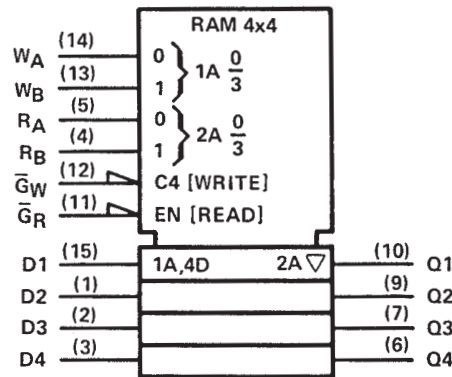


NC – No internal connection.

# SN54LS670, SN74LS670 4-BY-4 REGISTER FILES WITH 3-STATE OUTPUTS

SDLS193 – MARCH 1974 – REVISED MARCH 1988

## logic symbol†



†This symbol is in accordance with ANSI/IEEE Std. 91-1984 and IEC Publication 617-12. Pin numbers shown are for D, J, N, and W packages.

WRITE FUNCTION TABLE (SEE NOTES A, B, AND C)

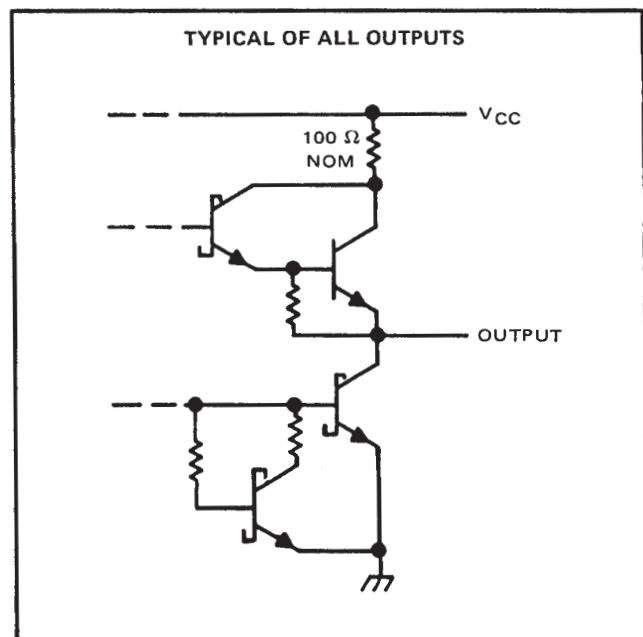
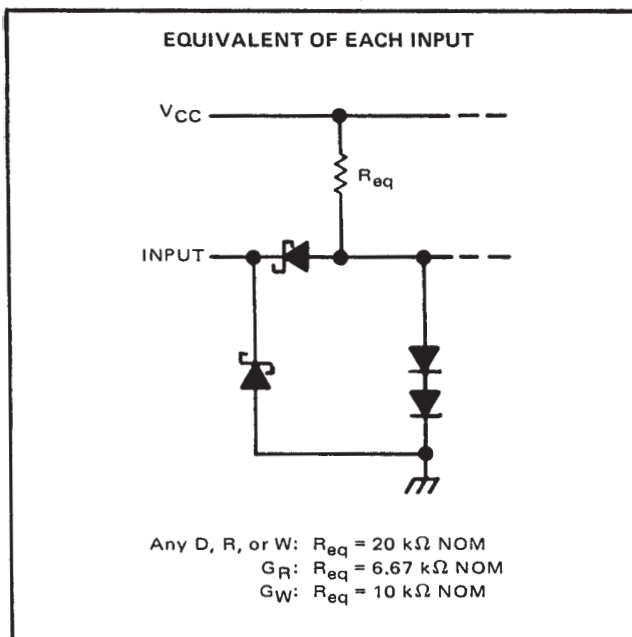
WRITE INPUTS			WORD			
WB	WA	GW	0	1	2	3
L	L	L	Q = D	Q <sub>0</sub>	Q <sub>0</sub>	Q <sub>0</sub>
L	H	L	Q <sub>0</sub>	Q = D	Q <sub>0</sub>	Q <sub>0</sub>
H	L	L	Q <sub>0</sub>	Q <sub>0</sub>	Q = D	Q <sub>0</sub>
H	H	L	Q <sub>0</sub>	Q <sub>0</sub>	Q <sub>0</sub>	Q = D
X	X	H	Q <sub>0</sub>	Q <sub>0</sub>	Q <sub>0</sub>	Q <sub>0</sub>

READ FUNCTION TABLE (SEE NOTES A AND D)

READ INPUTS			OUTPUTS			
RB	RA	GR	Q1	Q2	Q3	Q4
L	L	L	W0B1	W0B2	W0B3	W0B4
L	H	L	W1B1	W1B2	W1B3	W1B4
H	L	L	W2B1	W2B2	W2B3	W2B4
H	H	L	W3B1	W3B2	W3B3	W3B4
X	X	H	Z	Z	Z	Z

- NOTES: A. H = high level, L = low level, X = irrelevant, Z = high impedance (off)  
 B. (Q = D) = The four selected internal flip-flop outputs will assume the states applied to the four external data inputs.  
 C. Q<sub>0</sub> = the level of Q before the indicated input conditions were established.  
 D. W0B1 = The first bit of word 0, etc.

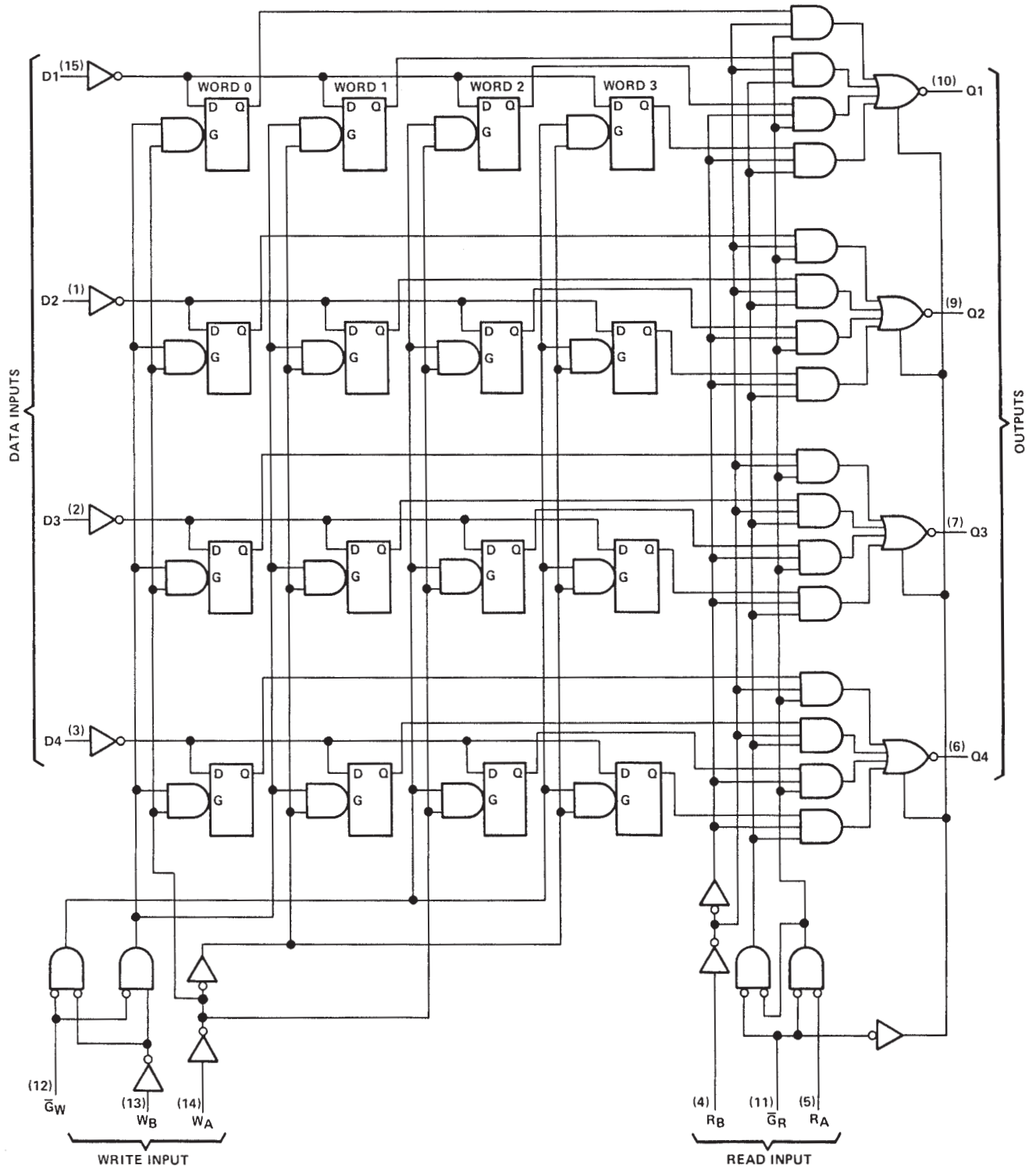
## schematics of inputs and outputs



# SN54LS670, SN74LS670 4-BY-4 REGISTER FILES WITH 3-STATE OUTPUTS

SDLS193 – MARCH 1974 – REVISED MARCH 1988

logic diagram (positive logic)



Pin numbers shown are for D, J, N, and W packages.

# SN54LS670, SN74LS670

## 4-BY-4 REGISTER FILES WITH 3-STATE OUTPUTS

SDLS193 – MARCH 1974 – REVISED MARCH 1988

### absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, $V_{CC}$ (see Note 1)	7 V
Input voltage	7 V
Off-state output voltage	5.5 V
Operating free-air temperature range: SN54LS670	-55°C to 125°C
SN74LS670	0°C to 70°C
Storage temperature range	-65°C to 150°C

### recommended operating conditions

	SN54LS670			SN74LS670			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, $V_{CC}$	4.5	5	5.5	4.75	5	5.25	V
High-level output current, $I_{OH}$			-1			-2.6	mA
Low-level output current, $I_{OL}$			4			8	mA
Width of write-enable or read-enable pulse, $t_W$	25			25			ns
Setup times, high- or low-level data (see Figure 2)	Data input with respect to write enable, $t_{SU}(D)$	10		10			ns
	Write select with respect to write enable, $t_{SU}(W)$	15		15			ns
Hold times, high- or low-level data (see Note 2 and Figure 2)	Data input with respect to write enable, $t_H(D)$	15		15			ns
	Write select with respect to write enable, $t_H(W)$	5		5			ns
Latch time for new data, $t_{latch}$ (see Note 3)	25			25			ns
Operating free-air temperature range, $T_A$	-55		125	0		70	°C

- NOTES: 1. Voltage values are with respect to network ground terminal.
2. Write-select setup time will protect the data written into the previous address. If protection of data in the previous address is not required,  $t_{SU}(W)$  can be ignored as any address selection sustained for the final 30 ns of the write-enable pulse and during  $t_H(W)$  will result in data being written into that location. Depending on the duration of the input conditions, one or a number of previous addresses may have been written into.
3. Latch time is the time allowed for the internal output of the latch to assume the state of new data. See Figure 2. This is important only when attempting to read from a location immediately after that location has received new data.



# SN54LS670, SN74LS670

## 4-BY-4 REGISTER FILES WITH 3-STATE OUTPUTS

SDLS193 – MARCH 1974 – REVISED MARCH 1988

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS†	SN54LS670			SN74LS670			UNIT	
		MIN	TYP‡	MAX	MIN	TYP‡	MAX		
V <sub>IH</sub> High-level input voltage		2			2			V	
V <sub>IL</sub> Low-level input voltage				0.7			0.8	V	
V <sub>IK</sub> Input clamp voltage	V <sub>CC</sub> = MIN, I <sub>I</sub> = -18 mA			-1.5			-1.5	V	
V <sub>OH</sub> High-level output voltage	V <sub>CC</sub> = MIN, V <sub>IH</sub> = 2 V, V <sub>IL</sub> = V <sub>IL max</sub>	I <sub>OH</sub> = -1 mA			2.4	3.4		V	
		I <sub>OH</sub> = -2.6 mA					2.4 3.1		
V <sub>OL</sub> Low-level output voltage	V <sub>CC</sub> = MIN, V <sub>IH</sub> = 2 V, V <sub>IL</sub> = V <sub>IL max</sub>	I <sub>OL</sub> = 4 mA			0.25	0.4	0.25 0.4	V	
		I <sub>OL</sub> = 8 mA					0.35 0.5		
I <sub>OZH</sub> Off-state output current, high-level voltage applied	V <sub>CC</sub> = MAX, V <sub>IH</sub> = 2 V, V <sub>O</sub> = 2.7 V			20			20	μA	
I <sub>OZL</sub> Off-state output current, low-level voltage applied	V <sub>CC</sub> = MAX, V <sub>IH</sub> = 2 V, V <sub>O</sub> = 0.4 V			-20			-20	μA	
I <sub>I</sub> Input current at maximum input voltage	V <sub>CC</sub> = MAX, V <sub>I</sub> = 7 V	Any D, R, or W					0.1	0.1	mA
		$\overline{G}_W$					0.2	0.2	
		$\overline{G}_R$					0.3	0.3	
I <sub>IH</sub> High-level input current	V <sub>CC</sub> = MAX, V <sub>I</sub> = 2.7 V	Any D, R, or W					20	20	μA
		$\overline{G}_W$					40	40	
		$\overline{G}_R$					60	60	
I <sub>IL</sub> Low-level input current	V <sub>CC</sub> = MAX, V <sub>I</sub> = 0.4 V	Any D, R, or W					-0.4	-0.4	mA
		$\overline{G}_W$					-0.8	-0.8	
		$\overline{G}_R$					-1.2	-1.2	
I <sub>OS</sub> Short-circuit output current§	V <sub>CC</sub> = MAX			-30	-130		-30	-130	mA
I <sub>CC</sub> Supply current	V <sub>CC</sub> = MAX, See Note 4			30	50		30	50	mA

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡All typical values are at V<sub>CC</sub> = 5 V, T<sub>A</sub> = 25°C.

§Not more than one output should be shorted at a time, and duration of the short-circuit should not exceed one second.

NOTE 4: Maximum I<sub>CC</sub> is guaranteed for the following worst-case conditions: 4.5 V is applied to all data inputs and both enable inputs, all address inputs are grounded and all outputs are open.

switching characteristics, V<sub>CC</sub> = 5 V, T<sub>A</sub> = 25°C

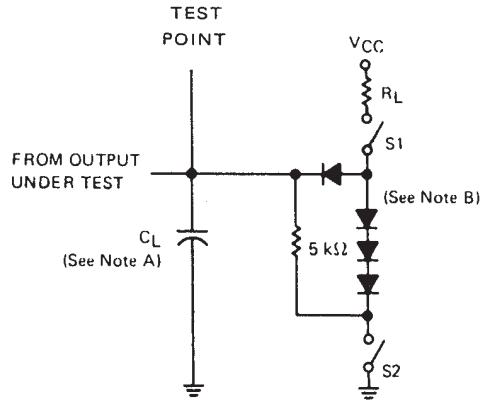
PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t <sub>PLH</sub>	Read select	Any Q	C <sub>L</sub> = 15 pF, R <sub>L</sub> = 2 kΩ, See Figures 1 and 2		23	40	ns
t <sub>PHL</sub>					25	45	
t <sub>PLH</sub>	Write enable	Any Q	C <sub>L</sub> = 15 pF, R <sub>L</sub> = 2 kΩ, See Figures 1 and 3		26	45	ns
t <sub>PHL</sub>					28	50	
t <sub>PLH</sub>	Data	Any Q	See Figures 1 and 3		25	45	ns
t <sub>PHL</sub>					23	40	
t <sub>PZH</sub>	Read enable	Any Q	C <sub>L</sub> = 15 pF, R <sub>L</sub> = 2 kΩ, See Figures 1 and 4		15	35	ns
t <sub>PZL</sub>					22	40	
t <sub>PHZ</sub>			C <sub>L</sub> = 5 pF, R <sub>L</sub> = 2 kΩ, See Figures 1 and 4		30	50	ns
t <sub>PLZ</sub>					16	35	



# SN54LS670, SN74LS670 4-BY-4 REGISTER FILES WITH 3-STATE OUTPUTS

SDLS193 – MARCH 1974 – REVISED MARCH 1988

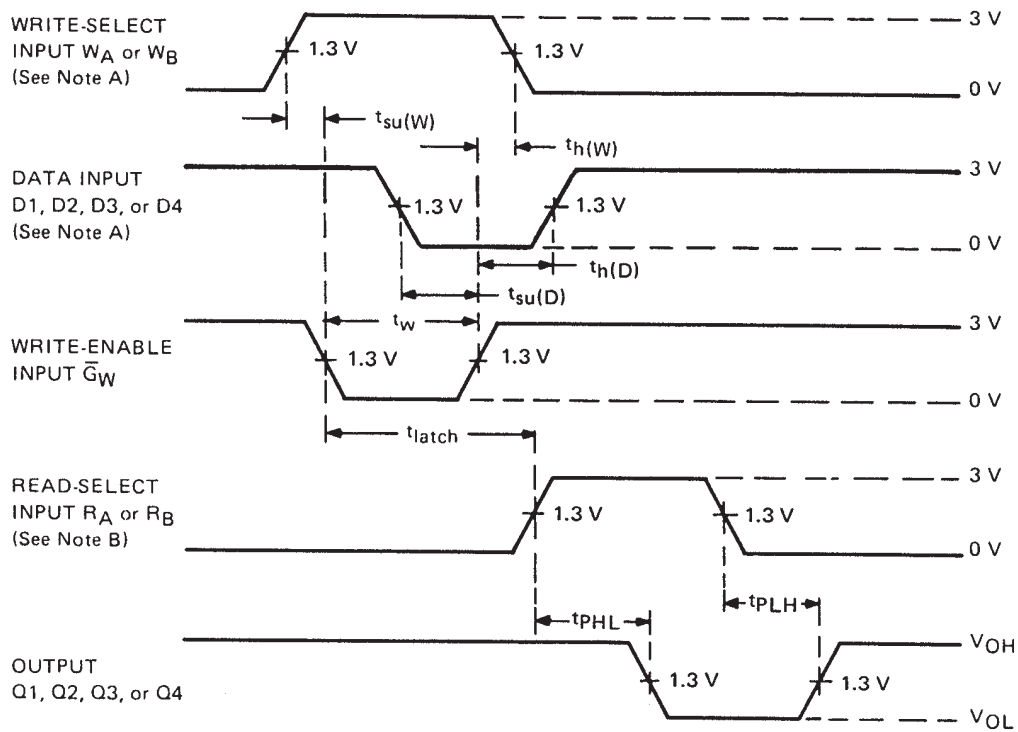
## PARAMETER MEASUREMENT INFORMATION



NOTES: A.  $C_L$  includes probe and jig capacitance.  
B. All diodes are 1N3064 or equivalent.

LOAD CIRCUIT

FIGURE 1



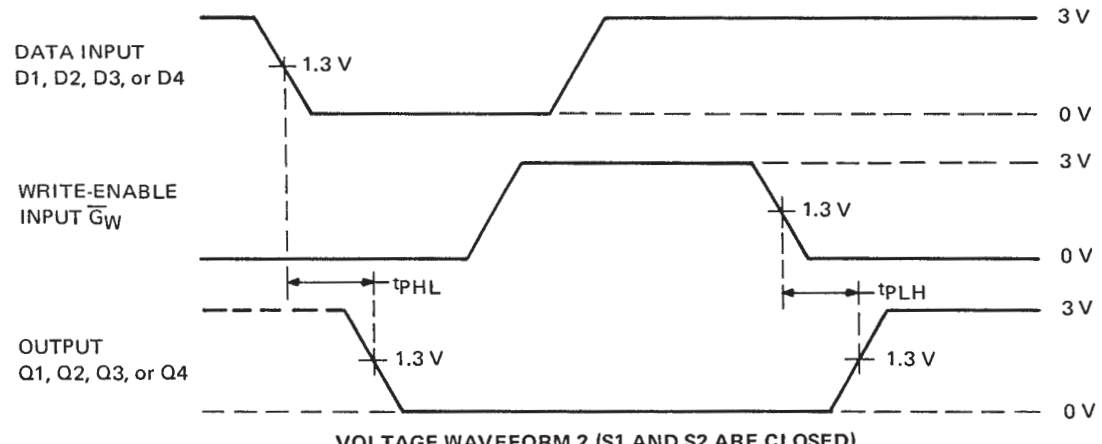
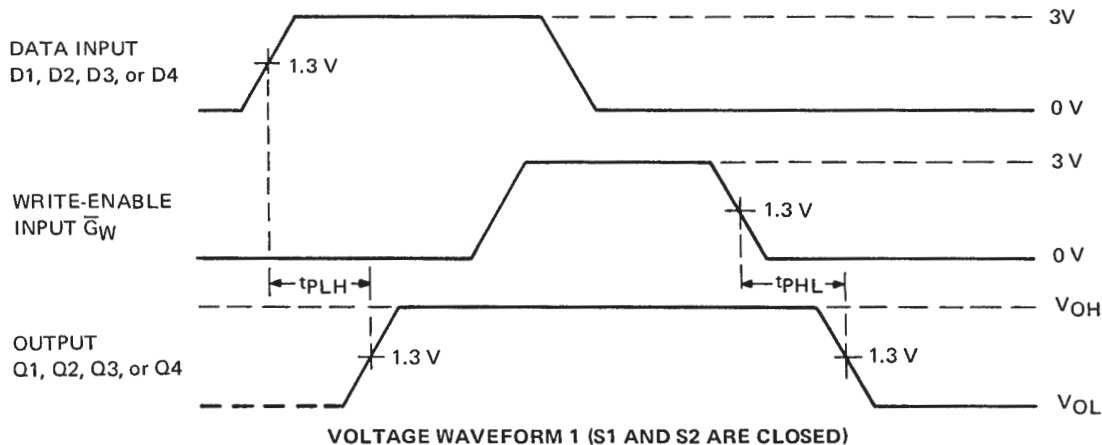
VOLTAGE WAVEFORMS (S1 AND S2 ARE CLOSED)

NOTES: A. High-level input pulses at the select and data inputs are illustrated; however, times associated with low-level pulses are measured from the same reference points.  
B. When measuring delay times from a read-select input, the read-enable input is low.  
C. Input waveforms are supplied by generators having the following characteristics:  $PRR \leq 2$  MHz,  $Z_{out} \approx 50 \Omega$ , duty cycle  $\leq 50\%$ ,  $t_r \leq 15$  ns,  $t_f \leq 6$  ns.

FIGURE 2

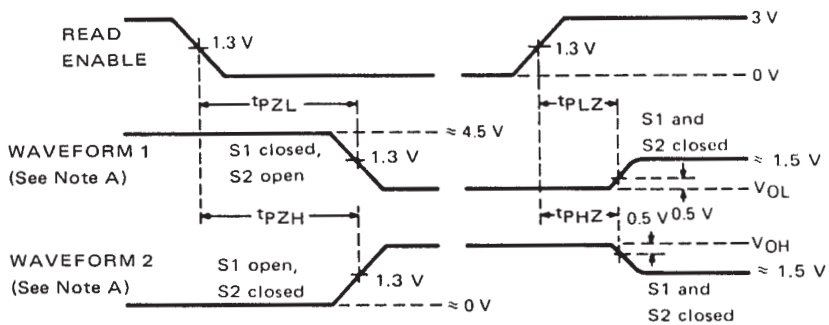


PARAMETER MEASUREMENT INFORMATION



- NOTES: A. Each select address is tested. Prior to the start of each of the above tests both write and read address inputs are stabilized with  $W_A = R_A$  and  $W_B = R_B$ . During the test  $G_R$  is low.  
B. Input waveforms are supplied by generators having the following characteristics:  $PRR \leq 1$  MHz,  $Z_{out} \approx 50 \Omega$ , duty cycle  $\leq 50\%$ ,  $t_r \leq 15$  ns,  $t_f \leq 6$  ns.

FIGURE 3



VOLTAGE WAVEFORMS  
ENABLE AND DISABLE TIMES, THREE-STATE OUTPUTS

- NOTES: A. Waveforms 1 is for an output with internal conditions such that the output is low except when disabled by the read-enable input. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the read-enable input.  
B. When measuring delay times from the read-enable input, both read-select inputs have been established at steady states.  
C. Input waveforms are supplied by generators having the following characteristics:  $PRR \leq 1$  MHz,  $Z_{out} \approx 50 \Omega$ , duty cycle  $\leq 50\%$ ,  $t_r \leq 15$  ns,  $t_f \leq 6$  ns.

FIGURE 4

**PACKAGING INFORMATION**

Orderable Device	Status <sup>(1)</sup>	Package Type	Package Drawing	Pins	Package Qty	Eco Plan <sup>(2)</sup>	Lead/Ball Finish	MSL Peak Temp <sup>(3)</sup>
5962-7704201VEA	ACTIVE	CDIP	J	16	1	TBD	A42	N / A for Pkg Type
5962-7704201VFA	ACTIVE	CFP	W	16	1	TBD	A42	N / A for Pkg Type
5962-7704201VFA	ACTIVE	CFP	W	16	1	TBD	A42	N / A for Pkg Type
7704201EA	ACTIVE	CDIP	J	16	1	TBD	A42	N / A for Pkg Type
7704201EA	ACTIVE	CDIP	J	16	1	TBD	A42	N / A for Pkg Type
7704201FA	ACTIVE	CFP	W	16	1	TBD	A42	N / A for Pkg Type
7704201FA	ACTIVE	CFP	W	16	1	TBD	A42	N / A for Pkg Type
SN54LS670J	ACTIVE	CDIP	J	16	1	TBD	A42	N / A for Pkg Type
SN54LS670J	ACTIVE	CDIP	J	16	1	TBD	A42	N / A for Pkg Type
SN74LS670D	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LS670D	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LS670DE4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LS670DE4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LS670DG4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LS670DG4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LS670DR	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LS670DR	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LS670DRE4	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LS670DRE4	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LS670DRG4	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LS670DRG4	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LS670N	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
SN74LS670N	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
SN74LS670N3	OBSOLETE	PDIP	N	16		TBD	Call TI	Call TI
SN74LS670N3	OBSOLETE	PDIP	N	16		TBD	Call TI	Call TI
SN74LS670NE4	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
SN74LS670NE4	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
SN74LS670NSR	ACTIVE	SO	NS	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LS670NSR	ACTIVE	SO	NS	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM



Orderable Device	Status <sup>(1)</sup>	Package Type	Package Drawing	Pins	Package Qty	Eco Plan <sup>(2)</sup>	Lead/Ball Finish	MSL Peak Temp <sup>(3)</sup>
SN74LS670NSRE4	ACTIVE	SO	NS	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LS670NSRE4	ACTIVE	SO	NS	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LS670NSRG4	ACTIVE	SO	NS	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LS670NSRG4	ACTIVE	SO	NS	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SNJ54LS670FK	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type
SNJ54LS670FK	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type
SNJ54LS670J	ACTIVE	CDIP	J	16	1	TBD	A42	N / A for Pkg Type
SNJ54LS670J	ACTIVE	CDIP	J	16	1	TBD	A42	N / A for Pkg Type
SNJ54LS670W	ACTIVE	CFP	W	16	1	TBD	A42	N / A for Pkg Type
SNJ54LS670W	ACTIVE	CFP	W	16	1	TBD	A42	N / A for Pkg Type

<sup>(1)</sup> The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

<sup>(2)</sup> Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

<sup>(3)</sup> MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

**Important Information and Disclaimer:** The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

**TAPE AND REEL INFORMATION**



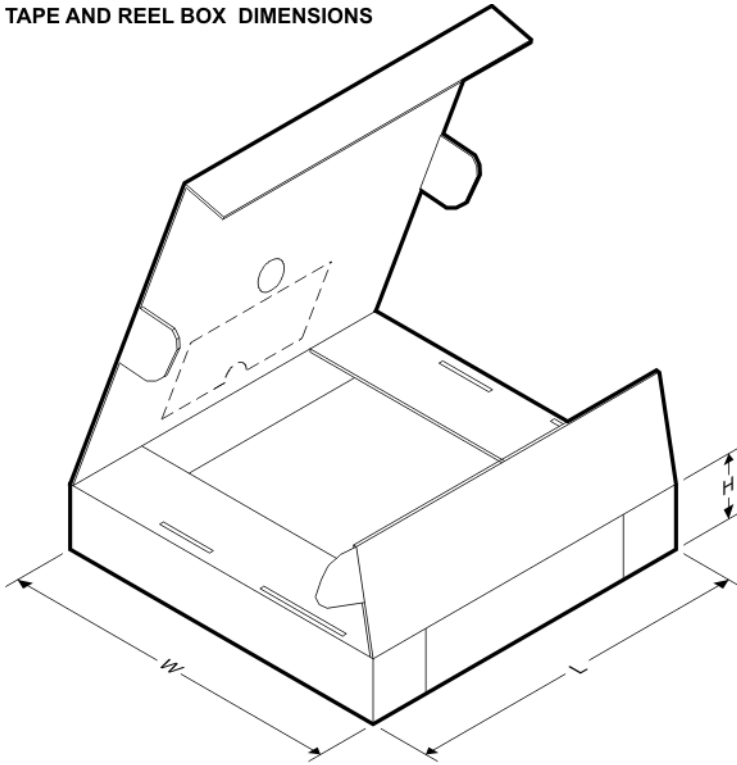
**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74LS670DR	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
SN74LS670NSR	SO	NS	16	2000	330.0	16.4	8.2	10.5	2.5	12.0	16.0	Q1

**TAPE AND REEL BOX DIMENSIONS**

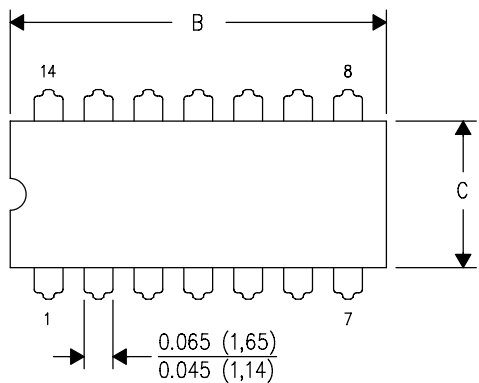


\*All dimensions are nominal

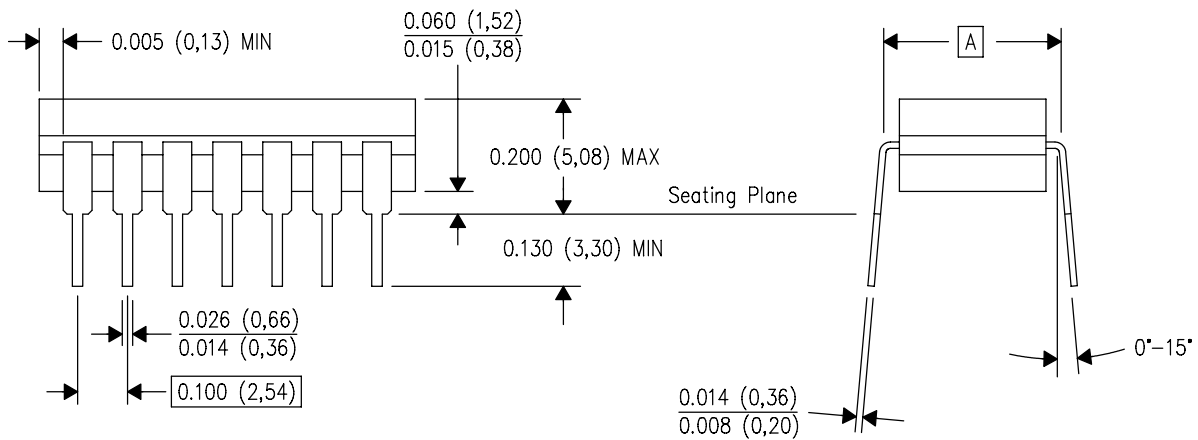
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74LS670DR	SOIC	D	16	2500	333.2	345.9	28.6
SN74LS670NSR	SO	NS	16	2000	346.0	346.0	33.0

J (R-GDIP-T\*\*)   
 14 LEADS SHOWN

CERAMIC DUAL IN-LINE PACKAGE



DIM \ PINS **	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)

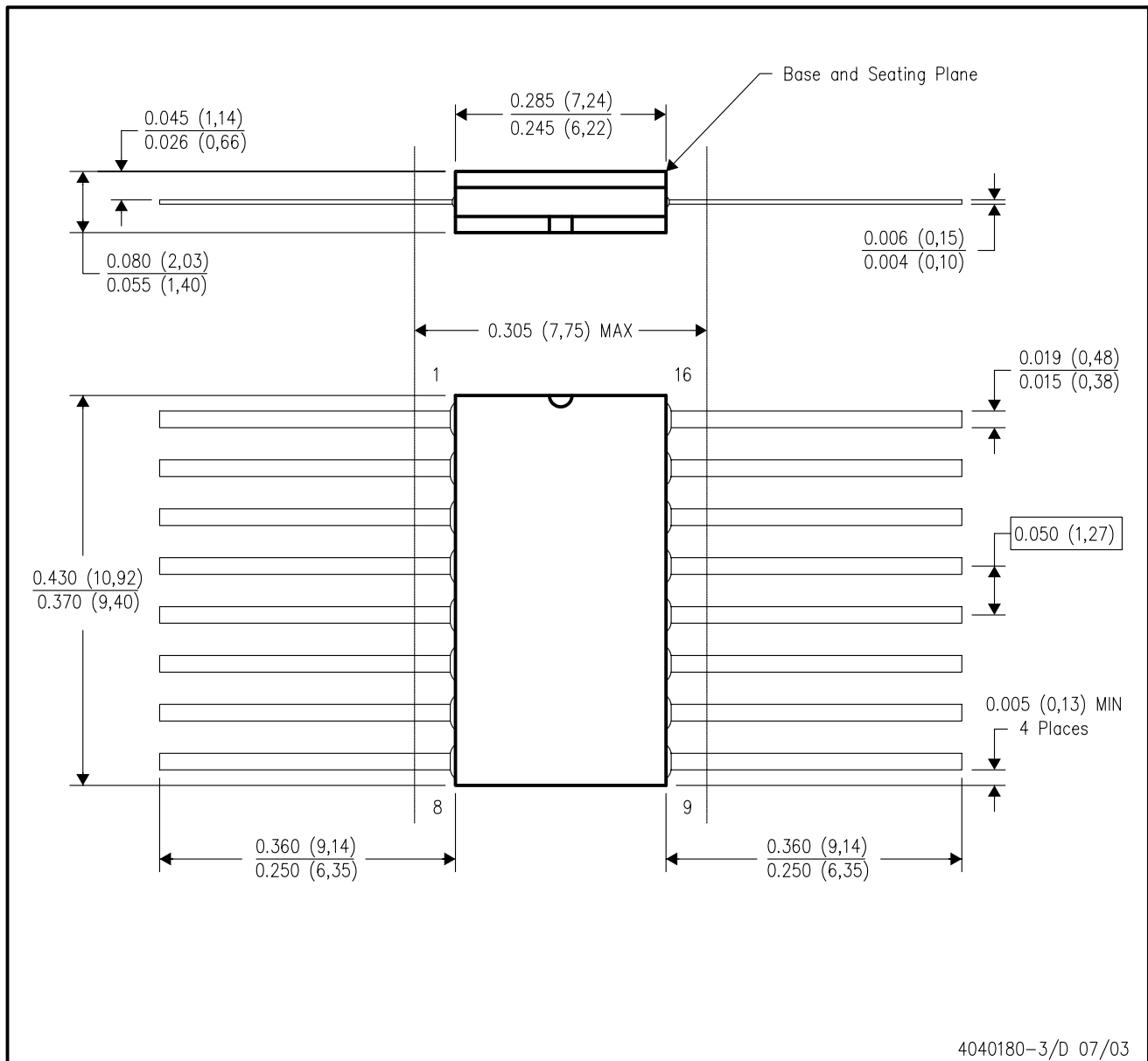


4040083/F 03/03

- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. This package is hermetically sealed with a ceramic lid using glass frit.
  - D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
  - E. Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

W (R-GDFP-F16)

CERAMIC DUAL FLATPACK

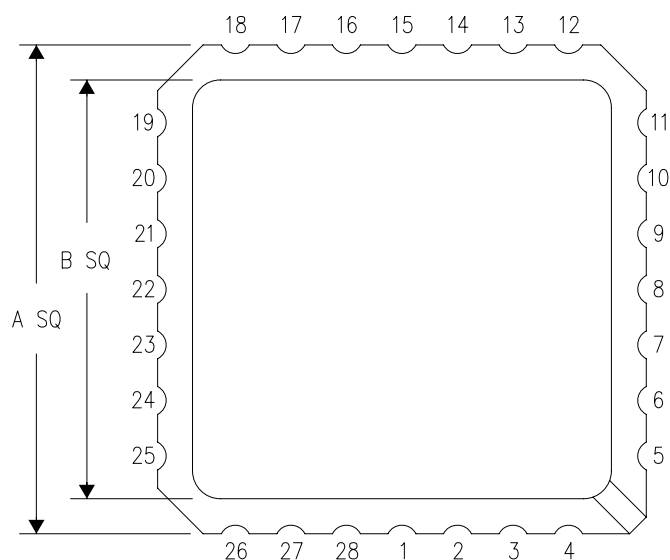


- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. This package can be hermetically sealed with a ceramic lid using glass frit.
  - D. Index point is provided on cap for terminal identification only.
  - E. Falls within MIL STD 1835 GDFP1-F16 and JEDEC MO-092AC

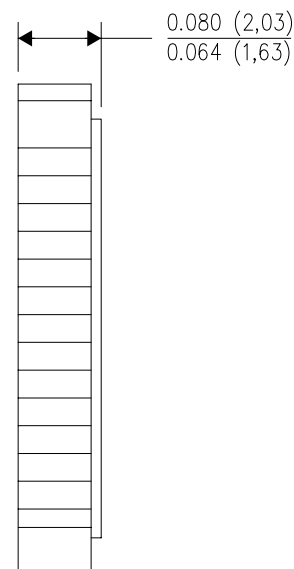
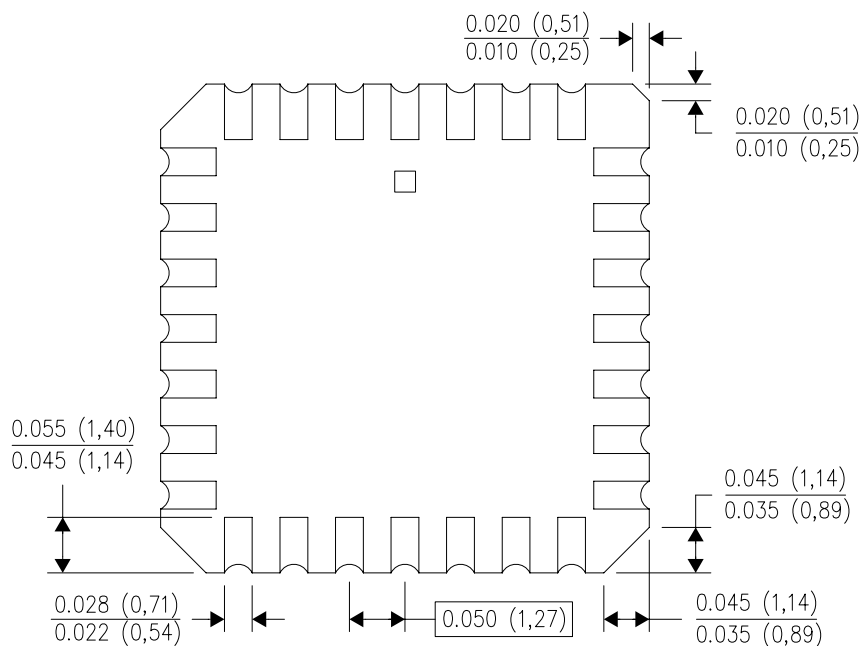
FK (S-CQCC-N\*\*)

LEADLESS CERAMIC CHIP CARRIER

28 TERMINAL SHOWN



NO. OF TERMINALS **	A		B	
	MIN	MAX	MIN	MAX
20	0.342 (8,69)	0.358 (9,09)	0.307 (7,80)	0.358 (9,09)
28	0.442 (11,23)	0.458 (11,63)	0.406 (10,31)	0.458 (11,63)
44	0.640 (16,26)	0.660 (16,76)	0.495 (12,58)	0.560 (14,22)
52	0.740 (18,78)	0.761 (19,32)	0.495 (12,58)	0.560 (14,22)
68	0.938 (23,83)	0.962 (24,43)	0.850 (21,6)	0.858 (21,8)
84	1.141 (28,99)	1.165 (29,59)	1.047 (26,6)	1.063 (27,0)



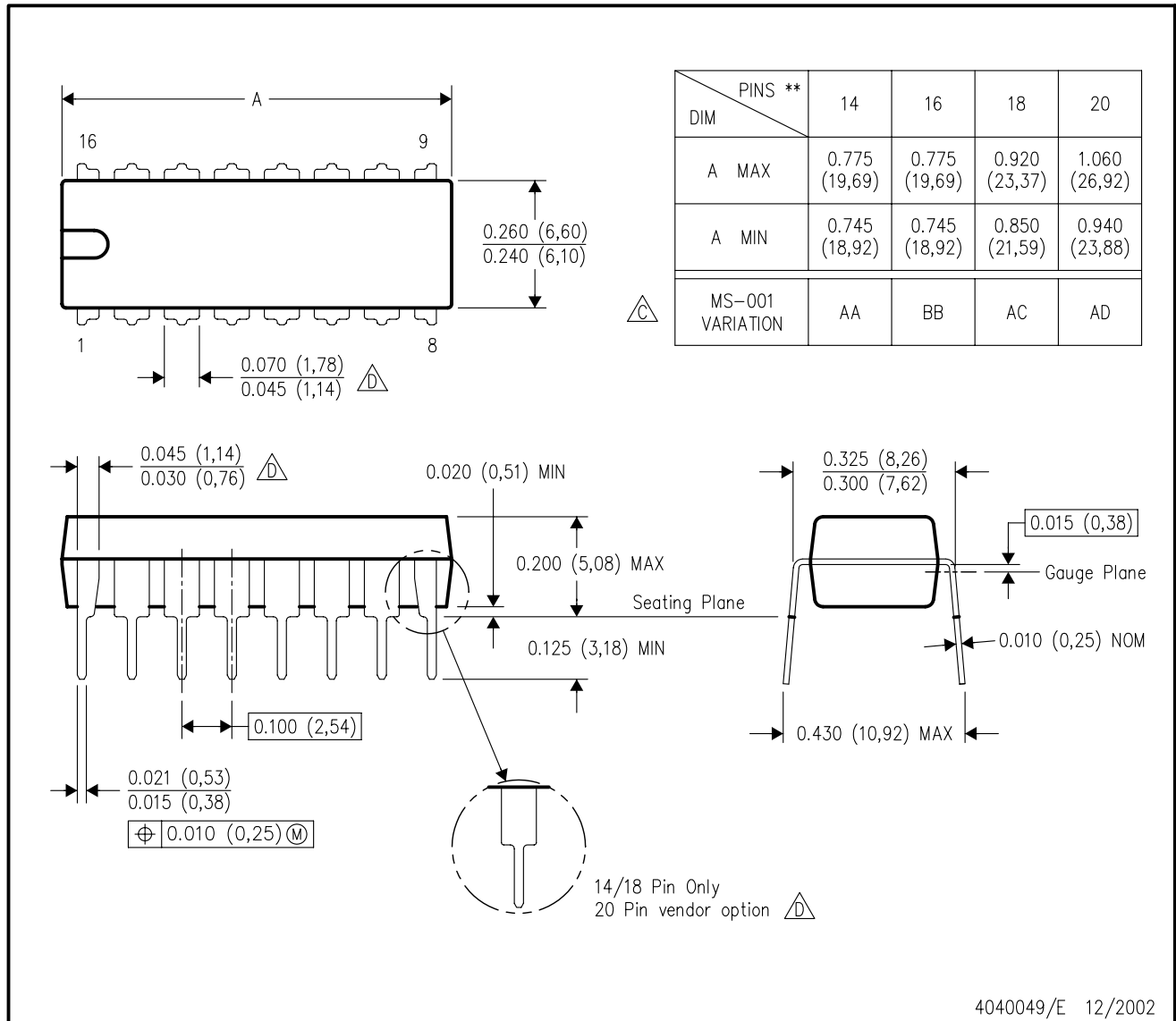
4040140/D 01/11

- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. This package can be hermetically sealed with a metal lid.
  - D. Falls within JEDEC MS-004

N (R-PDIP-T\*\*)

PLASTIC DUAL-IN-LINE PACKAGE

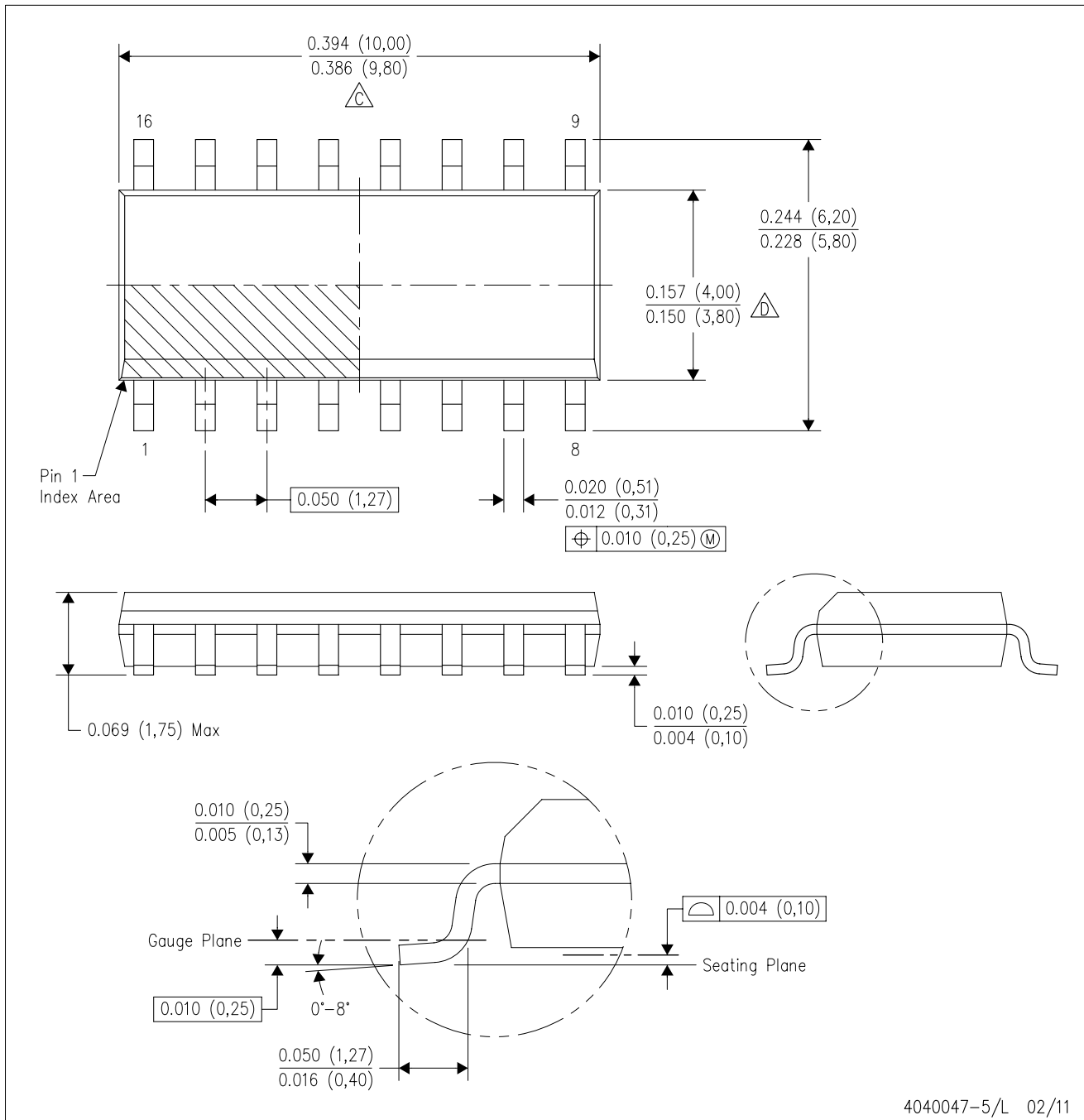
16 PINS SHOWN





- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
  - The 20 pin end lead shoulder width is a vendor option, either half or full width.

D (R-PDSO-G16)

PLASTIC SMALL OUTLINE



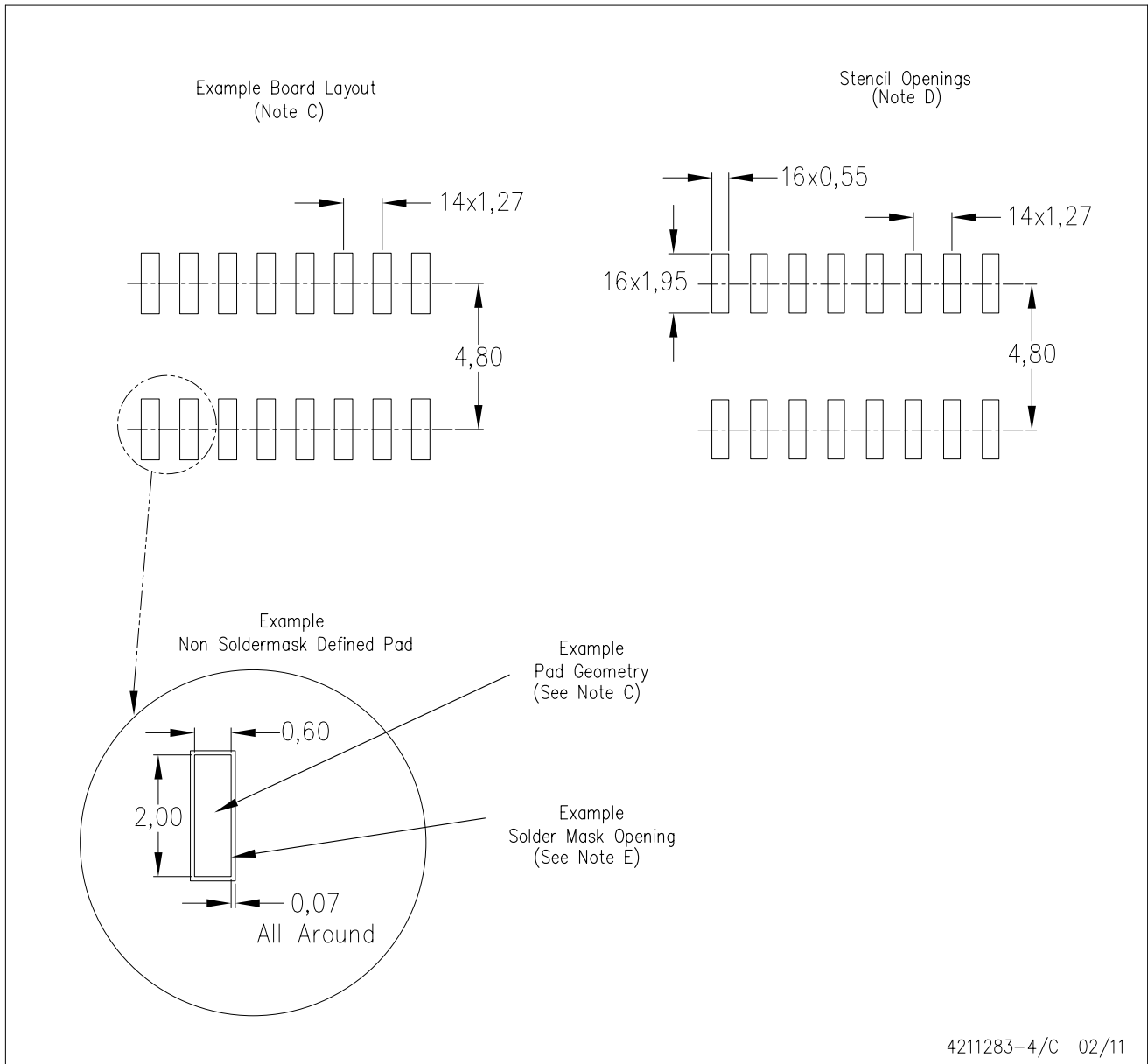
4040047-5/L 02/11

- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  -  Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
  -  Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
  - E. Reference JEDEC MS-012 variation AC.



D (R-PDSO-G16)

PLASTIC SMALL OUTLINE



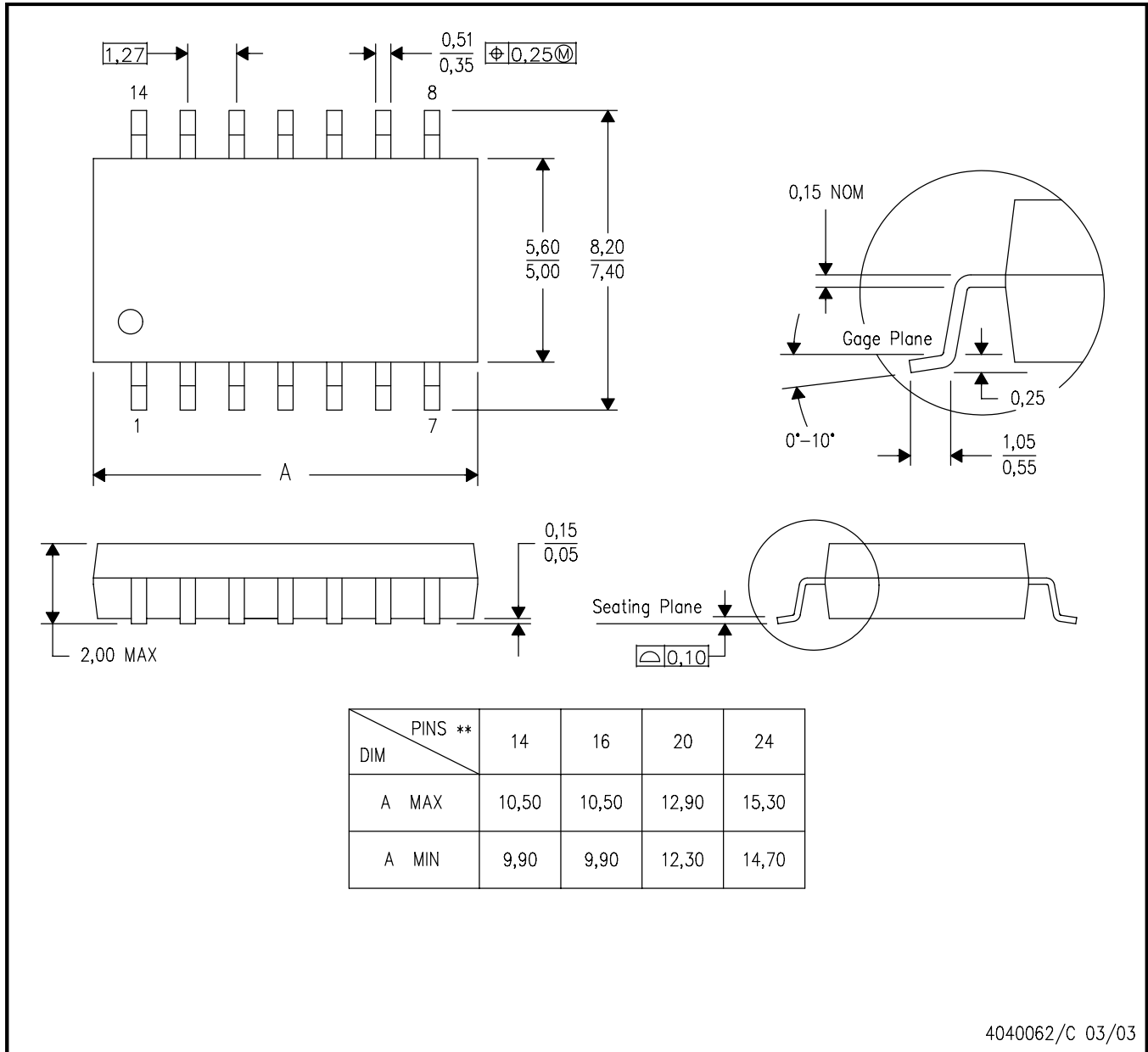
- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Publication IPC-7351 is recommended for alternate designs.
  - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
  - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

## MECHANICAL DATA

**NS (R-PDSO-G\*\*)**

**PLASTIC SMALL-OUTLINE PACKAGE**

**14-PINS SHOWN**



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

## IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, modifications, enhancements, improvements, and other changes to its products and services at any time and to discontinue any product or service without notice. Customers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All products are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its hardware products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by government requirements, testing of all parameters of each product is not necessarily performed.

TI assumes no liability for applications assistance or customer product design. Customers are responsible for their products and applications using TI components. To minimize the risks associated with customer products and applications, customers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any TI patent right, copyright, mask work right, or other TI intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information published by TI regarding third-party products or services does not constitute a license from TI to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of TI information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. Reproduction of this information with alteration is an unfair and deceptive business practice. TI is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

Resale of TI products or services with statements different from or beyond the parameters stated by TI for that product or service voids all express and any implied warranties for the associated TI product or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

TI products are not authorized for use in safety-critical applications (such as life support) where a failure of the TI product would reasonably be expected to cause severe personal injury or death, unless officers of the parties have executed an agreement specifically governing such use. Buyers represent that they have all necessary expertise in the safety and regulatory ramifications of their applications, and acknowledge and agree that they are solely responsible for all legal, regulatory and safety-related requirements concerning their products and any use of TI products in such safety-critical applications, notwithstanding any applications-related information or support that may be provided by TI. Further, Buyers must fully indemnify TI and its representatives against any damages arising out of the use of TI products in such safety-critical applications.

TI products are neither designed nor intended for use in military/aerospace applications or environments unless the TI products are specifically designated by TI as military-grade or "enhanced plastic." Only products designated by TI as military-grade meet military specifications. Buyers acknowledge and agree that any such use of TI products which TI has not designated as military-grade is solely at the Buyer's risk, and that they are solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI products are neither designed nor intended for use in automotive applications or environments unless the specific TI products are designated by TI as compliant with ISO/TS 16949 requirements. Buyers acknowledge and agree that, if they use any non-designated products in automotive applications, TI will not be responsible for any failure to meet such requirements.

Following are URLs where you can obtain information on other Texas Instruments products and application solutions:

### Products

Audio	<a href="http://www.ti.com/audio">www.ti.com/audio</a>
Amplifiers	<a href="http://amplifier.ti.com">amplifier.ti.com</a>
Data Converters	<a href="http://dataconverter.ti.com">dataconverter.ti.com</a>
DLP® Products	<a href="http://www.dlp.com">www.dlp.com</a>
DSP	<a href="http://dsp.ti.com">dsp.ti.com</a>
Clocks and Timers	<a href="http://www.ti.com/clocks">www.ti.com/clocks</a>
Interface	<a href="http://interface.ti.com">interface.ti.com</a>
Logic	<a href="http://logic.ti.com">logic.ti.com</a>
Power Mgmt	<a href="http://power.ti.com">power.ti.com</a>
Microcontrollers	<a href="http://microcontroller.ti.com">microcontroller.ti.com</a>
RFID	<a href="http://www.ti-rfid.com">www.ti-rfid.com</a>
RF/IF and ZigBee® Solutions	<a href="http://www.ti.com/lprf">www.ti.com/lprf</a>

### Applications

Communications and Telecom	<a href="http://www.ti.com/communications">www.ti.com/communications</a>
Computers and Peripherals	<a href="http://www.ti.com/computers">www.ti.com/computers</a>
Consumer Electronics	<a href="http://www.ti.com/consumer-apps">www.ti.com/consumer-apps</a>
Energy and Lighting	<a href="http://www.ti.com/energy">www.ti.com/energy</a>
Industrial	<a href="http://www.ti.com/industrial">www.ti.com/industrial</a>
Medical	<a href="http://www.ti.com/medical">www.ti.com/medical</a>
Security	<a href="http://www.ti.com/security">www.ti.com/security</a>
Space, Avionics and Defense	<a href="http://www.ti.com/space-avionics-defense">www.ti.com/space-avionics-defense</a>
Transportation and Automotive	<a href="http://www.ti.com/automotive">www.ti.com/automotive</a>
Video and Imaging	<a href="http://www.ti.com/video">www.ti.com/video</a>
Wireless	<a href="http://www.ti.com/wireless-apps">www.ti.com/wireless-apps</a>

TI E2E Community Home Page

[e2e.ti.com](http://e2e.ti.com)

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265  
Copyright © 2011, Texas Instruments Incorporated