3.3-V RS-485 TRANSCEIVER

Check for Samples: SN65HVD11-HT

FEATURES

- **Operates With a 3.3-V Supply**
- **Bus-Pin ESD Protection Exceeds 16-kV Human-Body Model (HBM)**
- **1/8 Unit-Load Option Available (up to 256 Nodes on Bus)**
- **Optional Driver Output Transition Times for Signaling Rates (1) of 1 Mbps, 10 Mbps, and 32 Mbps**
- **Based on ANSI TIA/EIA-485-A**
- **Bus-Pin Short Circuit Protection From –7 V to 12 V**
- **Open-Circuit, Idle-Bus, and Shorted-Bus Fail-Safe Receiver**
- **Glitch-Free Power-Up and Power-Down Protection for Hot-Plugging Applications**
- **SN75176 Footprint**

APPLICATIONS

- **Down-Hole Drilling**
- **High Temperature Environments**
- **Digital Motor Controls**
- **Utility Meters**
- **Chassis-to-Chassis Interconnects**
- **Electronic Security Stations**
- **Industrial Process Control**
- **Building Automation**
- **Point-of-Sale (POS) Terminals and Networks**

SUPPORTS EXTREME TEMPERATURE APPLICATIONS

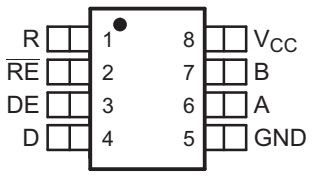
- **Controlled Baseline**
- **One Assembly/Test Site**
- **One Fabrication Site**
- **Available in Extreme (–55°C/210°C) Temperature Range (2)**
- **Extended Product Life Cycle**
- **Extended Product-Change Notification**
- **Product Traceability**
- **Texas Instruments' high temperature products utilize highly optimized silicon (die) solutions with design and process enhancements to maximize performance over extended temperatures.**

DESCRIPTION/ORDERING INFORMATION

The SN65HVD11 combines a 3-state differential line driver and differential input line receiver that operates with a single 3.3-V power supply. It is designed for balanced transmission lines and meets or exceeds ANSI TIA/EIA-485-A and ISO 8482:1993, with the exception that the thermal shutdown is removed. This differential bus transceiver is a monolithic integrated circuit designed for bidirectional data communication on multipoint bus-transmission lines. The driver and receiver have active-high and active-low enables, respectively, that can be externally connected together to function as direction control.

The driver differential outputs and receiver differential inputs connect internally to form a differential input/ output (I/O) bus port that is designed to offer minimum loading to the bus when the driver is disabled or V_{CC} = 0.

D OR JD OR HKJ PACKAGE
(TOP VIEW)



(1) The signaling rate of a line is the number of voltage transitions that are made per second expressed in the units bits per second (bps).

(2) Custom temperature ranges available

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

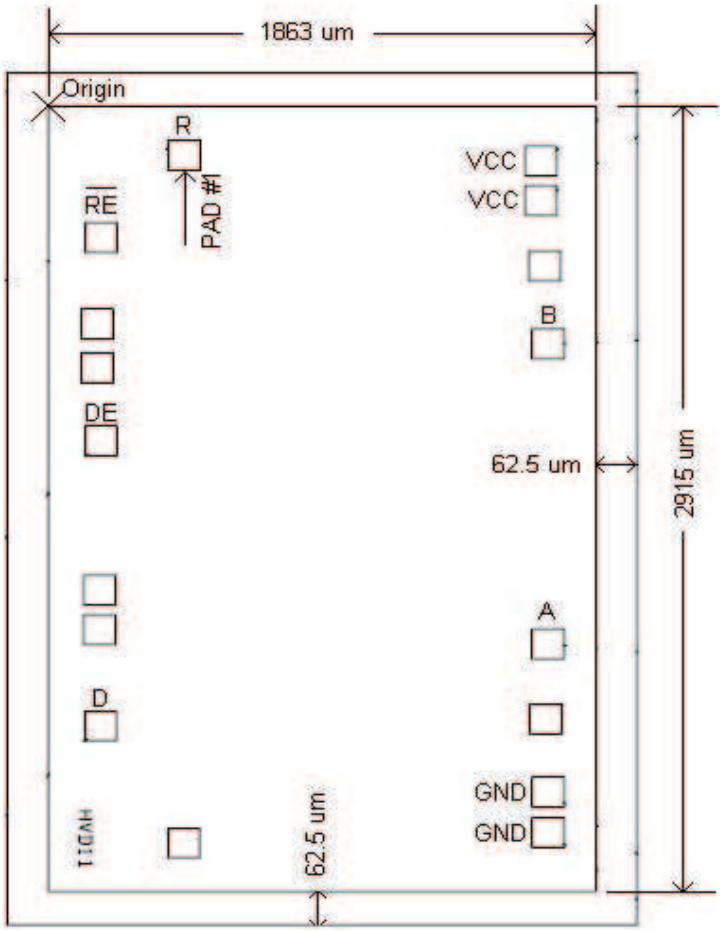
BARE DIE INFORMATION

DIE THICKNESS	BACKSIDE FINISH	BACKSIDE POTENTIAL	BOND PAD METALLIZATION COMPOSITION
15 mils.	Silicon with backgrind	GND	Cu-Ni-Pd

Table 1. Bond Pad Coordinates in Microns - Rev A

DESCRIPTION(1)	PAD NUMBER	a	b	c	d
R	1	69.30	372.15	185.30	489.15
~RE	2	388.75	71.50	503.75	186.50
DNC	3	722.40	55.40	839.40	172.40
DNC	4	891.40	55.40	1008.40	172.40
DE	5	1174.80	71.50	1289.80	186.50
DNC	6	1754.35	65.40	1869.35	180.40
DNC	7	1907.35	65.40	2022.35	180.40
D	8	2280.55	69.50	2395.55	184.50
DNC	9	2733.50	371.50	2848.50	486.50
GND	10	2691	1693.10	2808	1810.10
GND	11	2535	1693.10	2652	1810.10
DNC	12	2253.45	1685.65	2368.45	1800.65
A	13	1961.55	1693.10	2078.55	1810.10
B	14	799.55	1693.10	916.55	1810.10
DNC	15	498.35	1681.20	613.35	1796.20
VCC	16	244.80	1668.50	359.80	1783.50
VCC	17	91.80	1668.50	206.80	1783.50

(1) DNC = Do Not Connect



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

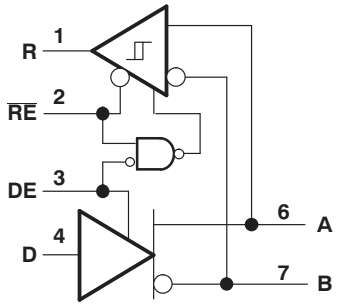
ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

ORDERING INFORMATION(1)

SIGNALING RATE	UNIT LOADS	T_A	PACKAGE(2)	TOP-SIDE MARKING
			CDIP	
10 Mbps	1/8	–55°C to 210°C	SN65HVD11SJD	SN65HVD11SJD
10 Mbps	1/8	–55°C to 210°C	SN65HVD11SKGDA	
10 Mbps	1/8	–55°C to 210°C	SN65HVD11SHKJ	SN65HVD11SHKJ
10 Mbps	1/8	–55°C to 175°C	SN65HVD11HD	HD11

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI Web site at www.ti.com.
(2) Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

FUNCTIONAL BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS(1) (2)

over operating free-air temperature range (unless otherwise noted)

				VALUE	UNIT
V_{CC}	Supply voltage range			–0.3 to 6	V
	Voltage range at A or B			–9 to 14	V
	Input voltage range at D, DE, R, or $\overline{RE}$			–0.5 to V_{CC} + 0.5	V
	Voltage input range, transient pulse, A and B, through 100 Ω (see Figure 12)			–50 to 50	V
I_O	Receiver output current range			–11 to 11	mA
	Electrostatic discharge	Human-Body Model (HBM)(3)	A, B, and GND	16	kV
			All pins	4	
		Charged-Device Model (CDM)(4)	All pins charge	1	
	Continuous total power dissipation			See Dissipation Ratings Table	

(1) Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values, except differential I/O bus voltages, are with respect to network ground terminal.
(3) Tested in accordance with JEDEC Standard 22, Test Method A114-A.
(4) Tested in accordance with JEDEC Standard 22, Test Method C101.

RECOMMENDED OPERATING CONDITIONS

			T_A = –55°C to 125°C			T_A = 175°C			T_A = 210°C			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		3		3.6	3		3.6	3		3.6	V
V_I or V_{IC}	Voltage at any bus terminal (separately or common mode)		-7(1)		12	-7(1)		12	-7(1)		12	V
V_{IH}	High-level input voltage	D, DE, $\overline{RE}$	2		V_{CC}	2		V_{CC}	2		V_{CC}	V
V_{IL}	Low-level input voltage	D, DE, $\overline{RE}$	0		0.8	0		0.8	0		0.8	V
V_{ID}	Differential input voltage	Figure 8	-12		12	-12		12	-12		12	V
I_{OH}	High-level output current	Driver	-60			-60			-60			mA
		Receiver	-8			-8			-8			
I_{OL}	Low-level output current	Driver			60			60			60	mA
		Receiver			8			8			8	
R_L	Differential load resistance		54	60		54	60		54	60		Ω
C_L	Differential load capacitance			50			50			50		pF
	Signaling rate				10			10			10	Mbps
T_J(2)	Operating junction temperature			129			179			214		°C

(1) The algebraic convention, in which the least-positive (most-negative) limit is designated as minimum, is used in this data sheet.
(2) See Thermal Characteristics table for information regarding this specification.

DRIVER ELECTRICAL CHARACTERISTICS

over recommended operating conditions (unless otherwise noted)

PARAMETER			TEST CONDITIONS		T_A = –55°C to 125°C			T_A = 175°C(1)			T_A = 210°C(2)			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
V_{IK}	Input clamp voltage		I_I = –18 mA		–1.5			–1.5			–1.5			V
$\|V_{OD}\|$	Differential output voltage		I_O = 0		2		V_{CC}	2		V_{CC}	2		V_{CC}	V
			R_L = 54 Ω, See Figure 2		1.0			1			1			
			V_{test} = –7 V to 12 V, See Figure 3		1.0			1			1			
$\Delta\|V_{OD}\|$	Change in magnitude of differential output voltage		V_{test} = –7 V to 12 V, See Figure 2 and Figure 3		-0.2		0.2	-0.25		0.25	-0.25		0.25	V
$V_{OC(PP)}$	Peak-to-peak common-mode output voltage		See Figure 4			400			400			400		mV
$V_{OC(SS)}$	Steady-state common-mode output voltage		See Figure 4		1.4		2.5	1.4		2.5	1.4		2.5	V
$\Delta V_{OC(SS)}$	Change in steady-state common-mode output voltage		See Figure 4		–0.06		0.06	–0.06		0.06	–0.06		0.06	V
I_{OZ}	High-impedance output current		See receiver input currents											
I_I	Input current	D			–100		0	–100		3	–100		3	µA
		DE			0		100	0		100	0		100	
I_{OS}	Short-circuit output current		–7 V ≤ V_O ≤ 12 V		–250		250	–250		250	–250		250	mA
$C_{(OD)}$	Differential output capacitance		V_{OD} = 0.4 sin (4E6πt) + 0.5 V, DE = 0 V			18			18			18		pF
I_{CC}	Supply current		$\overline{RE}$ = V_{CC}, D and DE = V_{CC}, No load	Receiver disabled and driver enabled		11	15.5		11.5	17.5		14	18	mA
			$\overline{RE}$ = V_{CC}, D = V_{CC}, DE = 0 V, No load	Receiver disabled and driver disabled (standby)		2.5	20		20	150		175	450	µA
			$\overline{RE}$ = 0 V, D and DE = V_{CC}, No load	Receiver enabled and driver enabled		11	15.5		11	17.5		11	18	mA

(1) Minimum and maximum parameters are characterized for operation at T_A = 175°C but may not be production tested at that temperature. Production test limits with statistical guardbands are used to ensure high temperature performance.

(2) Minimum and maximum parameters are characterized for operation at T_A = 210°C but may not be production tested at that temperature. Production test limits with statistical guardbands are used to ensure high temperature performance.

DRIVER SWITCHING CHARACTERISTICS

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A = –55°C to 125°C			T_A = 175°C(1)			T_A = 210°C(2)			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
t_{PLH}	Propagation delay time, low-to-high-level output	R_L = 54 Ω, C_L = 50 pF, See Figure 5	18	25	40	18	25	40	18	25	40	ns
t_{PHL}	Propagation delay time, high-to-low-level output		18	25	40	18	25	40	18	25	40	ns
t_r	Differential output signal rise time		10	21	30	10	22	30	10	22	30	ns
t_f	Differential output signal fall time		10	21	30	10	22	30	10	22	30	ns
$t_{sk(p)}$	Pulse skew ($\lvert t_{PHL} - t_{PLH} \rvert$)				2.5			2.5			2.5	ns
$t_{sk(pp)}$(3)	Part-to-part skew (t_{PHL} or t_{PLH})				11			11			11	ns
t_{PZH}	Propagation delay time, high-impedance to high-level output	R_L = 110 Ω, $\overline{RE}$ = 0 V, See Figure 6			55			55			55	ns
t_{PHZ}	Propagation delay time, high-level to high-impedance output				55			55			55	ns
t_{PZL}	Propagation delay time, high-impedance to low-level output	R_L = 110 Ω, $\overline{RE}$ = 0 V, See Figure 7			55			55			55	ns
t_{PLZ}	Propagation delay time, low-level to high-impedance output				75			75			75	ns
t_{PZH}	Propagation delay time, standby to high-level output	R_L = 110 Ω, $\overline{RE}$ = 3 V, See Figure 6			6			6			6	µs
t_{PZL}	Propagation delay time, standby to low-level output	R_L = 110 Ω, $\overline{RE}$ = 3 V, See Figure 7			6			6			6	µs

(1) Minimum and maximum parameters are characterized for operation at T_A = 175°C but may not be production tested at that temperature. Production test limits with statistical guardbands are used to ensure high temperature performance.

(2) Minimum and maximum parameters are characterized for operation at T_A = 210°C but may not be production tested at that temperature. Production test limits with statistical guardbands are used to ensure high temperature performance.

(3) $t_{sk(pp)}$ is the magnitude of the difference in propagation delay times between any specified terminals of two devices when both devices operate with the same supply voltages, at the same temperature, and have identical packages and test circuits.

RECEIVER ELECTRICAL CHARACTERISTICS

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS		T_A = –55°C to 125°C			T_A = 175°C (1)			T_A = 210°C (2)			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
V_{IT+}	Positive-going input threshold voltage	I_O = –8 mA				–0.01			–0.01			–0.01	V
$V_{IT–}$	Negative-going input threshold voltage	I_O = 8 mA		–0.2			–0.2			–0.2			V
V_{hys}	Hysteresis voltage (V_{IT+} – $V_{IT–}$)				35			41			41		mV
V_{IK}	Enable-input clamp voltage	I_I = –18 mA		–1.5			–1.5			–1.5			V
V_{OH}	High-level output voltage	V_{ID} = 200 mV, I_{OH} = –8 mA, See Figure 8		2.4			2.4			2.4			V
V_{OL}	Low-level output voltage	V_{ID} = –200 mV, I_{OL} = 8 mA, See Figure 8				0.4			0.4			0.4	V
I_{OZ}	High-impedance state output current	V_O = 0 or V_{CC}, $\overline{RE}$ = V_{CC}		–1		1	–1		1	–1		1	µA
I_I	Bus input current	V_A or V_B = 12 V	Other input at 0 V		0.075	0.11		0.1	0.15		0.1	0.15	mA
		V_A or V_B = 12 V, V_{CC} = 0 V			0.085	0.13		0.12	0.16		0.12	0.16	
		V_A or V_B = –7 V		–0.1	–0.05		–0.3	–0.15		–0.3	–0.15		
		V_A or V_B = –7 V, V_{CC} = 0 V		–0.1	–0.05		–0.3	–0.15		–0.3	–0.15		
I_{IH}	High-level input current, $\overline{RE}$	V_{IH} = 2 V		–30		0	–30		3	–30		3	µA
I_{IL}	Low-level input current, $\overline{RE}$	V_{IL} = 0.8 V		–30		0	–30		0	–30		0	µA
C_{ID}	Differential input capacitance	V_{ID} = 0.4 sin (4E6πt) + 0.5 V, DE at 0 V			15			18			18		pF
I_{CC}	Supply current	$\overline{RE}$ = 0 V, D and DE = 0 V, No load	Receiver enabled and driver disabled		5	8		7.5	8.5		7.5	10	mA
		$\overline{RE}$ = V_{CC}, D = V_{CC}, DE = 0 V, No load	Receiver disabled and driver disabled (standby)		2.5	20		12.5	200		175	450	µA
		$\overline{RE}$ = 0 V, D and DE = V_{CC}, No load	Receiver enabled and driver enabled		11	15.5		11.5	17.5		14	18	mA

(1) Minimum and maximum parameters are characterized for operation at T_A = 175°C but may not be production tested at that temperature. Production test limits with statistical guardbands are used to ensure high temperature performance.

(2) Minimum and maximum parameters are characterized for operation at T_A = 210°C but may not be production tested at that temperature. Production test limits with statistical guardbands are used to ensure high temperature performance.

RECEIVER SWITCHING CHARACTERISTICS

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A = –55°C to 125°C			T_A = 175°C(1)			T_A = 210°C(2)			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
t_{PLH}	Propagation delay time, low-to-high-level output	V_{ID} = –1.5 V to 1.5 V, C_L = 15 pF, See Figure 9	30	55	70	30	55	70	30	55	70	ns
t_{PHL}	Propagation delay time, high-to-low-level output		30	55	70	30	55	70	30	55	70	ns
$t_{sk(p)}$	Pulse skew ($\lvert t_{PHL} - t_{PLH} \rvert$)				4			4			4	ns
$t_{sk(pp)}$(3)	Part-to-part skew				15			15			15	ns
t_r	Output signal rise time	C_L = 15 pF, See Figure 9	1	3	5	1	4	5	1	4	5	ns
t_f	Output signal fall time		1	3	5	1	4	5	1	4	5	ns
t_{PZH}(2)	Output enable time to high level	C_L = 15 pF, DE = 3 V, See Figure 10			15			15			15	ns
t_{PZL}(2)	Output enable time to low level				15			15			15	ns
t_{PHZ}	Output disable time from high level				20			20			20	ns
t_{PLZ}	Output disable time from low level				15			15			15	ns
t_{PZH}(3)	Propagation delay time, standby-to-high-level output	C_L = 15 pF, DE = 0, See Figure 11			6			6			6	µs
t_{PZL}(3)	Propagation delay time, standby-to-low-level output				6			6			6	µs

(1) Minimum and maximum parameters are characterized for operation at T_A = 175°C but may not be production tested at that temperature. Production test limits with statistical guardbands are used to ensure high temperature performance.
(2) Minimum and maximum parameters are characterized for operation at T_A = 210°C but may not be production tested at that temperature. Production test limits with statistical guardbands are used to ensure high temperature performance.
(3) $t_{sk(pp)}$ is the magnitude of the difference in propagation delay times between any specified terminals of two devices when both devices operate with the same supply voltages, at the same temperature, and have identical packages and test circuits.

THERMAL CHARACTERISTICS FOR JD PACKAGE

over operating free-air temperature range unless otherwise noted (1)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
θ_{JA}	Junction-to-ambient thermal resistance(2)	High-K board(3), No airflow	JD pkg		64.9		°C/W
		No airflow	JD pkg		83.4		
θ_{JB}	Junction-to-board thermal resistance	High-K board without underfill	JD pkg		27.9		°C/W
θ_{JC}	Junction-to-case thermal resistance		JD pkg		6.49		°C/W
P_D	Device power dissipation	R_L= 60 Ω, C_L = 50 pF, DE = V_{CC}, $\overline{RE}$ = 0 V, Input to D a 50% duty cycle square wave at indicated signaling rate	HVD11 (10 Mbps)		165		mW

(1) See *Application Information* section for an explanation of these parameters.
(2) The intent of θ_{JA} specification is solely for a thermal performance comparison of one package to another in a standardized environment. This methodology is not meant to and will not predict the performance of a package in an application-specific environment.
(3) JED51-7, High Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages

THERMAL CHARACTERISTICS FOR HKJ PACKAGE

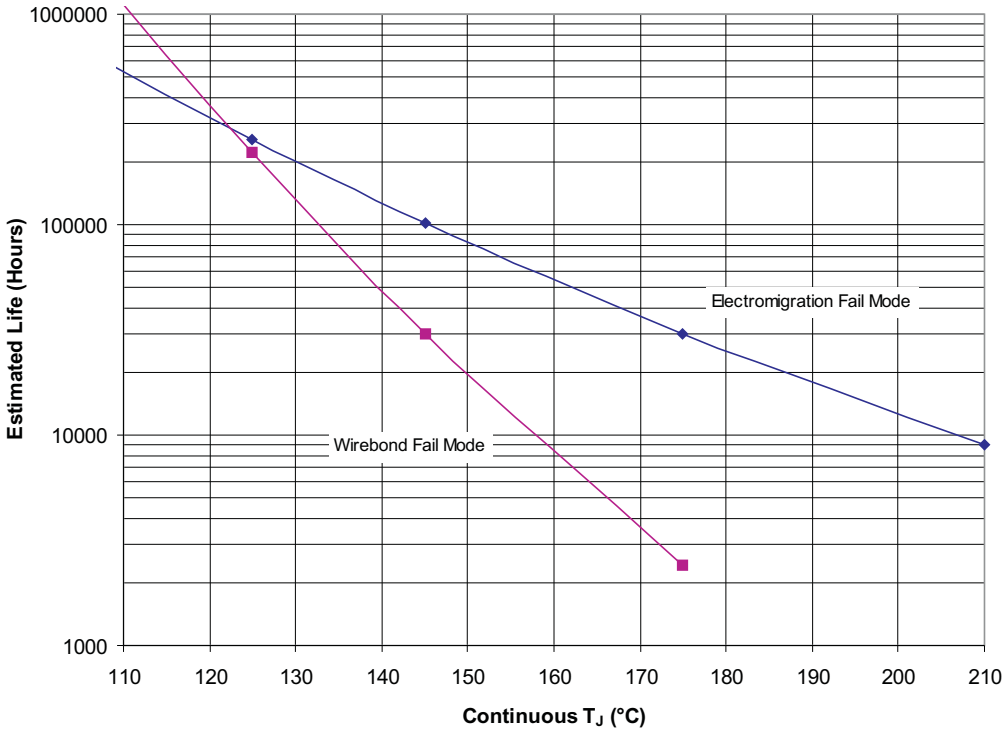
over operating free-air temperature range (unless otherwise noted)

PARAMETERS		MAX	UNIT
θ_{JC}	Junction-to-case thermal resistance (to bottom of case)	5.7	°C/W
	Junction-to-case thermal resistance (to top of case lid - as if formed dead bug)	13.7	

THERMAL CHARACTERISTICS FOR D PACKAGE

over operating free-air temperature range (unless otherwise noted)

PARAMETERS		MAX	UNIT
θ_{JC}	Junction-to-case thermal resistance (to bottom of case)	39.4	°C/W



(1) See data sheet for absolute maximum and minimum recommended operating conditions.

(2) Silicon operating life design goal is 10 years at 105°C junction temperature (does not include package interconnect life).

(3) The predicted operating lifetime vs. junction temperature is based on reliability modeling using electromigration as the dominant failure mechanism affecting device wearout for the specific device process and design characteristics.

(4) Wirebond fail mode applicable for D package only.

Figure 1. SN65HVD11SJD/SN65HVD11SKGDA/SN65HVD11SHKJ/SN65HVD11HD Operating Life Derating Chart

PARAMETER MEASUREMENT INFORMATION

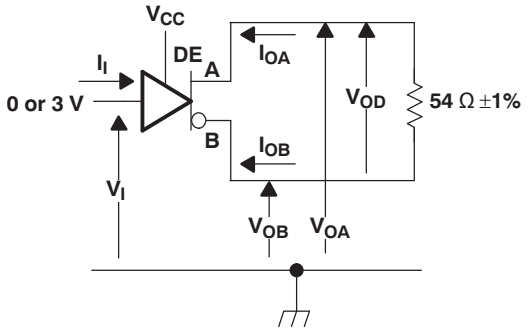


Figure 2. Driver V_{OD} Test Circuit and Voltage and Current Definitions

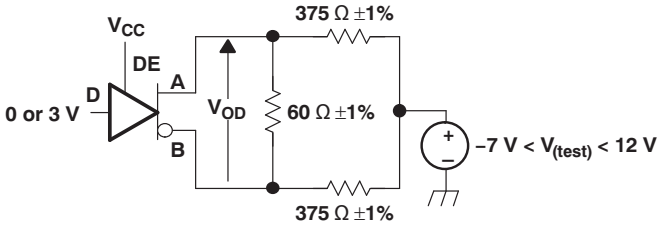
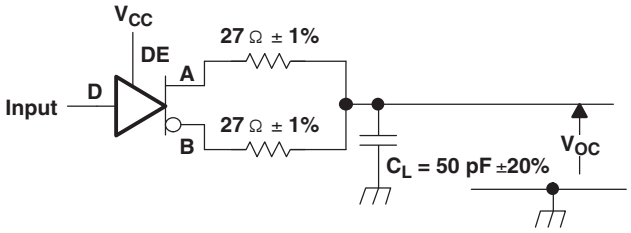
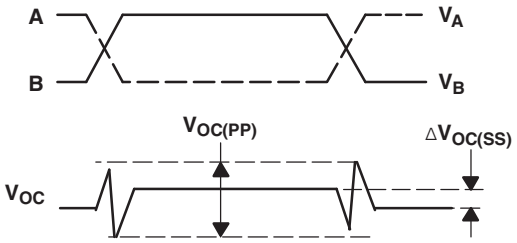


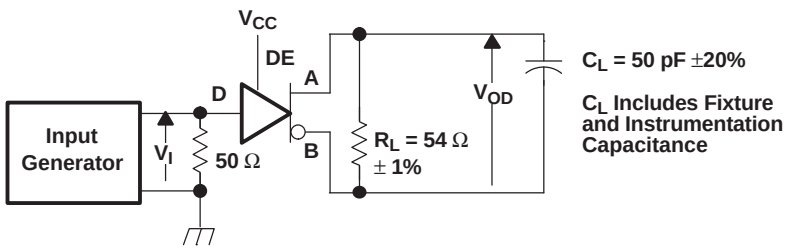
Figure 3. Driver V_{OD} With Common-Mode Loading Test Circuit

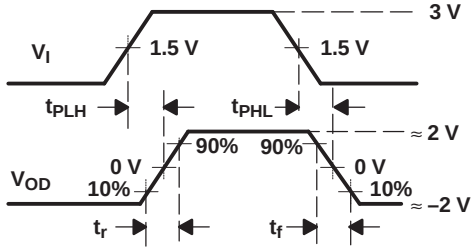




A. Input: PRR = 500 kHz, 50% Duty Cycle, t_r<6ns, t_f<6ns, Z_O = 50 Ω
B. C_L Includes fixture and instrumentation capacitance

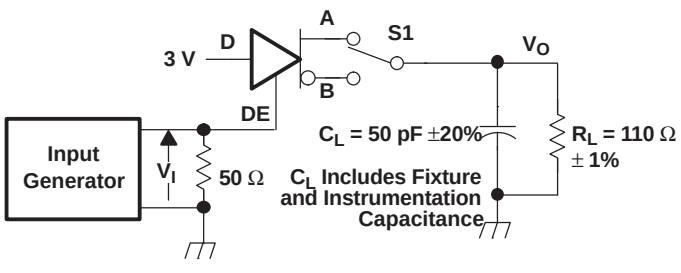
Figure 4. Test Circuit and Definitions for Driver Common-Mode Output Voltage

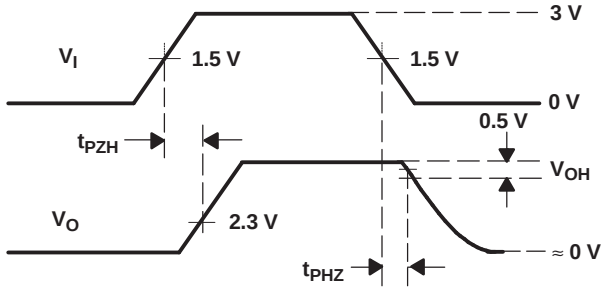




Generator: PRR = 500 kHz, 50% Duty Cycle, t_r <6 ns, t_f <6 ns, Z_o = 50 Ω

Figure 5. Driver Switching Test Circuit and Voltage Waveforms

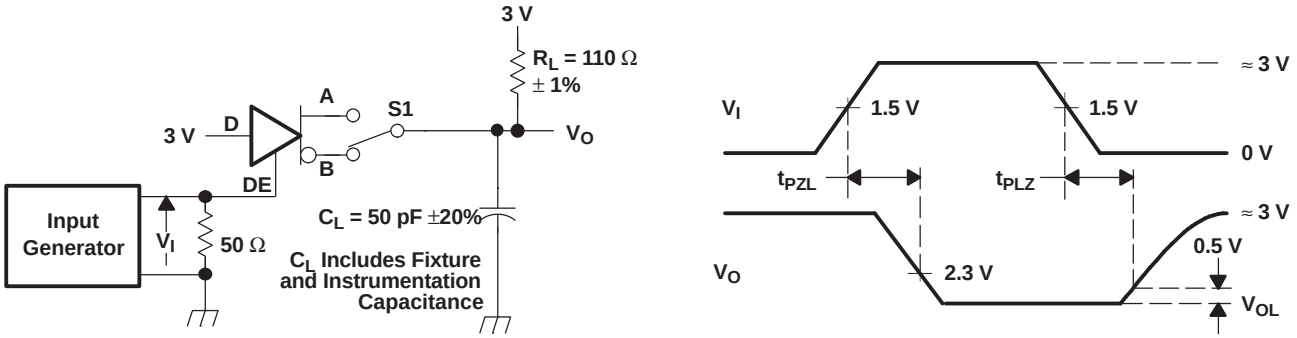




Generator: PRR = 500 kHz, 50% Duty Cycle, t_r <6 ns, t_f <6 ns, Z_o = 50 Ω

Figure 6. Driver High-Level Enable and Disable Time Test Circuit and Voltage Waveforms

PARAMETER MEASUREMENT INFORMATION (continued)



Generator: PRR = 500 kHz, 50% Duty Cycle, t_r <6 ns, t_f <6 ns, Z_o = 50 Ω

Figure 7. Driver Low-Level Output Enable and Disable Time Test Circuit and Voltage Waveforms

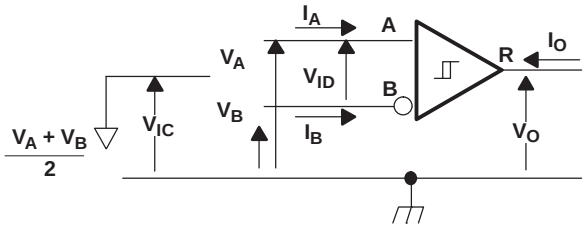
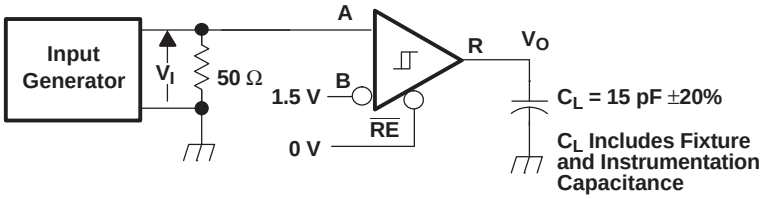


Figure 8. Receiver Voltage and Current Definitions



Generator: PRR = 500 kHz, 50% Duty Cycle, t_r <6 ns, t_f <6 ns, Z_o = 50 Ω

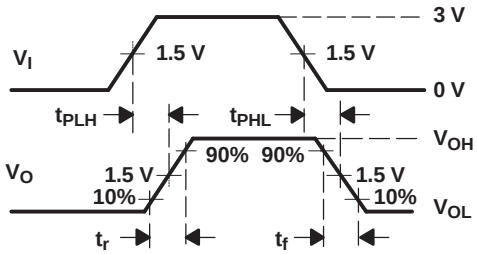
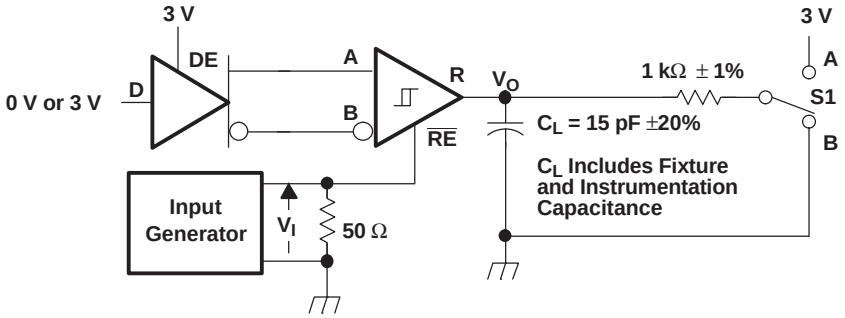


Figure 9. Receiver Switching Test Circuit and Voltage Waveforms

PARAMETER MEASUREMENT INFORMATION (continued)



Generator: PRR = 500 kHz, 50% Duty Cycle, t_r <6 ns, t_f <6 ns, Z_o = 50 Ω

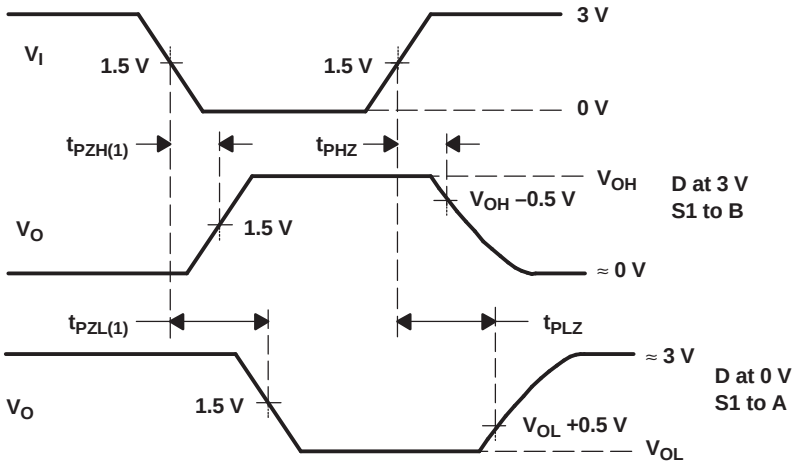


Figure 10. Receiver Enable and Disable Time Test Circuit and Voltage Waveforms With Drivers Enabled

PARAMETER MEASUREMENT INFORMATION (continued)

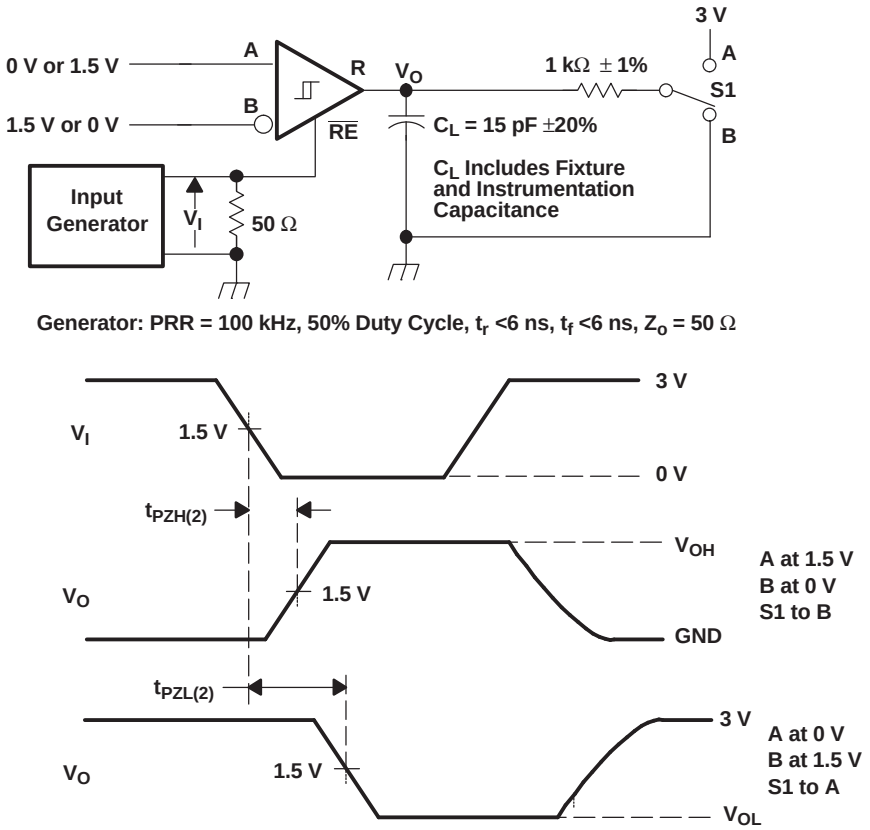
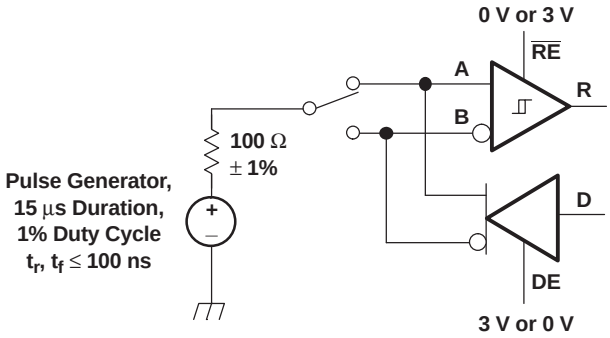


Figure 11. Receiver Enable Time From Standby (Driver Disabled)



NOTE: This test is conducted to test survivability only. Data stability at the R output is not specified.

Figure 12. Test Circuit, Transient Over Voltage Test

PARAMETER MEASUREMENT INFORMATION (continued)

FUNCTION TABLES

Table 2. DRIVER(1)

		OUTPUTS	
INPUT D	ENABLE DE	A	B
H	H	H	L
L	H	L	H
X	L	Z	Z
Open	H	H	L

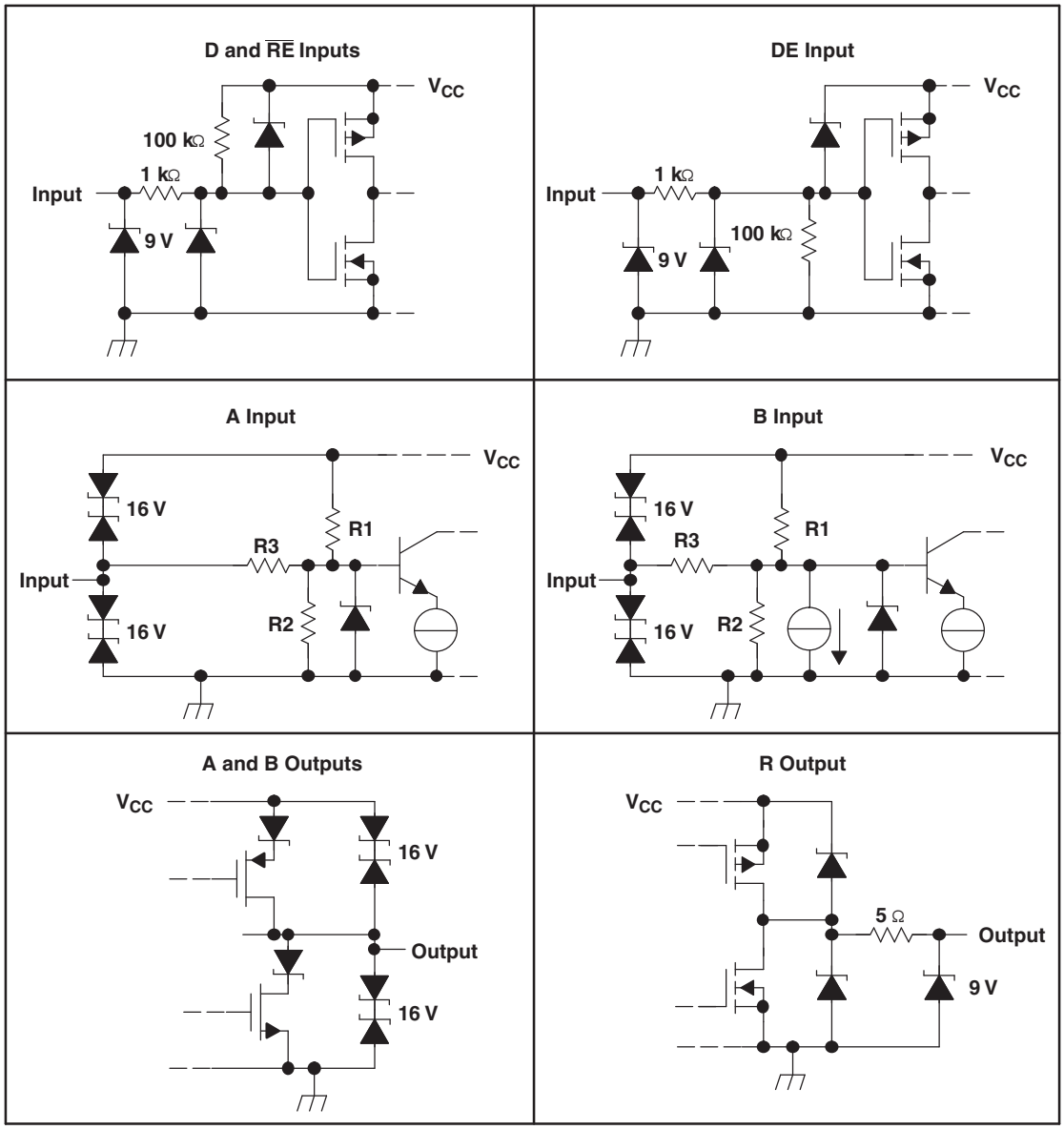
(1) H = high level
L = low level
Z = high impedance
X = irrelevant
? = indeterminate

Table 3. RECEIVER(1)

DIFFERENTIAL INPUTS $V_{ID} = V_A - V_B$	ENABLE $\overline{RE}$	OUTPUT R
$V_{ID} \le -0.2$ V	L	L
-0.2 V $< V_{ID} < -0.01$ V	L	?
-0.01 V $\le V_{ID}$	L	H
X	H	Z
Open circuit	L	H
Short circuit	L	H

(1) H = high level
L = low level
Z = high impedance
X = irrelevant
? = indeterminate

EQUIVALENT INPUT AND OUTPUT SCHEMATIC DIAGRAMS



R1/R2 = 36 kΩ

R3 = 180 kΩ

TYPICAL CHARACTERISTICS

RMS SUPPLY CURRENT vs SIGNALING RATE

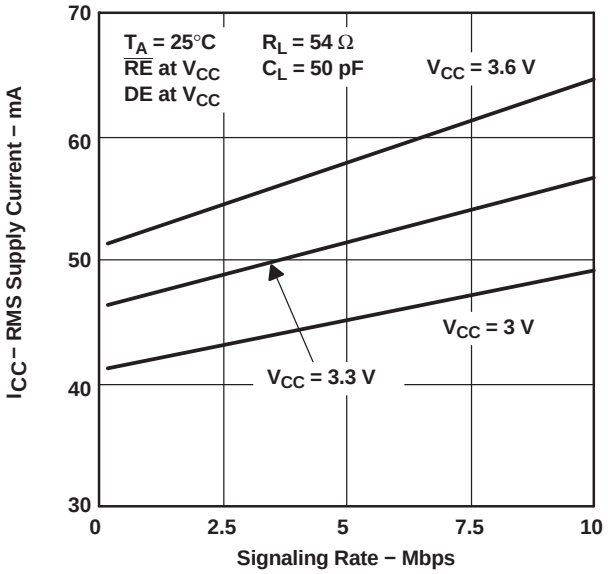


Figure 13.

BUS INPUT CURRENT vs BUS INPUT VOLTAGE

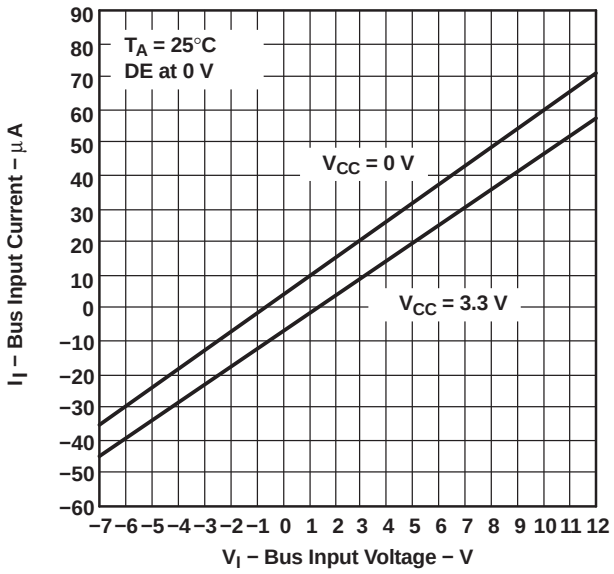


Figure 14.

HIGH-LEVEL OUTPUT CURRENT vs DRIVER HIGH-LEVEL OUTPUT VOLTAGE

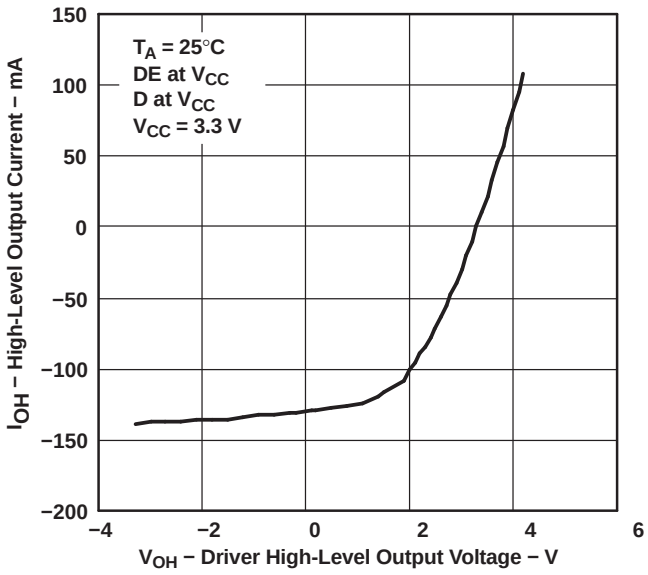


Figure 15.

LOW-LEVEL OUTPUT CURRENT vs DRIVER LOW-LEVEL OUTPUT VOLTAGE

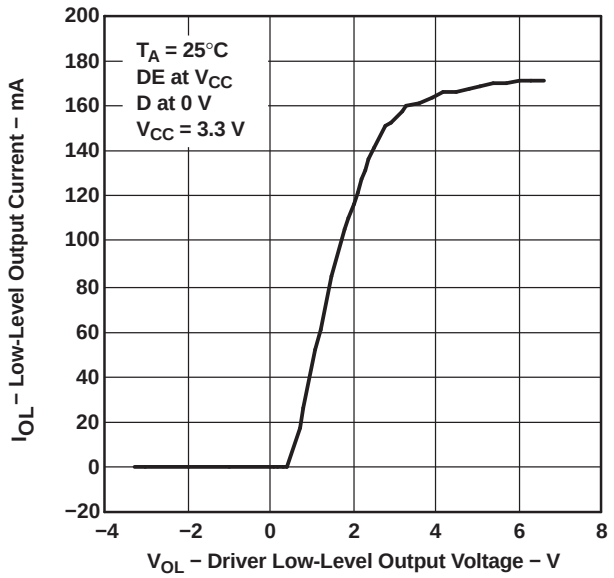


Figure 16.

TYPICAL CHARACTERISTICS (continued)

DRIVER DIFFERENTIAL OUTPUT vs FREE-AIR TEMPERATURE

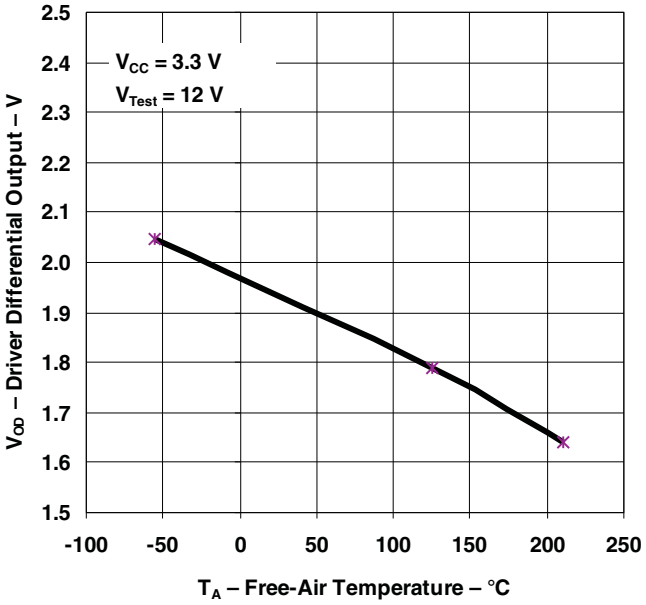


Figure 17.

DRIVER OUTPUT CURRENT vs SUPPLY VOLTAGE

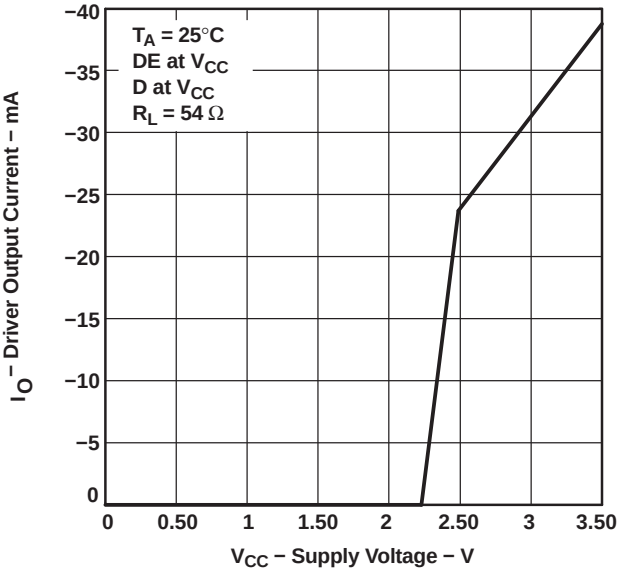


Figure 18.

ENABLE TIME vs COMMON-MODE VOLTAGE (SEE Figure 20)

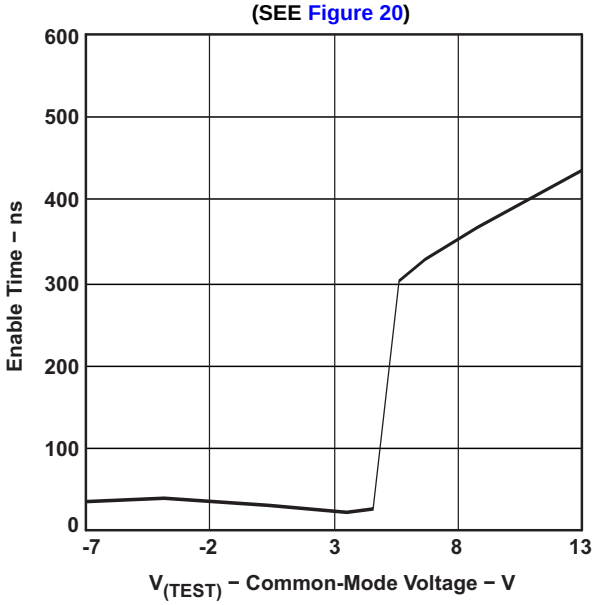


Figure 19.

TYPICAL CHARACTERISTICS (continued)

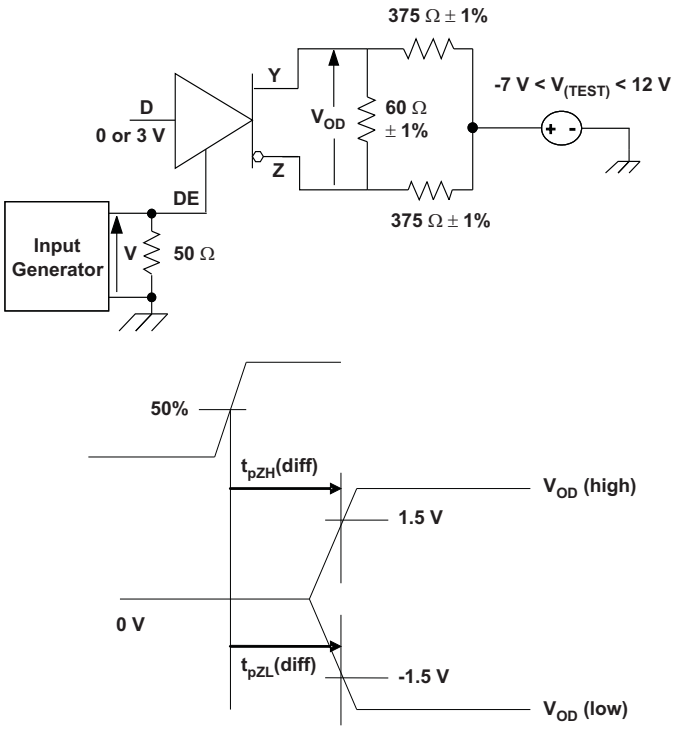
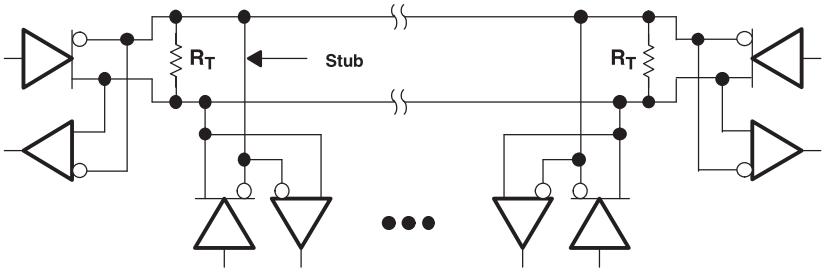


Figure 20. Driver Enable Time From DE to V_{OD}

The time $t_{pZL}(x)$ is the measure from DE to $V_{OD}(x)$. V_{OD} is valid when it is greater than 1.5 V.

APPLICATION INFORMATION



256 Devices on Bus

NOTE: The line should be terminated at both ends with its characteristic impedance ($R_T = Z_O$). Stub lengths off the main line should be kept as short as possible.

Figure 21. Typical Application Circuit

THERMAL CHARACTERISTICS OF IC PACKAGES

θ_{JA} **(Junction-to-Ambient Thermal Resistance)** is defined as the difference in junction temperature to ambient temperature divided by the operating power.

θ_{JA} is *not* a constant and is a strong function of:

- the PCB design (50% variation)
- altitude (20% variation)
- device power (5% variation)

θ_{JA} can be used to compare the thermal performance of packages if the specific test conditions are defined and used. Standardized testing includes specification of PCB construction, test chamber volume, sensor locations, and the thermal characteristics of holding fixtures. θ_{JA} is often misused when it is used to calculate junction temperatures for other installations.

TI uses two test PCBs as defined by JEDEC specifications. The low-k board gives *average* in-use condition thermal performance, and it consists of a single copper trace layer 25 mm long and 2-oz thick. The high-k board gives best *case* in-use condition, and it consists of two 1-oz buried power planes with a single copper trace layer 25 mm long and 2-oz thick. A 4% to 50% difference in θ_{JA} can be measured between these two test cards.

θ_{JC} **(Junction-to-Case Thermal Resistance)** is defined as difference in junction temperature to case divided by the operating power. It is measured by putting the mounted package up against a copper block cold plate to force heat to flow from die, through the mold compound into the copper block.

θ_{JC} is a useful thermal characteristic when a heatsink is applied to package. It is *not* a useful characteristic to predict junction temperature because it provides pessimistic numbers if the case temperature is measured in a nonstandard system and junction temperatures are backed out. It can be used with θ_{JB} in 1-dimensional thermal simulation of a package system.

θ_{JB} **(Junction-to-Board Thermal Resistance)** is defined as the difference in the junction temperature and the PCB temperature at the center of the package (closest to the die) when the PCB is clamped in a cold-plate structure. θ_{JB} is only defined for the high-k test card.

θ_{JB} provides an overall thermal resistance between the die and the PCB. It includes a bit of the PCB thermal resistance (especially for BGA's with thermal balls) and can be used for simple 1-dimensional network analysis of package system, see Figure 22.

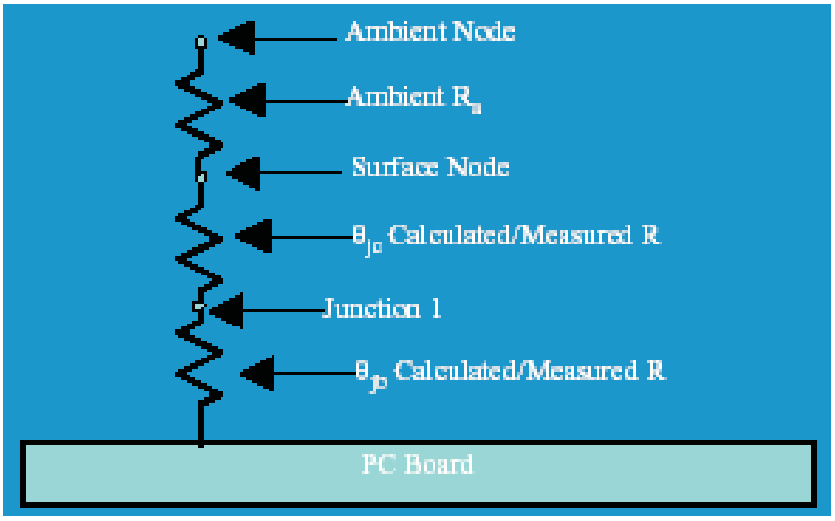


Figure 22. Thermal Resistance

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/ Ball Finish	MSL Peak Temp (3)	Samples (Requires Login)
SN65HVD11HD	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	Purchase Samples
SN65HVD11SHKJ	ACTIVE	CFP	HKJ	8	1	TBD	Call TI	N / A for Pkg Type	Call Local Sales Office
SN65HVD11SJD	ACTIVE	CDIP SB	JDJ	8	1	TBD	POST-PLATE	N / A for Pkg Type	Call Local Sales Office
SN65HVD11SKGDA	ACTIVE	XCEPT	KGD	0	130	TBD	Call TI	N / A for Pkg Type	Call Local Sales Office

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

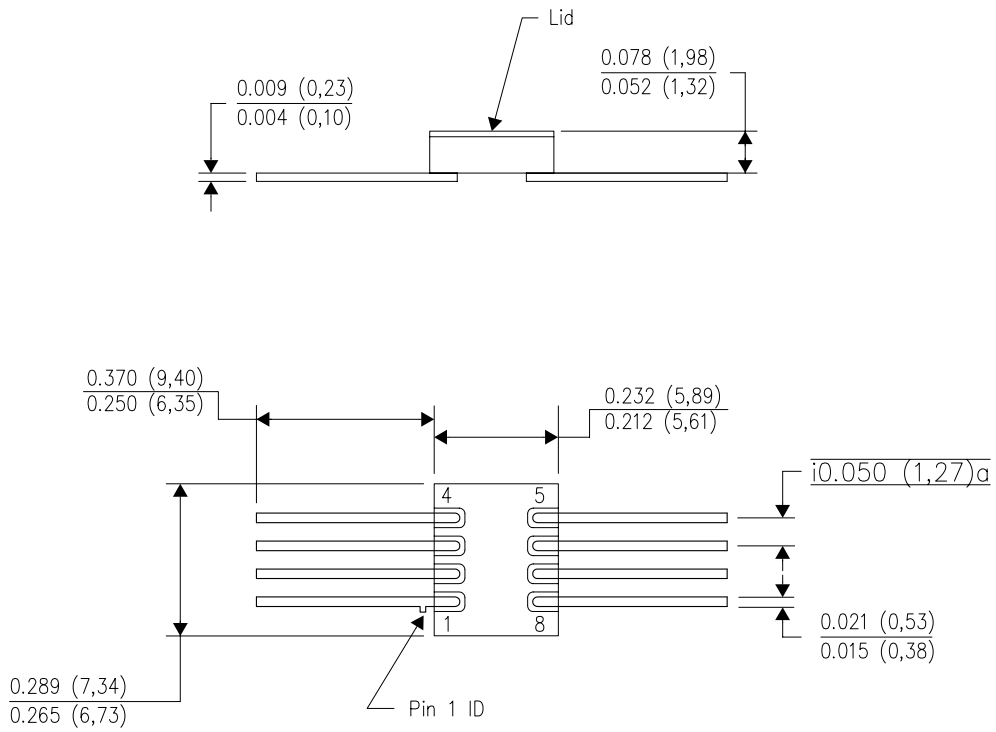
OTHER QUALIFIED VERSIONS OF SN65HVD11-HT :

- Catalog: SN65HVD11

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product

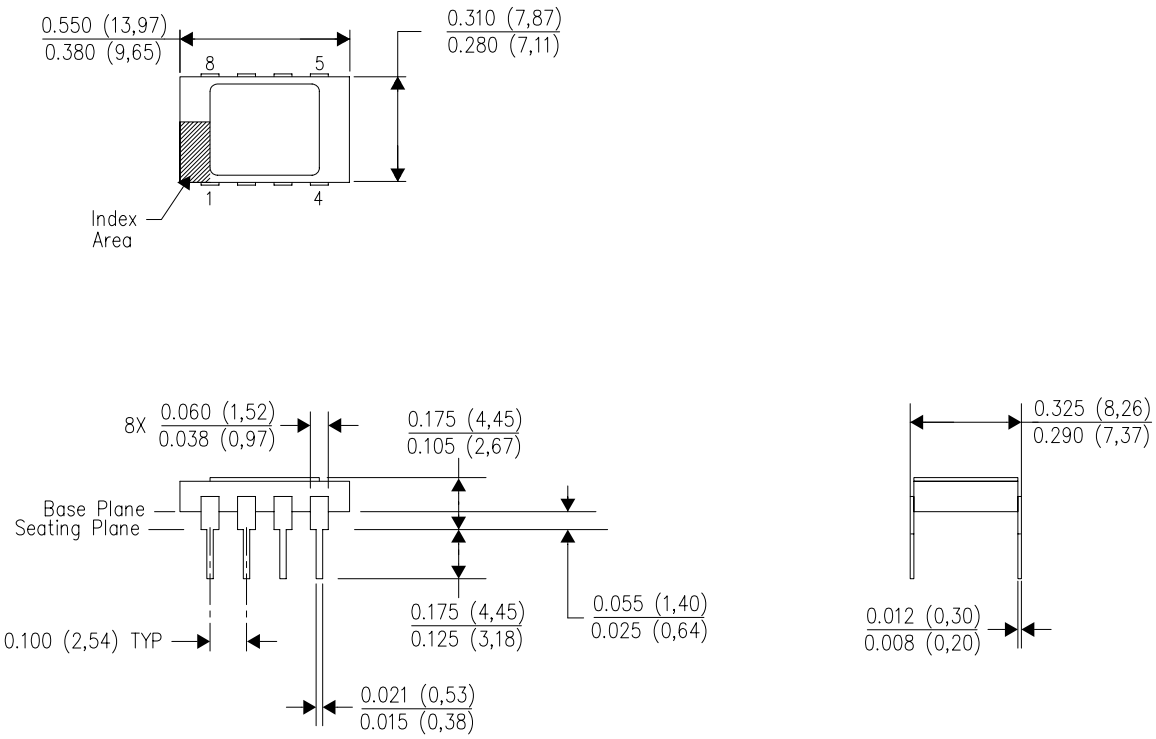
HKJ (R–CDFP–F8) CERAMIC DUAL FLATPACK



4209892/A 10/08

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package can be hermetically sealed with a metal lid.
D. The terminals will be gold plated.

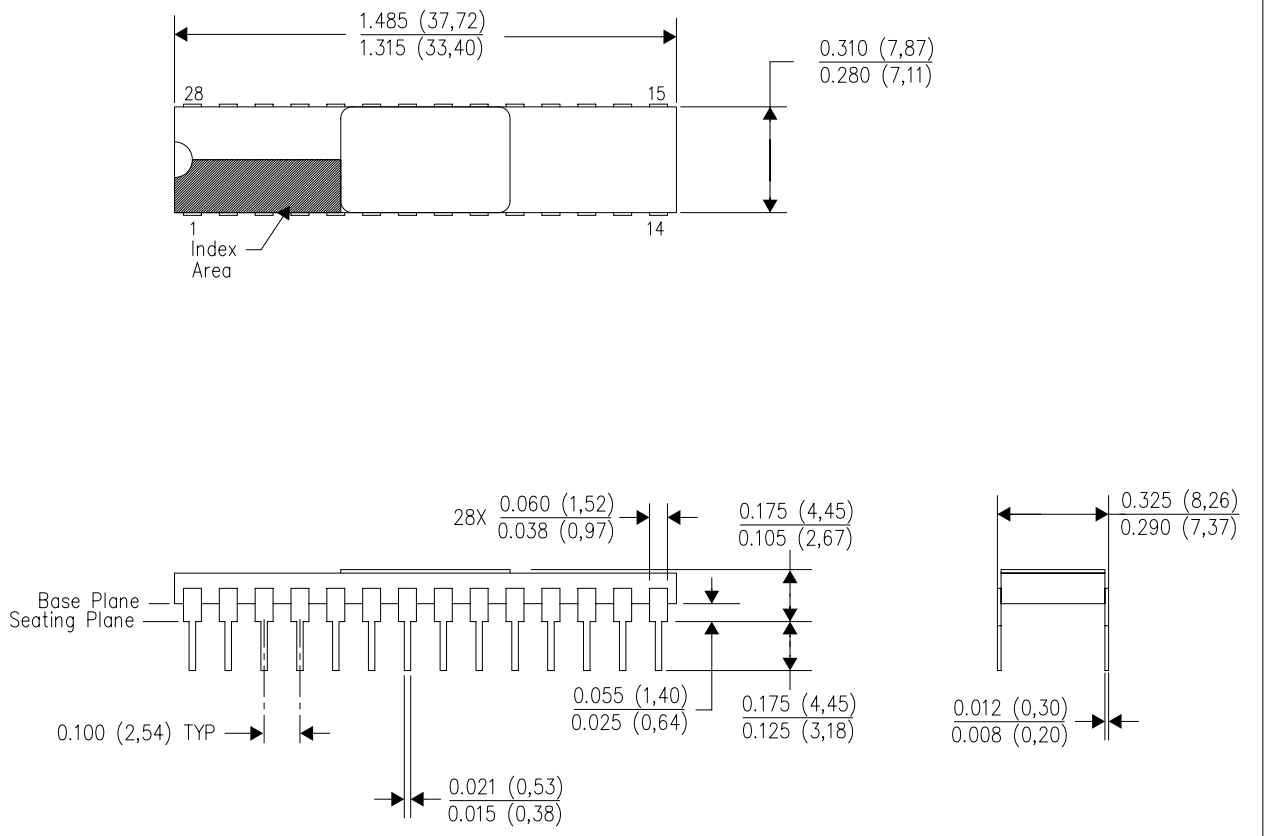
JDJ (R–CDIP–T8) CERAMIC DUAL IN–LINE PACKAGE



4202646–2/B 07/10

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Ceramic quad flatpack with flat leads brazed to non–conductive tie bar carrier.
D. This package is hermetically sealed with a metal lid.
E. The leads are gold plated and can be solderdipped.
F. Leads not shown for clarity purposes.
G. Lid and heat sink are connected to GND leads.

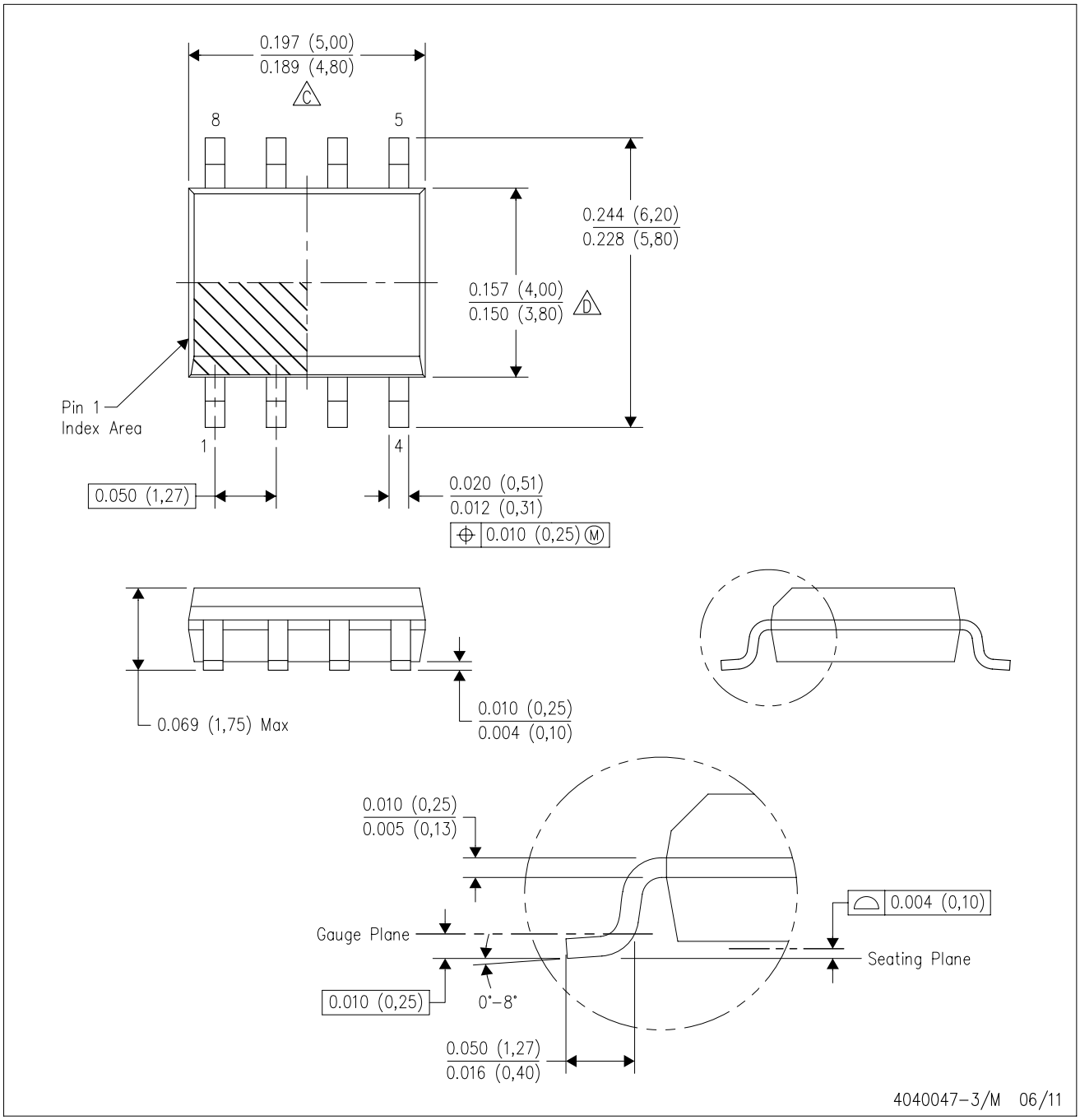
JDJ (R–CDIP–T28) CERAMIC DUAL IN–LINE PACKAGE



4202646–3/B 07/10

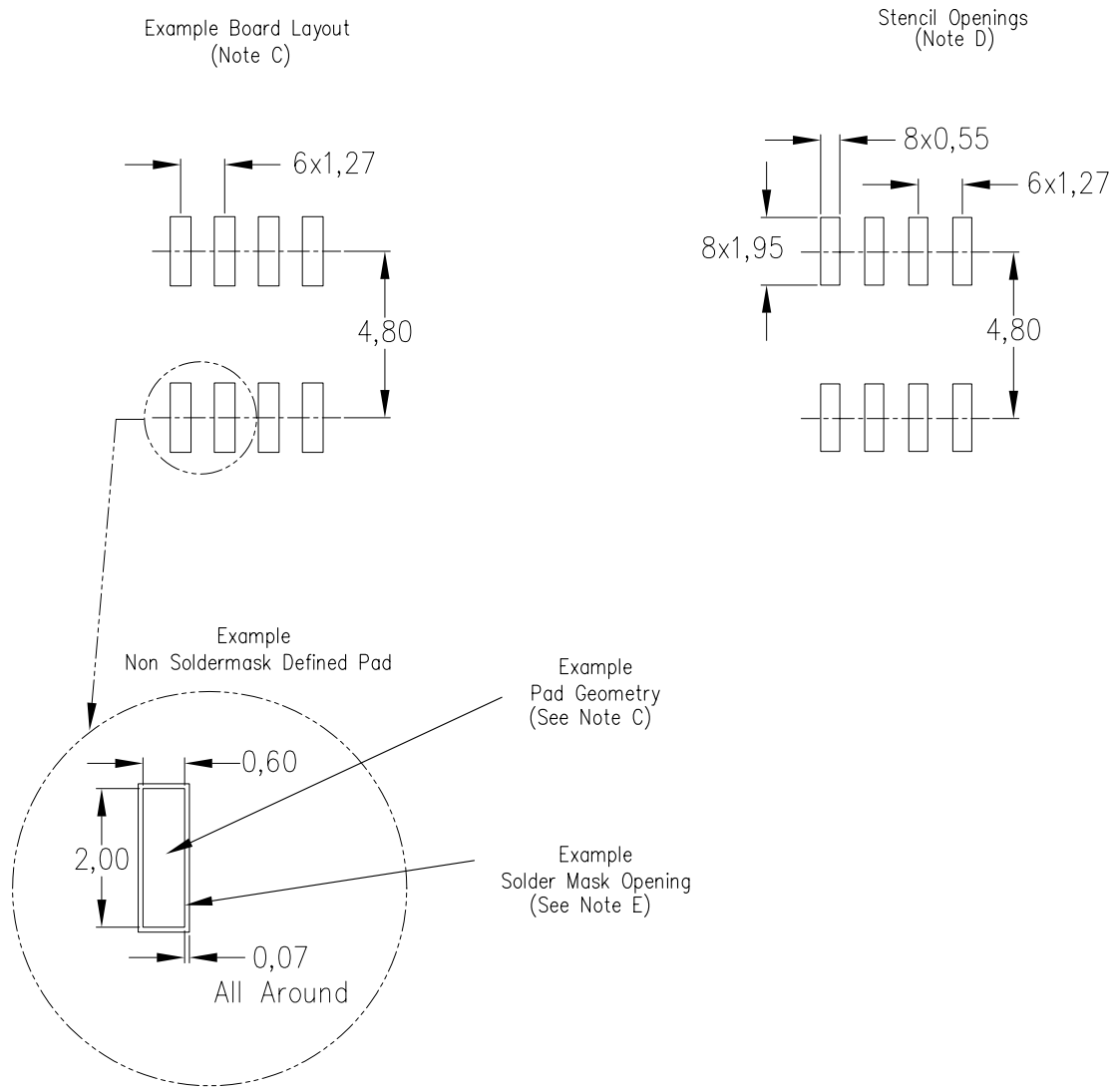
NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Ceramic quad flatpack with flat leads brazed to non–conductive tie bar carrier.
D. This package is hermetically sealed with a metal lid.
E. The leads are gold plated and can be solderdipped.
F. Leads not shown for clarity purposes.
G. Lid and heat sink are connected to GND leads.

D (R–PDSO–G8) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AA.

D (R–PDSO–G8) PLASTIC SMALL OUTLINE



4211283–2/C 02/11

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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