

## 3.3-V FULL-DUPLEX RS-485 DRIVERS AND RECEIVERS

### FEATURES

- **Controlled Baseline**
  - One Assembly Site
  - One Test Site
  - One Fabrication Site
- **Extended Temperature Performance of  $-55^{\circ}\text{C}$  to  $125^{\circ}\text{C}$**
- **Enhanced Diminishing Manufacturing Sources (DMS) Support**
- **Enhanced Product-Change Notification**
- **Qualification Pedigree<sup>(1)</sup>**
- **Available in the Texas Instruments NanoStar™ and NanoFree™ Packages**
- **1/8 Unit-Load Option Available (up to 256 Nodes on the Bus)**
- **Bus-Pin ESD Protection Exceeds 15-kV HBM**
- **Optional Driver Output Transition Times for Signaling Rates<sup>(2)</sup> of 1 Mbps, 5 Mbps, and 25 Mbps**
- **Low-Current Standby Mode:  $<1\ \mu\text{A}$**
- **Glitch-Free Power-Up and Power-Down Protection for Hot-Plugging Applications**
- **5-V-Tolerant Inputs**
- **Bus Idle, Open, and Short-Circuit Fail Safe**
- **Driver Current Limiting and Thermal Shutdown**
- **Meet or Exceed the Requirements of ANSI TIA/EIA-485-A and RS-422 Compatible**

(1) Component qualification in accordance with JEDEC and industry standards to ensure reliable operation over an extended temperature range. This includes, but is not limited to, Highly Accelerated Stress Test (HAST) or biased 85/85, temperature cycle, autoclave or unbiased HAST, electromigration, bond intermetallic life, and mold compound life. Such qualification testing should not be viewed as justifying use of this component beyond specified performance and environmental limits.

(2) The signaling rate of a line is the number of voltage transitions that are made per second expressed in the units bps (bits per second).

### APPLICATIONS

- **Utility Meters**
- **DTE/DCE Interfaces**
- **Industrial, Process, and Building Automation**
- **Point-of-Sale (POS) Terminals and Networks**

### DESCRIPTION

The SN65HVD3x devices are 3-state differential line drivers and differential-input line receivers that operate with 3.3-V power supply.

Each driver and receiver has separate input and output pins for full-duplex bus communication designs. They are designed for balanced transmission lines and interoperation with ANSI TIA/EIA-485A, TIA/EIA-422-B, ITU-T v.11, and ISO 8482:1993 standard-compliant devices.

The SN65HVD30, SN65HVD31, SN65HVD32, SN65HVD36, and SN65HVD37 are fully enabled with no external enabling pins. The SN65HVD36 and SN65HVD37 implement receiver equalization technology for improved performance in long distance applications.

The SN65HVD33, SN65HVD34, SN65HVD35, SN65HVD38, and SN65HVD39 have active-high driver enables and active-low receiver enables. A low (less than  $1\ \mu\text{A}$ ) standby current can be achieved by disabling both the driver and receiver. The SN65HVD38 and SN65HVD39 implement receiver equalization technology for improved performance in long distance applications.

The SN65HVD36 and SN65HVD38 implement receiver equalization technology for improved jitter performance on differential bus applications with data rates up to 20 Mbps at cable lengths up to 160 meters.

The SN65HVD37 and SN65HVD39 implement receiver equalization technology for improved jitter performance on differential bus applications with data rates in the range of 1 Mbps to 5 Mbps at cable lengths up to 1000 meters.

All devices are characterized for operation from  $-55^{\circ}\text{C}$  to  $125^{\circ}\text{C}$ .



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

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**IMPROVED REPLACEMENT FOR:**

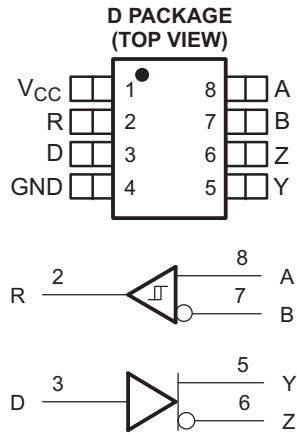
Part Number	Replace With	
xxx3491 xxx3490	SN65HVD33: SN65HVD30:	Better ESD protection (15 kV vs 2 kV or not specified), higher signaling rate (25 Mbps vs 20 Mbps), fractional unit load (64 nodes vs 32)
MAX3491E MAX3490E	SN65HVD33: SN65HVD30:	Higher signaling rate (25 Mbps vs 12 Mbps), fractional unit load (64 nodes vs 32)
MAX3076E MAX3077E	SN65HVD33: SN65HVD30:	Higher signaling rate (25 Mbps vs 16 Mbps), lower standby current (1 $\mu$ A vs 10 $\mu$ A)
MAX3073E MAX3074E	SN65HVD34: SN65HVD31:	Higher signaling rate (5 Mbps vs 500 kbps), lower standby current (1 $\mu$ A vs 10 $\mu$ A)
MAX3070E MAX3071E	SN65HVD35: SN65HVD32:	Higher signaling rate (1 Mbps vs 250 kbps), lower standby current (1 $\mu$ A vs 10 $\mu$ A)

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

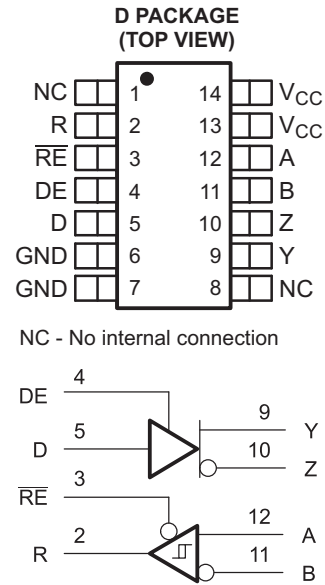


ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

**SN65HVD30, SN65HVD31, SN65HVD32, SN65HVD36,  
SN65HVD37**



**SN65HVD33, SN65HVD34, SN65HVD35, SN65HVD38,  
SN65HVD39**



**AVAILABLE OPTIONS<sup>(1)</sup>**

BASE PART NUMBER	SIGNALING RATE	UNIT LOADS	RECEIVER EQUALIZATION	ENABLES	SOIC MARKING
SN65HVD30MDREP	25 Mbps		No	No	HVD30EP
SN65HVD31MDREP <sup>(2)</sup>	5 Mbps	1/8	No	No	PREVIEW
SN65HVD32MDREP <sup>(2)</sup>	1 Mbps	1/8	No	No	PREVIEW
SN65HVD33MDREP	25 Mbps		No	Yes	HVD33EP
SN65HVD34MDREP <sup>(2)</sup>	5 Mbps	1/8	No	Yes	PREVIEW
SN65HVD35MDREP <sup>(2)</sup>	1 Mbps	1/8	No	Yes	PREVIEW
SN65HVD36MDREP <sup>(2)</sup>	25 Mbps		Yes	No	PREVIEW
SN65HVD37MDREP <sup>(2)</sup>	5 Mbps	1/8	Yes	No	PREVIEW
SN65HVD38MDREP <sup>(2)</sup>	25 Mbps		Yes	Yes	PREVIEW
SN65HVD39MDREP <sup>(2)</sup>	5 Mbps	1/8	Yes	Yes	PREVIEW

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI Web site at [www.ti.com](http://www.ti.com).

(2) Product Preview

**Absolute Maximum Ratings<sup>(1)(2)</sup>**

over operating free-air temperature range (unless otherwise noted)

		UNIT
$V_{CC}$	Supply voltage range	–0.3 V to 6 V
$V_{(A)}, V_{(B)}, V_{(Y)}, V_{(Z)}$	Voltage range at any bus terminal (A, B, Y, Z)	–9 V to 14 V
$V_{(TRANS)}$	Voltage input, transient pulse through 100 $\Omega$ (see <a href="#">Figure 12</a> ) (A, B, Y, Z) <sup>(3)</sup>	–50 V to 50 V
$V_I$	Input voltage range (D, DE, $\overline{RE}$ )	–0.5 V to 7 V
$P_{D(cont)}$	Continuous total power dissipation	Internally limited <sup>(4)</sup>
$I_O$	Output current (receiver output only, R)	11 mA
$T_J$	Junction temperature	165°C
$T_{STG}$	Storage temperature range	–65°C to 150°C

(1) Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under recommended operating conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) All voltage values, except differential I/O bus voltages, are with respect to network ground terminal.

(3) This tests survivability only and the output state of the receiver is not specified.

(4) The thermal shutdown protection circuit internally limits the continuous total power dissipation. Thermal shutdown typically occurs when the junction temperature reaches 165°C.

## Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V <sub>CC</sub>	Supply voltage	3		3.6	V
V <sub>I</sub> or V <sub>IC</sub>	Voltage at any bus terminal (separately or common mode)	-7 <sup>(1)</sup>		12	V
1/t <sub>UI</sub>	Signaling rate	'HVD30, 'HVD33, 'HVD36, 'HVD38		25	Mbps
		'HVD31, 'HVD34, 'HVD37, 'HVD39		5	
		'HVD32, 'HVD35		1	
R <sub>L</sub>	Differential load resistance	54	60		Ω
V <sub>IH</sub>	High-level input voltage	D, DE, RE		V <sub>CC</sub>	V
V <sub>IL</sub>	Low-level input voltage	D, DE, RE		0.8	V
V <sub>ID</sub>	Differential input voltage	-12		12	V
I <sub>OH</sub>	High-level output current	Driver	-60		mA
		Receiver	-8		
I <sub>OL</sub>	Low-level output current	Driver	60		mA
		Receiver	8		
T <sub>A</sub>	Ambient still-air temperature	-55		125 <sup>(2)</sup>	°C

- (1) The algebraic convention, in which the least positive (most negative) limit is designated as minimum, is used in this data sheet.  
 (2) Long-term high-temperature storage and/or extended use at maximum recommended operating conditions may result in a reduction of overall device life. See [http://www.ti.com/ep\\_quality](http://www.ti.com/ep_quality) for additional information on enhanced plastic packaging.

## Electrostatic Discharge Protection

PARAMETER	TEST CONDITIONS	TYP <sup>(1)</sup>	UNIT
Human-Body Model	Bus terminals and GND	±16	kV
Human-Body Model <sup>(2)</sup>	All pins	±4	
Charged-Device Model <sup>(3)</sup>	All pins	±1	

- (1) All typical values at 25°C with 3.3-V supply  
 (2) Tested in accordance with JEDEC Standard 22, Test Method A114-A  
 (3) Tested in accordance with JEDEC Standard 22, Test Method C101

## Driver Electrical Characteristics

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP <sup>(1)</sup>	MAX	UNIT
$V_{I(K)}$	Input clamp voltage	$I_I = -18$ mA	-1.5			V
$ V_{OD(SS)} $	Steady-state differential output voltage	$I_O = 0$	2.3		$V_{CC} + 0.1$	V
		$R_L = 54$ $\Omega$ , See <a href="#">Figure 1</a> (RS-485)	1.5	2		
		$R_L = 100$ $\Omega$ , See <a href="#">Figure 1</a> (RS-422)	2	2.3		
		$V_{test} = -7$ V to 12 V, See <a href="#">Figure 2</a>	1.5			
$\Delta V_{OD(SS)} $	Change in magnitude of steady-state differential output voltage between states	$R_L = 54$ $\Omega$ , See <a href="#">Figure 1</a> and <a href="#">Figure 2</a>	-0.2		0.2	V
$V_{OD(RING)}$	Differential output voltage overshoot and undershoot	$R_L = 54$ $\Omega$ , $C_L = 50$ pF, See <a href="#">Figure 5</a> and <a href="#">Figure 3</a>			10% <sup>(2)</sup>	V
$V_{OC(PP)}$	Peak-to-peak common-mode output voltage	'HVD30, 'HVD33, 'HVD36, 'HVD38		0.5		V
		'HVD31, 'HVD34, 'HVD37, 'HVD39, 'HVD32, 'HVD35	See <a href="#">Figure 4</a>	0.25		
$V_{OC(SS)}$	Steady-state common-mode output voltage	See <a href="#">Figure 4</a>	1.6		2.3	V
$\Delta V_{OC(SS)}$	Change in steady-state common-mode output voltage	See <a href="#">Figure 4</a>	-0.05		0.05	V
$I_{Z(Z)}$ or $I_{Y(Z)}$	High-impedance state output current	'HVD30, 'HVD31, 'HVD32, 'HVD36, 'HVD37	$V_{CC} = 0$ V, $V_Z$ or $V_Y = 12$ V, Other input at 0 V		90	$\mu$ A
			$V_{CC} = 0$ V, $V_Z$ or $V_Y = -7$ V, Other input at 0 V	-10		
		'HVD33, 'HVD34, 'HVD35, 'HVD38, 'HVD39	$V_{CC} = 3$ V or 0 V, DE = 0 V, $V_Z$ or $V_Y = 12$ V		90	
			$V_{CC} = 3$ V or 0 V, DE = 0 V, $V_Z$ or $V_Y = -7$ V	Other input at 0 V	-10	
$I_{Z(S)}$ or $I_{Y(S)}$	Short-circuit output current	$V_Z$ or $V_Y = -7$ V				mA
		$V_Z$ or $V_Y = 12$ V		$\pm 250$		
$I_I$	Input current	D, DE	0		100	$\mu$ A
$C_{(OD)}$	Differential output capacitance	$V_{OD} = 0.4 \sin(4E6\pi t) + 0.5$ V, DE at 0 V		16		pF

(1) All typical values at 25°C with 3.3-V supply

(2) 10% of the peak-to-peak differential output voltage swing, per TIA/EIA-485

## Driver Switching Characteristics

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP <sup>(1)</sup>	MAX	UNIT
$t_{PLH}$	Propagation delay time, low- to high-level output	'HVD30, 'HVD33, 'HVD36, 'HVD38	4	10	23	ns
		'HVD31, 'HVD34, 'HVD37, 'HVD39	25	38	65	
		'HVD32, 'HVD35	120	175	305	
$t_{PHL}$	Propagation delay time, high- to low-level output	'HVD30, 'HVD33, 'HVD36, 'HVD38	4	9	23	ns
		'HVD31, 'HVD34, 'HVD37, 'HVD39	25	38	65	
		'HVD32, 'HVD35	120	175	305	
$t_r$	Differential output signal rise time	'HVD30, 'HVD33, 'HVD36, 'HVD38	2.5	5	18	ns
		'HVD31, 'HVD34, 'HVD37, 'HVD39	20	37	60	
		'HVD32, 'HVD35	120	185	300	
$t_f$	Differential output signal fall time	'HVD30, 'HVD33, 'HVD36, 'HVD38	2.5	5	18	ns
		'HVD31, 'HVD34, 'HVD37, 'HVD39	20	35	60	
		'HVD32, 'HVD35	120	180	300	
$t_{sk(p)}$	Pulse skew ( $t_{PHL} - t_{PLH}$ )	'HVD30, 'HVD33, 'HVD36, 'HVD38		0.6		ns
		'HVD31, 'HVD34, 'HVD37, 'HVD39		2.0		
		'HVD32, 'HVD35		5.1		
$t_{PZH1}$	Propagation delay time, high-impedance to high-level output	'HVD33, 'HVD38			45	ns
		'HVD34, 'HVD39			235	
		'HVD35			490	
$t_{PHZ}$	Propagation delay time, high-level to high-impedance output	'HVD33, 'HVD38			25	ns
		'HVD34, 'HVD39			65	
		'HVD35			165	
$t_{PZL1}$	Propagation delay time, high-impedance to low-level output	'HVD33, 'HVD38			35	ns
		'HVD34, 'HVD39			190	
		'HVD35			490	
$t_{PLZ}$	Propagation delay time, low-level to high-impedance output	'HVD33, 'HVD38			30	ns
		'HVD34, 'HVD39			120	
		'HVD35			290	
$t_{PZH2}$	Propagation delay time, standby to high-level output	'HVD30			4000	ns
		'HVD33			5000	
$t_{PZL2}$	Propagation delay time, standby to low-level output	'HVD30			4000	ns
		'HVD33			5000	

(1) All typical values at 25°C with 3.3-V supply

## Receiver Electrical Characteristics

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP <sup>(1)</sup>	MAX	UNIT	
$V_{IT+}$	Positive-going differential input threshold voltage	$I_O = -8$ mA			-0.02	V	
$V_{IT-}$	Negative-going differential input threshold voltage	'HVD30		-0.15		V	
		'HVD33	$I_O = 8$ mA	-0.2			
$V_{hys}$	Hysteresis voltage ( $V_{IT+} - V_{IT-}$ )			50		mV	
$V_{IK}$	Enable-input clamp voltage	$I_I = -18$ mA	-1.5			V	
$V_O$	Output voltage	$V_{ID} = 200$ mV, $I_O = -8$ mA, See <a href="#">Figure 8</a>	2.4			V	
		$V_{ID} = -200$ mV, $I_O = 8$ mA, See <a href="#">Figure 8</a>			0.4		
$I_{O(Z)}$	High-impedance-state output current	$V_O = 0$ or $V_{CC}$ , $\overline{RE}$ at $V_{CC}$	-1		1	$\mu$ A	
$I_A$ or $I_B$	Bus input current	'HVD31, 'HVD32, 'HVD34, 'HVD35, 'HVD37, 'HVD39	$V_A$ or $V_B = 12$ V	Other input at 0 V	0.05	0.1	mA
			$V_A$ or $V_B = 12$ V, $V_{CC} = 0$ V		0.06	0.1	
			$V_A$ or $V_B = -7$ V		-0.10	-0.04	
			$V_A$ or $V_B = -7$ V, $V_{CC} = 0$ V		-0.10	-0.03	
	'HVD30, 'HVD33, 'HVD36, 'HVD38	$V_A$ or $V_B = 12$ V	Other input at 0 V	0.20	0.35		
		$V_A$ or $V_B = 12$ V, $V_{CC} = 0$ V		0.24	0.4		
		$V_A$ or $V_B = -7$ V		-0.35	-0.18		
		$V_A$ or $V_B = -7$ V, $V_{CC} = 0$ V		-0.25	-0.13		
$I_{IH}$	Input current, $\overline{RE}$	$V_{IH} = 0.8$ V or 2 V	-60			$\mu$ A	
$C_{ID}$	Differential input capacitance	$V_{ID} = 0.4 \sin(4E6\pi t) + 0.5$ V, DE at 0 V		15		pF	
<b>Supply Current</b>							
$I_{CC}$	Supply current	'HVD30	D at 0 V or $V_{CC}$ and no load		2.1	mA	
		'HVD31, 'HVD32		6.4			
		'HVD36, 'HVD37		7.9			
		'HVD33		$\overline{RE}$ at 0 V, D at 0 V or $V_{CC}$ , DE at 0 V, No load (receiver enabled and driver disabled)	1.8		
		'HVD34, 'HVD35		2.2			
		'HVD38, 'HVD39		3.8			
		'HVD33, 'HVD34, 'HVD35, 'HVD38, 'HVD39	$\overline{RE}$ at $V_{CC}$ , D at $V_{CC}$ , DE at 0 V, No load (receiver disabled and driver disabled)	0.022	1.5	$\mu$ A	
		'HVD33	$\overline{RE}$ at 0 V, D at 0 V or $V_{CC}$ , DE at $V_{CC}$ , No load (receiver enabled and driver enabled)		2.1	mA	
		'HVD34, 'HVD35		6.5			
		'HVD38		3.5			
		'HVD39		8			
		'HVD33	$\overline{RE}$ at $V_{CC}$ , D at 0 V or $V_{CC}$ , DE at $V_{CC}$ No load (receiver disabled and driver enabled)		1.8	mA	
		'HVD34, 'HVD35		6.2			
		'HVD38		2.5			
'HVD39	7						

(1) All typical values at 25°C with 3.3-V supply

## Receiver Switching Characteristics

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP <sup>(1)</sup>	MAX	UNIT	
t <sub>PLH</sub>	Propagation delay time, low- to high-level output	'HVD30, 'HVD33, 'HVD36, 'HVD38		26	60	ns	
		'HVD31, 'HVD32, 'HVD34, 'HVD35, 'HVD37, 'HVD39		47	70		
t <sub>PHL</sub>	Propagation delay time, high- to low-level output	'HVD30, 'HVD33, 'HVD36, 'HVD38		29	60	ns	
		'HVD31, 'HVD32, 'HVD34, 'HVD35, 'HVD37, 'HVD39		49	70		
t <sub>sk(p)</sub>	Pulse skew ( t <sub>PHL</sub> - t <sub>PLH</sub>  )	'HVD30, 'HVD33, 'HVD36, 'HVD37, 'HVD38, 'HVD39	V <sub>ID</sub> = -1.5 V to 1.5 V, C <sub>L</sub> = 15 pF, See <a href="#">Figure 9</a>		12	ns	
		'HVD31, 'HVD34, 'HVD32, 'HVD35			10		
t <sub>r</sub>	Output signal rise time	'HVD30			10	ns	
		'HVD33			18		
t <sub>f</sub>	Output signal fall time				12.5	ns	
t <sub>PHZ</sub>	Output disable time from high level	DE at 3 V			20	ns	
t <sub>PZH1</sub>	Output enable time to high level				20	ns	
t <sub>PZH2</sub>	Propagation delay time, standby to high-level output	'HVD30		DE at 0 V	C <sub>L</sub> = 15 pF, See <a href="#">Figure 10</a>	4000	ns
		'HVD33				5000	
t <sub>PLZ</sub>	Output disable time from low level	DE at 3 V			20	ns	
t <sub>PZL1</sub>	Output enable time to low level			20	ns		
t <sub>PZL2</sub>	Propagation delay time, standby to low-level output	'HVD30	DE at 0 V	C <sub>L</sub> = 15 pF, See <a href="#">Figure 11</a>	4000	ns	
		'HVD33			5000		

(1) All typical values 25°C with 3.3-V supply



## Receiver Equalization Characteristics

over recommended operating conditions (unless otherwise noted)

PARAMETER	TEST CONDITIONS		DEVICE	MIN	TYP <sup>(1)</sup>	MAX	UNIT
$t_{j(pp)}$ Peak-to-peak eye-pattern jitter	Pseudo-random NRZ code with a bit pattern length of $2^{16} - 1$ , Belden 3105A cable	25 Mbps	0 m	'HVD36, 'HVD38	PREVIEW		ns
			100 m	'HVD33 <sup>(2)</sup>	PREVIEW		
				'HVD36, 'HVD38	PREVIEW		
			150 m	'HVD33 <sup>(2)</sup>	PREVIEW		
				'HVD36, 'HVD38	PREVIEW		
			200 m	'HVD33 <sup>(2)</sup>	PREVIEW		
		'HVD36, 'HVD38		PREVIEW			
		10 Mbps	200 m	'HVD33 <sup>(2)</sup>	PREVIEW		
				'HVD36, 'HVD38	PREVIEW		
			250 m	'HVD33 <sup>(2)</sup>	PREVIEW		
				'HVD36, 'HVD38	PREVIEW		
			300 m	'HVD33 <sup>(2)</sup>	PREVIEW		
				'HVD36, 'HVD38	PREVIEW		
		5 Mbps	500 m	'HVD34 <sup>(2)</sup>	PREVIEW		
				'HVD37, 'HVD39	PREVIEW		
		3 Mbps	500 m	'HVD33 <sup>(2)</sup>	PREVIEW		
				'HVD34 <sup>(2)</sup>	PREVIEW		
				'HVD36, 'HVD38	PREVIEW		
				'HVD37, 'HVD39	PREVIEW		
		1 Mbps	1000 m	'HVD34 <sup>(2)</sup>	PREVIEW		
'HVD37, 'HVD39	PREVIEW						

(1) All typical values are at  $V_{CC} = 5\text{ V}$  and temperature =  $25^\circ\text{C}$ .

(2) The SN65HVD33 and the SN65HVD34 do not have receiver equalization, but are specified for comparison.

## Device Power Dissipation – $P_D$

DEVICE	TEST CONDITIONS	MIN	MAX	UNIT
'HVD30, 'HVD36 (25 Mbps)	$R_L = 60\ \Omega$ , $C_L = 50\ \text{pF}$ , Input to D a 50% duty cycle square wave at indicated signaling rate, $T_A = 85^\circ\text{C}$	197		mW
'HVD31, 'HVD37 (5 Mbps)		213		
'HVD32 (1 Mbps)		193		
'HVD33, 'HVD38 (25 Mbps)	$R_L = 60\ \Omega$ , $C_L = 50\ \text{pF}$ , DE at $V_{CC}$ , $\overline{RE}$ at 0 V, Input to D a 50% duty cycle square wave at indicated signaling rate, $T_A = 85^\circ\text{C}$	197		mW
'HVD34, 'HVD39 (5 Mbps)		193		
'HVD35 (1 Mbps)		248		

PARAMETER MEASUREMENT INFORMATION

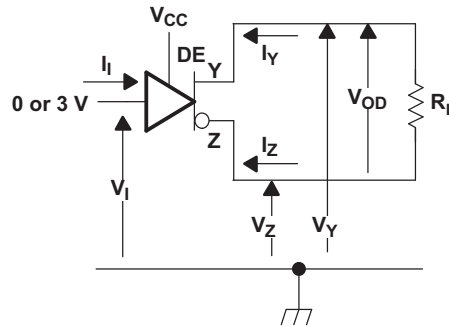


Figure 1. Driver  $V_{OD}$  Test Circuit and Voltage and Current Definitions

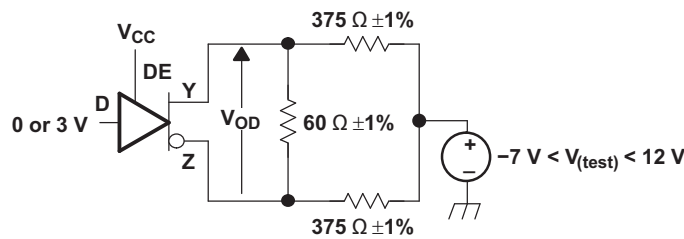


Figure 2. Driver  $V_{OD}$  With Common-Mode Loading Test Circuit

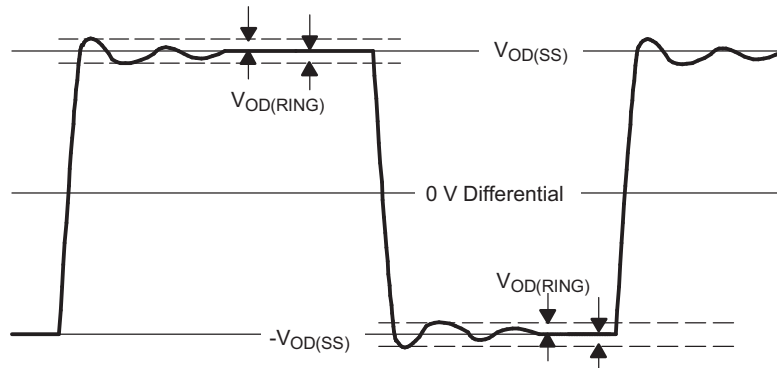
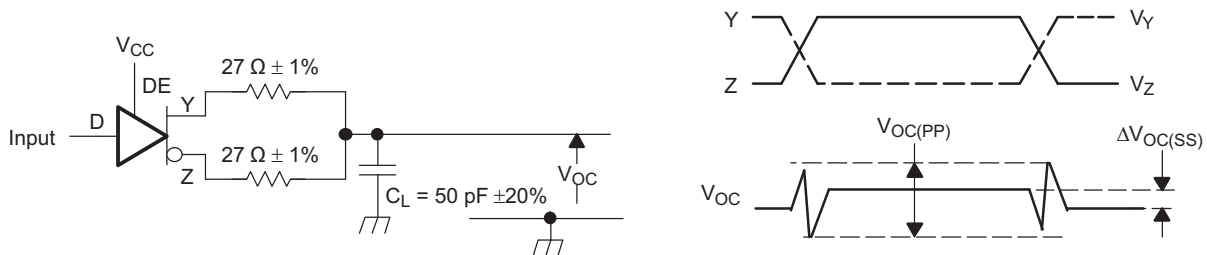


Figure 3.  $V_{OD(RING)}$  Waveform and Definitions

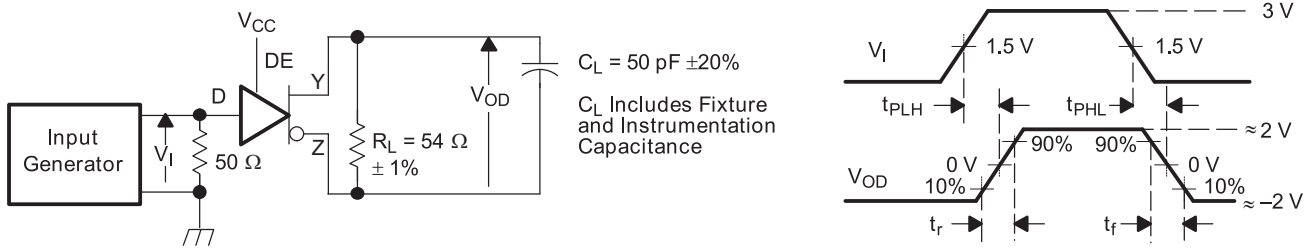
$V_{OD(RING)}$  is measured at four points on the output waveform, corresponding to overshoot and undershoot from the  $V_{OD(H)}$  and  $V_{OD(L)}$  steady state values.



Input: PRR = 500 kHz, 50% Duty Cycle,  $t_r < 6$  ns,  $t_f < 6$  ns,  $Z_o = 50 \Omega$

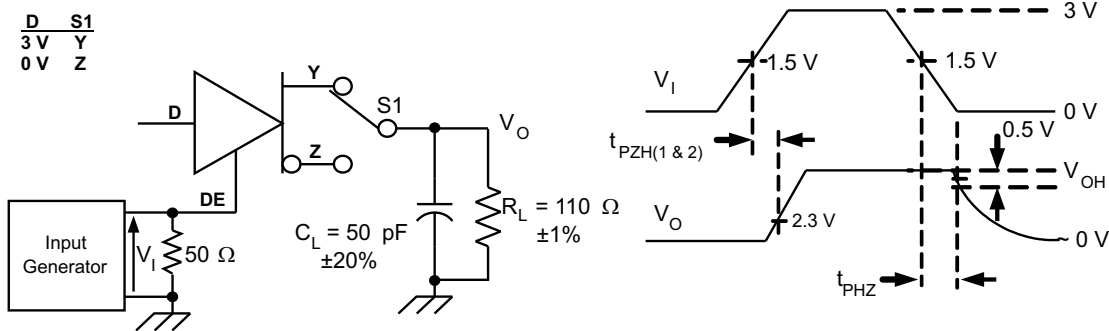
Figure 4. Test Circuit and Definitions for Driver Common-Mode Output Voltage

**PARAMETER MEASUREMENT INFORMATION (continued)**



A. Generator: PRR = 500 kHz, 50% Duty Cycle,  $t_r < 6$  ns,  $t_f < 6$  ns,  $Z_O = 50 \Omega$

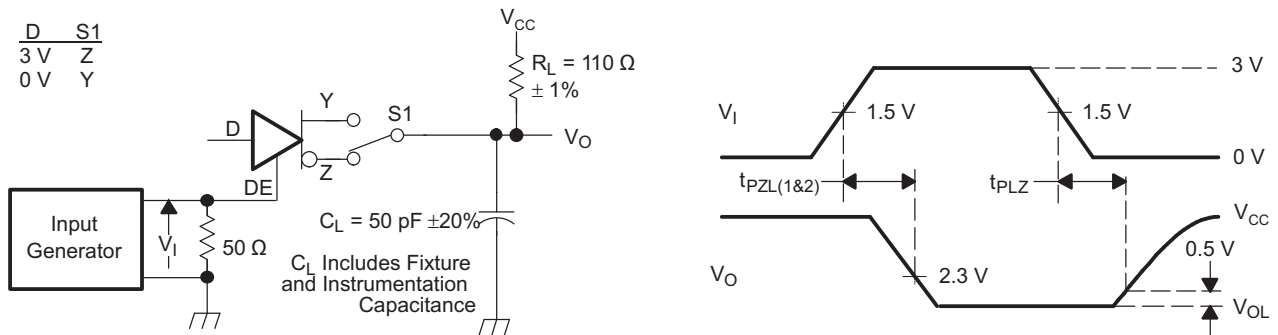
**Figure 5. Driver Switching Test Circuit and Voltage Waveforms**



A. Generator: PRR = 500 kHz, 50% Duty Cycle,  $t_r < 6$  ns,  $t_f < 6$  ns,  $Z_O = 50 \Omega$

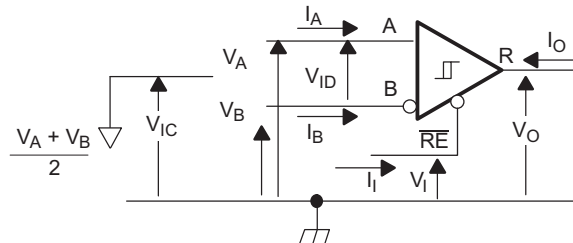
B.  $C_L$  Includes Fixture and Instrumentation Capacitance

**Figure 6. Driver High-Level Output Enable and Disable Time Test Circuit and Voltage Waveforms**



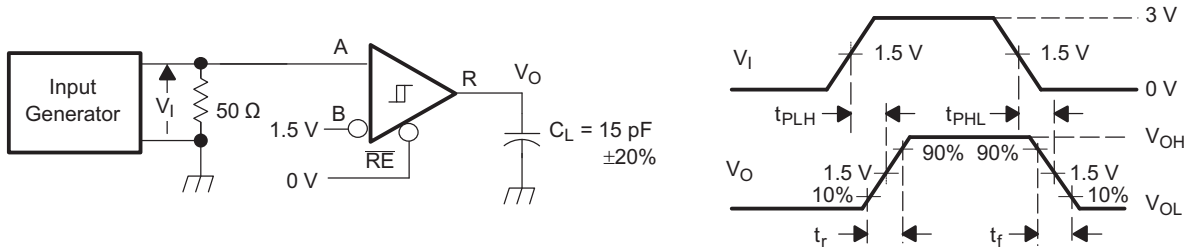
A. Generator: PRR = 500 kHz, 50% Duty Cycle,  $t_r < 6$  ns,  $t_f < 6$  ns,  $Z_O = 50 \Omega$

**Figure 7. Driver Low-Level Output Enable and Disable Time Test Circuit and Voltage Waveforms**



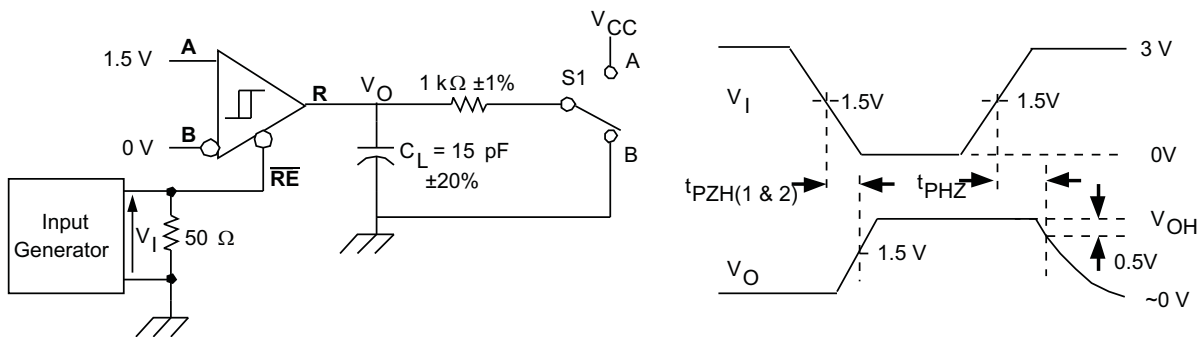
**Figure 8. Receiver Voltage and Current Definitions**

**PARAMETER MEASUREMENT INFORMATION (continued)**



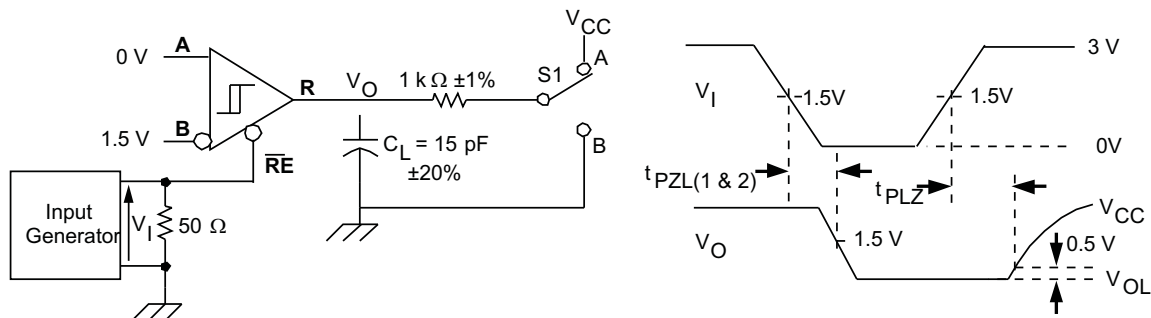
- A.  $C_L$  Includes Fixture and Instrumentation Capacitance
- B. Generator: PRR = 500 kHz, 50% Duty Cycle,  $t_r < 6$  ns,  $t_f < 6$  ns,  $Z_O = 50 \Omega$

**Figure 9. Receiver Switching Test Circuit and Voltage Waveforms**



- A. Generator: PRR = 500 kHz, 50% Duty Cycle,  $t_r < 6$  ns,  $t_f < 6$  ns,  $Z_O = 50 \Omega$

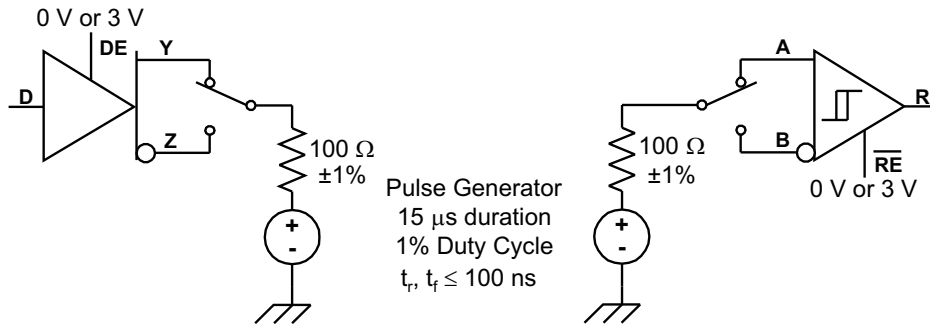
**Figure 10. Receiver High-Level Enable and Disable Time Test Circuit and Voltage Waveforms**



- A. Generator: PRR = 500 kHz, 50% Duty Cycle,  $t_r < 6$  ns,  $t_f < 6$  ns,  $Z_O = 50 \Omega$

**Figure 11. Receiver Enable Time From Standby (Driver Disabled)**

**PARAMETER MEASUREMENT INFORMATION (continued)**

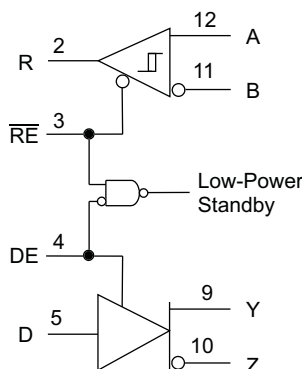


**Figure 12. Test Circuit, Transient Over Voltage Test**

## DEVICE INFORMATION

### Low-Power Standby Mode

When both the driver and receiver are disabled (DE low and  $\overline{RE}$  high), the device is in standby mode. If the enable inputs are in this state for less than 60 ns, the device does not enter standby mode. This guards against inadvertently entering standby mode during driver/receiver enabling. Only when the enable inputs are held in this state for 300 ns or more, the device is assured to be in standby mode. In this low-power standby mode, most internal circuitry is powered down, and the supply current is typically less than 1 nA. When either the driver or the receiver is re-enabled, the internal circuitry becomes active.



**Figure 13. Low-Power Standby Logic Diagram**

If only the driver is re-enabled (DE transitions to high), the driver outputs are driven according to the D input after the enable times given by  $t_{PZH2}$  and  $t_{PZL2}$  in the driver switching characteristics. If the D input is open when the driver is enabled, the driver outputs default to A high and B low, in accordance with the driver fail-safe feature.

If only the receiver is re-enabled ( $\overline{RE}$  transitions to low), the receiver output is driven according to the state of the bus inputs (A and B) after the enable times given by  $t_{PZH2}$  and  $t_{PZL2}$  in the receiver switching characteristics. If there is no valid state on the bus, the receiver responds as described in the fail-safe operation section.

If both the receiver and driver are re-enabled simultaneously, the receiver output is driven according to the state of the bus inputs (A and B) and the driver output is driven according to the D input. Note that the state of the active driver affects the inputs to the receiver. Therefore, the receiver outputs are valid as soon as the driver outputs are valid.

**DEVICE INFORMATION (continued)**

**FUNCTION TABLES**

**SN65HVD33, SN65HVD34, SN65HVD35, SN65HVD38, SN65HVD39 DRIVER<sup>(1)</sup>**

INPUTS		OUTPUTS	
D	DE	Y	Z
H	H	H	L
L	H	L	H
X	L or open	Z	Z
Open	H	L	H

(1) H = high level, L = low level, Z = high impedance, X = irrelevant

**Table 1. SN65HVD33, SN65HVD34, SN65HVD35, SN65HVD38, SN65HVD39 RECEIVERSLLS6651132<sup>(1)</sup>**

DIFFERENTIAL INPUTS $V_{ID} = V_{(A)} - V_{(B)}$	ENABLE RE	OUTPUT R
$V_{ID} \leq -0.2$ V	L	L
$-0.2$ V < $V_{ID} < -0.02$ V	L	?
$-0.02$ V $\leq V_{ID}$	L	H
X	H or open	Z
Open circuit	L	H
Idle circuit	L	H
Short circuit, $V_{(A)} = V_{(B)}$	L	H

(1) H = high level, L = low level, Z = high impedance, X = irrelevant, ? = indeterminate

**SN65HVD30, SN65HVD31, SN65HVD32, SN65HVD36, SN65HVD37 DRIVER<sup>(1)</sup>**

INPUT D	OUTPUTS	
	Y	Z
H	H	L
L	L	H
Open	L	H

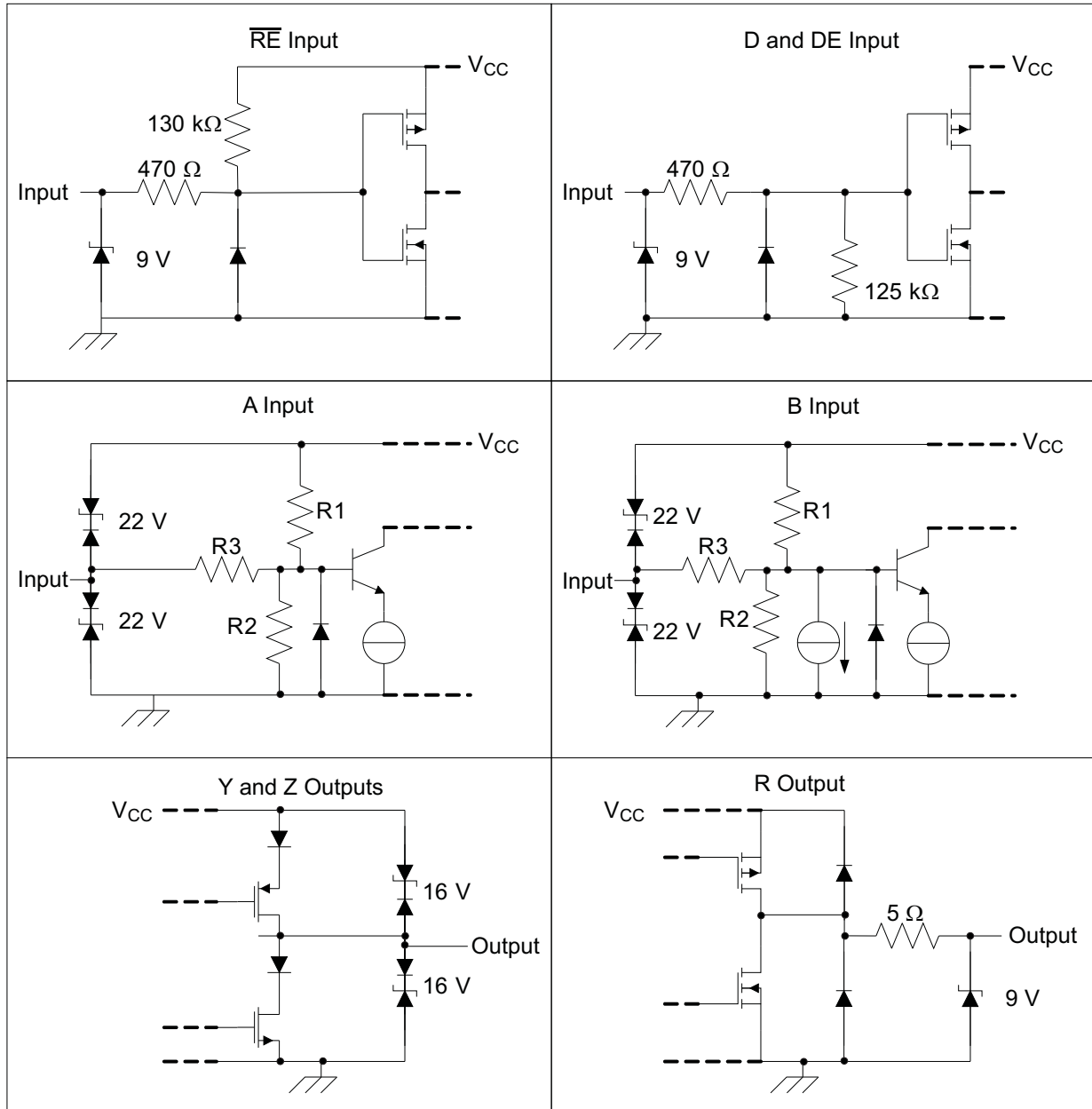
(1) H = high level, L = low level

**SN65HVD30, SN65HVD31, SN65HVD32, SN65HVD36, SN65HVD37 RECEIVER<sup>(1)</sup>**

DIFFERENTIAL INPUTS $V_{ID} = V_{(A)} - V_{(B)}$	OUTPUT R
$V_{ID} \leq -0.15$ V	L
$-0.15$ V < $V_{ID} < -0.02$ V	?
$-0.02$ V $\leq V_{ID}$	H
Open circuit	H
Idle circuit	H
Short circuit, $V_{(A)} = V_{(B)}$	H

(1) H = high level, L = low level, ? = indeterminate

**EQUIVALENT INPUT AND OUTPUT SCHEMATIC DIAGRAMS**



	<b>R1/R2</b>	<b>R3</b>
SN65HVD30, SN65HVD33, SN65HVD36, SN65HVD38	9 kΩ	45 kΩ
SN65HVD31, SN65HVD32, SN65HVD34, SN65HVD35, SN65HVD37, SN65HVD38, SN65HVD39	36 kΩ	180 kΩ



**TYPICAL CHARACTERISTICS**

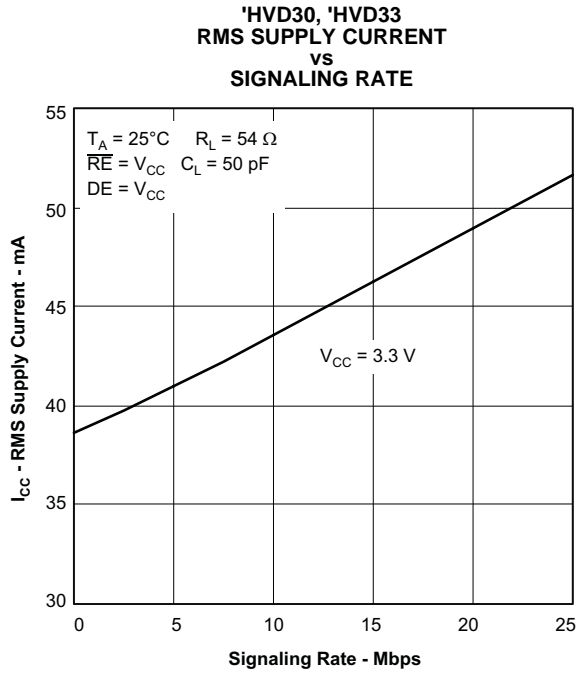


Figure 14.

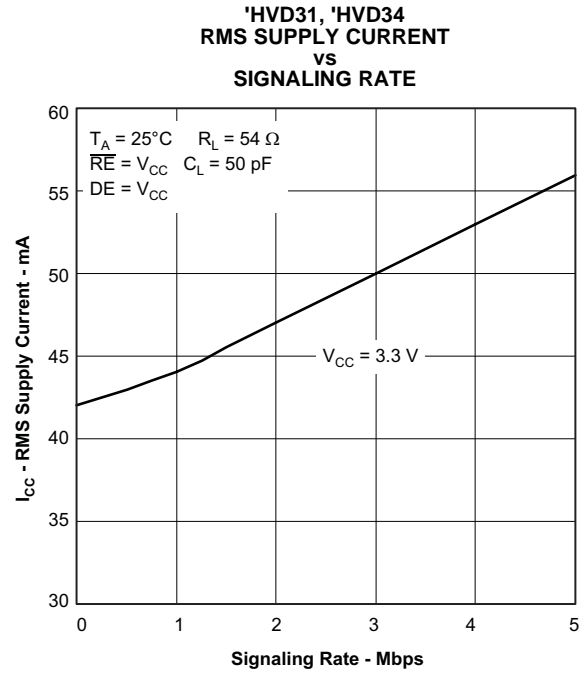


Figure 15.

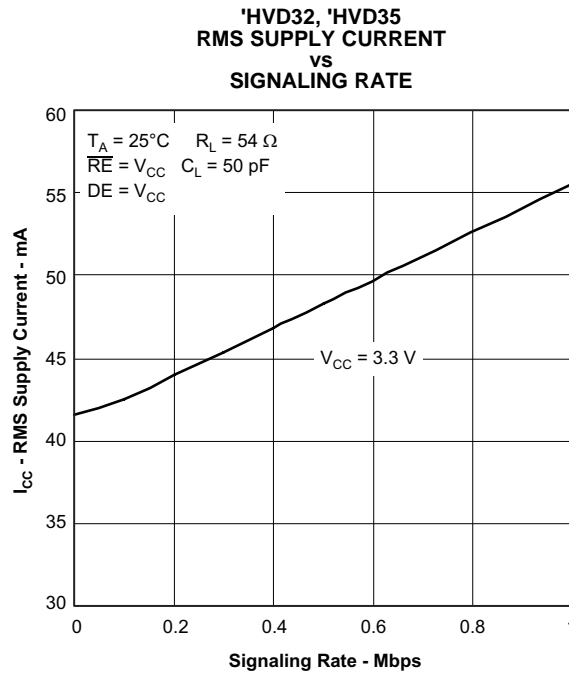


Figure 16.

**TYPICAL CHARACTERISTICS (continued)**

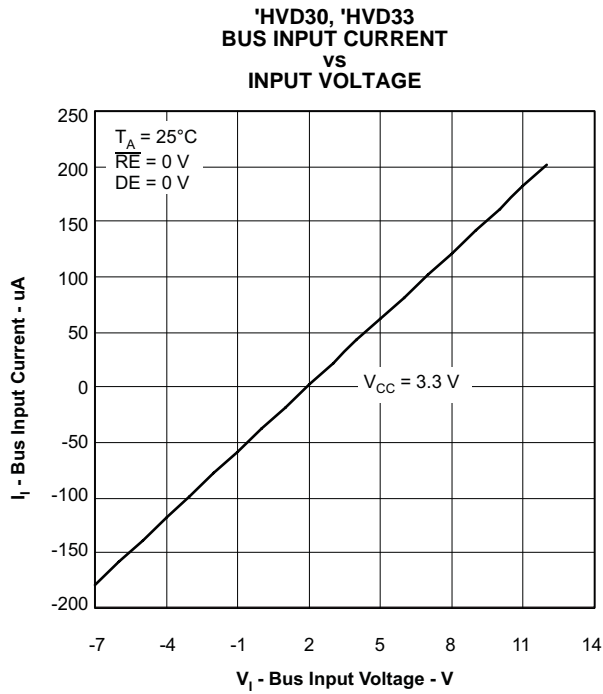


Figure 17.

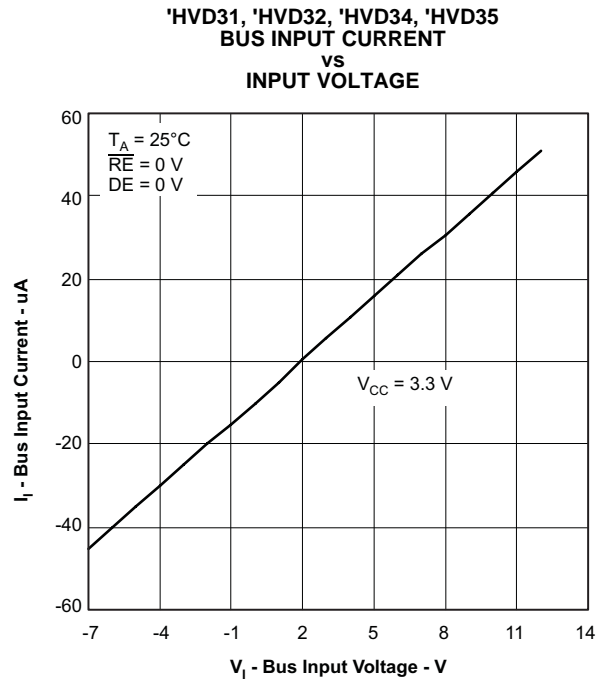


Figure 18.

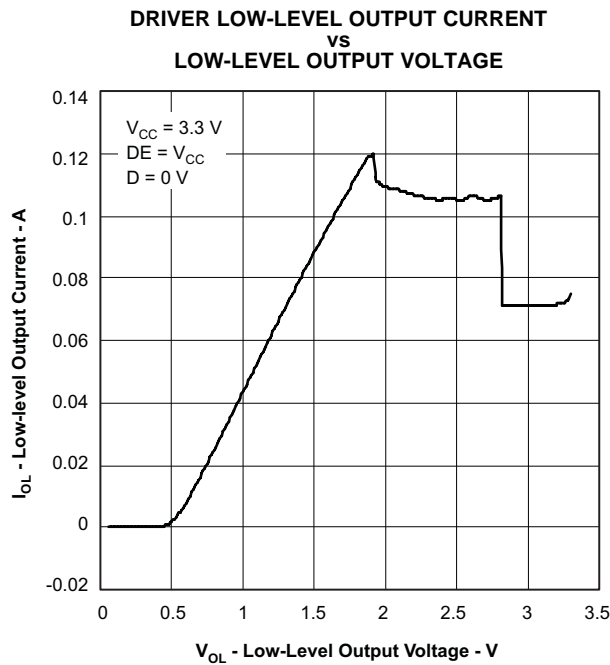


Figure 19.

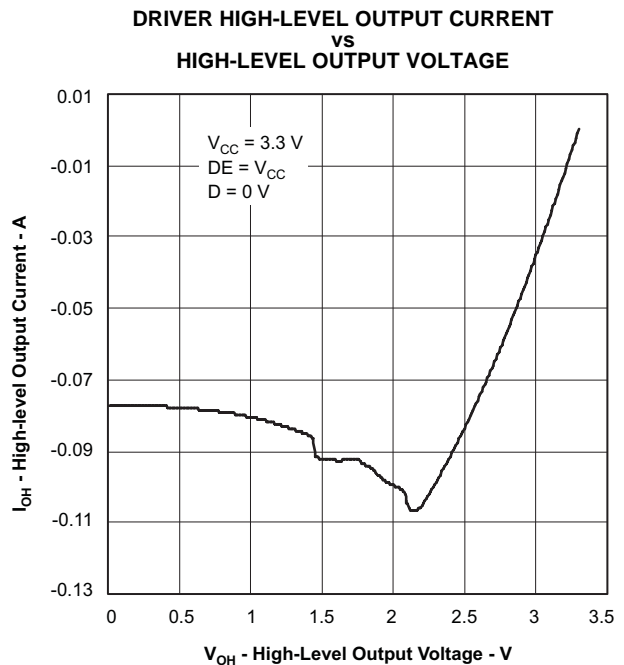
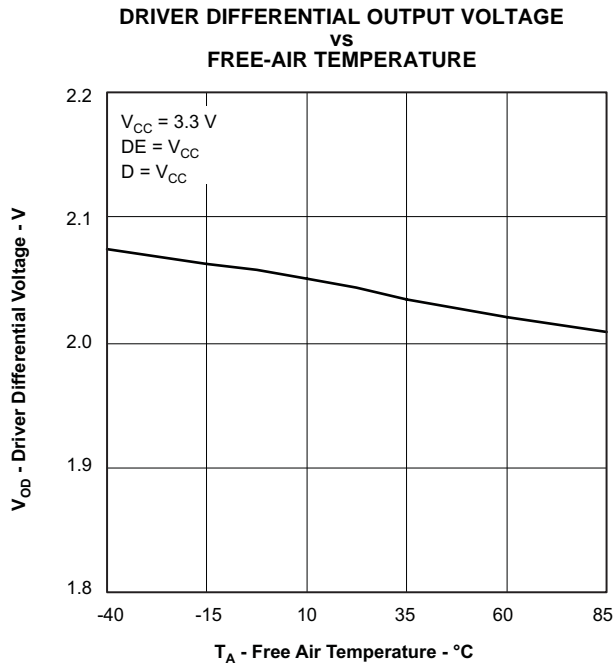
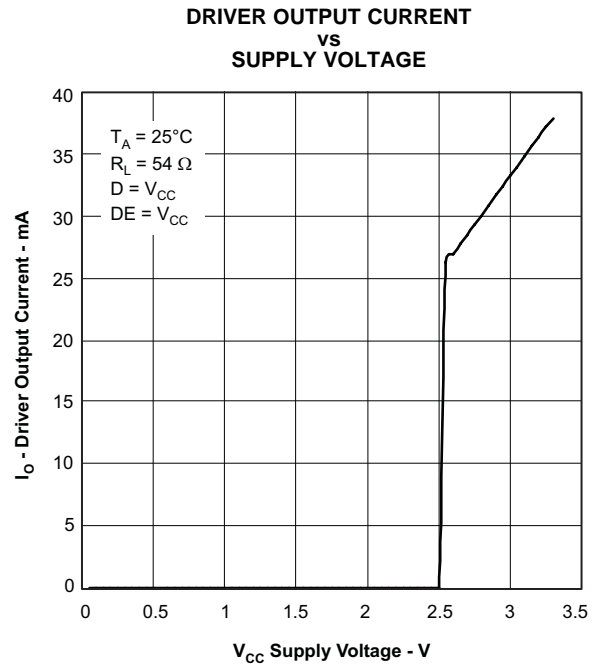


Figure 20.

**TYPICAL CHARACTERISTICS (continued)**



**Figure 21.**



**Figure 22.**

**PACKAGING INFORMATION**

Orderable Device	Status <sup>(1)</sup>	Package Type	Package Drawing	Pins	Package Qty	Eco Plan <sup>(2)</sup>	Lead/Ball Finish	MSL Peak Temp <sup>(3)</sup>
SN65HVD30MDREP	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN65HVD30MDREPG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN65HVD33MDREP	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN65HVD33MDREPG4	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
V62/06634-01XE	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
V62/06634-04YE	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM

<sup>(1)</sup> The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

<sup>(2)</sup> Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

<sup>(3)</sup> MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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**OTHER QUALIFIED VERSIONS OF SN65HVD30-EP, SN65HVD33-EP :**

- Catalog: [SN65HVD30](#), [SN65HVD33](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product

**TAPE AND REEL INFORMATION**



**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN65HVD30MDREP	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
SN65HVD33MDREP	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1

**TAPE AND REEL BOX DIMENSIONS**



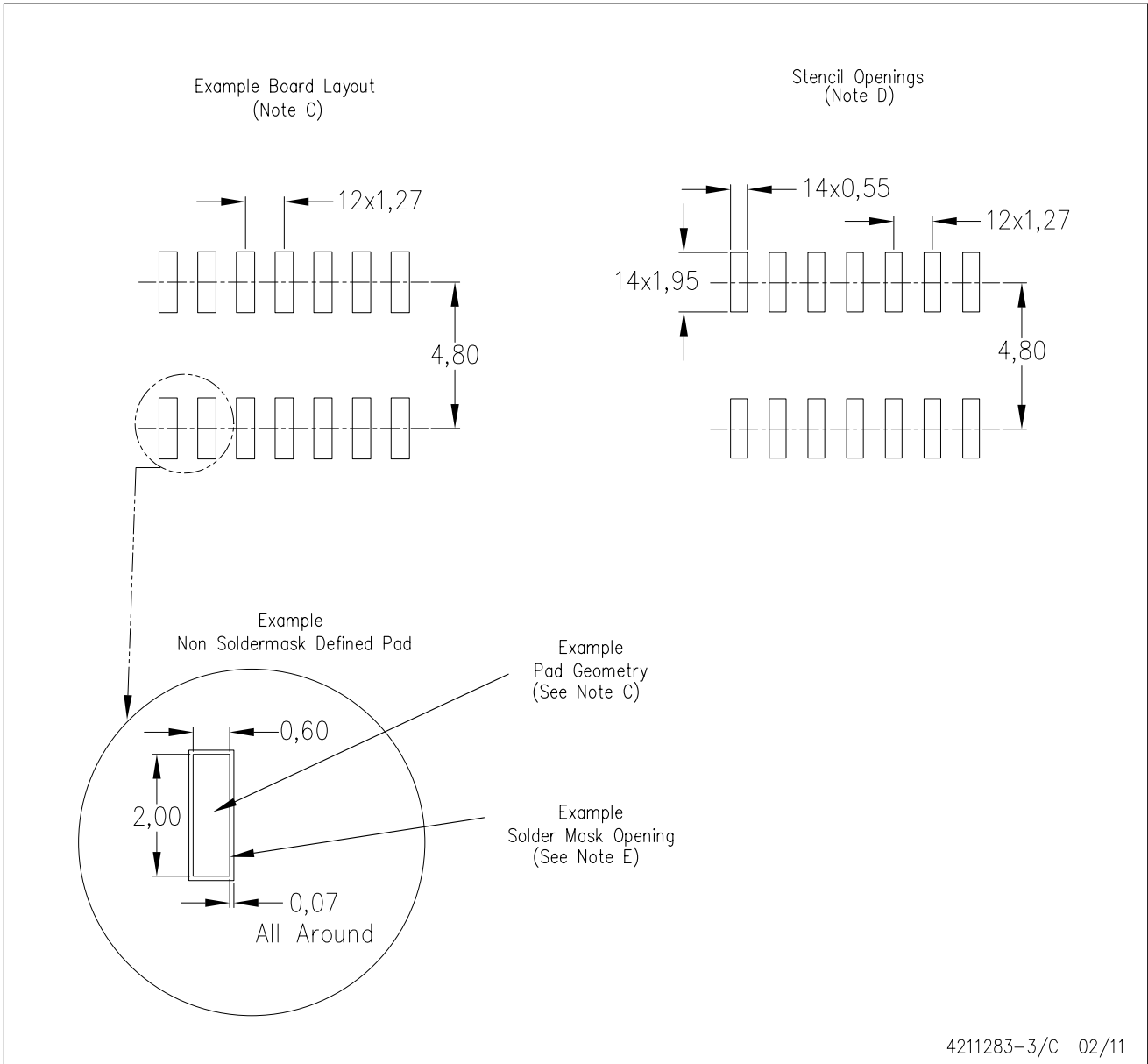
\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN65HVD30MDREP	SOIC	D	8	2500	346.0	346.0	29.0
SN65HVD33MDREP	SOIC	D	14	2500	333.2	345.9	28.6



D (R-PDSO-G14)

PLASTIC SMALL OUTLINE

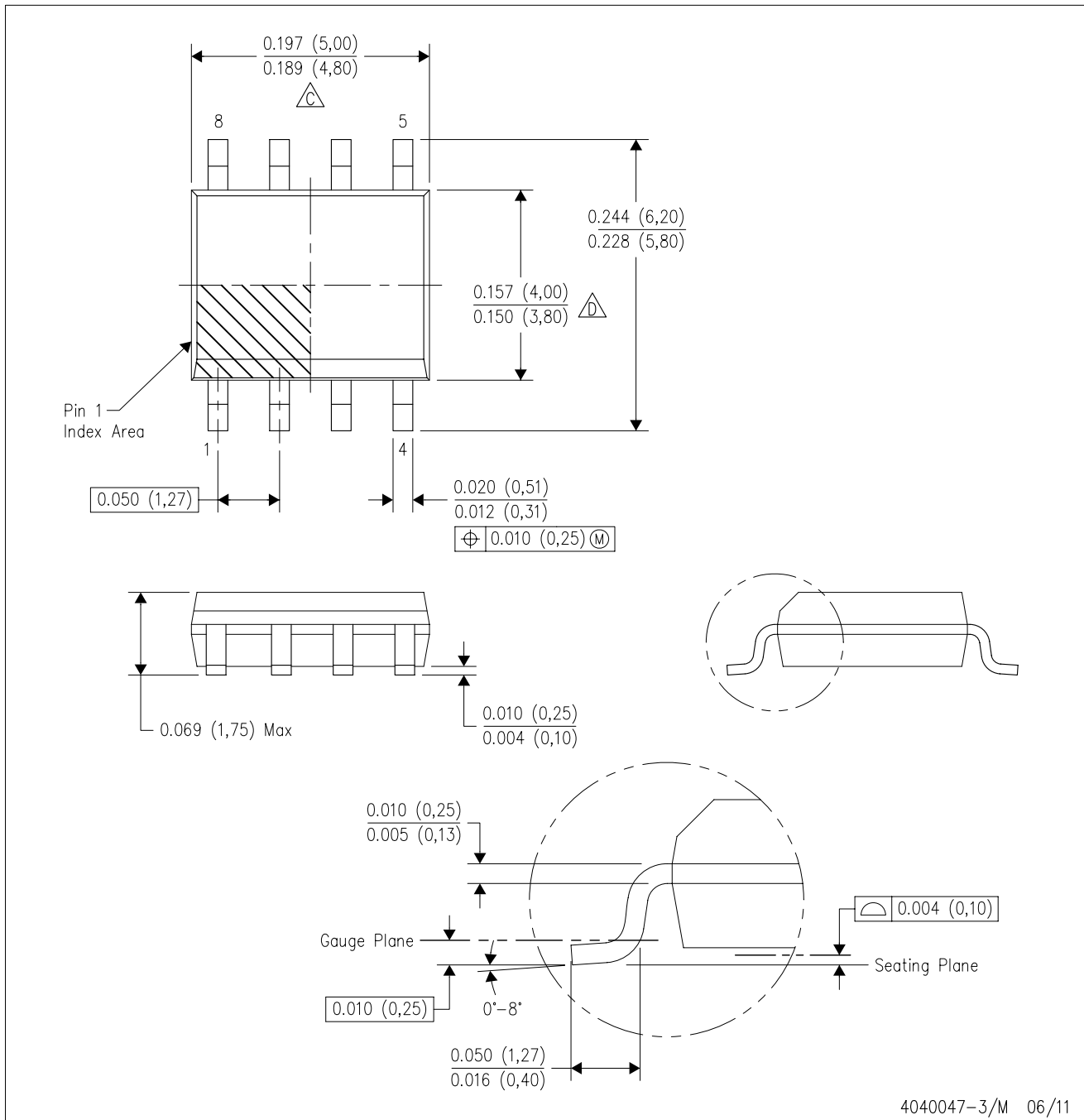




- NOTES:
- All linear dimensions are in millimeters.
  - This drawing is subject to change without notice.
  - Publication IPC-7351 is recommended for alternate designs.
  - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
  - Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.



D (R-PDSO-G8)

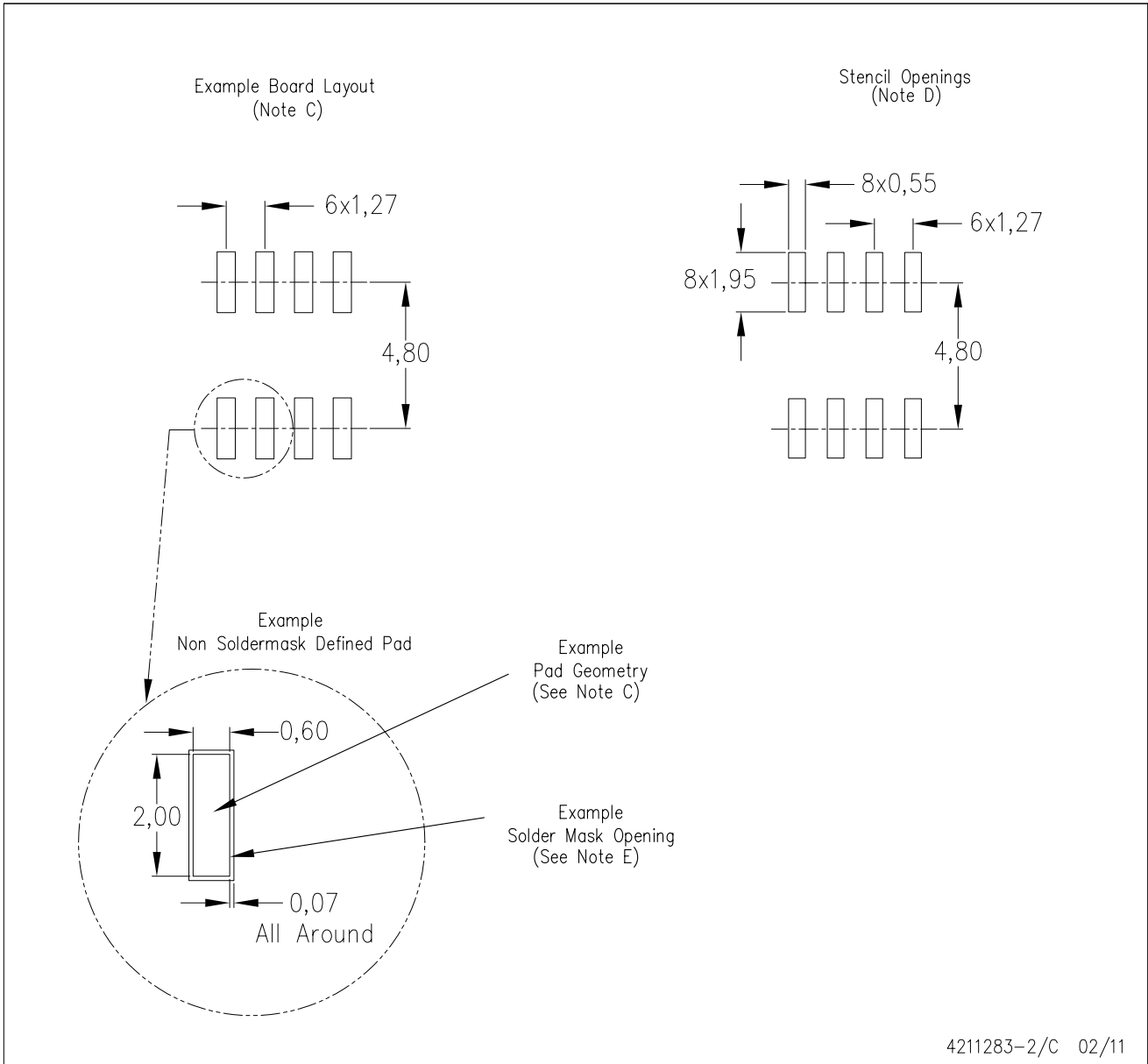
PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  -  Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
  -  Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
  - E. Reference JEDEC MS-012 variation AA.

D (R-PDSO-G8)

PLASTIC SMALL OUTLINE



- NOTES:
- All linear dimensions are in millimeters.
  - This drawing is subject to change without notice.
  - Publication IPC-7351 is recommended for alternate designs.
  - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
  - Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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Energy and Lighting	<a href="http://www.ti.com/energy">www.ti.com/energy</a>
Industrial	<a href="http://www.ti.com/industrial">www.ti.com/industrial</a>
Medical	<a href="http://www.ti.com/medical">www.ti.com/medical</a>
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