

# SN74HSTL162822

## 14-BIT TO 28-BIT HSTL-TO-LVTTL MEMORY ADDRESS LATCH

SCES091A – DECEMBER 1996 – REVISED APRIL 1997

- Member of the Texas Instruments Widebus™ Family
- Inputs Meet JEDEC HSTL Standard JESD8-6
- All Outputs Have Equivalent 25-Ω Series Resistors
- Packaged in Plastic Thin Shrink Small-Outline Package

### description

This 14-bit to 28-bit D-type latch is designed for 3.15-V to 3.45-V  $V_{CC}$  operation. HSTL levels are expected on the inputs. LVTTL levels are driven on the Q outputs.

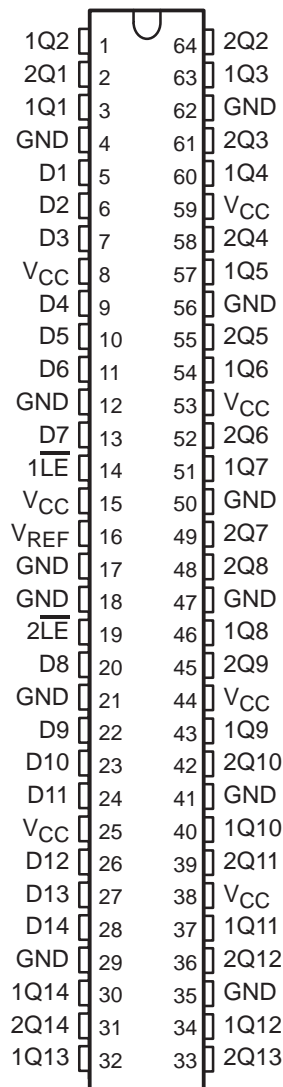
All outputs are designed to sink up to 12 mA and include 25-Ω series resistors to reduce overshoot and undershoot.

The SN74HSTL162822 is particularly suitable for driving an address bus to two banks of memory. Each bank of 14 outputs is controlled with its own latch-enable ( $\overline{LE}$ ) input.

Each of the 14 data (D) inputs is tied to the inputs of two D-type latches, which provide true data at the outputs. While  $\overline{LE}$  is low, the outputs (Q) of the corresponding 14 latches follow the D inputs. When  $\overline{LE}$  is taken high, the Q outputs are latched at the levels set up at the D inputs.

The SN74HSTL162822 is characterized for operation from -40°C to 90°C.

**DGG PACKAGE  
(TOP VIEW)**



**FUNCTION TABLE**

INPUTS		OUTPUT
$\overline{LE}$	D	Q
L	H	H
L	L	L
H	X	$Q_0^\dagger$

† Output level before the indicated steady-state input conditions were established



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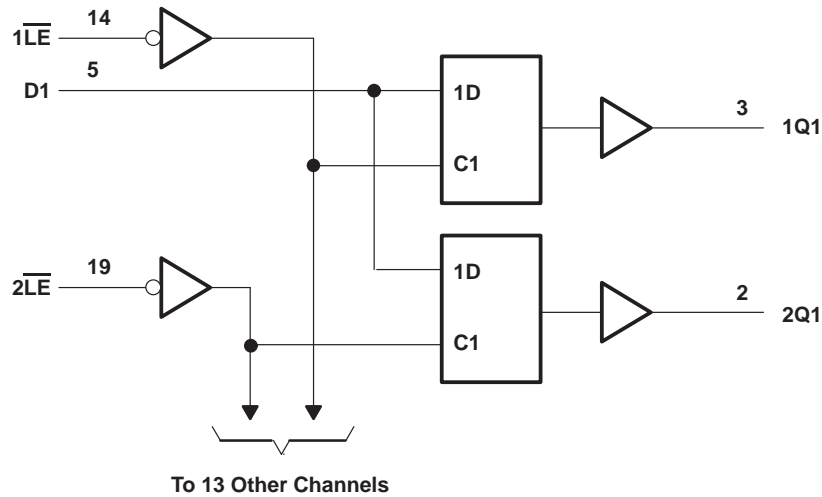
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### logic diagram (positive logic)



### absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, $V_{CC}$	–0.5 V to 4.6 V
Input voltage range, $V_I$ (see Note 1)	–0.5 V to $V_{CC} + 0.5$ V
Output voltage range, $V_O$ (see Note 1)	–0.5 V to $V_{CC} + 0.5$ V
Input clamp current, $I_{IK}$ ( $V_I < 0$ )	–50 mA
Output clamp current, $I_{OK}$ ( $V_O < 0$ or $V_O > V_{CC}$ ) (see Note 2)	±50 mA
Continuous output current, $I_O$ ( $V_O = 0$ to $V_{CC}$ )	±50 mA
Continuous current through each $V_{CC}$ or GND	±100 mA
Package thermal impedance, $\theta_{JA}$ (see Note 3)	74°C/W
Storage temperature range, $T_{stg}$	–65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.  
 2. This current flows only when the output is in the high state and  $V_O > V_{CC}$ .  
 3. The package thermal impedance is calculated in accordance with EIA/JEDEC Std JESD51.

### recommended operating conditions (see Note 4)

		MIN	NOM	MAX	UNIT
$V_{CC}$	Supply voltage	3.15		3.45	V
$V_{REF}$	Reference voltage	0.68	0.75	0.9	V
$V_I$	Input voltage	0		1.5	V
$V_{IH}$	High-level input voltage	All pins		$V_{REF} + 100$ mV	V
$V_{IL}$	Low-level input voltage	All pins		$V_{REF} - 100$ mV	V
$I_{OH}$	High-level output current			–12	mA
$I_{OL}$	Low-level output current			12	
$T_A$	Operating free-air temperature	–40		90	°C

NOTE 4: Unused inputs must be held high or low to prevent them from floating.

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**electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)**

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
$V_{IK}$		$V_{CC} = 3.15\text{ V}$ , $I_I = -18\text{ mA}$			-1.2	V
$V_{OH}$		$V_{CC} = 3.15\text{ V}$ , $I_{OH} = -12\text{ mA}$	2.2			V
$V_{OL}$		$V_{CC} = 3.15\text{ V}$ , $I_{OL} = 12\text{ mA}$			0.8	V
$I_I$	Control inputs	$V_{CC} = 3.45\text{ V}$			5	$\mu\text{A}$
	Data inputs				5	
	$V_{REF}$		$V_I = 0\text{ or }1.5\text{ V}$		90	
$I_{CC}$		$V_{CC} = 3.45\text{ V}$ , $V_I = 0\text{ or }1.5\text{ V}$	50	100		mA
$C_i$	Control inputs	$V_{CC} = 0\text{ or }3.3\text{ V}$ ,	$V_I = 0\text{ or }3.3\text{ V}$		2	pF
	Data inputs	$V_{CC} = 0\text{ or }3.3\text{ V}$ ,	$V_I = 0\text{ or }3.3\text{ V}$		2	
$C_o$	Outputs	$V_{CC} = 0$ ,	$V_O = 0$		4	pF

† All typical values are at  $V_{CC} = 3.3\text{ V}$ ,  $T_A = 25^\circ\text{C}$ .

**timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 1)**

		$V_{CC} = 3.3\text{ V}$ $\pm 0.15\text{ V}$		UNIT
		MIN	MAX	
$t_w$	Pulse duration, $\overline{LE}$ low	3		ns
$t_{su}$	Setup time, D before $\overline{LE}\uparrow$	2		ns
$t_h$	Hold time, D after $\overline{LE}\uparrow$	1		ns

**switching characteristics over recommended operating free-air temperature range,  $V_{REF} = 0.75\text{ V}$**

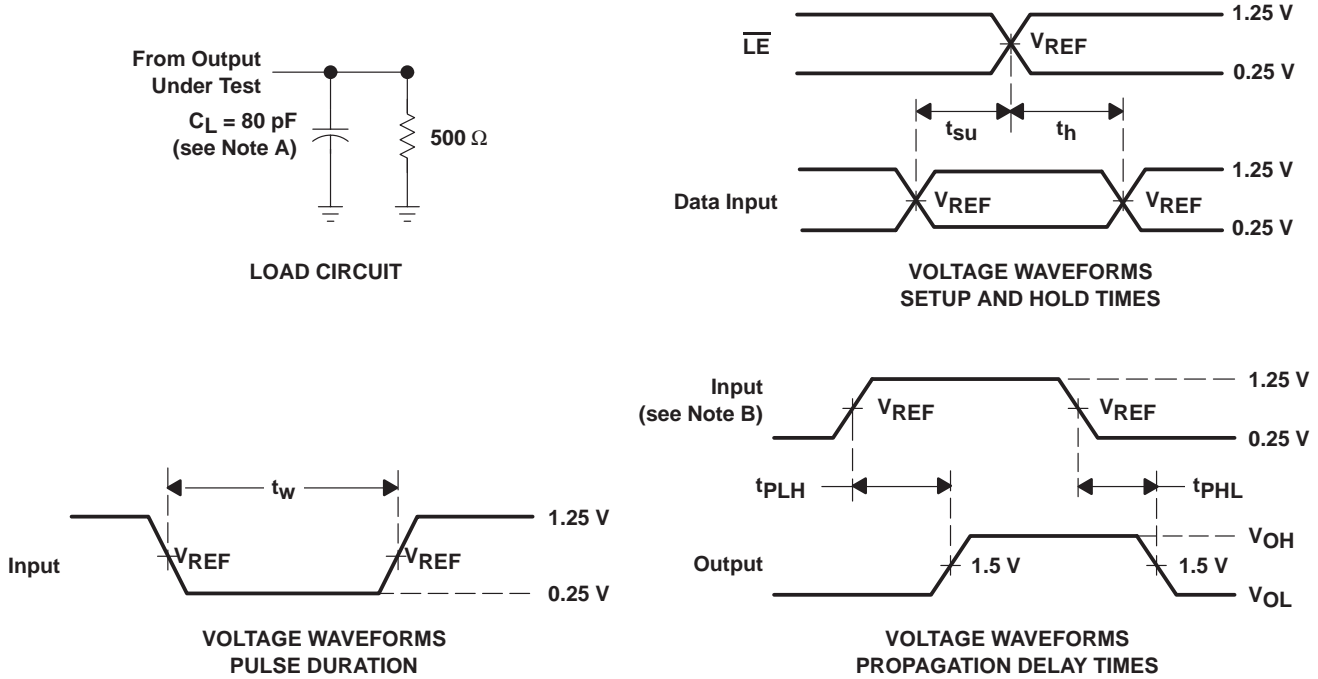
PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC} = 3.3\text{ V}$ $\pm 0.15\text{ V}$		UNIT
			MIN	MAX	
$t_{pd}$	D	Q	1.6	5	ns
	$\overline{LE}$		1.7	5.7	

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### PARAMETER MEASUREMENT INFORMATION



- NOTES:
- A.  $C_L$  includes probe and jig capacitance.
  - B. All input pulses are supplied by generators having the following characteristics:  $PRR \leq 10$  MHz,  $Z_O = 50 \Omega$ ,  $t_r \leq 1$  ns,  $t_f \leq 1$  ns.
  - C. The outputs are measured one at a time with one transition per measurement.
  - D.  $t_{PHL}$  and  $t_{PLH}$  are the same as  $t_{pd}$ .

Figure 1. Load Circuit and Voltage Waveforms

**PACKAGING INFORMATION**

Orderable Device	Status <sup>(1)</sup>	Package Type	Package Drawing	Pins	Package Qty	Eco Plan <sup>(2)</sup>	Lead/Ball Finish	MSL Peak Temp <sup>(3)</sup>
74HSTL162822DGGRE4	ACTIVE	TSSOP	DGG	64	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
74HSTL162822DGGRG4	ACTIVE	TSSOP	DGG	64	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74HSTL162822DGGR	ACTIVE	TSSOP	DGG	64	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM

<sup>(1)</sup> The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBsolete:** TI has discontinued the production of the device.

<sup>(2)</sup> Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

<sup>(3)</sup> MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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**TAPE AND REEL INFORMATION**



**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74HSTL162822DGGR	TSSOP	DGG	64	2000	330.0	24.4	8.4	17.3	1.7	12.0	24.0	Q1

**TAPE AND REEL BOX DIMENSIONS**



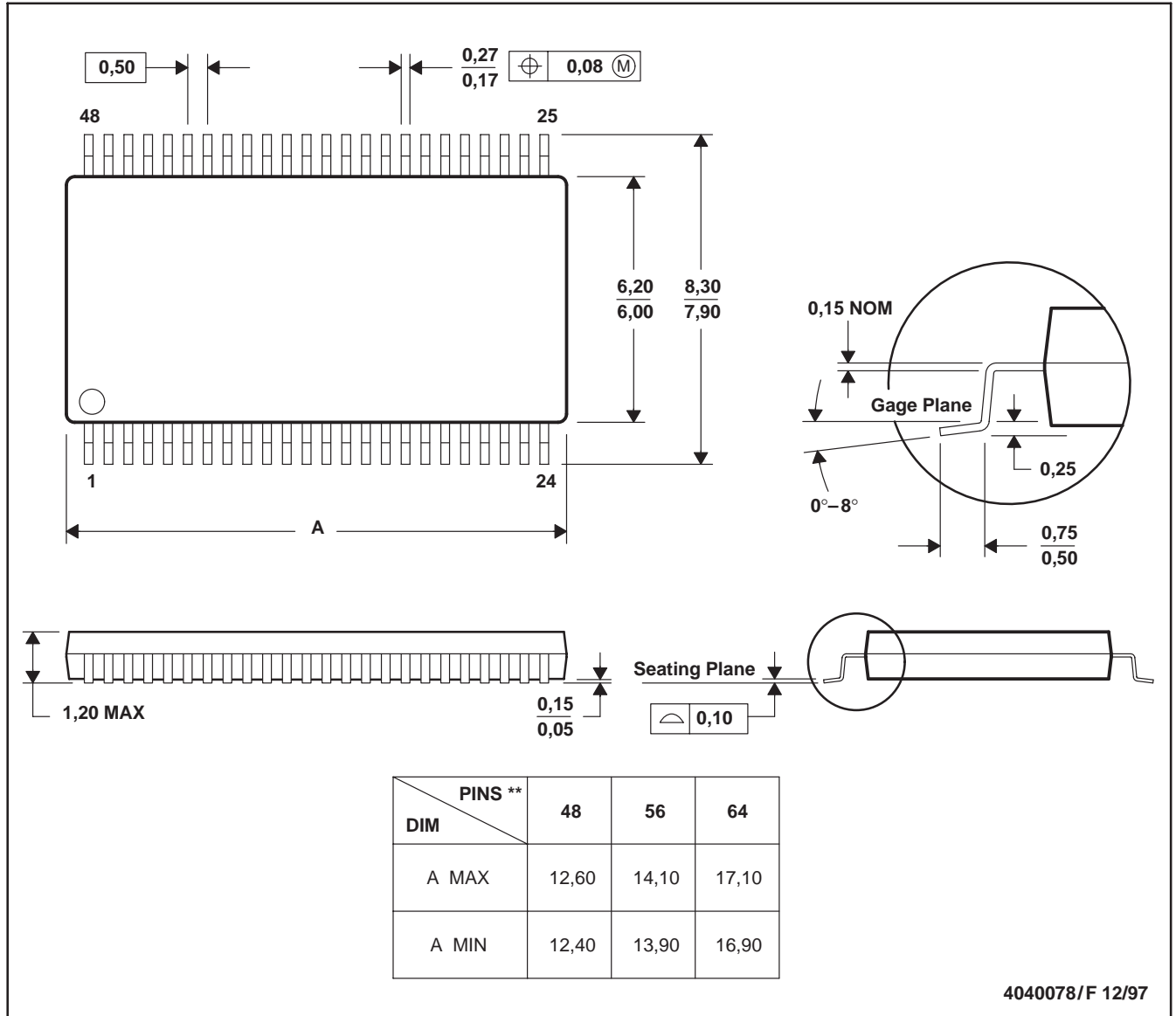
\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74HSTL162822DGGR	TSSOP	DGG	64	2000	346.0	346.0	41.0

DGG (R-PDSO-G\*\*)

PLASTIC SMALL-OUTLINE PACKAGE

48 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.  
 B. This drawing is subject to change without notice.  
 C. Body dimensions do not include mold protrusion not to exceed 0,15.  
 D. Falls within JEDEC MO-153



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