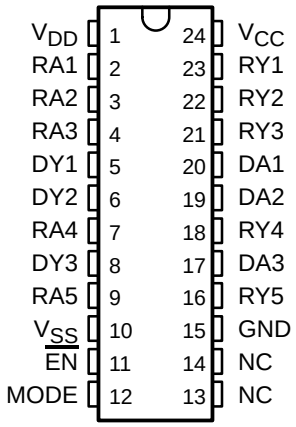
- **Single-Chip RS-232 Interface for IBM™ PC-Compatible Serial Port**
- **Designed to Transmit and Receive 4-μs Pulses (Equivalent to 256 kbit/s)**
- **Standby Power Is Less Than 750 μW Maximum**
- **Wide Supply-Voltage Range . . . 4.75 V to 15 V**
- **Driver Output Slew Rates Are Internally Controlled to 30 V/μs Maximum**
- **RS-232 Bus-Pin ESD Protection Exceeds:**
  – 15 kV, Human-Body Model
- **Receiver Input Hysteresis . . . 1000 mV Typical**
- **Three Drivers and Five Receivers Meet or Exceed the Requirements of TIA/EIA-232-F and ITU v.28 Standards**
- **Complements the SN75LP196**
- **One Receiver Remains Active During WAKE-UP Mode (100 μA Maximum)**
- **Matches Flow-Through Pinout of Industry-Standard SN75185, SN75C185, and SN75LP185, With Additional Control Pins**
- **Package Options Include Plastic Shrink Small-Outline (DB), Small-Outline (DW), and Thin Shrink Small-Outline (PW) Packages, and Standard Plastic (NT) DIPs**

DB, DW, NT, OR PW PACKAGE
(TOP VIEW)



NC – No internal connection

description

The SN75LPE185 is a low-power bipolar device containing three drivers and five receivers, with 15-kV ESD protection on the bus pins, with respect to each other. Bus pins are defined as those pins that tie directly to the serial-port connector, including GND. The pinout matches the flow-through design of the industry-standard SN75185, SN75C185, and SN75LP185, with the addition of four pins for control signals. The flow-through pinout of the device allows easy interconnection of the universal asynchronous receiver/transmitter (UART) and serial-port connector of the IBM™ PC compatibles. The SN75LPE185 provides a rugged, low-cost solution for this function, with the combination of bipolar processing and 15-kV ESD protection.

The SN75LPE185 has an internal slew-rate control to provide a maximum rate of change in the output signal of 30 V/μs. The driver output swing is clamped at ±6 V to enable the higher data rates associated with this device and to reduce EMI emissions. Although the driver outputs are clamped, the outputs can handle voltages up to ±15 V without damage.

description (continued)

The device has flexible control options for power management when the serial port is inactive. A common disable for all of the drivers and receivers is provided with the active-low enable ($\overline{EN}$) input. The mode-control (MODE) input selects between the STANDBY and WAKE-UP modes. With a low-level input on MODE and a high-level input on $\overline{EN}$, one receiver remains active, while the remaining drivers and receivers are disabled to implement the WAKE-UP mode. With a high-level input on both MODE and $\overline{EN}$, all drivers and receivers are disabled to implement the STANDBY mode. The outputs of the drivers are in the high-impedance state when the device is powered off. To ensure the outputs of the receivers are in a known output level (as listed in the *Application Information* section of this data sheet) when the device is powered off, in STANDBY mode, or in WAKE-UP mode, external pullup/pulldown circuitry must be provided. All the logic inputs accept 3.3-V or 5-V input signals.

The SN75LPE185 complies with the requirements of TIA/EIA-232-F and ITU v.28 standards. These standards are for data interchange between a host computer and peripheral at signaling rates up to 20 kbit/s. The switching speeds of the SN75LPE185 support rates up to 256 kbit/s.

The SN75LPE185 is characterized for operation from 0°C to 70°C.

AVAILABLE OPTIONS

T_A	PACKAGED DEVICES			
	PLASTIC SHRINK SMALL OUTLINE (DB)	PLASTIC SMALL OUTLINE (DW)	PLASTIC THIN SHRINK SMALL OUTLINE (PW)	PLASTIC DIP (NT)
0°C to 70°C	SN75LPE185DBR	SN75LPE185DW	SN75LPE185PWR	SN75LPE185NT

The DB and PW packages are only available taped and reeled. The DW package is also available taped and reeled. Add the suffix R to device type (e.g., SN75LPE185DWR).

Function Tables

DRIVERS

INPUT DA	ENABLE $\overline{EN}$	OUTPUT DY
X	H	Z
H	L	L
L	L	H
Open	L	L
H	Open	L
L	Open	H

H = high level, L = low level,
X = irrelevant, Z = high impedance (off)

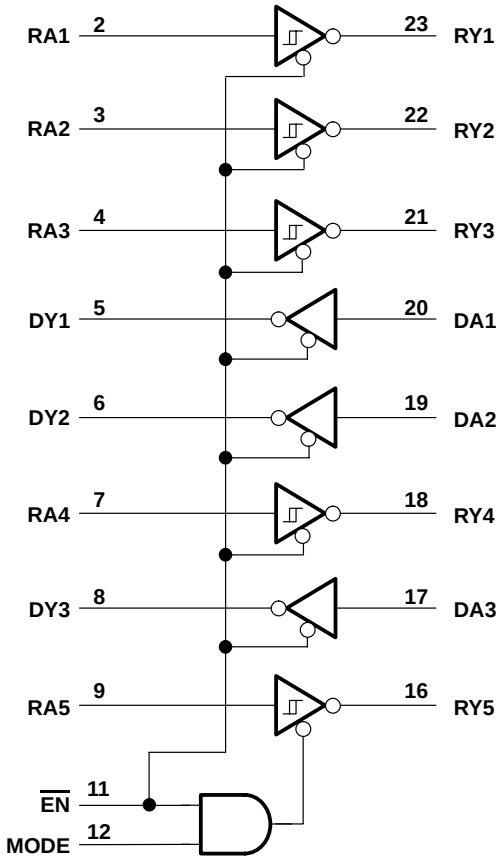
Function Tables (Continued)

RECEIVERS

INPUTS		ENABLE INPUTS		OUTPUTS	
RA1–RA4	RA5	$\overline{EN}$	MODE	RY1–RY4	RY5
H	H	L	X	L	L
L	L	L	X	H	H
X	H	H	L	Z	L
X	L	H	L	Z	H
X	X	H	H	Z	Z
Open	Open	L	X	H	H
H	H	L	Open	L	L
L	L	L	Open	H	H
X	H	H	Open	Z	L
X	L	H	Open	Z	H
H	H	Open	X	L	L
L	L	Open	X	H	H

H = high level, L = low level, X = irrelevant, Z = high impedance (off)

functional logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Positive supply voltage range: V_{CC} (see Note 1) . . . . . –0.5 V to 7 V
V_{DD} (see Note 1) . . . . . –0.5 V to 15 V
Negative supply voltage range, V_{SS} (see Note 1) . . . . . 0.5 V to –15 V
Receiver input voltage range, V_I (RA) . . . . . –30 V to 30 V
Driver input voltage range, V_I (DA, $\overline{EN}$, MODE) . . . . . –0.5 V to V_{CC} + 0.4 V
Receiver output voltage range, V_O (RY) . . . . . –0.5 V to 6 V
Driver output voltage range, V_O (DY) . . . . . –15 V to 15 V
Electrostatic discharge, bus pins: Human-body model (see Note 2) . . . . . Class 3: 15 kV
Machine model (see Note 2) . . . . . Class 3: 500 V
Electrostatic discharge, all pins: Human-body model (see Note 2) . . . . . Class 3: 5 kV
Machine model (see Note 2) . . . . . Class 3: 200 V
Package thermal impedance, θ_{JA} (see Note 3): DB package . . . . . 63°C/W
(see Note 3): DW package . . . . . 46°C/W
(see Note 4): NT package . . . . . 67°C/W
(see Note 3): PW package . . . . . 88°C/W
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds . . . . . 260°C
Storage temperature range, T_{stg} . . . . . –65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltage values are with respect to network ground terminal unless otherwise noted.
2. Per MIL-STD-883 Method 3015.7
3. The package thermal impedance is calculated in accordance with JESD 51-7.
4. The package thermal impedance is calculated in accordance with JESD 51-3.

recommended operating conditions

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage (see Note 5)		4.75	5	5.25	V
V_{DD}	Supply voltage		9	12	15	V
V_{SS}	Supply voltage		–9	–12	–15	V
V_{IH}	High-level input voltage	DA, $\overline{EN}$, MODE	2			V
V_{IL}	Low-level input voltage	DA, $\overline{EN}$, MODE			0.8	V
V_I	Receiver input voltage range	RA	–25		25	V
I_{OH}	High-level output current	RY			–1	mA
I_{OL}	Low-level output current	RY			2	mA
T_A	Operating free-air temperature		0		70	°C

NOTE 5: V_{CC} cannot be greater than V_{DD}.

supply currents over the recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
I_{CC}	Supply current for V_{CC}	No load, All inputs at minimum V_{OH} or maximum V_{OL}	V_{DD} = 9 V, V_{SS} = –9 V, $\overline{EN}$ at GND, See Note 6			1000	µA
			V_{DD} = 12 V, V_{SS} = –12 V, $\overline{EN}$ at GND			1000	
			$\overline{EN}$, MODE at V_{CC}			650	
			$\overline{EN}$ at V_{CC}, MODE at GND			700	
I_{DD}	Supply current for V_{DD}	No load, All inputs at minimum V_{OH} or maximum V_{OL}	V_{DD} = 9 V, V_{SS} = –9 V, $\overline{EN}$ at GND, See Note 6			800	µA
			V_{DD} = 12 V, V_{SS} = –12 V, $\overline{EN}$ at GND			800	
			$\overline{EN}$, MODE at V_{CC}			20	
			$\overline{EN}$ at V_{CC}, MODE at GND			20	
I_{SS}	Supply current for V_{SS}	No load, All inputs at minimum V_{OH} or maximum V_{OL}	V_{DD} = 9 V, V_{SS} = –9 V, $\overline{EN}$ at GND, See Note 6			–625	µA
			V_{DD} = 12 V, V_{SS} = –12 V, $\overline{EN}$ at GND			–625	
			$\overline{EN}$, MODE at V_{CC}			–50	
			$\overline{EN}$ at V_{CC}, MODE at GND			–50	

NOTE 6: Minimum RS-232 driver output voltages are not attained with ±5-V supplies.

driver electrical characteristics over the recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage	V_I = 0.8 V, R_L = 3 kΩ, See Figure 1	V_{DD} = 9 V, V_{SS} = –9 V, $\overline{EN}$ at GND, See Note 6	5	5.8	6.6	V
			V_{DD} = 12 V, V_{SS} = –12 V, $\overline{EN}$ at GND, See Note 7	5	5.8	6.6	
V_{OL}	Low-level output voltage	V_I = 2 V, R_L = 3 K, See Figure 1	V_{DD} = 9 V, V_{SS} = –9 V, $\overline{EN}$ at GND, See Note 6	–5	–5.8	–6.9	V
			V_{DD} = 12 V, V_{SS} = –12 V, $\overline{EN}$ at GND, See Note 7	–5	–5.8	–6.9	
I_{IH}	High-level input current	V_I at V_{CC}				1	µA
I_{IL}	Low-level input current	V_I at GND				–1	µA
I_{OZ}	High-impedance output current	V_{CC} = 5 V, V_{DD} = 12 V, V_{SS} = –12 V, –5 V ≤ V_O ≤ 5 V				±100	µA
$I_{OS(H)}$	Short-circuit high-level output current	V_O = GND or V_{SS},	See Figure 2 and Note 8		–30	–55	mA
$I_{OS(L)}$	Short-circuit low-level output current	V_O = GND or V_{SS},	See Figure 2 and Note 8		30	55	mA
r_o	Output resistance	V_{DD} = V_{SS} = V_{CC} = 0,	V_O = 2 V	300			Ω

NOTES: 6. Minimum RS-232 driver output voltages are not attained with ±5-V supplies.
7. Maximum output swing is limited to ±5.5 V to enable the higher data rates associated with this device and to reduce EMI emissions.
8. Not more than one output should be shorted at one time.

driver switching characteristics over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{PHL}	Propagation delay time, high- to low-level output	R_L = 3 kΩ to 7 kΩ,	C_L = 15 pF, See Figure 1	300	800	1600	ns
t_{PLH}	Propagation delay time, low- to high-level output	R_L = 3 kΩ to 7 kΩ,	C_L = 15 pF, See Figure 1	300	800	1600	ns
t_{PZL}	Driver output-enable time to low-level output	R_L = 3 kΩ to 7 kΩ, C_L = 15 pF	STANDBY or WAKE-UP modes, See Figures 1 and 6 and Note 7		50	100	µs
t_{PZH}	Driver output-enable time to high-level output	R_L = 3 kΩ to 7 kΩ, C_L = 15 pF	STANDBY or WAKE-UP modes, See Figures 1 and 6 and Note 7		50	100	µs
t_{PLZ}	Driver output-disable time from low-level output	R_L = 3 kΩ to 7 kΩ, C_L = 15 pF	STANDBY or WAKE-UP modes, See Figures 1 and 6 and Note 7		50	100	µs
t_{PHZ}	Driver output-disable time from high-level output	R_L = 3 kΩ to 7 kΩ, C_L = 15 pF	STANDBY or WAKE-UP modes, See Figures 1 and 6 and Note 7		50	100	µs
t_{TLH}	Transition time, low- to high-level output	V_{CC} = 5 V, V_{DD} = 12 V, V_{SS} = –12 V, R_L = 3 kΩ to 7 kΩ, See Figure 1 and Note 7	Using 10%-to-90% transition region, Driver speed = 250 kbit/s, C_L = 15 pF	375		2240	ns
			Using ±3-V transition region, Driver speed = 250 kbit/s, C_L = 15 pF	200		1500	
			Using ±2-V transition region, Driver speed = 250 kbit/s, C_L = 15 pF	133		1000	
			Using ±3-V transition region, Driver speed = 125 kbit/s, C_L = 2500 pF			2750	
t_{THL}	Transition time, high- to low-level output	V_{CC} = 5 V, V_{DD} = 12 V, V_{SS} = –12 V, R_L = 3 kΩ to 7 kΩ, See Figure 1 and Note 7	Using 10%-to-90% transition region, Driver speed = 250 kbit/s, C_L = 15 pF	375		2240	ns
			Using ±3-V transition region, Driver speed = 250 kbit/s, C_L = 15 pF	200		1500	
			Using ±2-V transition region, Driver speed = 250 kbit/s, C_L = 15 pF	133		1000	
			Using ±3-V transition region, Driver speed = 125 kbit/s, C_L = 2500 pF			2750	
SR	Output slew rate	V_{CC} = 5 V, V_{DD} = 12 V, V_{SS} = –12 V, R_L = 3 kΩ to 7 kΩ, C_L = 15 pF, See Note 7	Using ±3-V transition region, Driver speed = 0 to 250 kbit/s	4	20	30	V/µs

NOTE 7: Maximum output swing is limited to ±5.5 V to enable the higher data rates associated with this device and to reduce EMI emissions.

receiver electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

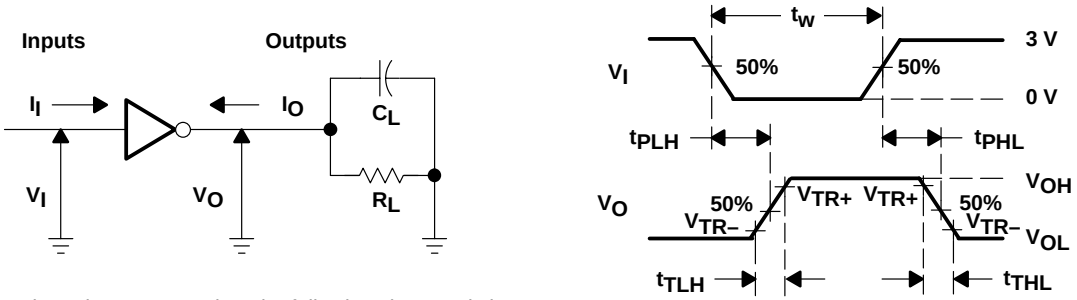
PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{IT+}	Positive-going input threshold voltage	See Figure 3		1.6	2	2.55	V
V_{IT-}	Negative-going input threshold voltage	See Figure 3		0.6	1	1.45	V
V_{HYS}	Input hysteresis, $V_{IT+} - V_{IT-}$	See Figure 3		600	1100		mV
V_{OH}	High-level output voltage	I_{OH} = –1 mA		2.5	3.9		V
V_{OL}	Low-level output voltage	I_{OL} = 2 mA			0.33	0.5	V
I_{IH}	High-level input current	V_I = 3 V		0.43	0.6	1	mA
		V_I = 25 V		3.6	5.1	8.3	
I_{IL}	Low-level input current	V_I = –3 V		–0.43	–0.6	–1	mA
		V_I = –25 V		–3.6	–5.1	–8.3	
$I_{OS(H)}$	Short-circuit high-level output current	V_O = 0,	See Figure 5 and Note 8			–20	mA
$I_{OS(L)}$	Short-circuit low-level output current	$V_O = V_{CC}$,	See Figure 5 and Note 8			20	mA
I_{OZ}	High-impedance output current	V_{CC}= 0 or 5 V,	0.3 V ≤ V_O ≤ V_{CC}			±100	µA
R_{IN}	Input resistance	V_I = ±3 V to ±25 V		3	5	7	kΩ

NOTE 8: Not more than one output should be shorted at one time.

receiver switching characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PHL}	Propagation delay time, high- to low-level output	STANDBY mode C_L = 50 pF, See Figures 4 and 7		400	900	ns
t_{PLH}	Propagation delay time, low- to high-level output			400	900	ns
t_{TLH}	Transition time low- to high-level output			200	500	ns
t_{THL}	Transition time high- to low-level output			200	400	ns
$t_{SK(P)}$	Pulse skew $\lvert t_{PLH} - t_{PHL} \rvert$			200	425	ns
t_{PZL}	Receiver output-enable time to low-level output			50	100	µs
t_{PZH}	Receiver output-enable time to high-level output			50	100	µs
t_{PLZ}	Receiver output-disable time from low-level output			50	100	µs
t_{PHZ}	Receiver output-disable time from high-level output			50	100	µs
t_{PHL}	Propagation delay time, high- to low-level output (WAKE-UP mode)			500	1500	ns
t_{PLH}	Propagation delay time, low- to high-level output (WAKE-UP mode)			500	1500	ns

PARAMETER MEASUREMENT INFORMATION



NOTES: A. The pulse generator has the following characteristics:
For C_L < 1000 pF: t_W = 4 µs, PRR = 250 kbit/s, Z_O = 50 Ω, $t_r = t_f$ < 50 ns.
For C_L = 2500 pF: t_W = 8 µs, PRR = 125 kbit/s, Z_O = 50 Ω, $t_r = t_f$ < 50 ns.
B. C_L includes probe and jig capacitance.

Figure 1. Driver Parameter Test Circuit and Waveform

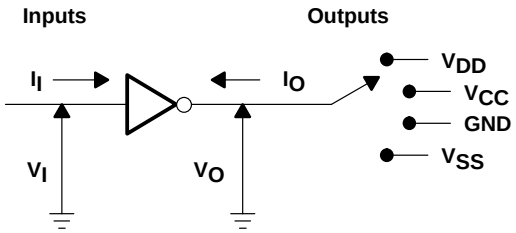


Figure 2. Driver I_{OS} Test

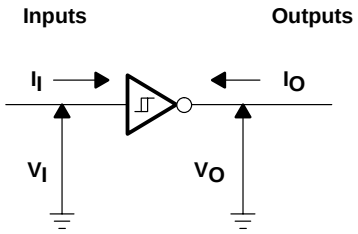
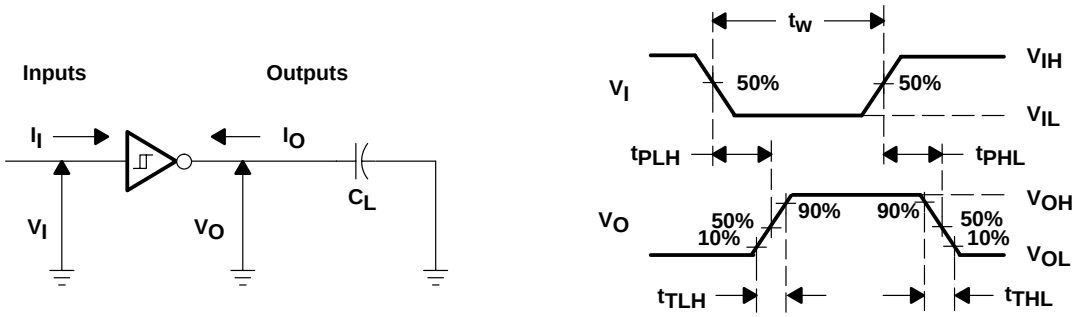


Figure 3. Receiver V_{IT} Test



NOTES: A. The pulse generator has the following characteristics: t_W = 4 µs, PRR = 250 kbit/s, Z_O = 50 Ω, $t_r = t_f$ < 50 ns.
B. C_L includes probe and jig capacitance.

Figure 4. Receiver Parameter Test Circuit and Waveform

PARAMETER MEASUREMENT INFORMATION

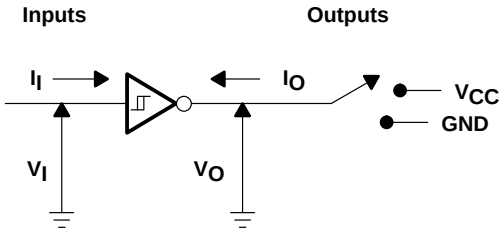
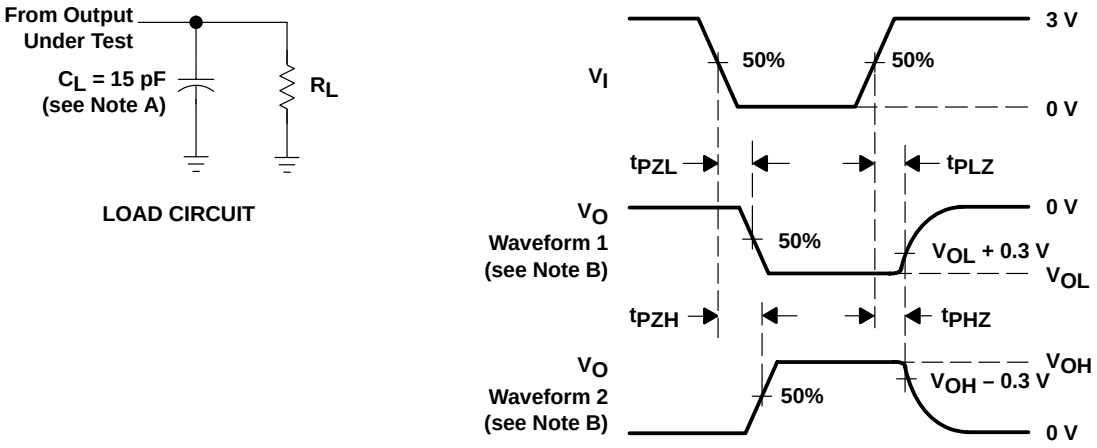


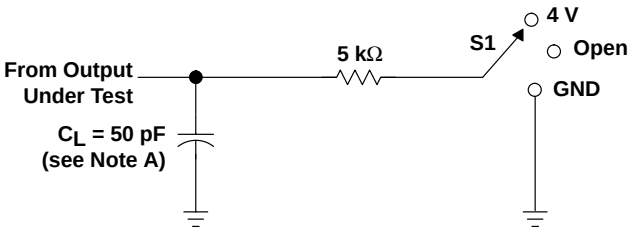
Figure 5. Receiver I_{OS} Test



NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR = 250 kbit/s, Z_O = 50 Ω, $t_r = t_f < 50$ ns.
D. The outputs are measured one at a time with one transition per measurement.

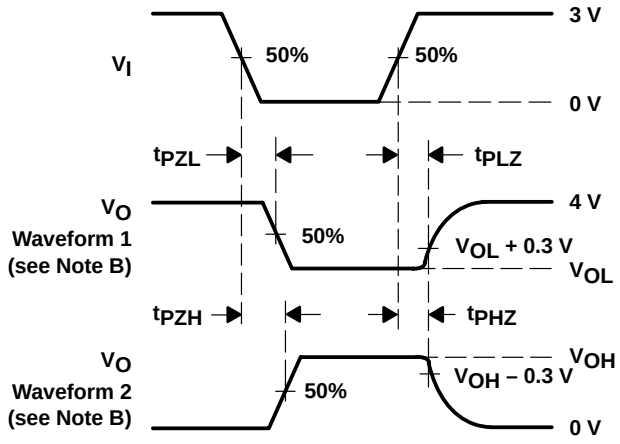
Figure 6. Driver 3-State Parameter Load Circuit and Voltage Waveforms

PARAMETER MEASUREMENT INFORMATION



TEST	S1
t_{PHL}/t_{PLH}	Open
t_{PLZ}/t_{PZL}	4 V
t_{PHZ}/t_{PZH}	GND

LOAD CIRCUIT



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR = 250 kbit/s, Z_O = 50 Ω, $t_r = t_f < 50$ ns.
D. The outputs are measured one at a time with one transition per measurement.

Figure 7. Receiver 3-State Parameter Load Circuit and Voltage Waveforms

APPLICATION INFORMATION

receiver output states

RECEIVER KNOWN OUTPUT STATES DURING POWER-DOWN, STANDBY, OR WAKE-UP MODES		
RECEIVER NUMBER	**SIGNAL NAME**	**RECEIVER OUTPUT**
RY1	$\overline{\text{DCD}}$	High
RY2	$\overline{\text{DSR}}$	High
RY3	RX	Low
RY4	$\overline{\text{CTS}}$	High
RY5	$\overline{\text{RI}}$	High

fault protection during power down

Diodes placed in series with the V_{DD} and V_{SS} leads protect the SN75LPE185 in the fault condition, in which the device outputs are shorted to ±15 V and the power supplies are at low voltage and provide low-impedance paths to ground.

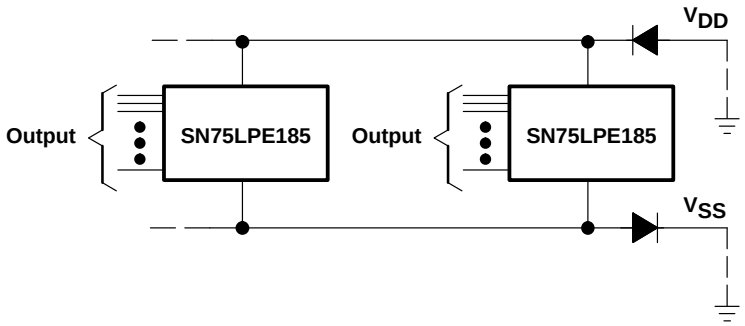


Figure 8. Power-Supply Protection to Meet Power-Off Fault Conditions of TIA/EIA-232-F

APPLICATION INFORMATION

WAKE-UP mode

While in the WAKE-UP mode, all the drivers and receivers of the SN75LPE185 device are in the high-impedance state, except for receiver 5, which can be used as a ring indicator function. In this mode, the current drawn from the power supplies is low, to conserve power.

In today's PCs, board designers are becoming more concerned about power consumption. The flexibility of the SN75LPE185 during WAKE-UP mode allows the designer to operate the device at auxiliary power-supply voltages below specified levels. The SN75LPE185 functions properly during WAKE-UP mode, using the following power-supply conditions:

(a) V_{CC} = 4.75 V, V_{DD} = 9 V, and V_{SS} = –9 V (data-sheet specifications)
(b) V_{CC} = 5 V, V_{DD} = 5 V, and V_{SS} = –5 V
(c) V_{CC} = 5 V, V_{DD} = open, and V_{SS} = open
(d) V_{CC} = 5 V, V_{DD} = 5 V, and V_{SS} is shorted to the most negative supply.

Condition (a) describes the minimum supply voltages necessary for the device to comply fully to specifications.

Conditions (b) and (d) describe the condition where a –5-V supply is not available during auxiliary power. In this case, V_{SS} must be shorted to the most negative supply (i.e., GND or a voltage source close to, but below GND).

Condition (c) states V_{DD} and V_{SS} power supplies can be shut off.

In all cases, GND is understood to be 0 V, and the power-supply voltages should never exceed the absolute maximum ratings.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/ Ball Finish	MSL Peak Temp (3)	Samples (Requires Login)
SN75LPE185DWR	ACTIVE	SOIC	DW	24	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	Purchase Samples
SN75LPE185DWRE4	ACTIVE	SOIC	DW	24	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	Purchase Samples
SN75LPE185DWRG4	ACTIVE	SOIC	DW	24	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	Purchase Samples
SN75LPE185NT	ACTIVE	PDIP	NT	24	15	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	Purchase Samples
SN75LPE185NTE4	ACTIVE	PDIP	NT	24	15	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	Purchase Samples

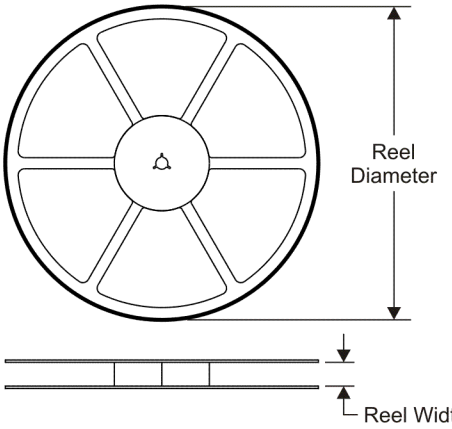
(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

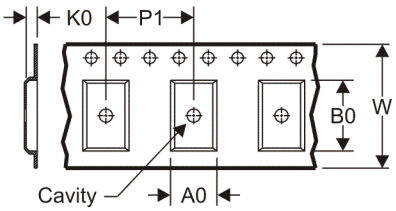
(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

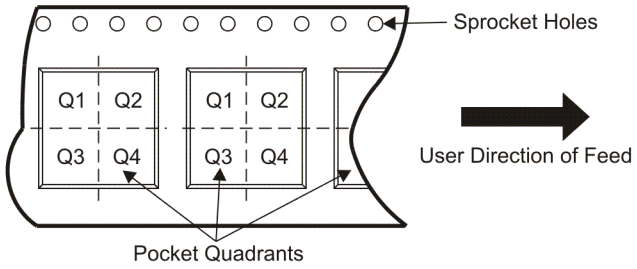


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

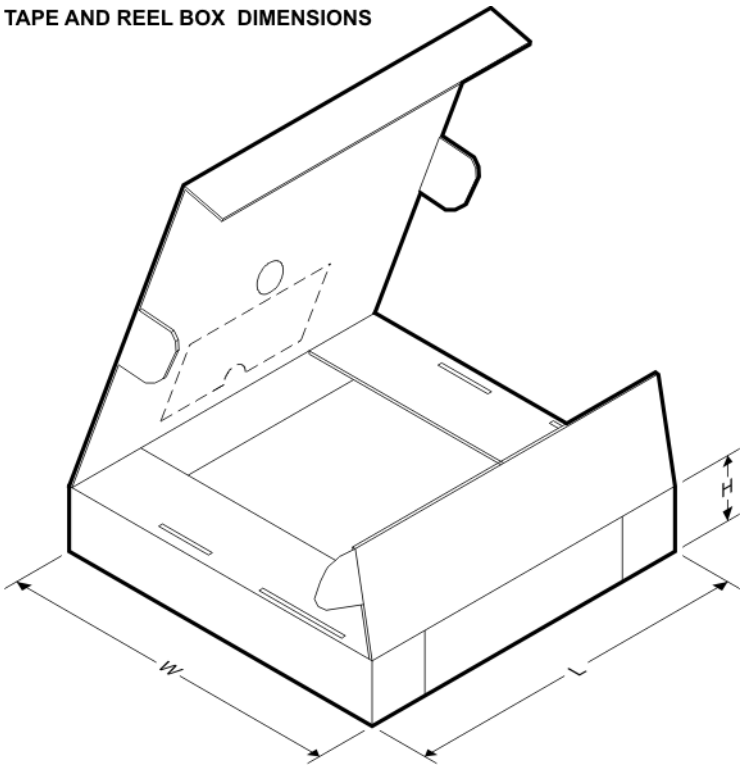
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN75LPE185DWR	SOIC	DW	24	2000	330.0	24.4	10.75	15.7	2.7	12.0	24.0	Q1

TAPE AND REEL BOX DIMENSIONS

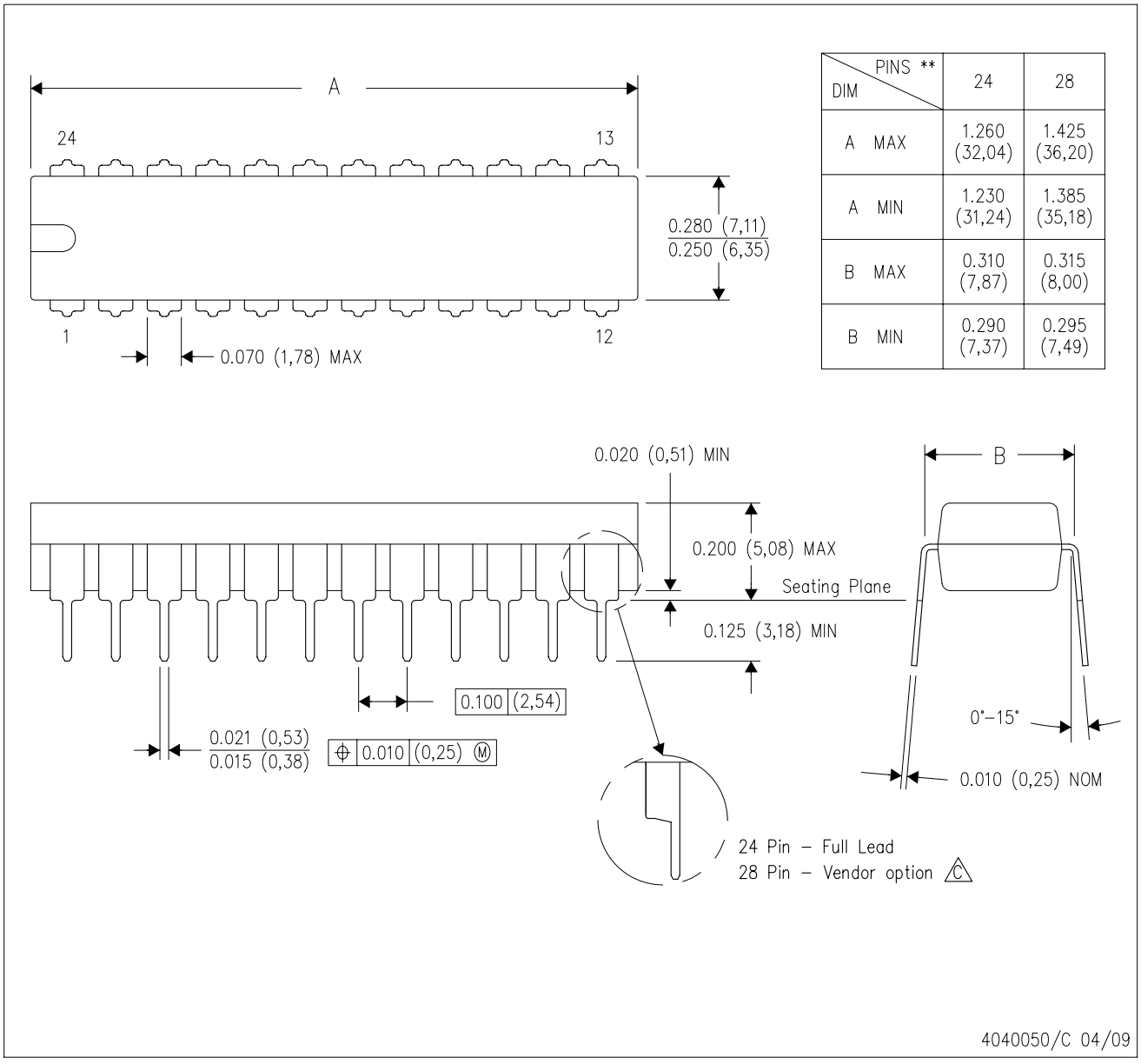


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN75LPE185DWR	SOIC	DW	24	2000	346.0	346.0	41.0

NT (R–PDIP–T**) PLASTIC DUAL–IN–LINE PACKAGE

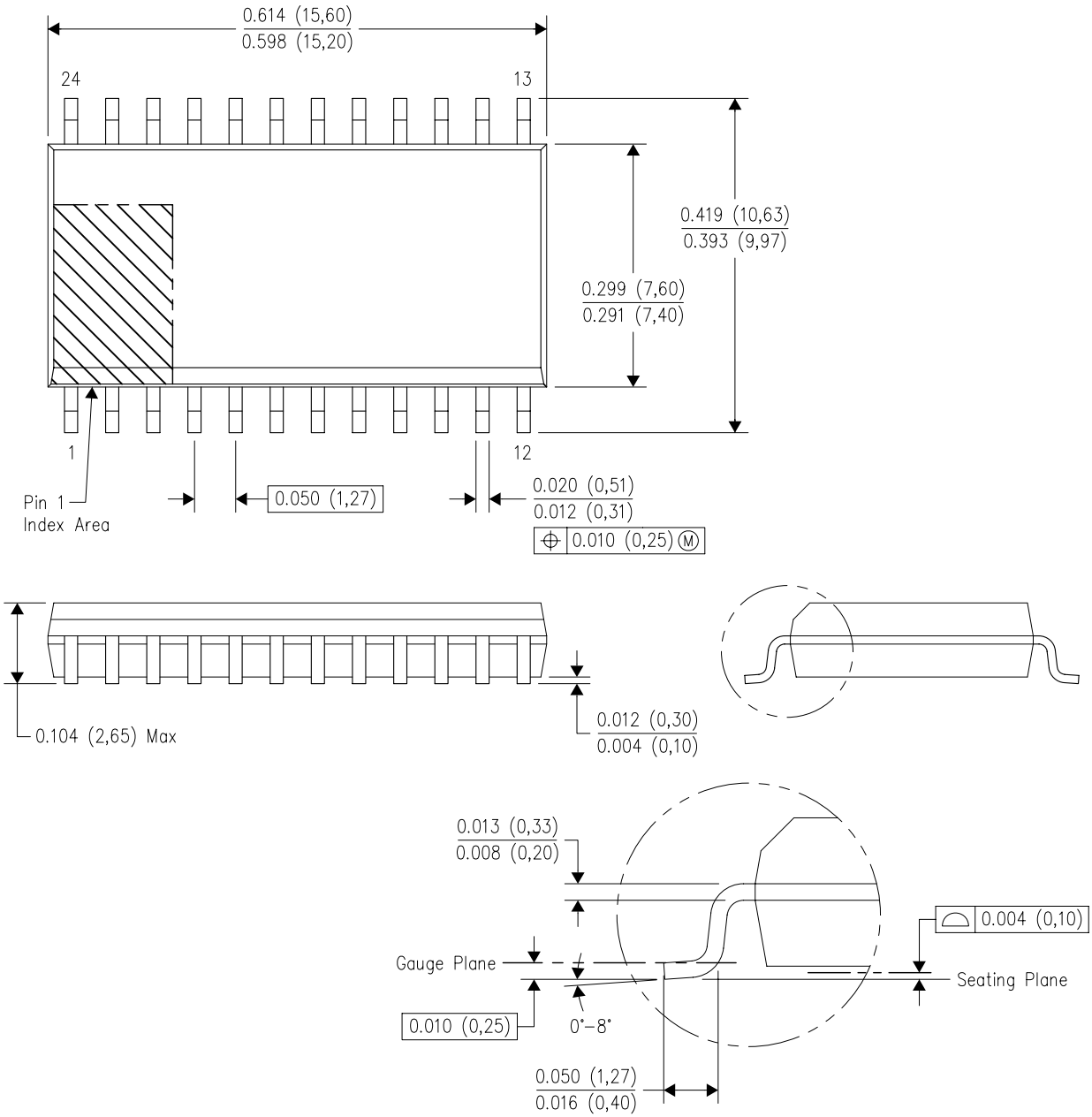
24 PINS SHOWN



DIM \ PINS **	24	28
A MAX	1.260 (32,04)	1.425 (36,20)
A MIN	1.230 (31,24)	1.385 (35,18)
B MAX	0.310 (7,87)	0.315 (8,00)
B MIN	0.290 (7,37)	0.295 (7,49)

NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. The 28 pin end lead shoulder width is a vendor option, either half or full width.

DW (R–PDSO–G24) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in inches (millimeters). Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
D. Falls within JEDEC MS–013 variation AD.

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