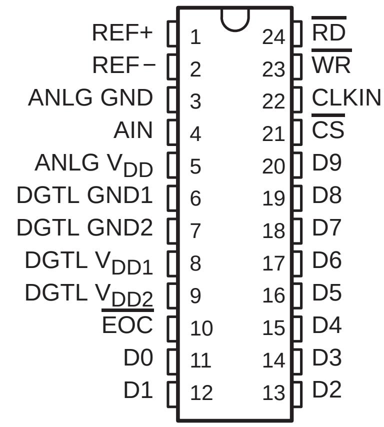
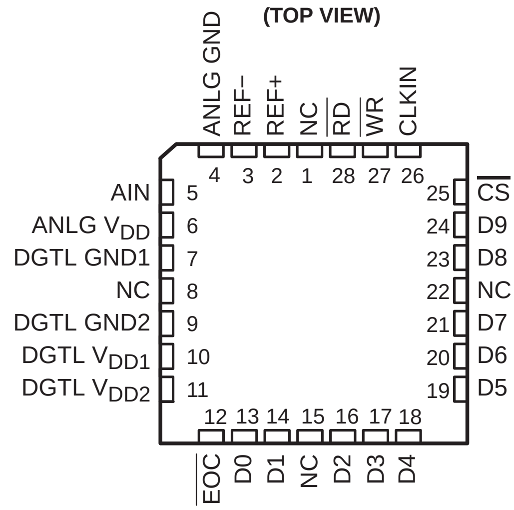
- **Power Dissipation . . . 40 mW Max**
- **Advanced LinEPIC™ Single-Poly Process Provides Close Capacitor Matching for Better Accuracy**
- **Fast Parallel Processing for DSP and μP Interface**
- **Either External or Internal Clock Can Be Used**
- **Conversion Time . . . 6 μs**
- **Total Unadjusted Error . . . ±1 LSB Max**
- **CMOS Technology**

J† OR DW PACKAGE
(TOP VIEW)



† Refer to the mechanical data for the JW package.

FK OR FN PACKAGE
(TOP VIEW)



NC − No internal connection

description

The TLC1550x and TLC1551 are data acquisition analog-to-digital converters (ADCs) using a 10-bit, switched-capacitor, successive-approximation network. A high-speed, 3-state parallel port directly interfaces to a digital signal processor (DSP) or microprocessor (μP) system data bus. D0 through D9 are the digital output terminals with D0 being the least significant bit (LSB). Separate power terminals for the analog and digital portions minimize noise pickup in the supply leads. Additionally, the digital power is divided into two parts to separate the lower current logic from the higher current bus drivers. An external clock can be applied to CLKIN to override the internal system clock if desired.

The TLC1550I and TLC1551I are characterized for operation from −40°C to 85°C. The TLC1550M is characterized over the full military range of −55°C to 125°C.

AVAILABLE OPTIONS

T_A	PACKAGE			
	CERAMIC CHIP CARRIER (FK)	PLASTIC CHIP CARRIER (FN)	CERAMIC DIP (J)	SOIC (DW)
−40°C to 85°C	—	TLC1550IFN TLC1551IFN	—	TLC1550IDW TLC1551IDW
−55°C to 125°C	TLC1550MFK	—	TLC1550MJ	—

This device contains circuits to protect its inputs and outputs against damage due to high static voltages or electrostatic fields. These circuits have been qualified to protect this device against electrostatic discharges (ESD) of up to 2 kV according to MIL-STD-883C, Method 3015; however, it is advised that precautions be taken to avoid application of any voltage higher than maximum-rated voltages to these high-impedance circuits. During storage or handling, the device leads should be shorted together or the device should be placed in conductive foam. In a circuit, unused inputs should always be connected to an appropriated logic voltage level, preferably either V_{CC} or ground.

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

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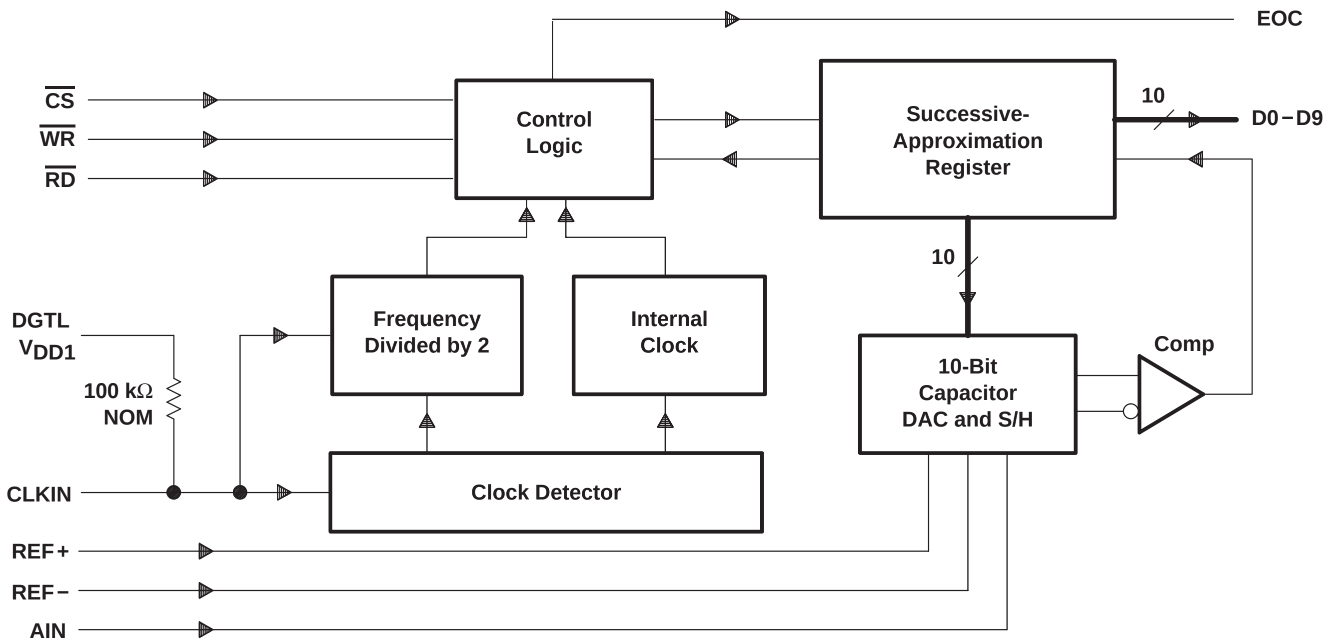
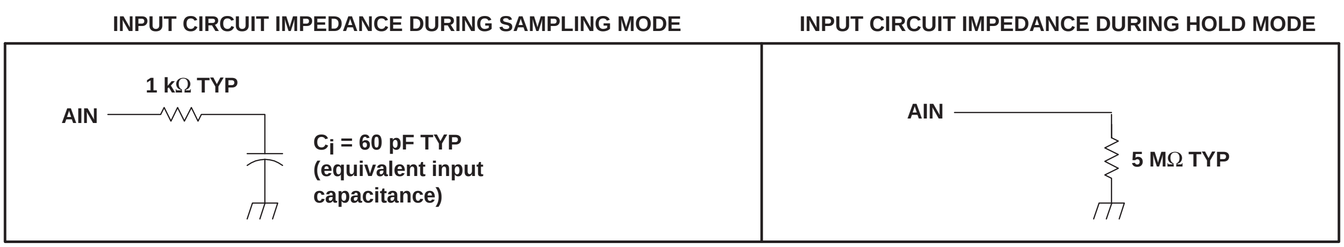
functional block diagram



typical equivalent inputs



Terminal Functions

TERMINAL NAME	NO.†	NO.‡	DESCRIPTION
ANLG GND	4	3	Analog ground. The reference point for the voltage applied on terminals ANLG V_{DD}, AIN, REF+, and REF−.
AIN	5	4	Analog voltage input. The voltage applied to AIN is converted to the equivalent digital output.
ANLG V_{DD}	6	5	Analog positive power supply voltage. The voltage applied to this terminal is designated V_{DD3}.
CLKIN	26	22	Clock input. CLKIN is used for external clocking instead of using the internal system clock. It usually takes a few microseconds before the internal clock is disabled. To use the internal clock, CLKIN should be tied high or left unconnected.
$\overline{CS}$	25	21	Chip-select. $\overline{CS}$ must be low for $\overline{RD}$ or $\overline{WR}$ to be recognized by the A/D converter.
D0	13	11	Data bus output. D0 is bit 1 (LSB).
D1	14	12	Data bus output. D1 is bit 2.
D2	16	13	Data bus output. D2 is bit 3.
D3	17	14	Data bus output. D3 is bit 4.
D4	18	15	Data bus output. D4 is bit 5.
D5	19	16	Data bus output. D5 is bit 6.
D6	20	17	Data bus output. D6 is bit 7.
D7	21	18	Data bus output. D7 is bit 8.
D8	23	19	Data bus output. D8 is bit 9.
D9	24	20	Data bus output. D9 is bit 10 (MSB).
DGTL GND1	7	6	Digital ground 1. The ground for power supply DGTL V_{DD1} and is the substrate connection
DGTL GND2	9	7	Digital ground 2. The ground for power supply DGTL V_{DD2}
DGTL V_{DD1}	10	8	Digital positive power-supply voltage 1. DGTL V_{DD1} supplies the logic. The voltage applied to DGTL V_{DD1} is designated V_{DD1}.
DGTL V_{DD2}	11	9	Digital positive power-supply voltage 2. DGTL V_{DD2} supplies only the higher-current output buffers. The voltage applied to DGTL V_{DD2} is designated V_{DD2}.
$\overline{EOC}$	12	10	End-of-conversion. $\overline{EOC}$ goes low indicating that conversion is complete and the results have been transferred to the output latch. $\overline{EOC}$ can be connected to the µP- or DSP-interrupt terminal or can be continuously polled.
$\overline{RD}$	28	24	Read input. When $\overline{CS}$ is low and $\overline{RD}$ is taken low, the data is placed on the data bus from the output latch. The output latch stores the conversion results at the most recent negative edge of $\overline{EOC}$. The falling edge of $\overline{RD}$ resets $\overline{EOC}$ to a high within the $t_{d(EOC)}$ specifications.
REF+	2	1	Positive voltage-reference input. Any analog input that is greater than or equal to the voltage on REF+ converts to 1111111111. Analog input voltages between REF+ and REF− convert to the appropriate result in a ratiometric manner.
REF−	3	2	Negative voltage reference input. Any analog input that is less than or equal to the voltage on REF− converts to 0000000000.
$\overline{WR}$	27	23	Write input. When $\overline{CS}$ is low, conversion is started on the rising edge of $\overline{WR}$. On this rising edge, the ADC holds the analog input until conversion is completed. Before and after the conversion period, which is given by t_{conv}, the ADC remains in the sampling mode.

† Terminal numbers for FK and FN packages.
‡ Terminal numbers for J, DW, and NW packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{DD1}, V_{DD2}, and V_{DD3} (see Note 1) . . . . . 6.5 V
Input voltage range, V_I (any input) . . . . . −0.3 V to V_{DD} + 0.3 V
Output voltage range, V_O . . . . . −0.3 V to V_{DD} + 0.3 V
Peak input current (any digital input) . . . . . ±10 mA
Peak total input current (all inputs) . . . . . ±30 mA
Operating free-air temperature range, T_A: TLC1550I, TLC1551I . . . . . −40°C to 85°C
TLC1550M . . . . . −55°C to 125°C
Storage temperature range, T_{stg} . . . . . −65°C to 150°C
Case temperature for 10 seconds: FK or FN package . . . . . 260°C
Lead temperature 1,6 mm (1/16 inch) from the case for 10 seconds: J or NW package . . . . . 260°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: V_{DD1} is the voltage measured at DGTL V_{DD1} with respect to DGND1. V_{DD2} is the voltage measured at DGTL V_{DD2} with respect to the DGND2. V_{DD3} is the voltage measured at ANLG V_{DD} with respect to AGND. For these specifications, all ground terminals are tied together (and represent 0 V). When V_{DD1}, V_{DD2}, and V_{DD3} are equal, they are referred to simply as V_{DD}.

recommended operating conditions

		MIN	NOM	MAX	UNIT
Supply voltage, V_{DD1}, V_{DD2}, V_{DD3}		4.75	5	5.5	V
Positive reference voltage, V_{REF+} (see Note 2)			V_{DD3}		V
Negative reference voltage, V_{REF-} (see Note 2)			0		V
Differential reference voltage, $V_{REF+} - V_{REF-}$ (see Note 2)				V_{DD3}	V
Analog input voltage range		0		V_{DD3}	V
High-level control input voltage, V_{IH}		2			V
Low-level control input voltage, V_{IL}				0.8	V
Input clock frequency, $f_{(CLKIN)}$		0.5		7.8	MHz
Setup time, $\overline{CS}$ low before $\overline{WR}$ or $\overline{RD}$ goes low, $t_{su(CS)}$		0			ns
Hold time, $\overline{CS}$ low after $\overline{WR}$ or $\overline{RD}$ goes high, $t_{h(CS)}$		0			ns
$\overline{WR}$ or $\overline{RD}$ pulse duration, $t_{w(WR)}$		50			ns
Input clock low pulse duration, $t_{w(L-CLKIN)}$		40% of period		80% of period	
Operating free-air temperature, T_A	TLC155xI	−40		85	°C
	TLC1550M	−55		125	°C

NOTE 2: Analog input voltages greater than that applied to REF+ convert to all 1s (1111111111), while input voltages less than that applied to REF− convert to all 0s (0000000000). The total unadjusted error may increase as this differential voltage falls below 4.75 V.

electrical characteristics over recommended operating free-air temperature range, $V_{DD} = V_{REF+} = 4.75$ V to 5.5 V and $V_{REF-} = 0$ (unless otherwise noted)

PARAMETER			TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{OH}	High-level output voltage		V_{DD} = 4.75 V,	I_{OH} = −360 µA	2.4			V
V_{OL}	Low-level output voltage		V_{DD} = 4.75 V, I_{OL} = 2.4 mA	T_A = 25°C			0.4	V
				T_A = −55°C to 125°C			0.5	
I_{OZ}	Off-state (high-impedance-state) output current		$V_O = V_{DD}$,	$\overline{CS}$ and $\overline{RD}$ at V_{DD}			10	µA
			V_O = 0,	$\overline{CS}$ and $\overline{RD}$ at V_{DD}			−10	
I_{IH}	High-level input current		$V_I = V_{DD}$			0.005	2.5	µA
I_{IL}	Low-level input current (except CLKIN)		V_I = 0		−2.5	−0.005		µA
I_{IL}	Low-level input current (CLKIN)				−50	−50		µA
I_{OS}	Short-circuit output current		V_O = 5 V,	T_A = 25°C	7	14		mA
			V_O = 0,	T_A = 25°C		−12	−6	
$I_{(DD)}$	Operating supply current		$\overline{CS}$ low and $\overline{RD}$ high			2	8	mA
C_i	Input capacitance	Analog inputs	See typical equivalent inputs TLC1550/1I			60	90*	pF
		Digital inputs				5	15*	

* On products compliant to MIL-STD-883, Class B, this parameter is not production tested.
† All typical values are at V_{DD} = 5 V, T_A = 25°C.

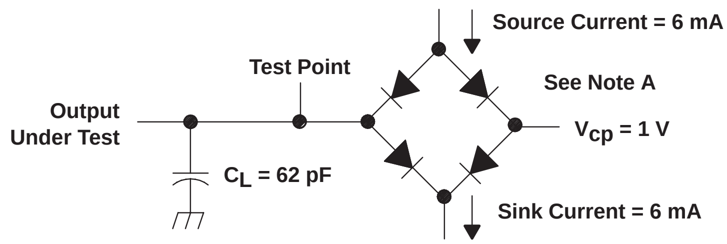
operating characteristics over recommended operating free-air temperature range with internal clock and minimum sampling time of 4 µs, $V_{DD} = V_{REF+} = 5$ V and $V_{REF-} = 0$ (unless otherwise noted)

PARAMETER			TEST CONDITIONS	T_A†	MIN	TYP‡	MAX	UNIT
E_L	Linearity error	TLC1550I	See Note 3	Full range			±0.5	LSB
		TLC1551I		Full range			±1	
		TLC1550M		25°C			±0.5	
				Full range			±1	
E_{ZS}	Zero-scale error	TLC1550I	See Notes 2 and 4	Full range			±0.5	LSB
		TLC1551I		Full range			±1	
		TLC1550M		25°C			±0.5	
				Full range			±1	
E_{FS}	Full-scale error	TLC1550I	See Notes 2 and 4	Full range			±0.5	LSB
		TLC1551I		Full range			±1	
		TLC1550M		25°C			±0.5	
				Full range			±1	
	Total unadjusted error	TLC1550I	See Note 5	Full range			±0.5	LSB
		TLC1551I		Full range			±1	
		TLC1550M		25°C			±1	
t_c	Conversion time		$f_{clock(external)}$ = 4.2 MHz or internal clock				6	µs
$t_{a(D)}$	Data access time after $\overline{RD}$ goes low		See Figure 3				35	ns
$t_{v(D)}$	Data valid time after $\overline{RD}$ goes high				5			ns
$t_{dis(D)}$	Disable time, delay time from $\overline{RD}$ high to high impedance						30	ns
$t_{d(EOC)}$	Delay time, $\overline{RD}$ low to $\overline{EOC}$ high				0	15		ns

† Full range is −40°C to 85°C for the TL155xI devices and −55°C to 125°C for the TLC1550M.
‡ All typical values are at V_{DD} = 5 V, T_A = 25°C.

NOTES: 2. Analog input voltages greater than that applied to REF+ convert to all 1s (1111111111), while input voltages less than that applied to REF− convert to all 0s (0000000000). The total unadjusted error may increase as this differential voltage falls below 4.75 V.
3. Linearity error is the difference between the actual analog value at the transition between any two adjacent steps and its ideal value after zero-scale error and full-scale error have been removed.
4. Zero-scale error is the difference between the actual mid-step value and the nominal mid-step value at specified zero scale. Full-scale error is the difference between the actual mid-step value and the nominal mid-step value at specified full scale.
5. Total unadjusted error is the difference between the actual analog value at the transition between any two adjacent steps and its ideal value. It includes contributions from zero-scale error, full-scale error, and linearity error.

PARAMETER MEASUREMENT INFORMATION



V_{cp} = voltage commutation point for switching between source and sink currents

NOTE A: Equivalent load circuit of the Teradyne A500 tester for timing parameter measurement

Figure 1. Test Load Circuit

APPLICATION INFORMATION

simplified analog input analysis

Using the circuit in Figure 2, the time required to charge the analog input capacitance from 0 to V_S within 1/2 LSB can be derived as follows:

The capacitance charging voltage is given by

$$V_C = V_S\left(1 - e^{-t_c/R_t C_i}\right) \quad (1)$$

Where:

$R_t = R_s + r_i$

The final voltage to 1/2 LSB is given by

$$V_C\,(1/2\ \text{LSB}) = V_S - (V_S/1024) \quad (2)$$

Equating equation 1 to equation 2 and solving for time t_c gives

$$V_S - \left(V_S/512\right) = V_S\left(1 - e^{-t_c/R_t C_i}\right) \quad (3)$$

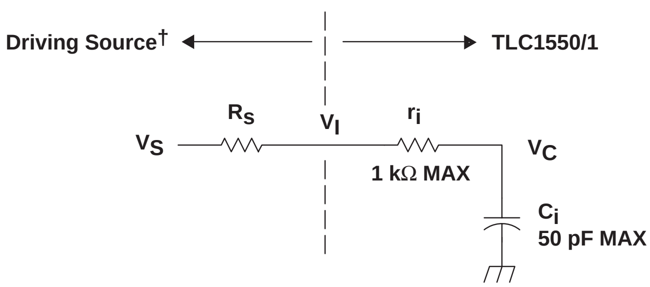
and

$$t_c\,(1/2\ \text{LSB}) = R_t \times C_i \times \ln(1024) \quad (4)$$

Therefore, with the values given, the time for the analog input signal to settle is

$$t_c\,(1/2\ \text{LSB}) = (R_s + 1\ \text{k}\Omega) \times 60\ \text{pF} \times \ln(1024) \quad (5)$$

This time must be less than the converter sample time shown in the timing diagrams.



V_I = Input voltage at AIN
V_S = External driving source voltage
R_s = Source resistance
r_i = Input resistance
C_i = Input capacitance

† Driving source requirements:
- Noise and distortion for the source must be equivalent to the resolution of the converter.
- R_s must be real at the input frequency.

Figure 2. Input Circuit Including the Driving Source

PRINCIPLES OF OPERATION

The operating sequence for complete data acquisition is shown in Figure 3. Processors can address the TLC1550 and TLC1551 as an external memory device by simply connecting the address lines to a decoder and the decoder output to $\overline{\text{CS}}$. Like other peripheral devices, the write ($\overline{\text{WR}}$) and read ($\overline{\text{RD}}$) input signals are valid only when $\overline{\text{CS}}$ is low. Once $\overline{\text{CS}}$ is low, the onboard system clock permits the conversion to begin with a simple write command and the converted data to be presented to the data bus with a simple read command. The device remains in a sampling (track) mode from the rising edge of $\overline{\text{EOC}}$ until conversion begins with the rising edge of $\overline{\text{WR}}$, which initiates the hold mode. After the hold mode begins, the clock controls the conversion automatically. When the conversion is complete, the end-of-conversion ($\overline{\text{EOC}}$) signal goes low indicating that the digital data has been transferred to the output latch. Lowering $\overline{\text{CS}}$ and $\overline{\text{RD}}$ then resets $\overline{\text{EOC}}$ and transfers the data to the data bus for the processor read cycle.

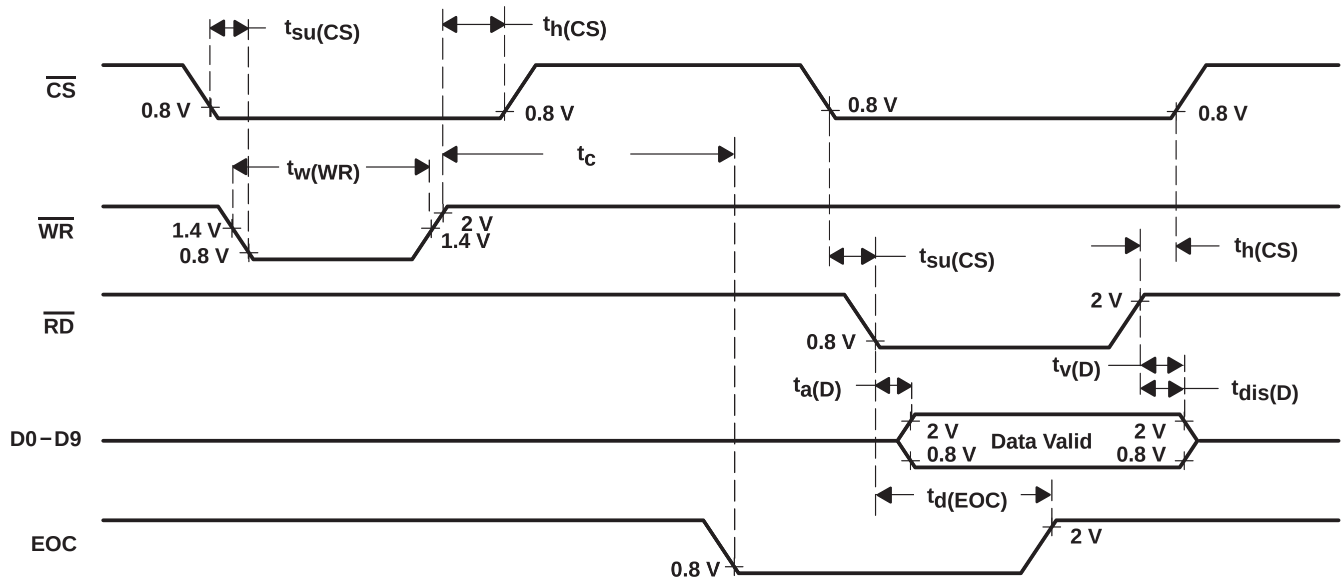


Figure 3. TLC1550 or TLC1551 Operating Sequence

PACKAGING INFORMATION

Orderable Device	Status [1]	Package Type	Package Drawing	Pins	Package Qty	Eco Plan [2]	Lead/Ball Finish	MSL Peak Temp [3]
TLC1550IDW	ACTIVE	SOIC	DW	24	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TLC1550IDWG4	ACTIVE	SOIC	DW	24	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TLC1550IDWR	ACTIVE	SOIC	DW	24	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TLC1550IDWRG4	ACTIVE	SOIC	DW	24	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TLC1550IFN	ACTIVE	PLCC	FN	28	37	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TLC1550IFNG4	ACTIVE	PLCC	FN	28	37	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TLC1550IFNR	ACTIVE	PLCC	FN	28	750	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TLC1550INW	OBSOLETE	PDIP	NW	24		TBD	Call TI	Call TI
TLC1550MFKB	OBSOLETE	LCCC	FK	28		TBD	Call TI	Call TI
TLC1550MJ	OBSOLETE	CDIP	J	24		TBD	Call TI	Call TI
TLC1550MJB	OBSOLETE	CDIP	J	24		TBD	Call TI	Call TI
TLC1551IDW	ACTIVE	SOIC	DW	24	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TLC1551IDWG4	ACTIVE	SOIC	DW	24	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TLC1551IDWR	ACTIVE	SOIC	DW	24	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TLC1551IDWRG4	ACTIVE	SOIC	DW	24	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TLC1551IFN	ACTIVE	PLCC	FN	28	37	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TLC1551IFNG4	ACTIVE	PLCC	FN	28	37	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM

[1] The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

[2] Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

[3] MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder

temperature.

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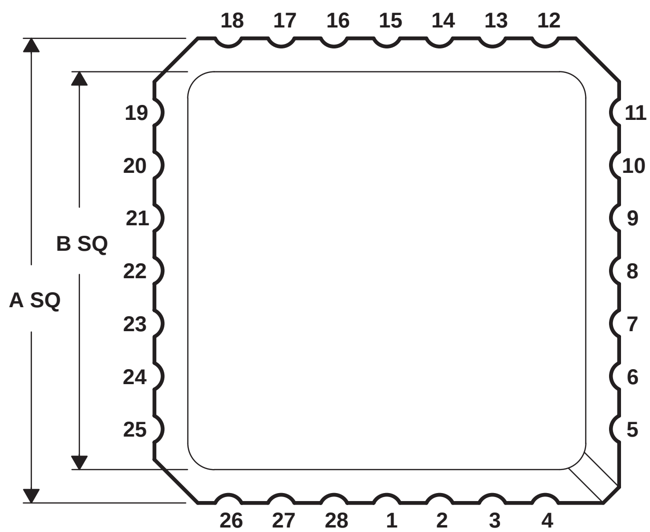
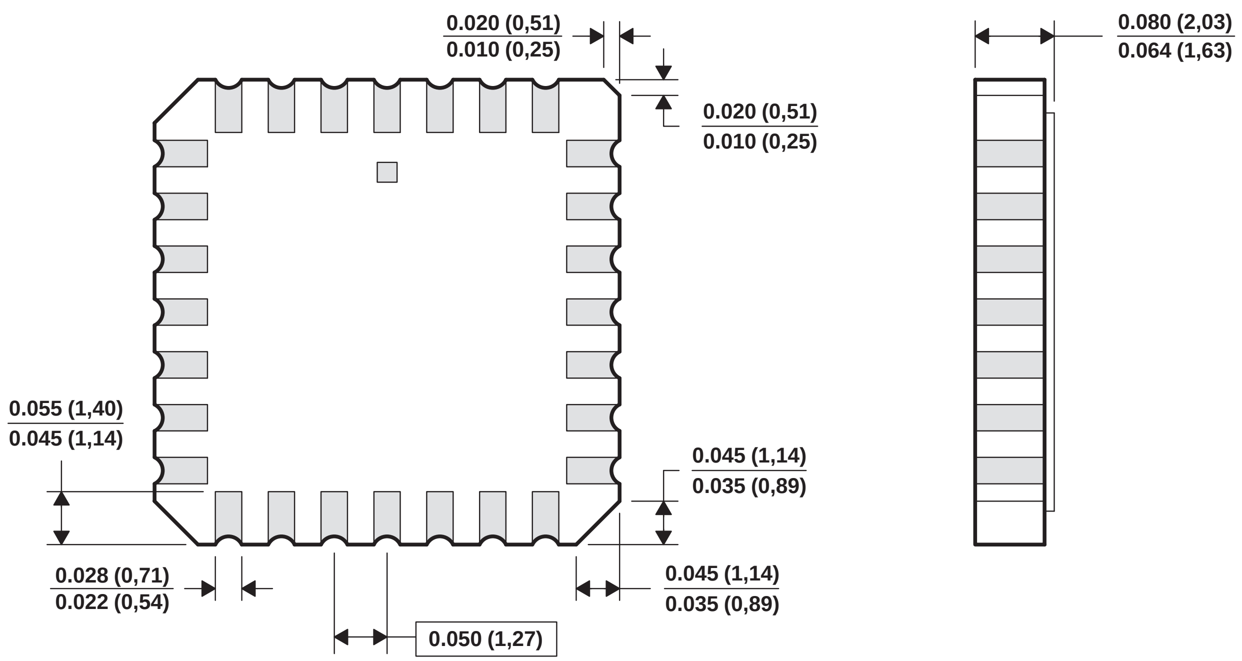
FK (S-CQCC-N)** **LEADLESS CERAMIC CHIP CARRIER**

28 TERMINAL SHOWN



NO. OF TERMINALS **	A		B	
	MIN	MAX	MIN	MAX
20	0.342 (8,69)	0.358 (9,09)	0.307 (7,80)	0.358 (9,09)
28	0.442 (11,23)	0.458 (11,63)	0.406 (10,31)	0.458 (11,63)
44	0.640 (16,26)	0.660 (16,76)	0.495 (12,58)	0.560 (14,22)
52	0.739 (18,78)	0.761 (19,32)	0.495 (12,58)	0.560 (14,22)
68	0.938 (23,83)	0.962 (24,43)	0.850 (21,6)	0.858 (21,8)
84	1.141 (28,99)	1.165 (29,59)	1.047 (26,6)	1.063 (27,0)



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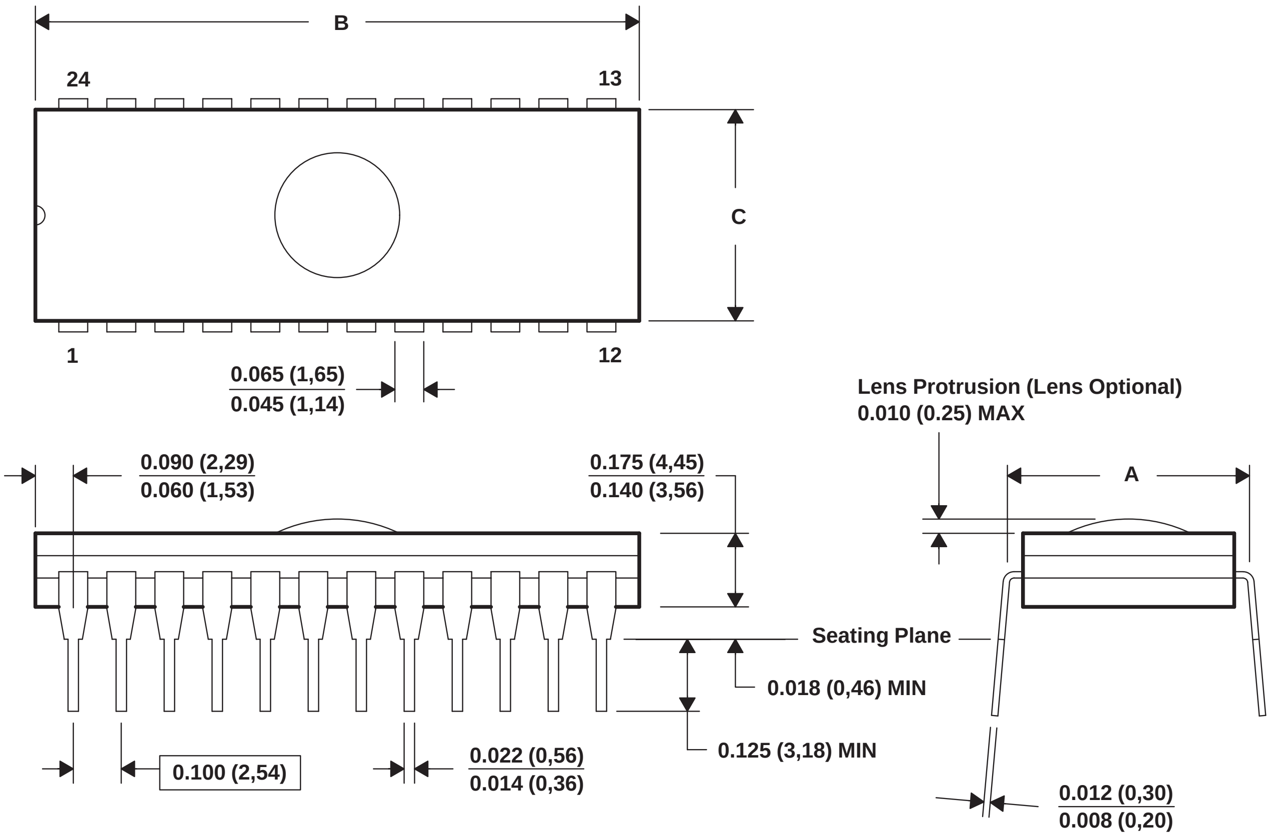
NOTES:
- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. This package can be hermetically sealed with a metal lid.
- D. The terminals are gold plated.
- E. Falls within JEDEC MS-004

J (R-GDIP-T)** **CERAMIC DUAL-IN-LINE PACKAGE**

24 PINS SHOWN

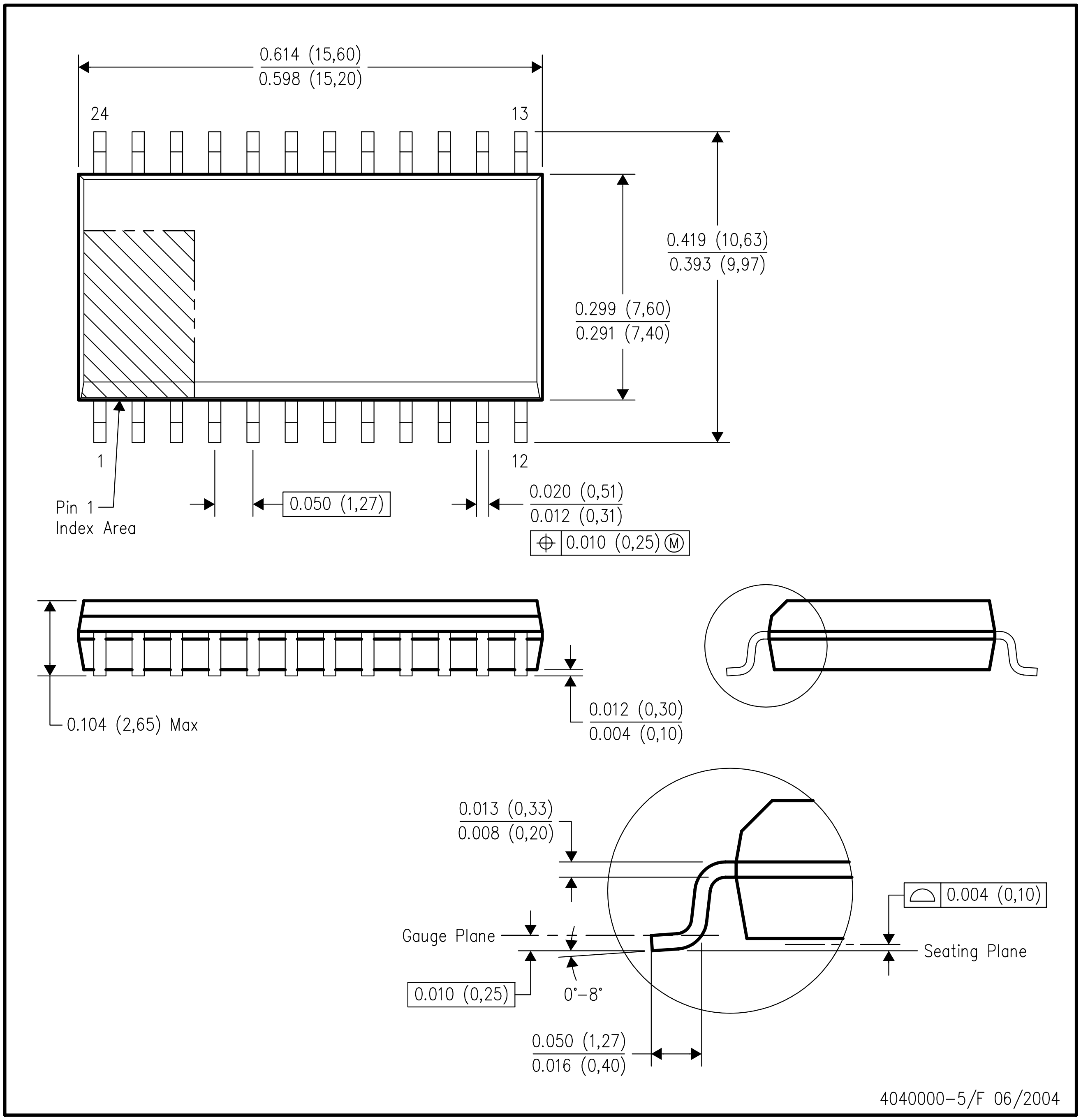


DIM \ PINS **		24		28		32		40	
		NARR	WIDE	NARR	WIDE	NARR	WIDE	NARR	WIDE
”A”	MAX	0.624(15,85)	0.624(15,85)	0.624(15,85)	0.624(15,85)	0.624(15,85)	0.624(15,85)	0.624(15,85)	0.624(15,85)
	MIN	0.590(14,99)	0.590(14,99)	0.590(14,99)	0.590(14,99)	0.590(14,99)	0.590(14,99)	0.590(14,99)	0.590(14,99)
”B”	MAX	1.265(32,13)	1.265(32,13)	1.465(37,21)	1.465(37,21)	1.668(42,37)	1.668(42,37)	2.068(52,53)	2.068(52,53)
	MIN	1.235(31,37)	1.235(31,37)	1.435(36,45)	1.435(36,45)	1.632(41,45)	1.632(41,45)	2.032(51,61)	2.032(51,61)
”C”	MAX	0.541(13,74)	0.598(15,19)	0.541(13,74)	0.598(15,19)	0.541(13,74)	0.598(15,19)	0.541(13,74)	0.598(15,19)
	MIN	0.514(13,06)	0.571(14,50)	0.514(13,06)	0.571(14,50)	0.514(13,06)	0.571(14,50)	0.514(13,06)	0.571(14,50)

4040084/C 10/97

NOTES:
- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. Window (lens) added to this group of packages (24-, 28-, 32-, 40-pin).
- D. This package can be hermetically sealed with a ceramic lid using glass frit.
- E. Index point is provided on cap for terminal identification.

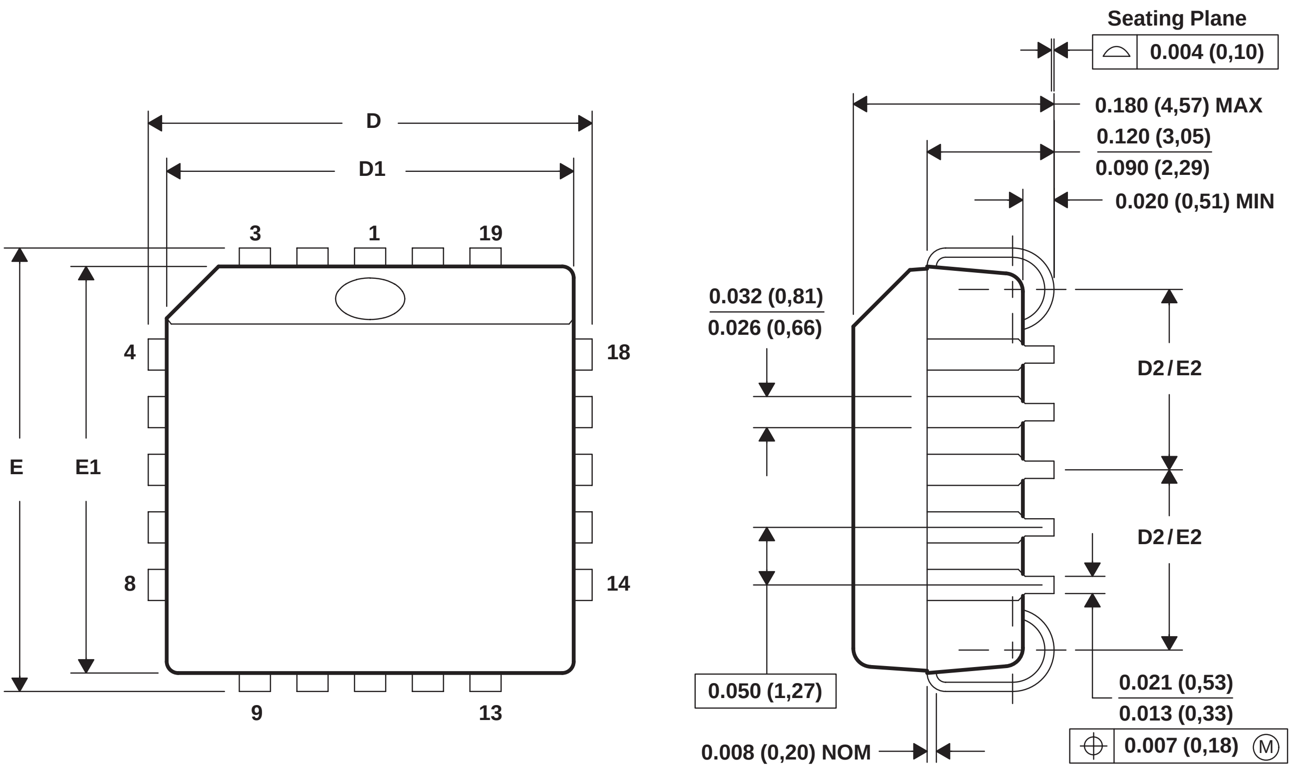
DW (R–PDSO–G24) PLASTIC SMALL–OUTLINE PACKAGE



NOTES:
- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
- D. Falls within JEDEC MS–013 variation AD.

FN (S-PQCC-J)** **PLASTIC J-LEADED CHIP CARRIER**

20 PIN SHOWN



NO. OF PINS **	D / E		D1 / E1		D2 / E2	
	MIN	MAX	MIN	MAX	MIN	MAX
20	0.385 (9,78)	0.395 (10,03)	0.350 (8,89)	0.356 (9,04)	0.141 (3,58)	0.169 (4,29)
28	0.485 (12,32)	0.495 (12,57)	0.450 (11,43)	0.456 (11,58)	0.191 (4,85)	0.219 (5,56)
44	0.685 (17,40)	0.695 (17,65)	0.650 (16,51)	0.656 (16,66)	0.291 (7,39)	0.319 (8,10)
52	0.785 (19,94)	0.795 (20,19)	0.750 (19,05)	0.756 (19,20)	0.341 (8,66)	0.369 (9,37)
68	0.985 (25,02)	0.995 (25,27)	0.950 (24,13)	0.958 (24,33)	0.441 (11,20)	0.469 (11,91)
84	1.185 (30,10)	1.195 (30,35)	1.150 (29,21)	1.158 (29,41)	0.541 (13,74)	0.569 (14,45)

4040005 / B 03/95

NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS-018