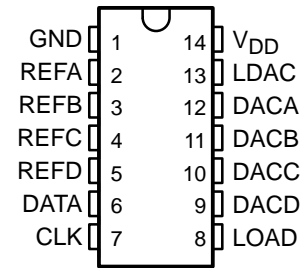


# TLC5620C, TLC5620I QUADRUPLE 8-BIT DIGITAL-TO-ANALOG CONVERTERS

SLAS081E – NOVEMBER 1994 – REVISED NOVEMBER 2001

- Four 8-Bit Voltage Output DACs
- 5-V Single-Supply Operation
- Serial Interface
- High-Impedance Reference Inputs
- Programmable 1 or 2 Times Output Range
- Simultaneous Update Facility
- Internal Power-On Reset
- Low-Power Consumption
- Half-Buffered Output

N OR D PACKAGE  
(TOP VIEW)



## applications

- Programmable Voltage Sources
- Digitally Controlled Amplifiers/Attenuators
- Mobile Communications
- Automatic Test Equipment
- Process Monitoring and Control
- Signal Synthesis

## description

The TLC5620C and TLC5620I are quadruple 8-bit voltage output digital-to-analog converters (DACs) with buffered reference inputs (high impedance). The DACs produce an output voltage that ranges between either one or two times the reference voltages and GND, and the DACs are monotonic. The device is simple to use, running from a single supply of 5 V. A power-on reset function is incorporated to ensure repeatable start-up conditions.

Digital control of the TLC5620C and TLC5620I are over a simple three-wire serial bus that is CMOS compatible and easily interfaced to all popular microprocessor and microcontroller devices. The 11-bit command word comprises eight bits of data, two DAC-select bits, and a range bit, the latter allowing selection between the times 1 or times 2 output range. The DAC registers are double buffered, allowing a complete set of new values to be written to the device, then all DAC outputs are updated simultaneously through control of LDAC. The digital inputs feature Schmitt triggers for high noise immunity.

The 14-terminal small-outline (D) package allows digital control of analog functions in space-critical applications. The TLC5620C is characterized for operation from 0°C to 70°C. The TLC5620I is characterized for operation from –40°C to 85°C. The TLC5620C and TLC5620I do not require external trimming.

### AVAILABLE OPTIONS

PACKAGE		
T <sub>A</sub>	SMALL OUTLINE (D)	PLASTIC DIP (N)
0°C to 70°C	TLC5620CD	TLC5620CN
–40°C to 85°C	TLC5620ID	TLC5620IN



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

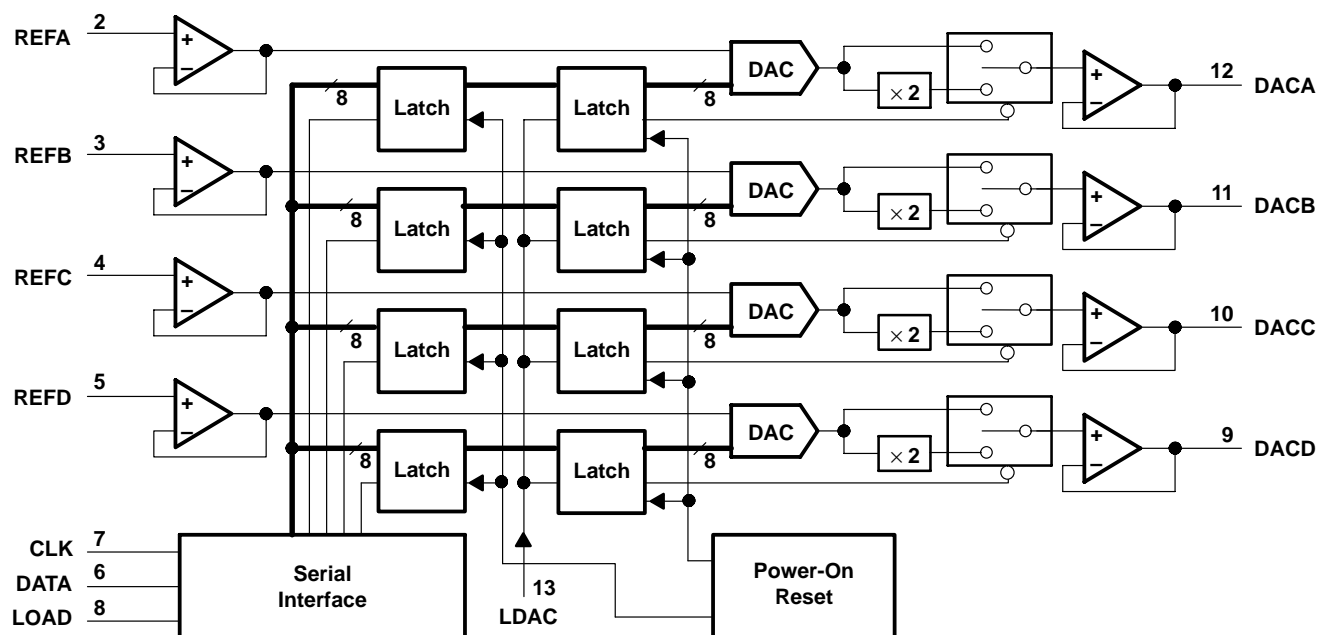
Copyright © 2001, Texas Instruments Incorporated

**TEXAS INSTRUMENTS**  
[www.BDITIC.com/TI](http://www.BDITIC.com/TI)  
POST OFFICE BOX 655303 • DALLAS, TEXAS 75266

# TLC5620C, TLC5620I QUADRUPLE 8-BIT DIGITAL-TO-ANALOG CONVERTERS

SLAS081E – NOVEMBER 1994 – REVISED NOVEMBER 2001

## functional block diagram



## Terminal Functions

TERMINAL NAME	NO.	I/O	DESCRIPTION
CLK	7	I	Serial interface clock. The input digital data is shifted into the serial interface register on the falling edge of the clock applied to the CLK terminal.
DACA	12	O	DAC A analog output
DACB	11	O	DAC B analog output
DACC	10	O	DAC C analog output
DACD	9	O	DAC D analog output
DATA	6	I	Serial interface digital data input. The digital code for the DAC is clocked into the serial interface register serially. Each data bit is clocked into the register on the falling edge of the clock signal.
GND	1	I	Ground return and reference terminal
LDAC	13	I	Load DAC. When the LDAC signal is high, no DAC output updates occur when the input digital data is read into the serial interface. The DAC outputs are only updated when LDAC is taken from high to low.
LOAD	8	I	Serial Interface load control. When LDAC is low, the falling edge of the LOAD signal latches the digital data into the output latch and immediately produces the analog voltage at the DAC output terminal.
REFA	2	I	Reference voltage input to DAC A. This voltage defines the output analog range.
REFB	3	I	Reference voltage input to DAC B. This voltage defines the output analog range.
REFC	4	I	Reference voltage input to DAC C. This voltage defines the output analog range.
REFD	5	I	Reference voltage input to DAC D. This voltage defines the output analog range.
VDD	14	I	Positive supply voltage

**detailed description**

The TLC5620 is implemented using four resistor-string DACs. The core of each DAC is a single resistor with 256 taps, corresponding to the 256 possible codes listed in Table 1. One end of each resistor string is connected to the GND terminal and the other end is fed from the output of the reference input buffer. Monotonicity is maintained by use of the resistor strings. Linearity depends upon the matching of the resistor elements and upon the performance of the output buffer. Since the inputs are buffered, the DACs always present a high-impedance load to the reference source.

Each DAC output is buffered by a configurable-gain output amplifier that can be programmed to times 1 or times 2 gain.

On power up, the DACs are reset to CODE 0.

Each output voltage is given by:

$$V_O(\text{DACA|B|C|D}) = \text{REF} \times \frac{\text{CODE}}{256} \times (1 + \text{RNG bit value})$$

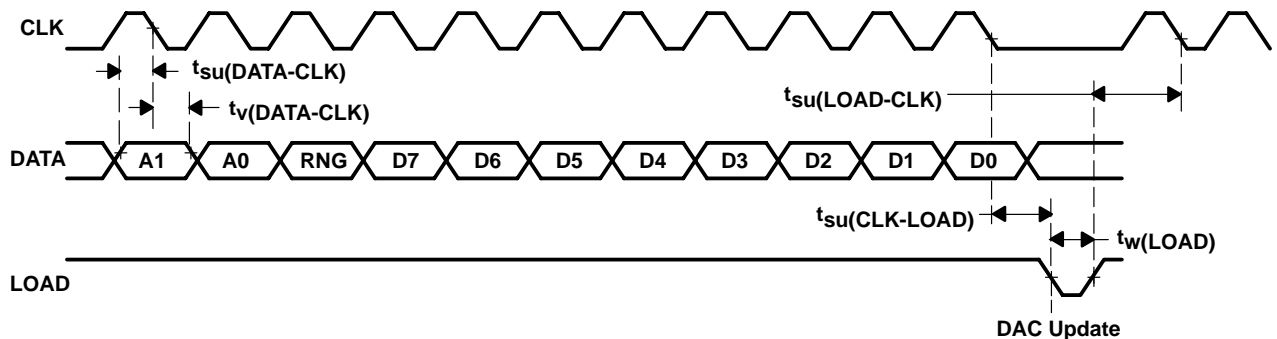
where CODE is in the range 0 to 255 and the range (RNG) bit is 0 or 1 within the serial control word.

**Table 1. Ideal Output Transfer**

D7	D6	D5	D4	D3	D2	D1	D0	OUTPUT VOLTAGE
0	0	0	0	0	0	0	0	GND
0	0	0	0	0	0	0	1	$(1/256) \times \text{REF} (1+\text{RNG})$
•	•	•	•	•	•	•	•	•
•	•	•	•	•	•	•	•	•
0	1	1	1	1	1	1	1	$(127/256) \times \text{REF} (1+\text{RNG})$
1	0	0	0	0	0	0	0	$(128/256) \times \text{REF} (1+\text{RNG})$
•	•	•	•	•	•	•	•	•
•	•	•	•	•	•	•	•	•
1	1	1	1	1	1	1	1	$(255/256) \times \text{REF} (1+\text{RNG})$

**data interface**

With LOAD high, data is clocked into the DATA terminal on each falling edge of CLK. Once all data bits have been clocked in, LOAD is pulsed low to transfer the data from the serial input register to the selected DAC as shown in Figure 1. When LDAC is low, the selected DAC output voltage is updated when LOAD goes low. When LDAC is high during serial programming, the new value is stored within the device and can be transferred to the DAC output at a later time by pulsing LDAC low as shown in Figure 2. Data is entered most significant bit (MSB) first. Data transfers using two 8-clock cycle periods are shown in Figures 3 and 4.



**Figure 1. LOAD-Controlled Update (LDAC = Low)**

# TLC5620C, TLC5620I QUADRUPLE 8-BIT DIGITAL-TO-ANALOG CONVERTERS

SLAS081E – NOVEMBER 1994 – REVISED NOVEMBER 2001

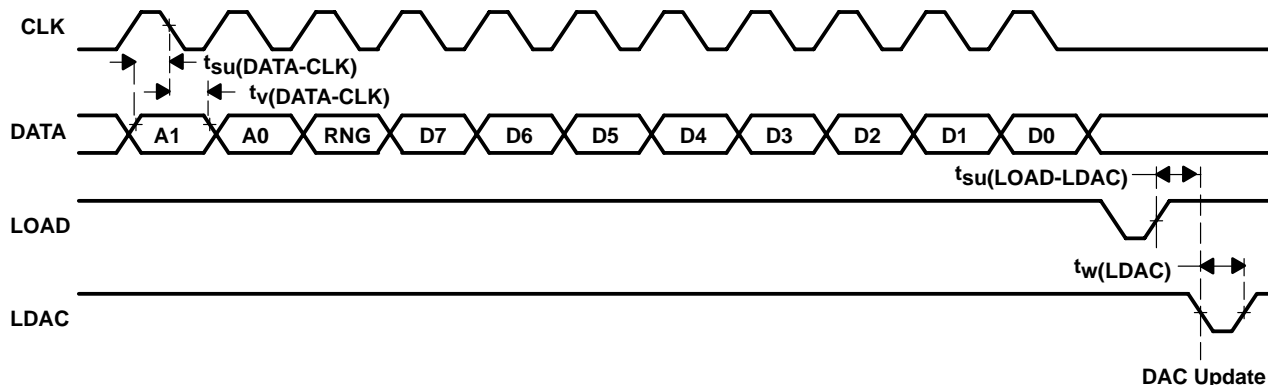


Figure 2. LDAC-Controlled Update

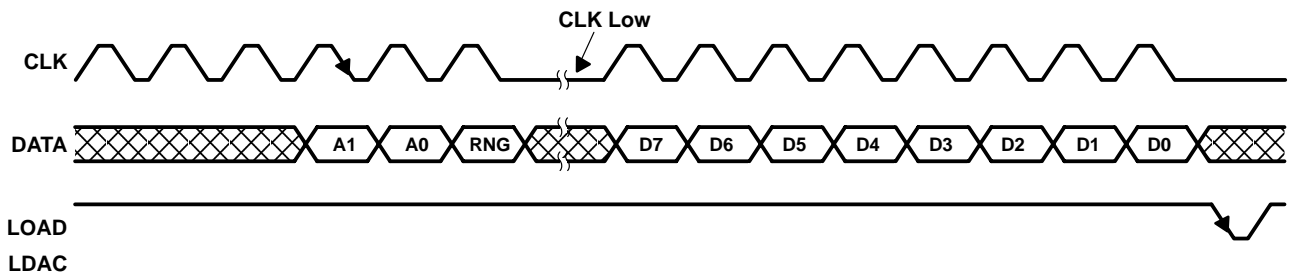


Figure 3. Load-Controlled Update Using 8-Bit Serial Word (LDAC = Low)

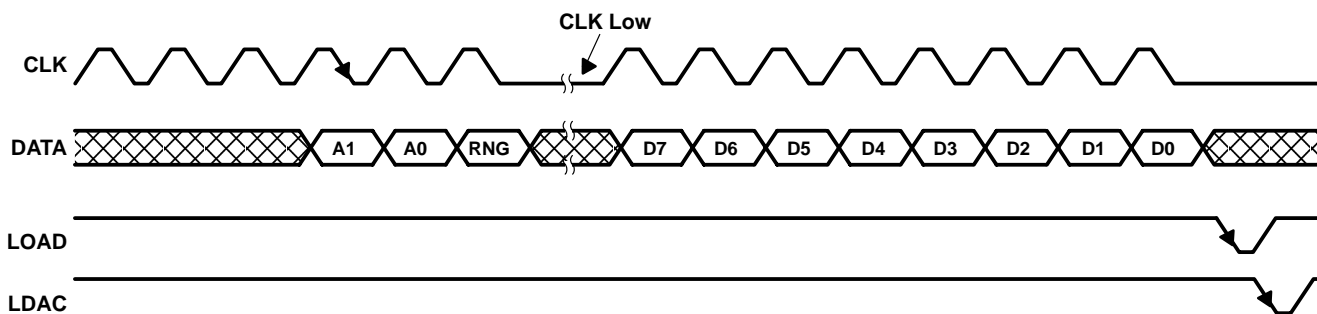


Figure 4. LDAC-Controlled Update Using 8-Bit Serial Word

Table 2 lists the A1 and A0 bits and the selection of the updated DACs. The RNG bit controls the DAC output range. When RNG = low, the output range is between the applied reference voltage and GND, and when RNG = high, the range is between twice the applied reference voltage and GND.

Table 2. Serial Input Decode

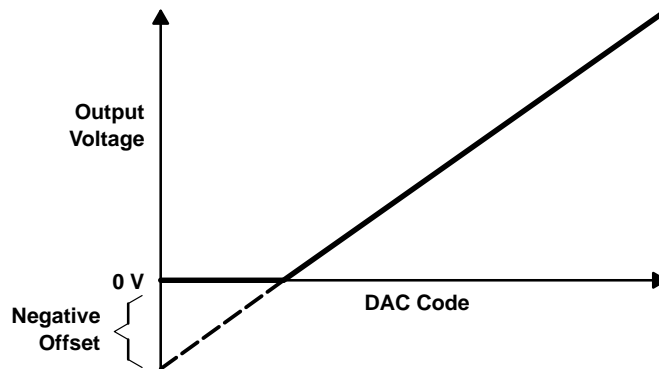
A1	A0	DAC UPDATED
0	0	DACA
0	1	DACB
1	0	DACC
1	1	DACD

**linearity, offset, and gain error using single-end supplies**

When an amplifier is operated from a single supply, the voltage offset can still be either positive or negative. With a positive offset voltage, the output voltage changes on the first code change. With a negative offset the output voltage may not change with the first code depending on the magnitude of the offset voltage.

The output amplifier attempts to drive the output to a negative voltage. However, because the most negative supply rail is ground, the output cannot drive below ground and clamps the output at 0 V.

The output voltage then remains at zero until the input code value produces a sufficient positive output voltage to overcome the negative offset voltage, resulting in the transfer function shown in Figure 5.



**Figure 5. Effect of Negative Offset (Single Supply)**

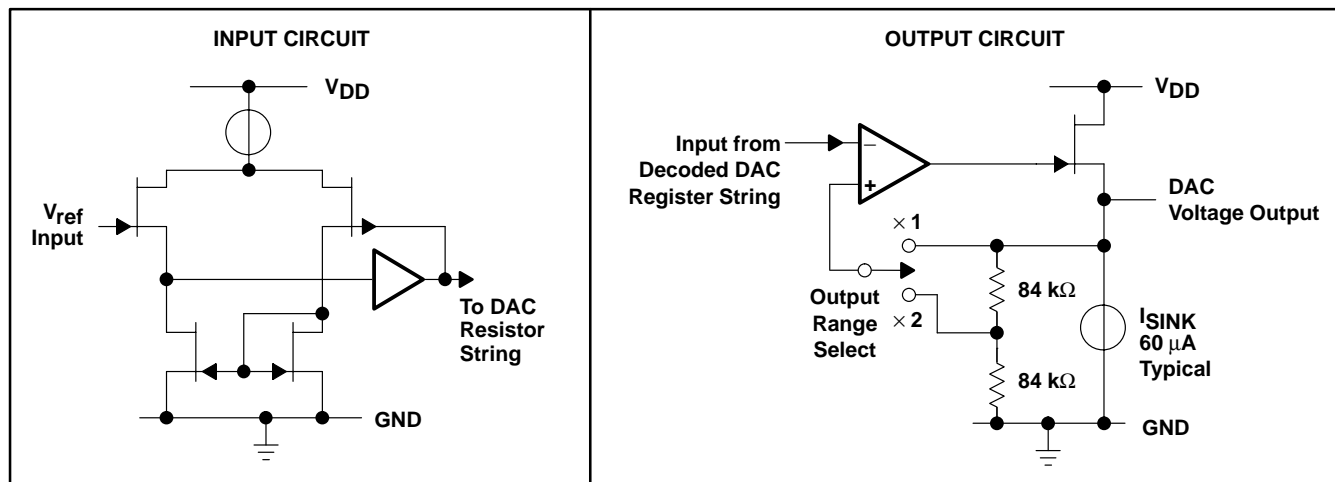
This offset error, not the linearity error, produces this breakpoint. The transfer function would have followed the dotted line if the output buffer could drive below ground.

For a DAC, linearity is measured between zero-input code (all inputs 0) and full-scale code (all inputs 1) after offset and full scale are adjusted out or accounted for in some way. However, single-supply operation does not allow for adjustment when the offset is negative due to the breakpoint in the transfer function. So the linearity is measured between full-scale code and the lowest code that produces a positive output voltage. The code is calculated from the maximum specification for the negative offset voltage.

# TLC5620C, TLC5620I QUADRUPLE 8-BIT DIGITAL-TO-ANALOG CONVERTERS

SLAS081E – NOVEMBER 1994 – REVISED NOVEMBER 2001

## equivalent inputs and outputs



## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage ( $V_{DD} - GND$ )	7 V
Digital input voltage range	$GND - 0.3 V$ to $V_{DD} + 0.3 V$
Reference input voltage range, $V_{ID}$	$GND - 0.3 V$ to $V_{DD} + 0.3 V$
Operating free-air temperature range, $T_A$ : TLC5620C	$0^\circ C$ to $70^\circ C$
TLC5620I	$-40^\circ C$ to $85^\circ C$
Storage temperature range, $T_{stg}$	$-50^\circ C$ to $150^\circ C$
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	$260^\circ C$

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

## recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, $V_{DD}$	4.75	5.25		V
High-level input voltage, $V_{IH}$	$0.8 V_{DD}$			V
Low-level input voltage, $V_{IL}$		0.8		V
Reference voltage, $V_{ref}$ [A B C D]		$V_{DD} - 1.5$		V
Analog full-scale output voltage, $R_L = 10 k\Omega$		3.5		V
Load resistance, $R_L$	10			$k\Omega$
Setup time, data input, $t_{su}(DATA-CLK)$ (see Figures 1 and 2)	50			ns
Valid time, data input valid after $CLK\downarrow$ , $t_v(DATA-CLK)$ (see Figures 1 and 2)	50			ns
Setup time, $CLK$ eleventh falling edge to $LOAD$ , $t_{su}(CLK-LOAD)$ (see Figure 1)	50			ns
Setup time, $LOAD\uparrow$ to $CLK\downarrow$ , $t_{su}(LOAD-CLK)$ (see Figure 1)	50			ns
Pulse duration, $LOAD$ , $t_w(LOAD)$ (see Figure 1)	250			ns
Pulse duration, $LDAC$ , $t_w(LDAC)$ (see Figure 2)	250			ns
Setup time, $LOAD\uparrow$ to $LDAC\downarrow$ , $t_{su}(LOAD-LDAC)$ (see Figure 2)	0			ns
$CLK$ frequency			1	MHz
Operating free-air temperature, $T_A$	TLC5620C	0	70	$^\circ C$
	TLC5620I	-40	85	$^\circ C$

# TLC5620C, TLC5620I

## QUADRUPLE 8-BIT DIGITAL-TO-ANALOG CONVERTERS

SLAS081E – NOVEMBER 1994 – REVISED NOVEMBER 2001

**electrical characteristics over recommended operating free-air temperature range,  $V_{DD} = 5\text{ V} \pm 5\%$ ,  $V_{ref} = 2\text{ V}$ ,  $\times 1$  gain output range (unless otherwise noted)**

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$I_{IH}$	High-level input current	$V_I = V_{DD}$			$\pm 10$	$\mu\text{A}$
$I_{IL}$	Low-level input current	$V_I = 0\text{ V}$			$\pm 10$	$\mu\text{A}$
$I_{O(\text{sink})}$	Output sink current	Each DAC output	20			$\mu\text{A}$
$I_{O(\text{source})}$	Output source current		2			$\text{mA}$
$C_i$	Input capacitance			15		$\text{pF}$
	Reference input capacitance			15		
$I_{DD}$	Supply current	$V_{DD} = 5\text{ V}$			2	$\text{mA}$
$I_{ref}$	Reference input current	$V_{DD} = 5\text{ V}$ , $V_{ref} = 2\text{ V}$			$\pm 10$	$\mu\text{A}$
$E_L$	Linearity error (end point corrected)	$V_{ref} = 2\text{ V}$ , $\times 2$ gain (see Note 1)			$\pm 1$	LSB
$E_D$	Differential-linearity error	$V_{ref} = 2\text{ V}$ , $\times 2$ gain (see Note 2)			$\pm 0.9$	LSB
$E_{ZS}$	Zero-scale error	$V_{ref} = 2\text{ V}$ , $\times 2$ gain (see Note 3)	0		30	$\text{mV}$
	Zero-scale-error temperature coefficient	$V_{ref} = 2\text{ V}$ , $\times 2$ gain (see Note 4)		10		$\mu\text{V}/^\circ\text{C}$
$E_{FS}$	Full-scale error	$V_{ref} = 2\text{ V}$ , $\times 2$ gain (see Note 5)			$\pm 60$	$\text{mV}$
	Full-scale-error temperature coefficient	$V_{ref} = 2\text{ V}$ , $\times 2$ gain (see Note 6)		$\pm 25$		$\mu\text{V}/^\circ\text{C}$
PSRR	Power-supply rejection ratio	See Notes 7 and 8		0.5		$\text{mV}/\text{V}$

- NOTES:
- Integral nonlinearity (INL) is the maximum deviation of the output from the line between zero and full scale (excluding the effects of zero code and full-scale errors).
  - Differential nonlinearity (DNL) is the difference between the measured and ideal 1 LSB amplitude change of any two adjacent codes. Monotonic means the output voltage changes in the same direction (or remains constant) as a change in the digital input code.
  - Zero-scale error is the deviation from zero voltage output when the digital input code is zero.
  - Zero-scale-error temperature coefficient is given by:  $ZSETC = [ZSE(T_{max}) - ZSE(T_{min})]/V_{ref} \times 10^6/(T_{max} - T_{min})$ .
  - Full-scale error is the deviation from the ideal full-scale output ( $V_{ref} - 1\text{ LSB}$ ) with an output load of 10 k $\Omega$ .
  - Full-scale-error temperature coefficient is given by:  $FSETC = [FSE(T_{max}) - FSE(T_{min})]/V_{ref} \times 10^6/(T_{max} - T_{min})$ .
  - Zero-scale-error rejection ratio (ZSE RR) is measured by varying the  $V_{DD}$  from 4.5 V to 5.5 V dc and measuring the proportion of this signal imposed on the zero-code output voltage.
  - Full-scale-error rejection ratio (FSE RR) is measured by varying the  $V_{DD}$  from 4.5 V to 5.5 V dc and measuring the proportion of this signal imposed on the full-scale output voltage.

**operating characteristics over recommended operating free-air temperature range,  $V_{DD} = 5\text{ V} \pm 5\%$ ,  $V_{ref} = 2\text{ V}$ ,  $\times 1$  gain output range (unless otherwise noted)**

	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Output slew rate	$C_L = 100\text{ pF}$ , $R_L = 10\text{ k}\Omega$		1		$\text{V}/\mu\text{s}$
Output settling time	To $\pm 0.5\text{ LSB}$ , $C_L = 100\text{ pF}$ , $R_L = 10\text{ k}\Omega$ , See Note 9		10		$\mu\text{s}$
Large-signal bandwidth	Measured at $-3\text{ dB}$ point		100		$\text{kHz}$
Digital crosstalk	$\text{CLK} = 1\text{-MHz}$ square wave measured at DACA-DACD		$-50$		$\text{dB}$
Reference feedthrough	See Note 10		$-60$		$\text{dB}$
Channel-to-channel isolation	See Note 11		$-60$		$\text{dB}$
Reference input bandwidth	See Note 12		100		$\text{kHz}$

- NOTES:
- Settling time is the time between a LOAD falling edge and the DAC output reaching full scale voltage within  $\pm 0.5\text{ LSB}$  starting from an initial output voltage equal to zero.
  - Reference feedthrough is measured at any DAC output with an input code = 00 hex with a  $V_{ref}$  input = 1 V dc + 1  $V_{pp}$  at 10 kHz.
  - Channel-to-channel isolation is measured by setting the input code of one DAC to FF hex and the code of all other DACs to 00 hex with  $V_{ref}$  input = 1 V dc + 1  $V_{pp}$  at 10 kHz.
  - Reference bandwidth is the  $-3\text{ dB}$  bandwidth with an input at  $V_{ref} = 1.25\text{ V}$  dc + 2  $V_{pp}$  and with a full-scale digital-input code.

# TLC5620C, TLC5620I QUADRUPLE 8-BIT DIGITAL-TO-ANALOG CONVERTERS

SLAS081E – NOVEMBER 1994 – REVISED NOVEMBER 2001

## PARAMETER MEASUREMENT INFORMATION

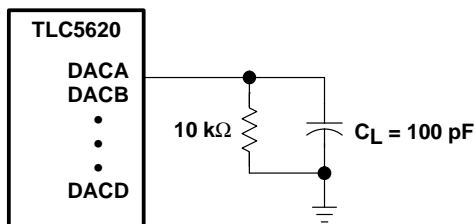


Figure 6. Slew, Settling Time, and Linearity Measurements

## TYPICAL CHARACTERISTICS

POSITIVE RISE AND SETTLING TIME

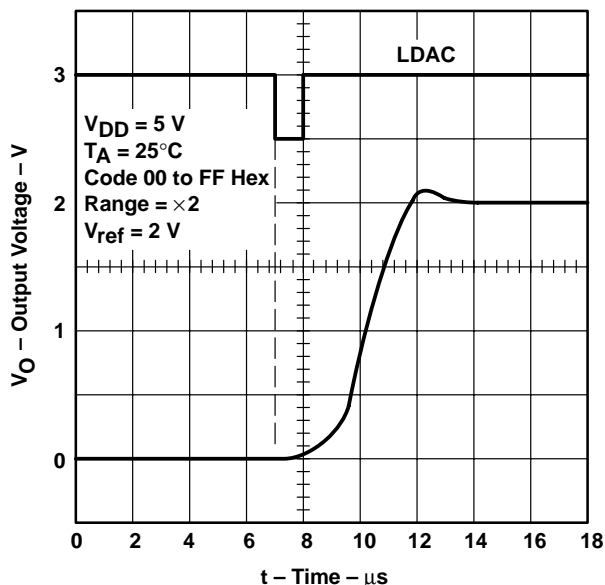


Figure 7

NEGATIVE FALL AND SETTLING TIME

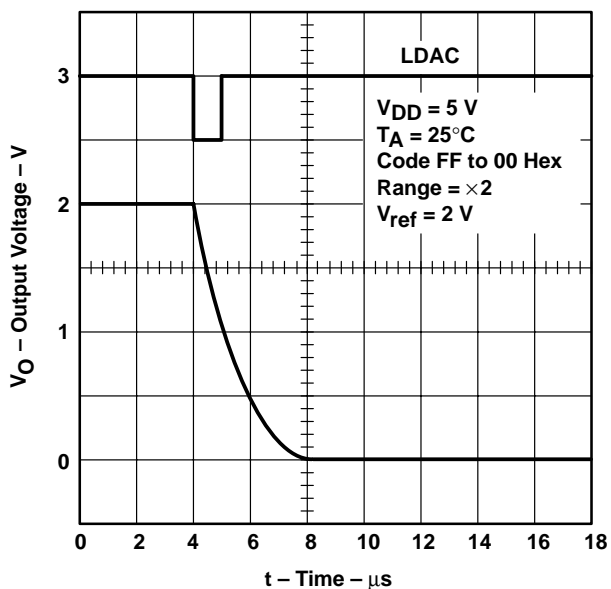


Figure 8



TYPICAL CHARACTERISTICS

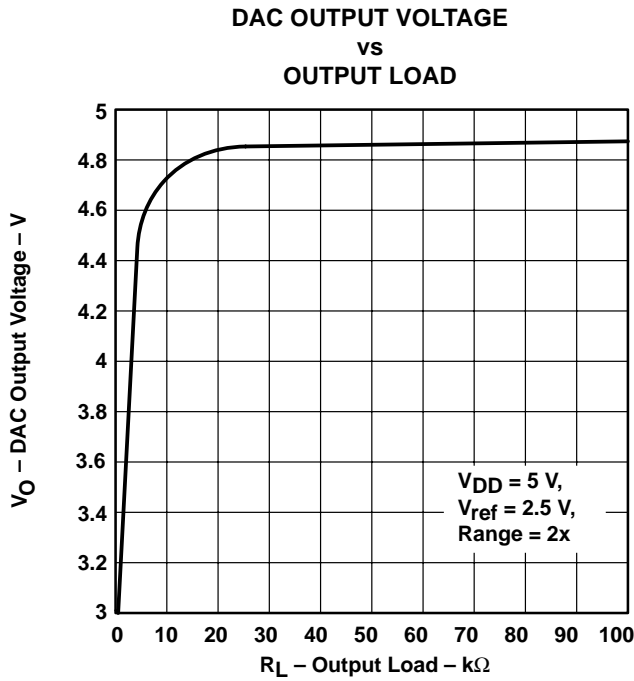


Figure 9

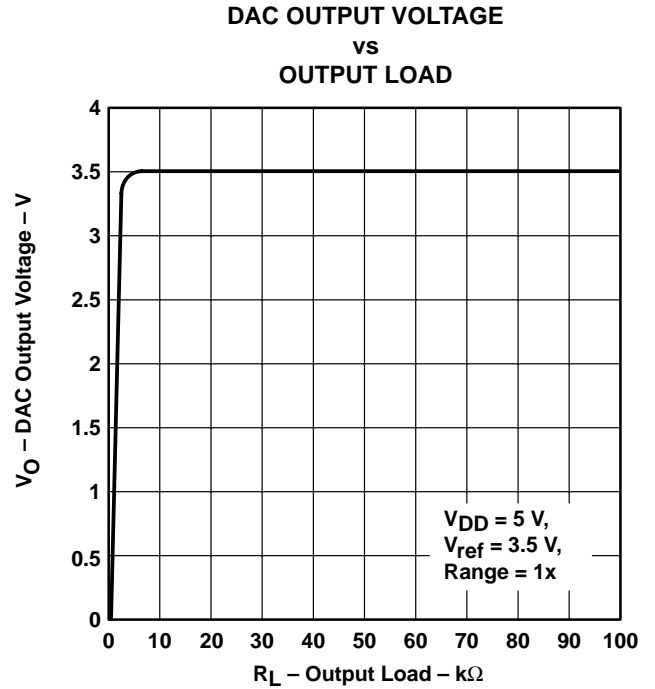


Figure 10

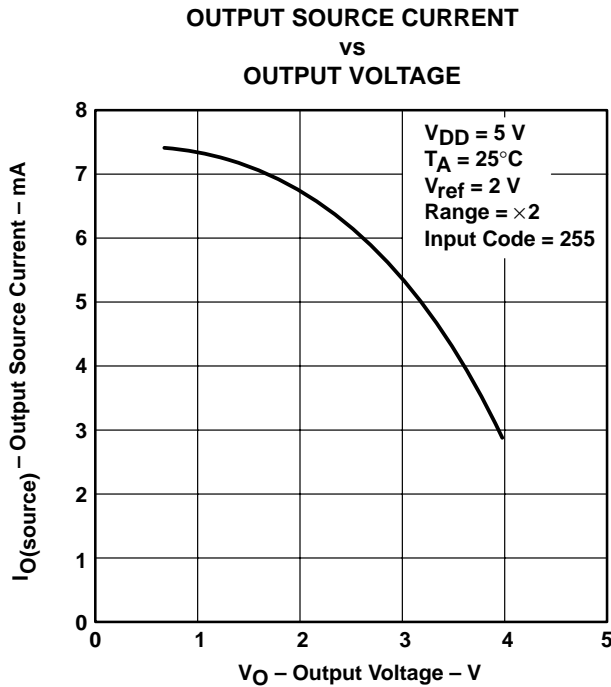


Figure 11

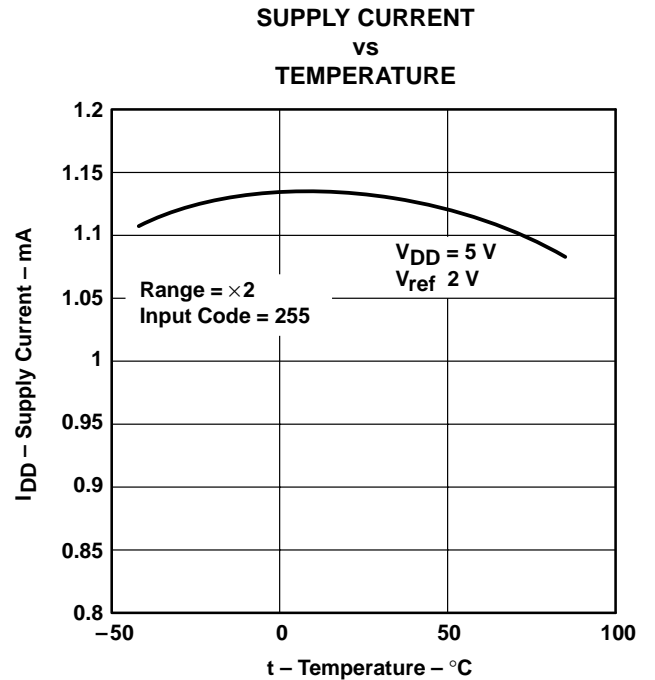


Figure 12

# TLC5620C, TLC5620I QUADRUPLE 8-BIT DIGITAL-TO-ANALOG CONVERTERS

SLAS081E – NOVEMBER 1994 – REVISED NOVEMBER 2001

## TYPICAL CHARACTERISTICS

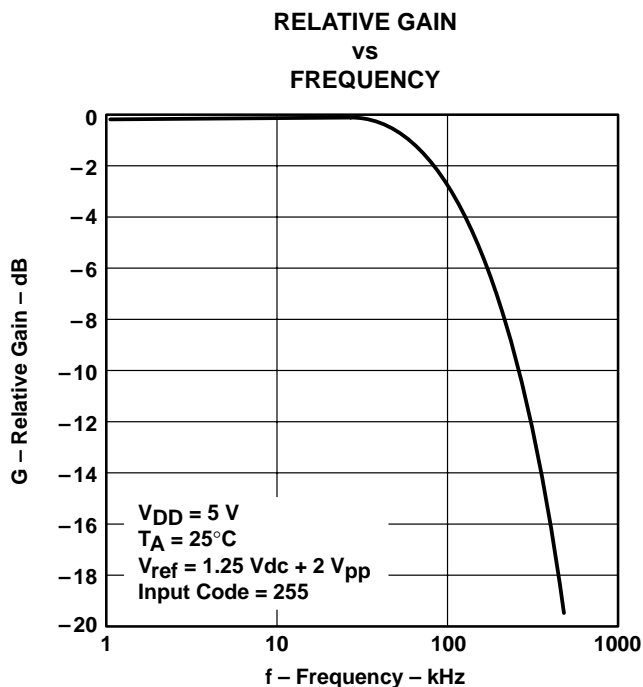


Figure 13

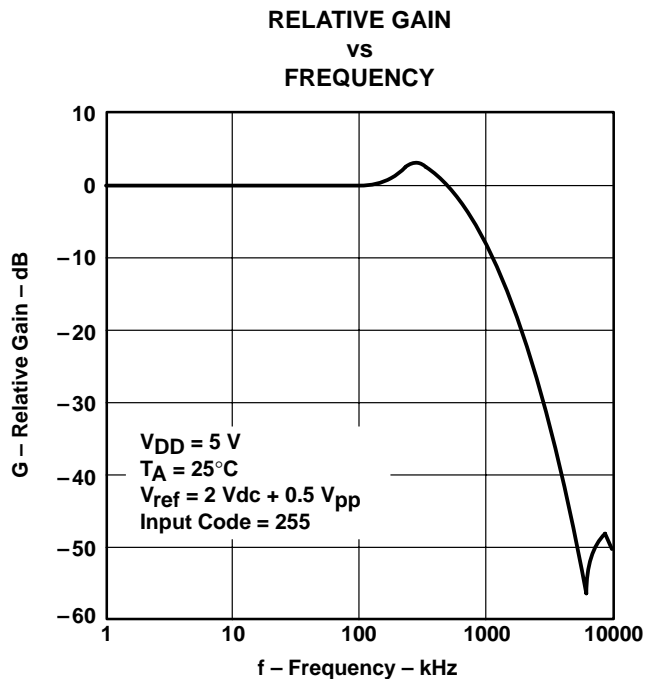
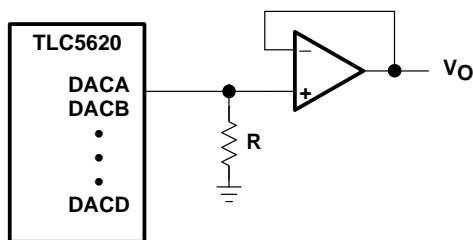


Figure 14

## APPLICATION INFORMATION



NOTE A: Resistor R ≥ 10 kΩ

Figure 15. Output Buffering Scheme

# TLC5620C, TLC5620I QUADRUPLE 8-BIT DIGITAL-TO-ANALOG CONVERTERS

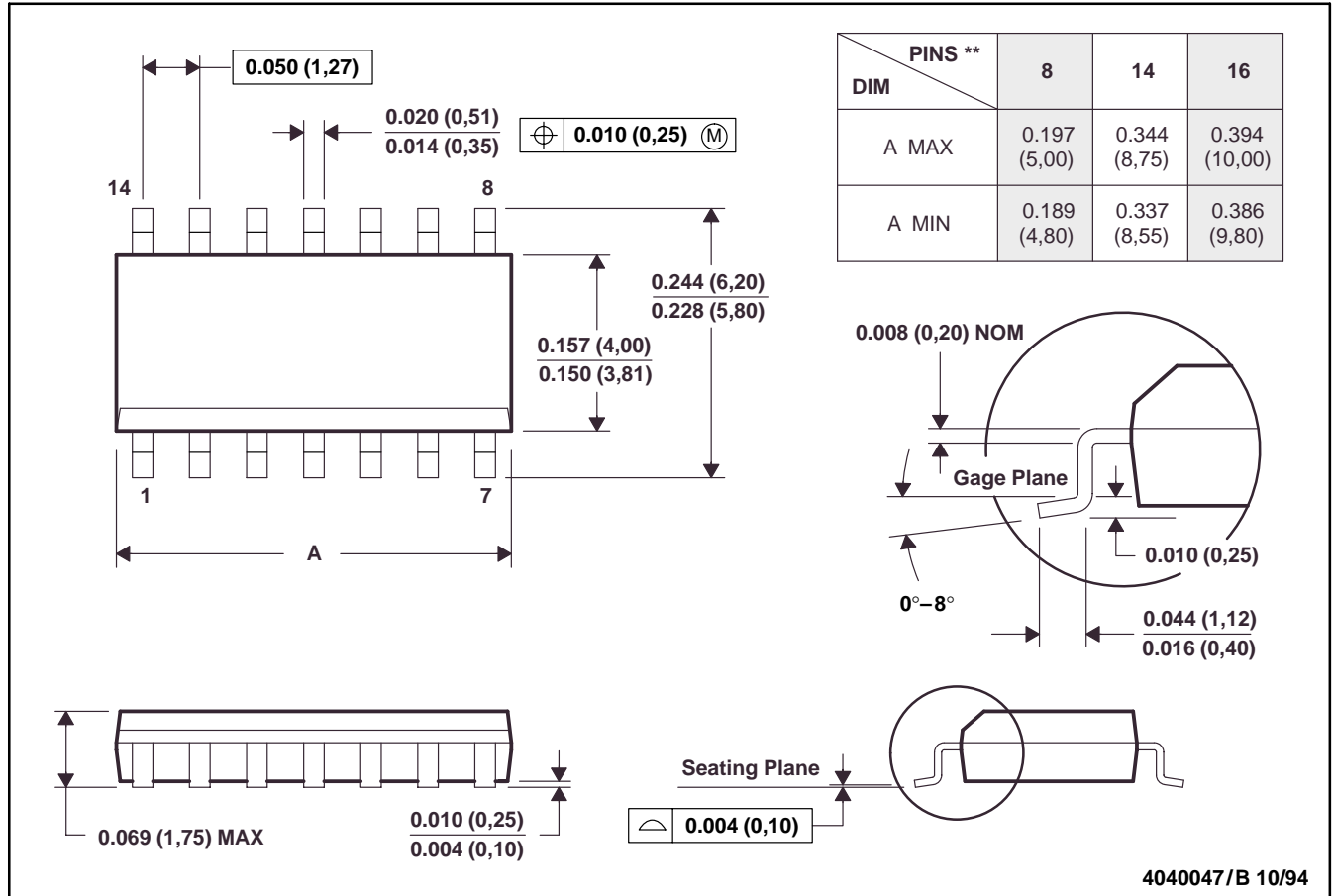
SLAS081E – NOVEMBER 1994 – REVISED NOVEMBER 2001

## MECHANICAL DATA

D (R-PDSO-G\*\*)

PLASTIC SMALL-OUTLINE PACKAGE

14 PIN SHOWN



- NOTES: A. All linear dimensions are in inches (millimeters).  
 B. This drawing is subject to change without notice.  
 C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).  
 D. Four center pins are connected to die mount pad.  
 E. Falls within JEDEC MS-012

# TLC5620C, TLC5620I QUADRUPLE 8-BIT DIGITAL-TO-ANALOG CONVERTERS

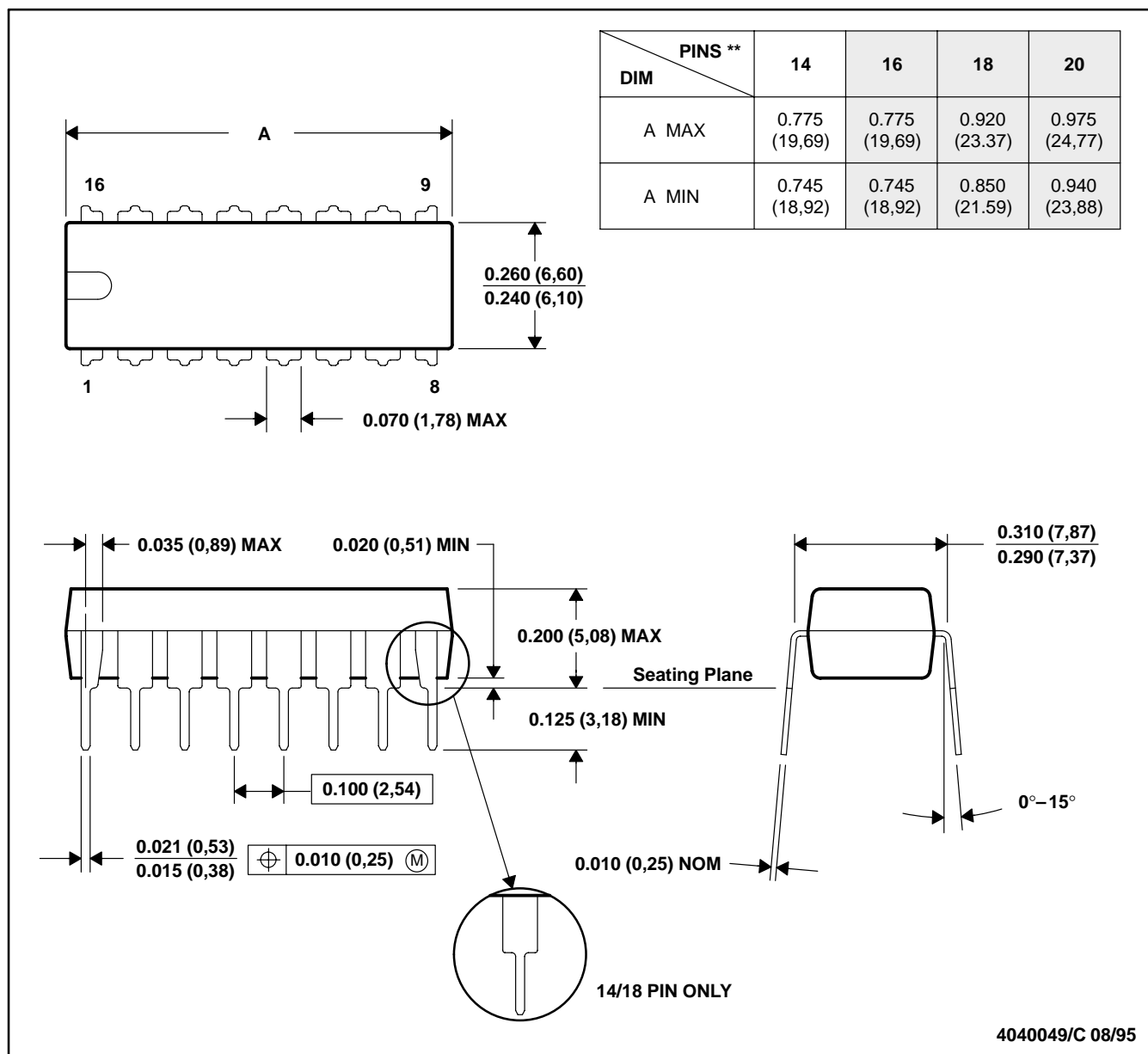
SLAS081E – NOVEMBER 1994 – REVISED NOVEMBER 2001

## MECHANICAL DATA

N (R-PDIP-T\*\*)

PLASTIC DUAL-IN-LINE PACKAGE

16 PIN SHOWN



- NOTES: A. All linear dimensions are in inches (millimeters).  
 B. This drawing is subject to change without notice.  
 C. Falls within JEDEC MS-001 (20-pin package is shorter than MS-001)

PACKAGING INFORMATION

Orderable Device	Status <sup>(1)</sup>	Package Type	Package Drawing	Pins	Package Qty	Eco Plan <sup>(2)</sup>	Lead/Ball Finish	MSL Peak Temp <sup>(3)</sup>
TLC5620CD	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TLC5620CDG4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TLC5620CDR	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TLC5620CDRG4	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TLC5620CN	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
TLC5620CNE4	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
TLC5620ID	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TLC5620IDG4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TLC5620IDR	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TLC5620IDRG4	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TLC5620IN	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
TLC5620INE4	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type

<sup>(1)</sup> The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

<sup>(2)</sup> Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

<sup>(3)</sup> MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

**Important Information and Disclaimer:** The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

**TAPE AND REEL INFORMATION**



**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TLC5620CDR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
TLC5620IDR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1

**TAPE AND REEL BOX DIMENSIONS**



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TLC5620CDR	SOIC	D	14	2500	346.0	346.0	33.0
TLC5620IDR	SOIC	D	14	2500	346.0	346.0	33.0



## IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, modifications, enhancements, improvements, and other changes to its products and services at any time and to discontinue any product or service without notice. Customers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All products are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its hardware products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by government requirements, testing of all parameters of each product is not necessarily performed.

TI assumes no liability for applications assistance or customer product design. Customers are responsible for their products and applications using TI components. To minimize the risks associated with customer products and applications, customers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any TI patent right, copyright, mask work right, or other TI intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information published by TI regarding third-party products or services does not constitute a license from TI to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of TI information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. Reproduction of this information with alteration is an unfair and deceptive business practice. TI is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

Resale of TI products or services with statements different from or beyond the parameters stated by TI for that product or service voids all express and any implied warranties for the associated TI product or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

TI products are not authorized for use in safety-critical applications (such as life support) where a failure of the TI product would reasonably be expected to cause severe personal injury or death, unless officers of the parties have executed an agreement specifically governing such use. Buyers represent that they have all necessary expertise in the safety and regulatory ramifications of their applications, and acknowledge and agree that they are solely responsible for all legal, regulatory and safety-related requirements concerning their products and any use of TI products in such safety-critical applications, notwithstanding any applications-related information or support that may be provided by TI. Further, Buyers must fully indemnify TI and its representatives against any damages arising out of the use of TI products in such safety-critical applications.

TI products are neither designed nor intended for use in military/aerospace applications or environments unless the TI products are specifically designated by TI as military-grade or "enhanced plastic." Only products designated by TI as military-grade meet military specifications. Buyers acknowledge and agree that any such use of TI products which TI has not designated as military-grade is solely at the Buyer's risk, and that they are solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI products are neither designed nor intended for use in automotive applications or environments unless the specific TI products are designated by TI as compliant with ISO/TS 16949 requirements. Buyers acknowledge and agree that, if they use any non-designated products in automotive applications, TI will not be responsible for any failure to meet such requirements.

Following are URLs where you can obtain information on other Texas Instruments products and application solutions:

### Products

Amplifiers	<a href="http://amplifier.ti.com">amplifier.ti.com</a>
Data Converters	<a href="http://dataconverter.ti.com">dataconverter.ti.com</a>
DSP	<a href="http://dsp.ti.com">dsp.ti.com</a>
Clocks and Timers	<a href="http://www.ti.com/clocks">www.ti.com/clocks</a>
Interface	<a href="http://interface.ti.com">interface.ti.com</a>
Logic	<a href="http://logic.ti.com">logic.ti.com</a>
Power Mgmt	<a href="http://power.ti.com">power.ti.com</a>
Microcontrollers	<a href="http://microcontroller.ti.com">microcontroller.ti.com</a>
RFID	<a href="http://www.ti-rfid.com">www.ti-rfid.com</a>
RF/IF and ZigBee® Solutions	<a href="http://www.ti.com/lprf">www.ti.com/lprf</a>

### Applications

Audio	<a href="http://www.ti.com/audio">www.ti.com/audio</a>
Automotive	<a href="http://www.ti.com/automotive">www.ti.com/automotive</a>
Broadband	<a href="http://www.ti.com/broadband">www.ti.com/broadband</a>
Digital Control	<a href="http://www.ti.com/digitalcontrol">www.ti.com/digitalcontrol</a>
Medical	<a href="http://www.ti.com/medical">www.ti.com/medical</a>
Military	<a href="http://www.ti.com/military">www.ti.com/military</a>
Optical Networking	<a href="http://www.ti.com/opticalnetwork">www.ti.com/opticalnetwork</a>
Security	<a href="http://www.ti.com/security">www.ti.com/security</a>
Telephony	<a href="http://www.ti.com/telephony">www.ti.com/telephony</a>
Video & Imaging	<a href="http://www.ti.com/video">www.ti.com/video</a>
Wireless	<a href="http://www.ti.com/wireless">www.ti.com/wireless</a>

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265  
Copyright © 2008, Texas Instruments Incorporated

[www.BDTIC.com/TI](http://www.BDTIC.com/TI)