

## LOW-POWER 16-CHANNEL CONSTANT-CURRENT LED SINK DRIVER

### FEATURES

- 16 Constant-Current Output Channels
- Matches Industry Standard IOUT to External Resistor Ratio
- Constant Output Current Invariant to Load Voltage Change
- Excellent Output Current Accuracy:
  - Between Channels: <  $\pm 5\%$  (Max)
  - Between ICs: <  $\pm 6\%$  (Max)
- Constant Output Current Range: 3 mA to 45 mA
- Output Current Adjusted By External Resistor
- Fast Response of Output Current,  $\overline{OE}$  (Min): 100 ns
- 30-MHz Clock Frequency
- Schmitt-Trigger Inputs
- 3.3-V to 5-V Supply Voltage
- Thermal Shutdown for Overtemperature Protection
- ESD Performance: 1-kV HBM

### APPLICATIONS

- Gaming Machine / Entertainment
- General LED Applications
- LED Display Systems
- Signs LED Lighting
- White Goods

### DESCRIPTION/ORDERING INFORMATION

The TLC59025 is designed for LED displays and LED lighting applications. The TLC59025 contains a 16-bit shift register and data latches, which convert serial input data into parallel output format. At the TLC59025 output stage, 16 regulated-current ports provide uniform and constant current for driving LEDs within a wide range of VF variations. Used in system design for LED display applications (e.g., LED panels), the TLC59025 provides great flexibility and device performance. Users can adjust the output current from 3 mA to 45 mA through an external resistor,  $R_{ext}$ , which gives flexibility in controlling the light intensity of LEDs. TLC59025 is designed for up to 17 V at the output port. The high clock frequency, 30 MHz, also satisfies the system requirements of high-volume data transmission.

The serial data is transferred into TLC59025 via SDI, shifted in the shift register, and transferred out via SDO. LE can latch the serial data in the shift register to the output latch.  $\overline{OE}$  enables the output drivers to sink current.

#### ORDERING INFORMATION<sup>(1)</sup>

$T_A$	PACKAGE <sup>(2)</sup>		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 85°C	PW	Reel of 2000	TLC59025IPWR	PREVIEW
	W-SOIC – DW	Reel of 2000	TLC59025IDWR	PREVIEW
	SSOP – DBQ	Reel of 2000	TLC59025IDBQR	TLC59025

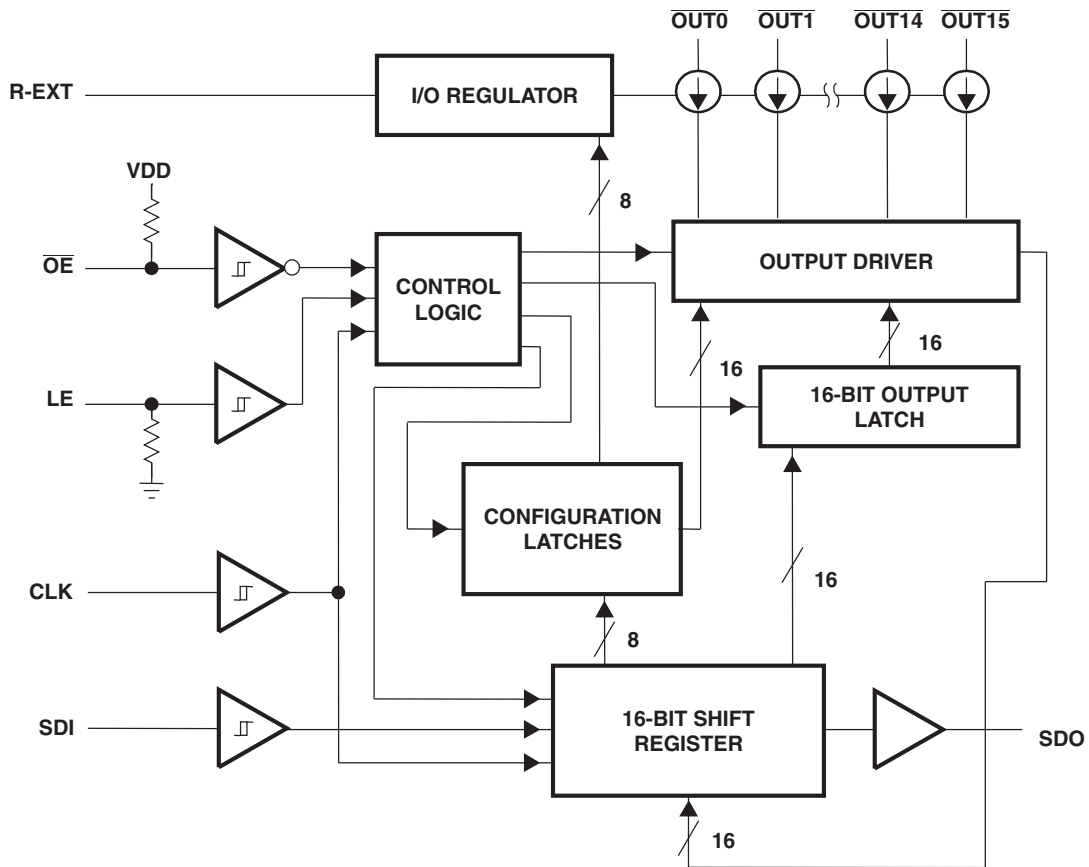
(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at [www.ti.com](http://www.ti.com).

(2) Package drawings, thermal data, and symbolization are available at [www.ti.com/packaging](http://www.ti.com/packaging).

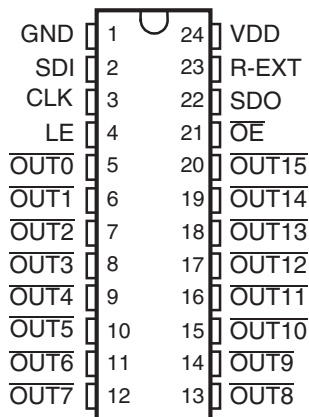


Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

BLOCK DIAGRAM



DBQ, DW, OR PWP PACKAGE  
(TOP VIEW)



Terminal Descriptions

TERMINAL NAME	DESCRIPTION
CLK	Clock input for data shift on rising edge
GND	Ground for control logic and current sink
LE	Data strobe input Serial data is transferred to the respective latch when LE is high. The data is latched when LE goes low. LE has an internal pull-down resistor.
$\overline{OE}$	Output enable When $\overline{OE}$ is active (low), the output drivers are enabled. When $\overline{OE}$ is high, all output drivers are turned OFF (blanked). $\overline{OE}$ has an internal pullup resistor.
$\overline{OUT0}$ – $\overline{OUT15}$	Constant-current outputs
R-EXT	Input used to connect an external resistor ( $R_{ext}$ ) for setting output currents
SDI	Serial-data input to the Shift register
SDO	Serial-data output to the following SDI of next driver IC or to the microcontroller
VDD	Supply voltage

### Timing Diagram

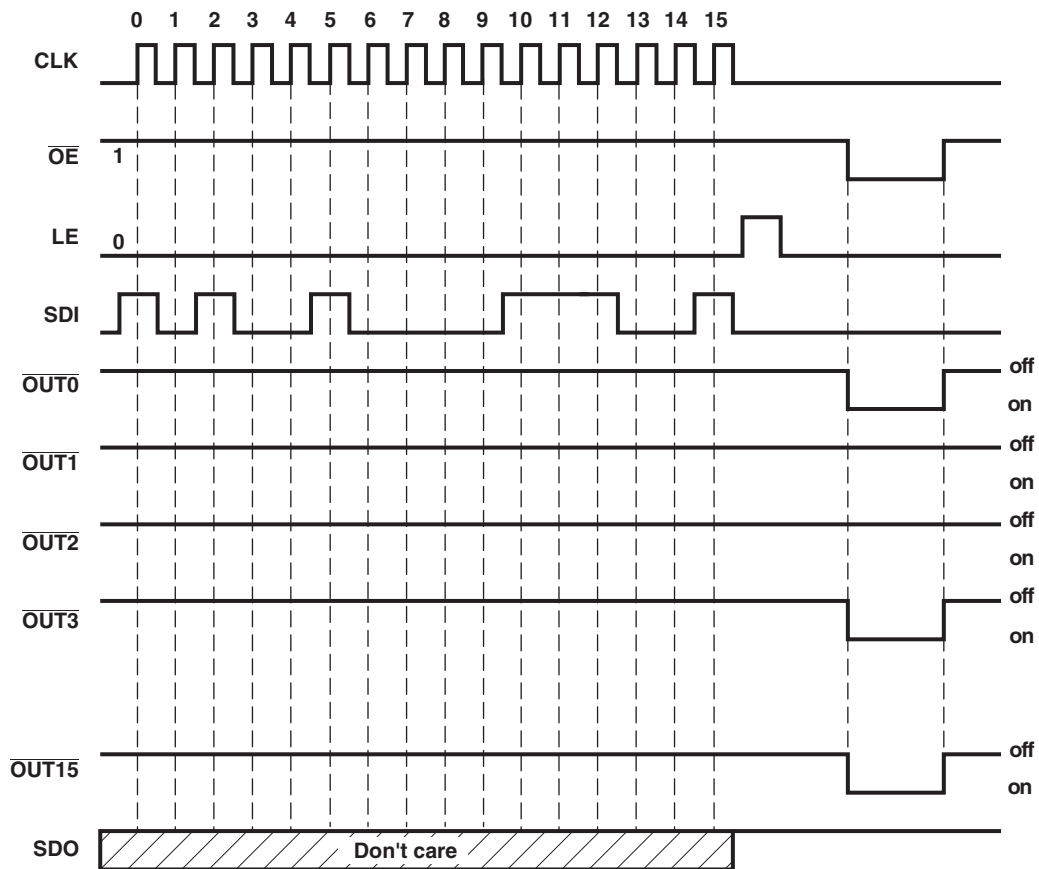


Figure 1. Timing Diagram

### Truth Table in Normal Operation

CLK	LE	$\overline{OE}$	SDI	$\overline{OUT0}...OUT15...OUT15$	SDO
↑	H	L	Dn	Dn...Dn – 7...Dn – 15	Dn – 15
↑	L	L	Dn + 1	No change	Dn – 14
↑	H	L	Dn + 2	Dn + 2...Dn – 5...Dn – 13	Dn – 13
↓	X	L	Dn + 3	Dn + 2...Dn – 5...Dn – 13	Dn – 13
↓	X	H	Dn + 3	off	Dn – 13

## Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
$V_{DD}$	Supply voltage	0	7	V
$V_I$	Input voltage	-0.4	$V_{DD} + 0.4$	V
$V_O$	Output voltage	-0.5	20	V
$I_{OUT}$	Output current		45	mA
$I_{GND}$	GND terminal current		750	mA
$T_A$	Operating free-air temperature range	-40	125	°C
$T_J$	Operating virtual-junction temperature range	-40	150	°C
$T_{stg}$	Storage temperature range	-55	150	°C

## Power Dissipation and Thermal Impedance

			MIN	MAX	UNIT	
$P_D$	Power dissipation	Mounted on JEDEC 4-layer board (JESD 51-7), No airflow, $T_A = 25^\circ\text{C}$ , $T_J = 125^\circ\text{C}$	DBQ package		1.6	W
			DW package		2.2	
			PW package		1.1	
$\theta_{JA}$	Thermal impedance, junction to free air	Mounted on JEDEC 1-layer board (JESD 51-3), No airflow	DBQ package		99.8	°C/W
			DW package		80.5	
			PW package		118.8	
		Mounted on JEDEC 4-layer board (JESD 51-7), No airflow	DBQ package		61.0	
			DW package		45.5	
			PW package		87.9	

## Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		TEST CONDITIONS		MIN	MAX	UNIT
$V_{DD}$	Supply voltage			3	5.5	V
$V_O$	Output voltage	$\overline{OUT0}$ to $\overline{OUT15}$			17	V
$I_O$	Output current	DC test circuit	$V_O \geq 0.6\text{ V}$	3		mA
			$V_O \geq 1\text{ V}$		45	
$I_{OH}$	High-level output current	SDO		-1		mA
$I_{OL}$	Low-level output current	SDO		1		mA
$V_{IH}$	High-level input voltage	CLK, $\overline{OE}$ , LE, and SDI		$0.7 \times V_{DD}$	$V_{DD}$	V
$V_{IL}$	Low-level input voltage	CLK, $\overline{OE}$ , LE, and SDI		GND	$0.3 \times V_{DD}$	V
$t_R$	Rise time	CLK			500	ns
$t_F$	Fall time	CLK			500	ns

## Recommended Timing

$V_{DD} = 3\text{ V}$  to  $5.5\text{ V}$  (unless otherwise noted)

		MIN	MAX	UNIT	
$t_{w(L)}$	LE pulse duration	15		ns	
$t_{w(CLK)}$	CLK pulse duration	15		ns	
$t_{w(OE)}$	$\overline{OE}$ pulse duration	300		ns	
$t_{su(D)}$	Setup time for SDI	3		ns	
$t_{h(D)}$	Hold time for SDI	2		ns	
$t_{su(L)}$	Setup time for LE	5		ns	
$t_{h(L)}$	Hold time for LE	5		ns	
$f_{CLK}$	Clock frequency	Cascade operation		30	MHz

## Electrical Characteristics

 $V_{DD} = 3\text{ V}$ ,  $T_J = -40^\circ\text{C}$  to  $125^\circ\text{C}$  (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT	
$V_{DD}$	Input voltage		3		5.5	V	
$V_O$	Output voltage				17	V	
$I_O$	Output current	$V_O \geq 0.6\text{ V}$	3			mA	
		$V_O \geq 1\text{ V}$			45		
$I_{OH}$	High-level output current, source		-1			mA	
$I_{OL}$	Low-level output current, sink		1				
$V_{IH}$	High-level input voltage		$0.7 \times V_{DD}$		$V_{DD}$	V	
$V_{IL}$	Low-level input voltage		GND		$0.3 \times V_{DD}$		
$I_{leak}$	Output leakage current	$V_{OH} = 17\text{ V}$	$T_J = 25^\circ\text{C}$		0.5	$\mu\text{A}$	
			$T_J = 125^\circ\text{C}$		2		
$V_{OH}$	High-level output voltage	SDO, $I_{OL} = -1\text{ mA}$	$V_{DD} - 0.4$			V	
$V_{OL}$	Low-level output voltage	SDO, $I_{OH} = 1\text{ mA}$			0.4	V	
$I_{O(1)}$	Output current 1	$V_{OUT} = 0.6\text{ V}$ , $R_{ext} = 1440\ \Omega$		13		mA	
	Output current error, die-die	$I_{OL} = 13\text{ mA}$ , $V_O = 0.6\text{ V}$ , $R_{ext} = 1440\ \Omega$ , $T_J = 25^\circ\text{C}$		$\pm 3$	$\pm 6$		%
	Output current error, channel-to-channel	$I_{OL} = 13\text{ mA}$ , $V_O = 0.6\text{ V}$ , $R_{ext} = 1440\ \Omega$ , $T_J = 25^\circ\text{C}$		$\pm 1.5$	$\pm 5$		
$I_{O(2)}$	Output current 2	$V_O = 0.8\text{ V}$ , $R_{ext} = 720\ \Omega$		26		mA	
	Output current error, die-die	$I_{OL} = 26\text{ mA}$ , $V_O = 0.8\text{ V}$ , $R_{ext} = 720\ \Omega$ , $T_J = 25^\circ\text{C}$		$\pm 3$	$\pm 6$		%
	Output current error, channel-to-channel	$I_{OL} = 26\text{ mA}$ , $V_O = 0.8\text{ V}$ , $R_{ext} = 720\ \Omega$ , $T_J = 25^\circ\text{C}$		$\pm 1.5$	$\pm 5$		
$I_{OUT}$ vs $V_{OUT}$	Output current vs output voltage regulation	$V_O = 1\text{ V}$ to $3\text{ V}$ , $I_O = 13\text{ mA}$		$\pm 0.1$		%V	
		$V_{DD} = 3.0\text{ V}$ to $5.5\text{ V}$ , $I_O = 13\text{ mA}$ to $45\text{ mA}$		$\pm 1$			
	Pullup resistance	$\overline{OE}$		500		k $\Omega$	
	Pulldown resistance	LE		500		k $\Omega$	
$T_{sd}$	Overtemperature shutdown <sup>(1)</sup>		150	175	200	$^\circ\text{C}$	
$T_{hys}$	Restart temperature hysteresis			15		$^\circ\text{C}$	
$I_{DD}$	Supply current	$R_{ext} = \text{Open}$		7	10	mA	
		$R_{ext} = 1440\ \Omega$		9	12		
		$R_{ext} = 720\ \Omega$		11	13		
$C_{IN}$	Input capacitance	$V_I = V_{DD}$ or GND, CLK, SDI, SDO, $\overline{OE}$			10	pF	

(1) Specified by design

## Electrical Characteristics

$V_{DD} = 5.5\text{ V}$ ,  $T_J = -40^\circ\text{C}$  to  $125^\circ\text{C}$  (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT	
$V_{DD}$	Input voltage		3		5.5	V	
$V_O$	Output voltage				17	V	
$I_O$	Output current	$V_O \geq 0.6\text{ V}$	3			mA	
		$V_O \geq 1\text{ V}$			45		
$I_{OH}$	High-level output current, source		-1			mA	
$I_{OL}$	Low-level output current, sink		1				
$V_{IH}$	High-level input voltage		$0.7 \times V_{DD}$		$V_{DD}$	V	
$V_{IL}$	Low-level input voltage		GND		$0.3 \times V_{DD}$		
$I_{leak}$	Output leakage current	$V_{OH} = 17\text{ V}$	$T_J = 25^\circ\text{C}$		0.5	$\mu\text{A}$	
			$T_J = 125^\circ\text{C}$		2		
$V_{OH}$	High-level output voltage	SDO, $I_{OL} = -1\text{ mA}$	$V_{DD} - 0.4$			V	
$V_{OL}$	Low-level output voltage	SDO, $I_{OH} = 1\text{ mA}$			0.4	V	
$I_{O(1)}$	Output current 1	$V_{OUT} = 0.6\text{ V}$ , $R_{ext} = 1440\ \Omega$		13		mA	
	Output current error, die-die	$I_{OL} = 13\text{ mA}$ , $V_O = 0.6\text{ V}$ , $R_{ext} = 1440\ \Omega$ , $T_J = 25^\circ\text{C}$		$\pm 3$	$\pm 6$		%
	Output current error, channel-to-channel	$I_{OL} = 13\text{ mA}$ , $V_O = 0.6\text{ V}$ , $R_{ext} = 1440\ \Omega$ , $T_J = 25^\circ\text{C}$		$\pm 1.5$	$\pm 5$		
$I_{O(2)}$	Output current 2	$V_O = 0.8\text{ V}$ , $R_{ext} = 720\ \Omega$		26		mA	
	Output current error, die-die	$I_{OL} = 26\text{ mA}$ , $V_O = 0.8\text{ V}$ , $R_{ext} = 720\ \Omega$ , $T_J = 25^\circ\text{C}$		$\pm 3$	$\pm 6$		%
	Output current error, channel-to-channel	$I_{OL} = 26\text{ mA}$ , $V_O = 0.8\text{ V}$ , $R_{ext} = 720\ \Omega$ , $T_J = 25^\circ\text{C}$		$\pm 1.5$	$\pm 5$		
$I_{OUT}$ vs $V_{OUT}$	Output current vs output voltage regulation	$V_O = 1\text{ V}$ to $3\text{ V}$ , $I_O = 26\text{ mA}$		$\pm 0.1$		%V	
		$V_{DD} = 3.0\text{ V}$ to $5.5\text{ V}$ , $I_O = 13\text{ mA}$ to $45\text{ mA}$		$\pm 1$			
	Pullup resistance	$\overline{OE}$		500		k $\Omega$	
	Pulldown resistance	LE		500		k $\Omega$	
$T_{sd}$	Overtemperature shutdown <sup>(1)</sup>		150	175	200	$^\circ\text{C}$	
$T_{hys}$	Restart temperature hysteresis			15		$^\circ\text{C}$	
$I_{DD}$	Supply current	$R_{ext} = \text{Open}$		9	11	mA	
		$R_{ext} = 1440\ \Omega$		12	14		
		$R_{ext} = 720\ \Omega$		14	16		
$C_{IN}$	Input capacitance	$V_I = V_{DD}$ or GND, CLK, SDI, SDO, $\overline{OE}$			10	pF	

(1) Specified by design



## Switching Characteristics

$V_{DD} = 3\text{ V}$ ,  $T_J = -40^\circ\text{C}$  to  $125^\circ\text{C}$  (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{PLH1}$	Low-to-high propagation delay time, CLK to $\overline{\text{OUTn}}$	$V_{IH} = V_{DD}$ , $V_{IL} = \text{GND}$ , $R_{\text{ext}} = 720\ \Omega$ , $V_L = 4\ \text{V}$ , $R_L = 88\ \Omega$ , $C_L = 10\ \text{pF}$	30	45	60	ns
$t_{PLH2}$	Low-to-high propagation delay time, LE to $\overline{\text{OUTn}}$		30	45	60	ns
$t_{PLH3}$	Low-to-high propagation delay time, $\overline{\text{OE}}$ to $\overline{\text{OUTn}}$		30	45	60	ns
$t_{PLH4}$	Low-to-high propagation delay time, CLK to SDO			30	40	ns
$t_{PHL1}$	High-to-low propagation delay time, CLK to $\overline{\text{OUTn}}$		40	65	100	ns
$t_{PHL2}$	High-to-low propagation delay time, LE to $\overline{\text{OUTn}}$		40	65	100	ns
$t_{PHL3}$	High-to-low propagation delay time, $\overline{\text{OE}}$ to $\overline{\text{OUTn}}$		40	65	100	ns
$t_{PHL4}$	High-to-low propagation delay time, CLK to SDO			30	40	ns
$t_{w(\text{CLK})}$	Pulse duration, CLK		15			ns
$t_{w(L)}$	Pulse duration LE		15			ns
$t_{w(\text{OE})}$	Pulse duration, $\overline{\text{OE}}$		300			ns
$t_{h(D)}$	Hold time, SDI		2			ns
$t_{su(D)}$	Setup time, SDI		3			ns
$t_{h(L)}$	Hold time, LE		5			ns
$t_{su(L)}$	Setup time, LE		5			ns
$t_r$	Rise time, CLK <sup>(1)</sup>				500	ns
$t_f$	Fall time, CLK <sup>(1)</sup>				500	ns
$t_{or}$	Rise time, outputs (off)		35	50	70	ns
$t_{of}$	Rise time, outputs (on)		15	50	120	ns
$f_{\text{CLK}}$	Clock frequency		Cascade operation			30

- (1) If the devices are connected in cascade and  $t_r$  or  $t_f$  is large, it may be critical to achieve the timing required for data transfer between two cascaded devices.

## Switching Characteristics

$V_{DD} = 5.5\text{ V}$ ,  $T_J = -40^\circ\text{C}$  to  $125^\circ\text{C}$  (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{PLH1}$	Low-to-high propagation delay time, CLK to $\overline{\text{OUTn}}$	$V_{IH} = V_{DD}$ , $V_{IL} = \text{GND}$ , $R_{\text{ext}} = 720\ \Omega$ , $V_L = 4\ \text{V}$ , $R_L = 88\ \Omega$ , $C_L = 10\ \text{pF}$	20	35	55	ns
$t_{PLH2}$	Low-to-high propagation delay time, LE to $\overline{\text{OUTn}}$		20	35	55	ns
$t_{PLH3}$	Low-to-high propagation delay time, $\overline{\text{OE}}$ to $\overline{\text{OUTn}}$		20	35	55	ns
$t_{PLH4}$	Low-to-high propagation delay time, CLK to SDO			20	30	ns
$t_{PHL1}$	High-to-low propagation delay time, CLK to $\overline{\text{OUTn}}$		15	28	42	ns
$t_{PHL2}$	High-to-low propagation delay time, LE to $\overline{\text{OUTn}}$		15	28	42	ns
$t_{PHL3}$	High-to-low propagation delay time, $\overline{\text{OE}}$ to $\overline{\text{OUTn}}$		15	28	42	ns
$t_{PHL4}$	High-to-low propagation delay time, CLK to SDO			20	30	ns
$t_{w(\text{CLK})}$	Pulse duration, CLK		10			ns
$t_{w(L)}$	Pulse duration LE		10			ns
$t_{w(\text{OE})}$	Pulse duration, $\overline{\text{OE}}$		200			ns
$t_{h(D)}$	Hold time, SDI		2			ns
$t_{su(D)}$	Setup time, SDI		3			ns
$t_{h(L)}$	Hold time, LE		5			ns
$t_{su(L)}$	Setup time, LE		5			ns
$t_r$	Rise time, CLK <sup>(1)</sup>				500	ns
$t_f$	Fall time, CLK <sup>(1)</sup>				500	ns
$t_{or}$	Rise time, outputs (off)		25	45	65	ns
$t_{of}$	Rise time, outputs (on)		7	12	20	ns
$f_{\text{CLK}}$	Clock frequency		Cascade operation			30

- (1) If the devices are connected in cascade and  $t_r$  or  $t_f$  is large, it may be critical to achieve the timing required for data transfer between two cascaded devices.

PARAMETER MEASUREMENT INFORMATION

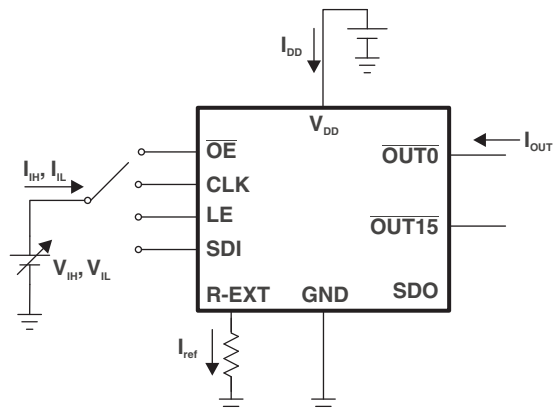


Figure 2. Test Circuit for Electrical Characteristics

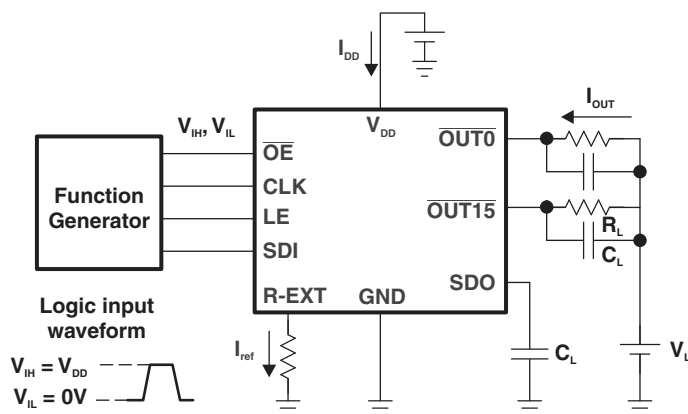


Figure 3. Test Circuit for Switching Characteristics

PARAMETER MEASUREMENT INFORMATION (continued)

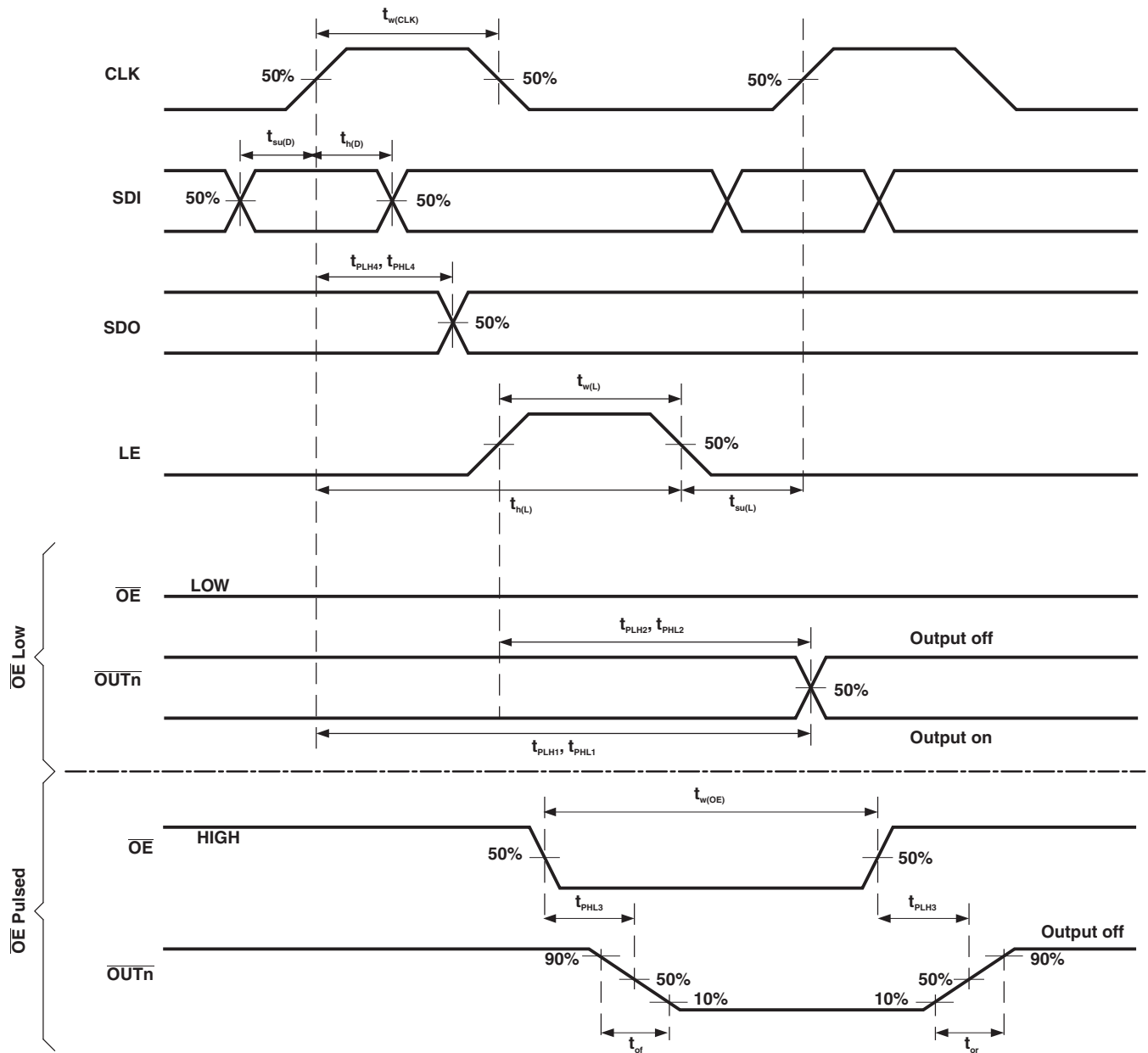


Figure 4. Normal Mode Timing Waveforms

## APPLICATION INFORMATION

### Operating Principles

#### Constant Current

In LED display applications, TLC59025 provides nearly no current variations from channel to channel and from IC to IC. While  $I_{OUT} \leq 45$  mA, the maximum current skew between channels is less than  $\pm 5\%$  and between ICs is less than  $\pm 6\%$ .

#### Adjusting Output Current

TLC59025 sets  $I_{OUT}$  based on the external resistor  $R_{ext}$ . Users can follow the below formulas to calculate the target output current  $I_{OUT,target}$  in the saturation region:

$I_{OUT,target} = (1.21 \text{ V} / R_{ext}) \times 15.5$ , where  $R_{ext}$  is the external resistance connected between R-EXT and GND.

Therefore, the default current is approximately 26 mA at 720  $\Omega$  and 13 mA at 1440  $\Omega$ . The default relationship after power on between  $I_{OUT,target}$  and  $R_{ext}$  is shown in Figure 5.

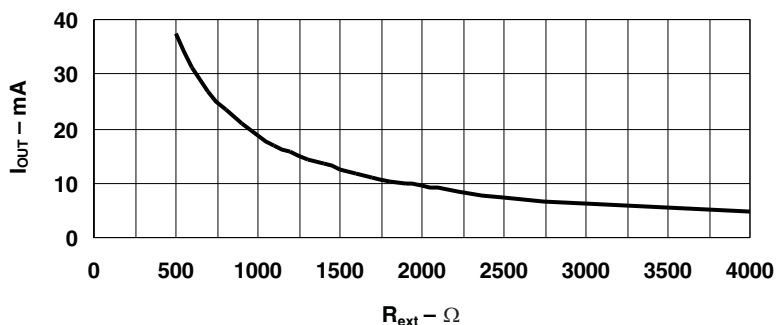


Figure 5. Default Relationship Curve Between  $I_{OUT,target}$  and  $R_{ext}$  After Power Up

Propagation Delay Times

$V_{DD} = 5\text{ V}$   
 $V_L = 4\text{ V}$   
 $R_{ext} = 840\ \Omega$   
 $R_L = 88\ \Omega$   
 $C_L = 10\text{ pF}$

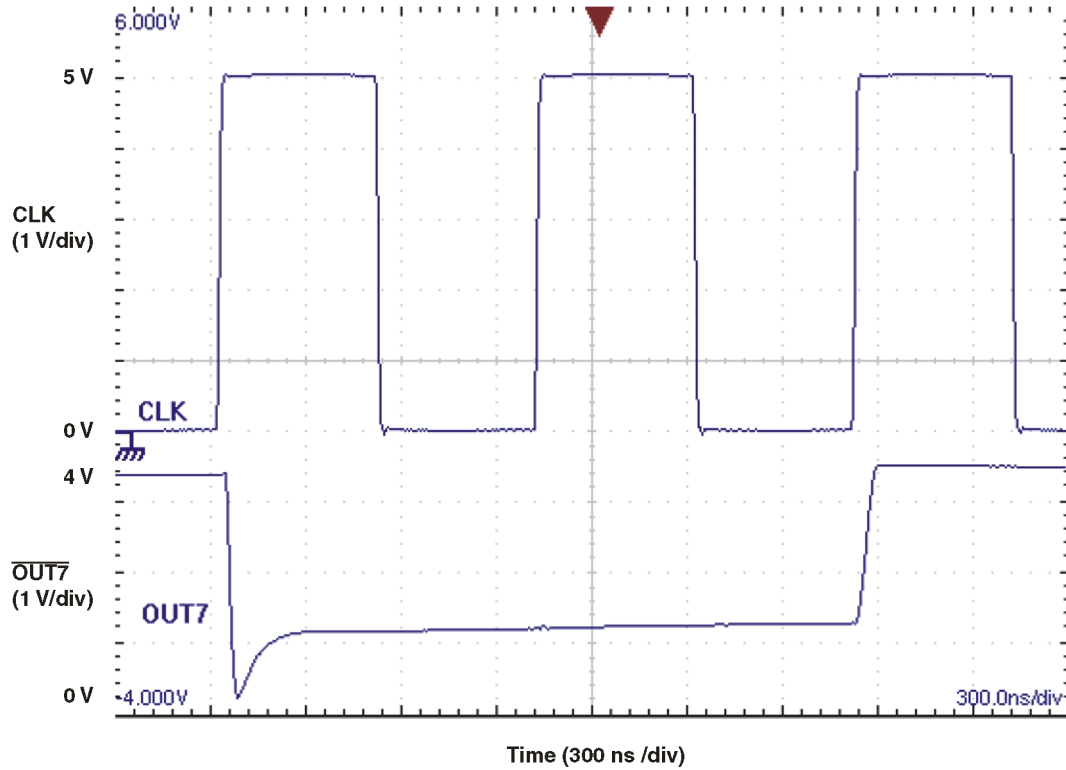


Figure 6. CLK to  $\overline{\text{OUT7}}$

$V_{DD} = 5\text{ V}$   
 $V_L = 4\text{ V}$   
 $R_{ext} = 840\ \Omega$   
 $R_L = 88\ \Omega$   
 $C_L = 10\text{ pF}$

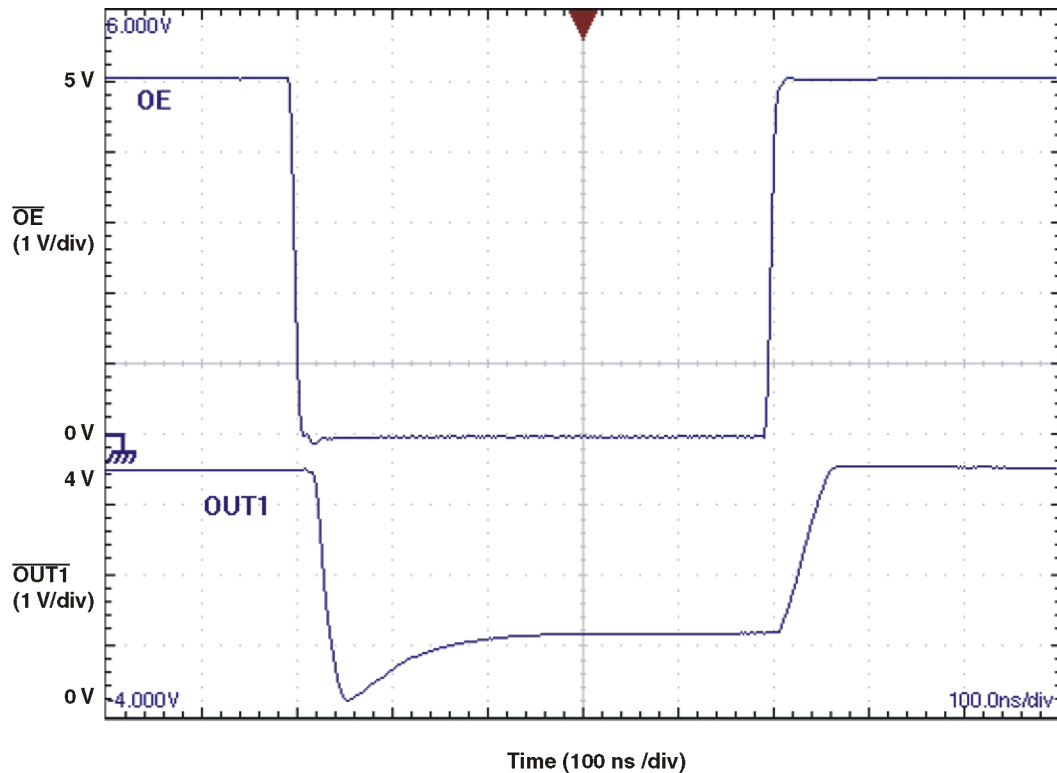


Figure 7.  $\overline{\text{OE}}$  to  $\overline{\text{OUT1}}$

$V_{DD} = 5\text{ V}$   
 $V_i = 4\text{ V}$   
 $R_{ext} = 840\ \Omega$   
 $R_L = 88\ \Omega$   
 $C_L = 10\text{ pF}$

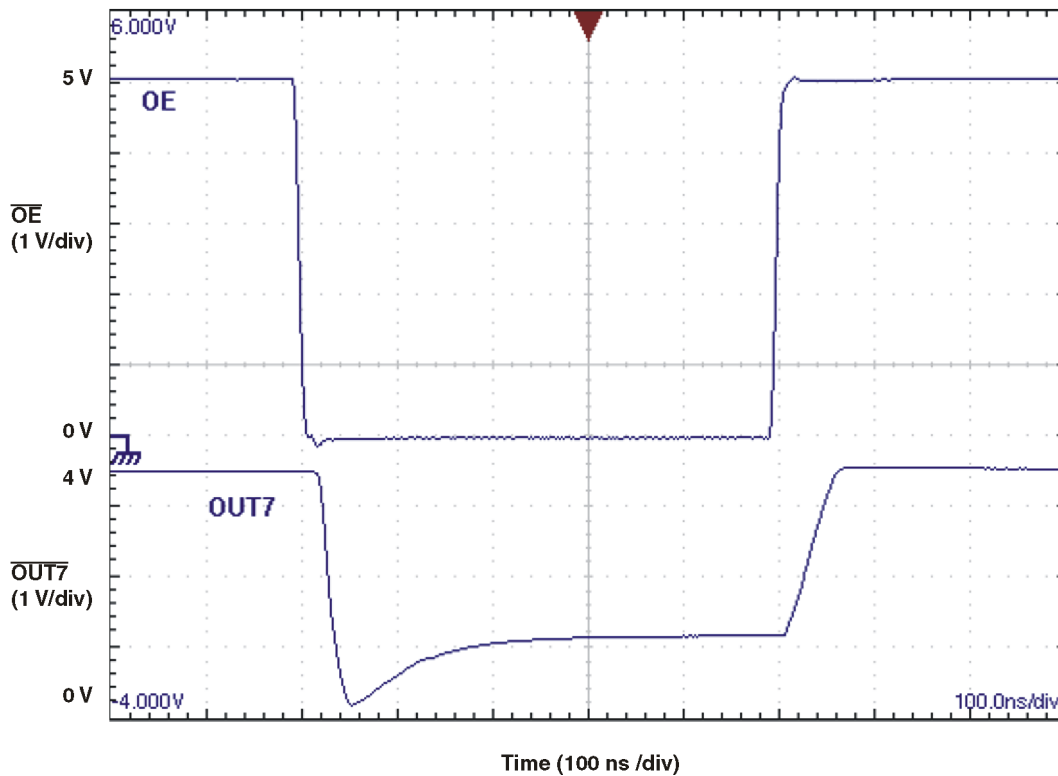


Figure 8.  $\overline{OE}$  to  $\overline{OUT7}$

**PACKAGING INFORMATION**

Orderable Device	Status <sup>(1)</sup>	Package Type	Package Drawing	Pins	Package Qty	Eco Plan <sup>(2)</sup>	Lead/Ball Finish	MSL Peak Temp <sup>(3)</sup>
TLC59025IDBQR	ACTIVE	SSOP/ QSOP	DBQ	24	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR

<sup>(1)</sup> The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

<sup>(2)</sup> Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

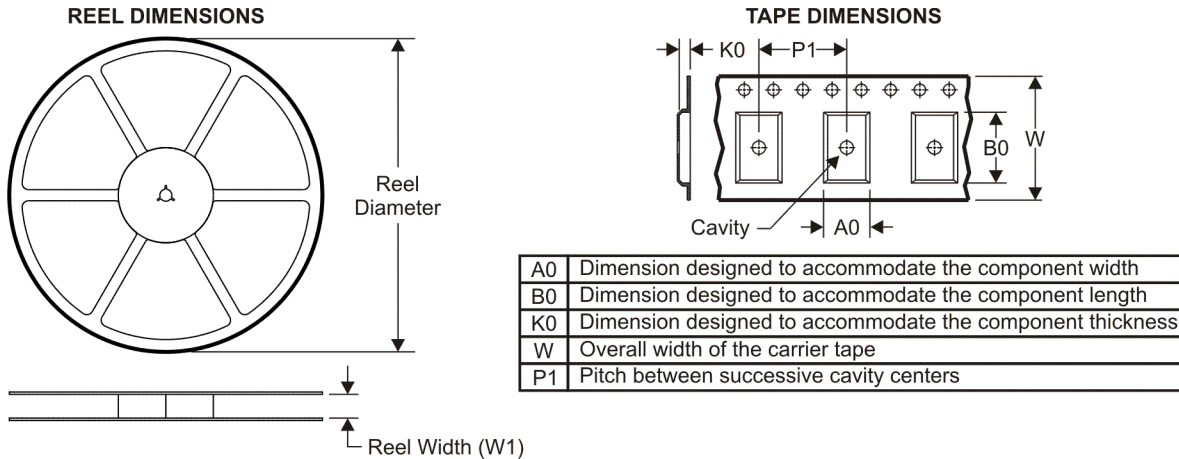
<sup>(3)</sup> MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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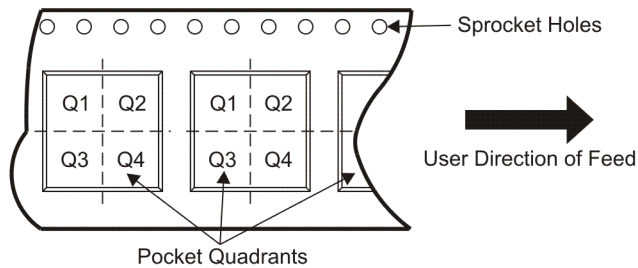
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**TAPE AND REEL INFORMATION**



**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TLC59025IDBQR	SSOP/QSOP	DBQ	24	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS

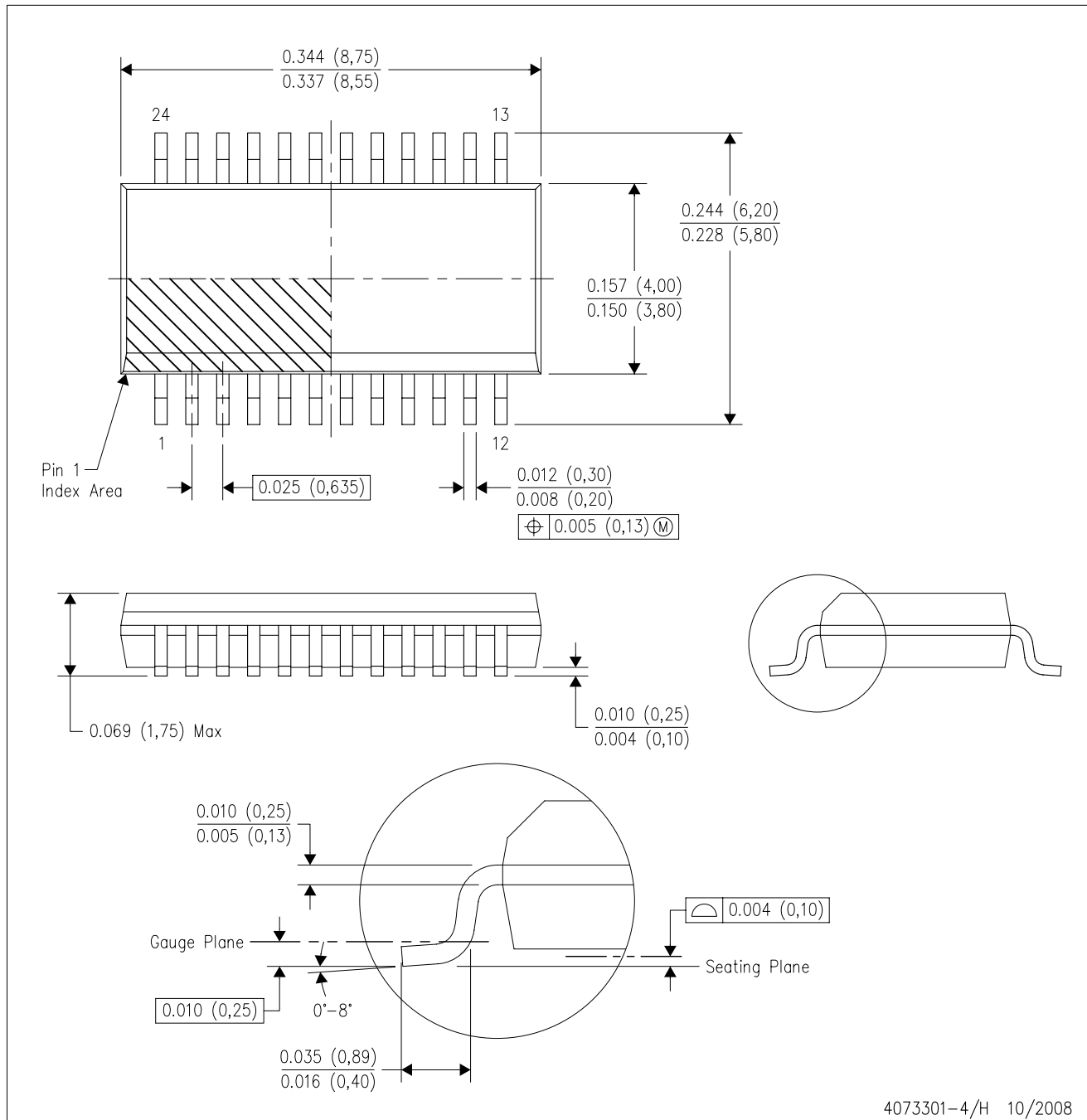


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TLC59025IDBQR	SSOP/QSOP	DBQ	24	2500	346.0	346.0	33.0

DBQ (R-PDSO-G24)

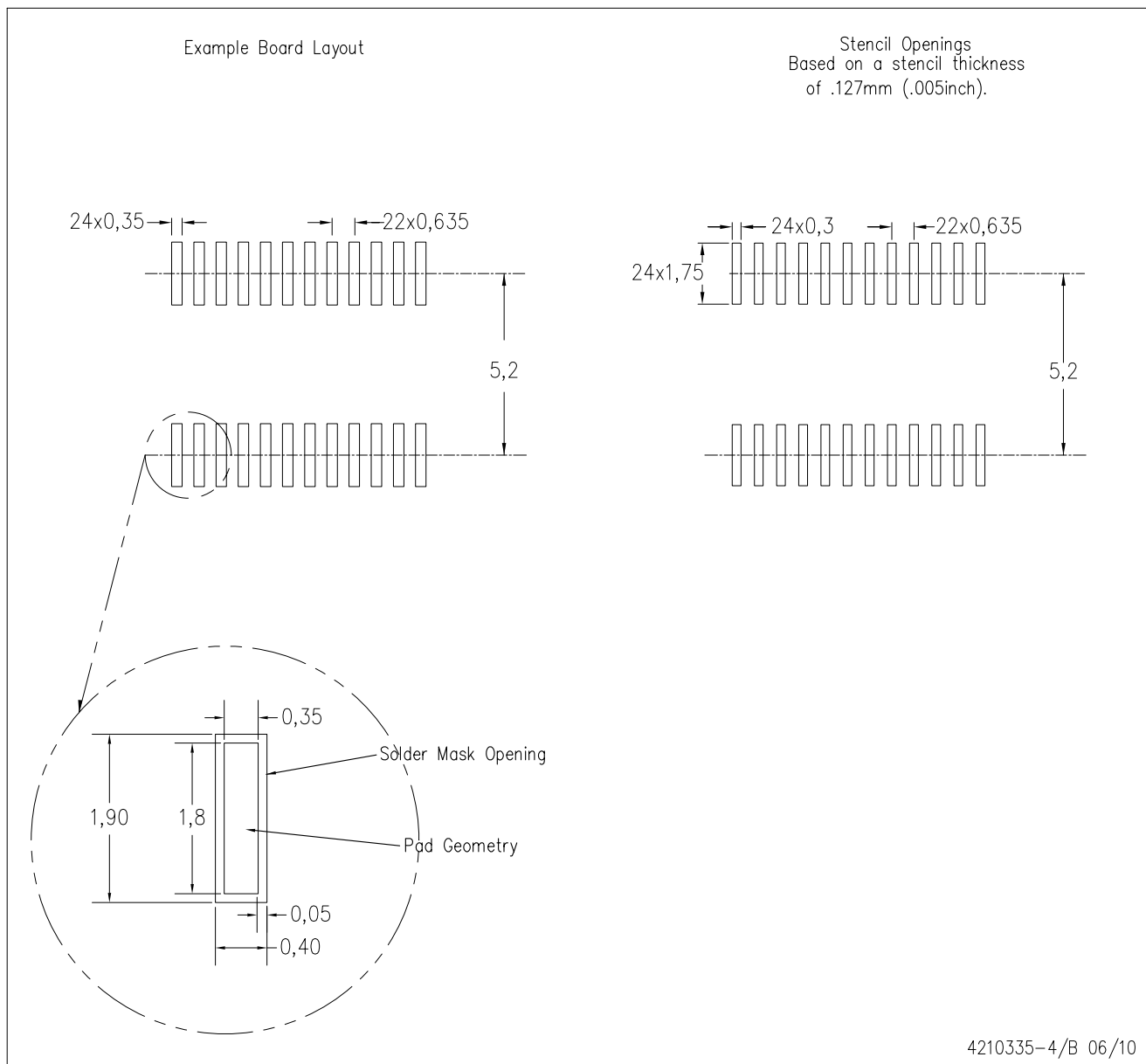
PLASTIC SMALL-OUTLINE PACKAGE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15) per side.
  - D. Falls within JEDEC MO-137 variation AE.

DBQ (R-PDSO-G24)

PLASTIC SMALL OUTLINE PACKAGE



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
  - D. Publication IPC-7351 is recommended for alternate designs.
  - E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC-7525 for other stencil recommendations.

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Logic	<a href="http://logic.ti.com">logic.ti.com</a>	Industrial	<a href="http://www.ti.com/industrial">www.ti.com/industrial</a>
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