- High-Performance Static CMOS Technology
- TMS470 16/32-Bit RISC Core (ARM7TDMI™)
  - 24-MHz System Clock (48-MHz Pipeline)
  - Independent 16/32-Bit Instruction Set
  - Open Architecture With Third-Party Support
  - Built-In Debug Module
- Integrated Memory
  - 128K-Byte Program Flash
    - One Bank With 10 Contiguous Sectors
  - 32K-Byte Program Flash with ECC
    - One Bank with 4 Contiguous Sectors
  - 8K-Byte Static RAM (SRAM)
- Operating Features
  - Low-Power Modes: Doze and Sleep
  - Industrial/Automotive Temperature Ranges
- System Module
  - 32-Bit Address Space Decoding
  - Bus Supervision for Memory/Peripherals
  - Real-Time Interrupt (RTI) Timer
  - Digital Watchdog (DWD) Timer
  - Analog Watchdog (AWD) Timer
  - Vectored Interrupt Module (VIM) with 32 Channels
  - System Integrity and Failure Detection
  - ICE Breaker
  - Cyclic Redundancy Checker (CRC) with Parallel Signature Analysis (PSA)
- Frequency-Modulated Zero-Pin Phase-Locked Loop ($FM_Z$PLL)-Based Clock Module With Prescaler
  - Multiply-by-8 Internal $FM_Z$PLL Option
- Six Communication Interfaces:
  - Serial Peripheral Interface (SPI)
    - 255 Programmable Baud Rates
  - Two Local Interconnect Network Interfaces (LINs)
    - Supports the Serial Communication Interface (SCI)
  - Standard CAN Controller (SCC)
    - 16-Mailbox Capacity
    - Fully Compliant With CAN Protocol, Version 2.0B
  - Class II Serial Interface B (C2SIb)
    - Normal 10.4 Kbps and 4X Mode 41.6 Kbps
  - Inter-Integrated Circuit (I2C) Module
    - Multi-Master and Slave Interfaces
    - Up to 400 Kbps (Fast Mode)
    - 7- and 10-Bit Address Capability
- High-End Timer (HET)
  - 29 Programmable I/O Channels:
    - 25 High-Resolution Pins
  - High-Resolution Share Feature (XOR)
  - High-End Timer RAM
    - 64-Instruction Capacity
- External Clock Prescale (ECP) Module
  - Programmable Low-Frequency External Clock (ECLK)
- 16-Channel 10-Bit Multi-Buffered ADC (MibADC)
  - 64-Word FIFO Buffer
  - Single- or Continuous-Conversion Modes
  - 1.55 μs Minimum Sample/Conversion Time
  - Calibration Mode and Self-Test Features
- 34 Dedicated General-Purpose I/O (GIO) Pins and 48 Additional Peripheral I/Os
- 32 External Interrupts
- On-Chip Scan-Base Emulation Logic, IEEE Standard 1149.1(1) (JTAG) Test-Access Port
- 144-Pin Pb-Free/Green Plastic Low-Profile Quad Flatpack (PGE Suffix)
- Development System Support Tools Available
  - Code Composer Studio™ Integrated Development Environment (IDE)
  - HET Assembler and Simulator
  - Real-Time In-Circuit Emulation
  - Flash Programming

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

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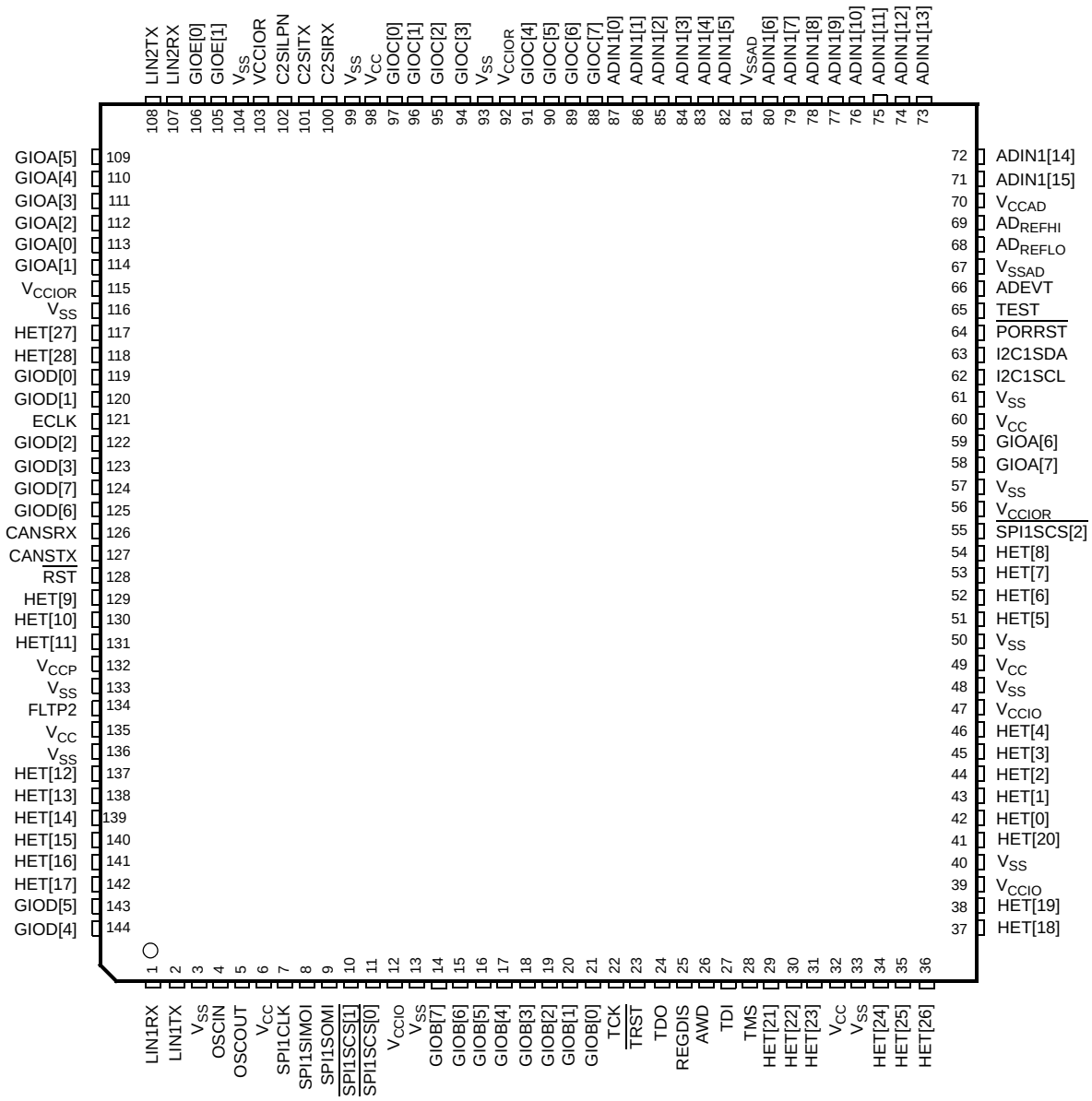
1 The test-access port is compatible with the IEEE Standard 1149.1-1990, *IEEE Standard Test-Access Port and Boundary Scan Architecture* specification. Boundary scan is not supported on this device.

**TMS470PLF111 144-PIN PGE PACKAGE (TOP VIEW)**



## description

The TMS470PLF111[1] devices are members of the Texas Instruments TMS470 family of general-purpose16/32-bit reduced instruction set computer (RISC) microcontrollers. The PLF111 microcontroller offers high performance utilizing the high-speed ARM7TDMI 16/32-bit RISC central processing unit (CPU), resulting in a high instruction throughput while maintaining greater code efficiency. The ARM7TDMI 16/32-bit RISC CPU views memory as a linear collection of bytes numbered upwards from zero. The TMS470PLF111 utilizes the big-endian format where the most significant byte of a word is stored at the lowest numbered byte and the least significant byte at the highest numbered byte.

High-end embedded control applications demand more performance from their controllers while maintaining low costs. The PLF111 RISC core architecture offers solutions to these performance and cost demands while maintaining low power consumption.

The real-time interrupt (RTI) module on the PLF111 has the option to be driven by the oscillator clock. The digital watchdog (DWD) is a 25-bit resettable decrementing counter that provides a system reset when the watchdog counter expires.

The PLF111 memory includes general-purpose SRAM supporting single-cycle read/write accesses in byte, half-word, and word modes.

The flash memory on this device is a nonvolatile, electrically erasable and programmable memory implemented with a 32-bit-wide data bus interface.The flash operates with a system clock frequency of up to 24 MHz. When in pipeline mode, the flash operates with a system clock frequency of up to 48 MHz. For more detailed information on the flash, see the flash section of this data sheet. The flash on the PLF111 device can be protected by means of ECC. This feature utilizes a single error correction and double error detection circuit (SECDED circuit) to correct single bit errors and detect double bit errors for each 64-bits of data. This is achieved by maintaining an 8-bit ECC checksum/code for each 64-bit double-word of memory space in a separate ECC RAM memory space.

The PLF111 device has six communication interfaces: SPI, two LINs, CAN (SCC), C2SI, and I2C. The SPI provides a convenient method of serial interaction for high-speed communications between similar shift-register type devices. The LIN is the local interconnect network interface which also supports the SCI - a full-duplex, serial I/O interface intended for asynchronous communication between the CPU and other peripherals using the standard non-return-to-zero (NRZ) format. The SCC uses a serial, multimaster communication protocol that efficiently supports distributed real-time control with robust communication rates of up to 1 megabit per second (Mbps). The SCC is ideal for applications operating in noisy and harsh environments (e.g., automotive and industrial fields) that require reliable serial communication or multiplexed wiring. The C2SIb allows the PLF111 to transmit and receive messages on a class II network following an SAE Standard J1850 Class B Data Communication Network Interface standard. The I2C module is a multi-master communication module providing an interface between the PLF111 microcontroller and an I2C-compatible device via the I2C serial bus. The I2C supports both 100 Kbps and 400 Kbps speeds.

The HET is an advanced intelligent timer that provides sophisticated timing functions for real-time applications. The timer is software-controlled, using a reduced instruction set, with a specialized timer micromachine and an attached I/O port. The HET can be used for compare, capture, or general-purpose I/O. It is especially well suited for applications requiring multiple sensor information and drive actuators with complex and accurate time pulses. The PLF111 HET peripheral contains the XOR-share feature. This feature allows two adjacent HET high- resolution channels to be XORed together, making it possible to output smaller pulses than a standard HET.

The PLF111 device has one 10-bit-resolution, sample-and-hold MibADC. Each of the MibADC channels can be grouped by software for sequential conversion sequences. There are three separate groupings, all three of which can be triggered by an external event. Each sequence can be converted once when triggered or configured for continuous conversion mode.

1 Throughout the remainder of this document, the TMS470PLF111 shall be referred to as either the full device name or PLF111.

## description (continued)

The frequency-modulated zero-pin phase-locked loop ($FM_Z$PLL) clock module contains a phase-locked loop, a clock-monitor circuit, a clock-enable circuit, and a prescaler (with prescale values of 1–8). The function of the $FM_Z$PLL is to multiply the external frequency reference to a higher frequency for internal use. The $FM_Z$PLL provides the input to the global clock module (GCM). The GCM module subsequently provides system clock (HCLK), real-time interrupt clock (RTICLK), CPU clock (GCLK), HET clock (VCLK2) and peripheral interface clock (VCLK) to all other PLF111 device modules.

The PLF111 device also has an external clock prescaler (ECP) module that when enabled, outputs a continuous external clock (ECLK). The ECLK frequency is a user-programmable ratio of the peripheral interface clock (VCLK) frequency.

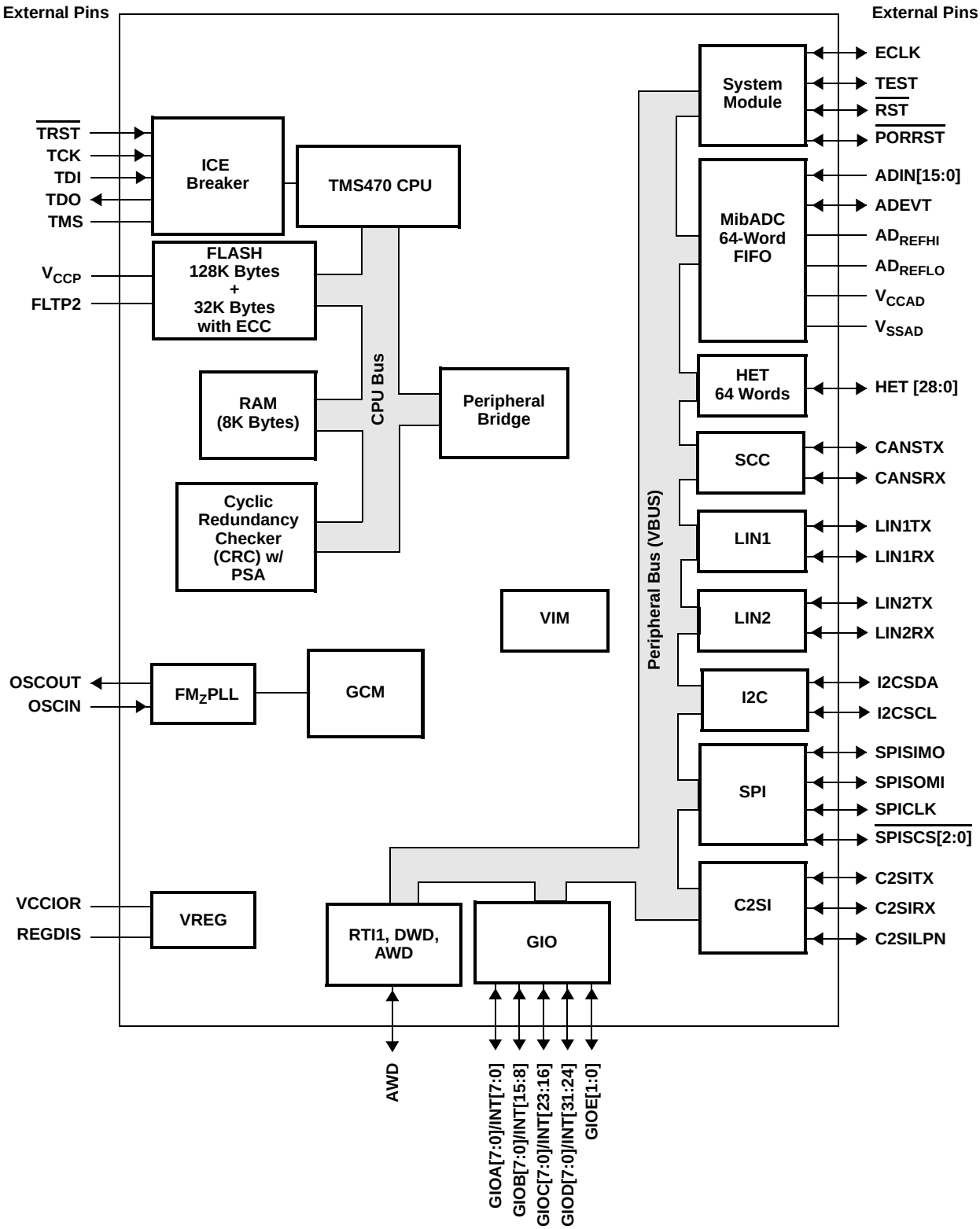
## device characteristics

The PLF111 device is a derivative of the F05 Platform Architecture. Table 1, Device Characteristics, identifies all the characteristics of the PLF111 device except the SYSTEM and CPU, which are generic.

**Table 1. Device Characteristics**

| CHARACTERISTICS | DEVICE DESCRIPTION TMS470PLF111 | COMMENTS FOR PLF111 |
|---|---|---|
| **MEMORY** | | |
| For device memory mapping, please see page 13. | | |
| INTERNAL MEMORY | Pipeline/Non-Pipeline<br><br>1 Bank 128K-Byte Flash<br>1 Bank 32K-Byte Flash with ECC<br>8K-Byte SRAM<br>CRC, 1-channel | Flash is pipeline-capable |
| **PERIPHERALS** | | |
| For the device-specific interrupt priority configurations, see the Interrupt Priority Table (Table 6, Interrupt Priority (VIM)). For the peripheral address ranges, see Table 3, Peripheral Memory and Table 4, Peripheral Select Map with Address Range. | | |
| CLOCK | $FM_ZPLL$ | Frequency-modulated zero-pin PLL has no external loop filter pins. |
| GENERAL-PURPOSE I/Os | 34 I/O | Ports A, B, C and D each have eight (8) external pins with external interrupt capability. Port E has only two (2) external pins. |
| ECP | YES | |
| LIN | 2 (2-pin) | Also supports SCI mode of operation |
| CAN (HECC and/or SCC) | SCC | |
| SPI | 1 | Three chip select pins. |
| C2SIb | 1 | |
| I2C | 1 | |
| HET with XOR Share | 29 I/O | The high-resolution (HR) SHARE feature allows even-numbered HR pins to share the next higher odd-numbered HR pin structures. This HR sharing is independent of whether or not the odd pin is available externally. If an odd pin is available externally and *shared*, then the odd pin can only be used as a general-purpose I/O. |
| HET RAM | 64-Instruction Capacity | |
| MibADC | 10-bit, 16-channel<br>64-word FIFO | Both the logic and registers for a full 16-channel MibADC are present. |
| CORE VOLTAGE | 1.8 V | |
| I/O VOLTAGE | 5 V | |
| PINS | 144 | |
| PACKAGE | PGE | |

## functional block diagram



## Terminal Functions

| TERMINAL NAME | TERMINAL PIN | INPUT VOLTAGE[1][2] | OUTPUT CURRENT[1][2] | INTERNAL PULLUP/ PULLDOWN[3] | DESCRIPTION |
|---|---|---|---|---|---|
| **HIGH-END TIMER (HET)** | | | | | |
| HET[0] | 42 | 5V | 2mA | 20 µA Programmable IPD | Timer input capture or output compare. The HET[28:0] applicable pins can be programmed as general-purpose input/output (GIO) pins. All are high-resolution pins.<br><br>The high-resolution (HR) SHARE feature allows even HR pins to share the next higher odd HR pin structures. This HR sharing is independent of whether or not the odd pin is available externally. If an odd pin is available externally and *shared*, then the odd pin can only be used as a general-purpose I/O. |
| HET[1] | 43 | | | | |
| HET[2] | 44 | | | | |
| HET[3] | 45 | | | | |
| HET[4] | 46 | | | | |
| HET[5] | 51 | | | | |
| HET[6] | 52 | | | | |
| HET[7] | 53 | | | | |
| HET[8] | 54 | | | | |
| HET[9] | 129 | | | | |
| HET[10] | 130 | | | | |
| HET[11] | 131 | | | | |
| HET[12] | 137 | | | | |
| HET[13] | 138 | | | | |
| HET[14] | 139 | | | | |
| HET[15] | 140 | | | | |
| HET[16] | 141 | | | | |
| HET[17] | 142 | | | | |
| HET[18] | 37 | | | | |
| HET[19] | 38 | | | | |
| HET[20] | 41 | | | | |
| HET[21] | 29 | | | | |
| HET[22] | 30 | | | | |
| HET[23] | 31 | | | | |
| HET[24] | 34 | | | | |
| HET[25] | 35 | | | | |
| HET[26] | 36 | | | | |
| HET[27] | 117 | | | | |
| HET[28] | 118 | | | | |
| **STANDARD CAN CONTROLLER (SCC)** | | | | | |
| CANSRX | 126 | 5V | 2mA | 20 uA IPU | SCC receive pin or GIO pin |
| CANSTX | 127 | | 4mA | | SCC transmit pin or GIO pin |
| **CLASS II SERIAL INTERFACE (C2SIB)** | | | | | |
| C2SILPN | 102 | 5V | 2mA | 20 µA Programmable IPU/IPD | C2SI module loopback enable pin or GIO pin |
| C2SIRX | 100 | | 2mA | | C2SI module receive data input pin or GIO pin |
| C2SITX | 101 | | 4mA | | C2SI module transmit data output pin or GIO pin |

1 PWR = power, GND = ground, REF = reference voltage, NC = no connect
2 All I/O pins, except $\overline{\text{RST}}$, are configured as inputs while $\overline{\text{PORRST}}$ is low and immediately after $\overline{\text{PORRST}}$ goes high.
3 IPD = internal pulldown, IPU = internal pullup (all internal pullups and pulldowns are active on input pins, independent of the $\overline{\text{PORRST}}$ state.). Programmable IPU's/IPD's are disabled by default, except for I2C1SDA and I2C1SCL.

## Terminal Functions (Continued)

| TERMINAL NAME | TERMINAL PIN | INPUT VOLTAGE[1][2] | OUTPUT CURRENT[1][2] | INTERNAL PULLUP/ PULL-DOWN[3] | DESCRIPTION |
|---|---|---|---|---|---|
| **GENERAL-PURPOSE I/O (GIO)** | | | | | |
| GIOA[0]/INT[0] | 113 | 5V | 2mA | 20 μA Programmable IPD/IPU | General-purpose input/output pins.<br><br>GIOA[7:0]/INT[7:0], GIOB[7:0]/INT[15:8], GIOC[7:0]/INT[23:16], and GIOD[7:0]/INT[31:24] are interrupt-capable pins. |
| GIOA[1]/INT[1] | 114 | | | | |
| GIOA[2]/INT[2] | 112 | | | | |
| GIOA[3]/INT[3] | 111 | | | | |
| GIOA[4]/INT[4] | 110 | | | | |
| GIOA[5]/INT[5] | 109 | | | | |
| GIOA[6]/INT[6] | 59 | | | | |
| GIOA[7]/INT[7] | 58 | | | | |
| GIOB[0]/INT[8] | 21 | | | | |
| GIOB[1]/INT[9] | 20 | | | | |
| GIOB[2]/INT[10] | 19 | | | | |
| GIOB[3]/INT[11] | 18 | | | | |
| GIOB[4]/INT[12] | 17 | | | | |
| GIOB[5]/INT[13] | 16 | | | | |
| GIOB[6]/INT[14] | 15 | | | | |
| GIOB[7]/INT[15] | 14 | | | | |
| GIOC[0]/INT[16] | 97 | | | | |
| GIOC[1]/INT[17] | 96 | | | | |
| GIOC[2]/INT[18] | 95 | | | | |
| GIOC[3]/INT[19] | 94 | | | | |
| GIOC[4]/INT[20] | 91 | | | | |
| GIOC[5]/INT[21] | 90 | | | | |
| GIOC[6]/INT[22] | 89 | | | | |
| GIOC[7]/INT[23] | 88 | | | | |
| GIOD[0]/INT[24] | 119 | | | | |
| GIOD[1]/INT[25] | 120 | | | | |
| GIOD[2]/INT[26] | 122 | | | | |
| GIOD[3]/INT[27] | 123 | | | | |
| GIOD[4]/INT[28] | 144 | | | | |
| GIOD[5]/INT[29] | 143 | | | | |
| GIOD[6]/INT[30] | 125 | | | | |
| GIOD[7]/INT[31] | 124 | | | | |
| GIOE[0] | 106 | | | | |
| GIOE[1] | 105 | | | | |

1 PWR = power, GND = ground, REF = reference voltage, NC = no connect
2 All I/O pins, except $\overline{\text{RST}}$, are configured as inputs while $\overline{\text{PORRST}}$ is low and immediately after $\overline{\text{PORRST}}$ goes high.
3 IPD = internal pulldown, IPU = internal pullup (all internal pullups and pulldowns are active on input pins, independent of the $\overline{\text{PORRST}}$ state.) Programmable IPU's/IPD's are disabled by default, except for I2C1SDA and I2C1SCL.

## Terminal Functions (Continued)

| TERMINAL NAME | TERMINAL PIN | INPUT VOLTAGE(1)(2) | OUTPUT CURRENT(1)(2) | INTERNAL PULLUP/ PULLDOWN(3) | DESCRIPTION |
|---|---|---|---|---|---|
| **MULTI-BUFFERED ANALOG-TO-DIGITAL CONVERTER (MibADC)** | | | | | |
| ADEVT | 66 | 5V | 2mA | 20 uA Programmable Pull-up/pull-down | MibADC event input. Can be programmed as a GIO pin. |
| ADIN[0] | 87 | 5V | | | MibADC analog input pins |
| ADIN[1] | 86 | | | | |
| ADIN[2] | 85 | | | | |
| ADIN[3] | 84 | | | | |
| ADIN[4] | 83 | | | | |
| ADIN[5] | 82 | | | | |
| ADIN[6] | 80 | | | | |
| ADIN[7] | 79 | | | | |
| ADIN[8] | 78 | | | | |
| ADIN[9] | 77 | | | | |
| ADIN[10] | 76 | | | | |
| ADIN[11] | 75 | | | | |
| ADIN[12] | 74 | | | | |
| ADIN[13] | 73 | | | | |
| ADIN[14] | 72 | | | | |
| ADIN[15] | 71 | | | | |
| $AD_{REFHI}$ | 69 | 5V REF | | | MibADC module high-voltage reference input |
| $AD_{REFLO}$ | 68 | GND REF | | | MibADC module low-voltage reference input |
| $V_{CCAD}$ | 70 | 5V REF | | | MibADC analog supply voltage |
| $V_{SSAD}$ | 67<br>81 | GND REF | | | MibADC analog ground reference |
| **SERIAL PERIPHERAL INTERFACE (SPI)** | | | | | |
| $\overline{SPISCS[0]}$ | 11 | 5V | 2mA | 20 uA Programmable Pull-up/pull-down | SPI slave chip select. Can be programmed as a GIO pin. |
| $\overline{SPISCS[1]}$ | 10 | | | | |
| $\overline{SPISCS[2]}$ | 55 | | | | |
| SPICLK | 7 | 5V | 4mA | | SPI clock. SPICLK can be programmed as a GIO pin. |
| SPISIMO | 8 | | | | SPI data stream. Slave in/master out. Can be programmed as a GIO pin. |
| SPISOMI | 9 | | | | SPI data stream. Slave out/master in. Can be programmed as a GIO pin. |
| **BUFFERED LOCAL INTERCONNECT NETWORK 1 (LIN1)** | | | | | |
| LIN1RX | 1 | 5V | 2mA | 20 uA Programmable Pull-up/pull-down | LIN1/SCI1 data receive.Ccan be programmed as a GIO pin. |
| LIN1TX | 2 | | | | LIN1/SCI1 data transmit. Can be programmed as a GIO pin. |
| **BUFFERED LOCAL INTERCONNECT NETWORK 2 (LIN2)** | | | | | |
| LIN2RX | 107 | 5V | 2mA | 20 uA Programmable Pull-up/pull-down | LIN2/SCI2 data receive. Can be programmed as a GIO pin. |
| LIN2TX | 108 | | | | LIN2/SCI2 data transmit. Can be programmed as a GIO pin. |

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3 IPD = internal pulldown, IPU = internal pullup (all internal pullups and pulldowns are active on input pins, independent of the $\overline{PORRST}$ state.) Programmable IPU's/IPD's are disabled by default, except for I2C1SDA and I2C1SCL.

## Terminal Functions (Continued)

| TERMINAL NAME | TERMINAL PIN | INPUT VOLTAGE[1][2] | OUTPUT CURRENT[1][2] | INTERNAL PULLUP/ PULLDOWN[3] | DESCRIPTION |
|---|---|---|---|---|---|
| **INTER-INTEGRATED CIRCUIT (I2C)** | | | | | |
| I2CSDA | 62 | 5V | 2mA | 20 μA Programmable Pull-up | I2C serial data pin or GIO pin |
| I2CSCL | 63 | | | | I2C serial clock pin or GIO pin |
| **FREQUENCY-MODULATED ZERO-PIN PHASE-LOCKED LOOP ($FM_Z$PLL)** | | | | | |
| OSCIN | 4 | 1.8-V | | | Crystal connection pin or external clock input |
| OSCOUT | 5 | | 8mA | | External crystal connection pin |
| **SYSTEM MODULE (SYS)** | | | | | |
| ECLK | 121 | 5V | 8mA | 20 uA Programmable Pull-up/pull-down | Bidirectional pin. ECLK can be programmed as a GIO pin or the output of VCLK. |
| $\overline{\text{PORRST}}$ | 64 | 5V | | IPD (100 μA) | Input master chip power-up reset. External $V_{CC}$ monitor circuitry must assert a power-on reset. |
| $\overline{\text{RST}}$ | 128 | 5V | 4mA | IPU (100 μA) | Bidirectional reset. The internal circuitry can assert a reset, and an external system reset can assert a device reset.<br>On this pin, the output buffer is implemented as an open drain (drives low only).<br>To ensure an external reset is not arbitrarily generated, TI recommends that an external pullup resistor be connected to this pin. |
| REGDIS | 25 | 5V | | IPD (100 μA) | Enables/disables the internal voltage regulator. Pulling this pin high disables the internal voltage regulator. Pulling this pin low enables the internal voltage regulator. **Low power modes are not supported if the internal voltage regulator is disabled.** |
| **WATCHDOG/REAL-TIME INTERRUPT (WD/RTI)** | | | | | |
| AWD | 26 | 5V | 8mA | | Analog watchdog reset. The AWD pin provides a system reset if the WD KEY is not written in time by the system, providing an external RC network circuit is connected. If the user is not using AWD, TI recommends that this pin be connected to ground or pulled down to ground by an external resistor.<br><br>For more details on the external RC network circuit, see the application note *Analog Watchdog Resistor, Capacitor and Discharge Interval Selection Constraints* (literature number SPNA005). |
| **TEST/DEBUG (T/D)** | | | | | |
| TCK | 22 | 5V | | IPD (100 μA) | Test clock. TCK controls the test hardware (JTAG). |
| TDI | 27 | 5V | | IPU (100 μA) | Test data in. TDI inputs serial data to the test instruction register, test data register, and programmable test address (JTAG). |
| TDO | 24 | | 8mA | | Test data out. TDO outputs serial data from the test instruction register, test data register, identification register, and programmable test address (JTAG). |
| TEST | 65 | 5V | | IPD (100 μA) | Test enable. Reserved for internal use only. TI recommends that this pin be connected to ground or pulled down to ground by an external resistor. |
| TMS | 28 | 5V | | IPU (100 μA) | Serial input for controlling the state of the CPU test access port (TAP) controller (JTAG). |
| $\overline{\text{TRST}}$ | 23 | 5V | | IPD (100 μA) | Test hardware reset to TAP. IEEE Standard 1149-1 (JTAG) Boundary-Scan Logic. |

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3 IPD = internal pulldown, IPU = internal pullup (all internal pullups and pulldowns are active on input pins, independent of the $\overline{\text{PORRST}}$ state.) Programmable IPU's/IPD's are disabled by default, except for I2C1SDA and I2C1SCL.

## Terminal Functions (Continued)

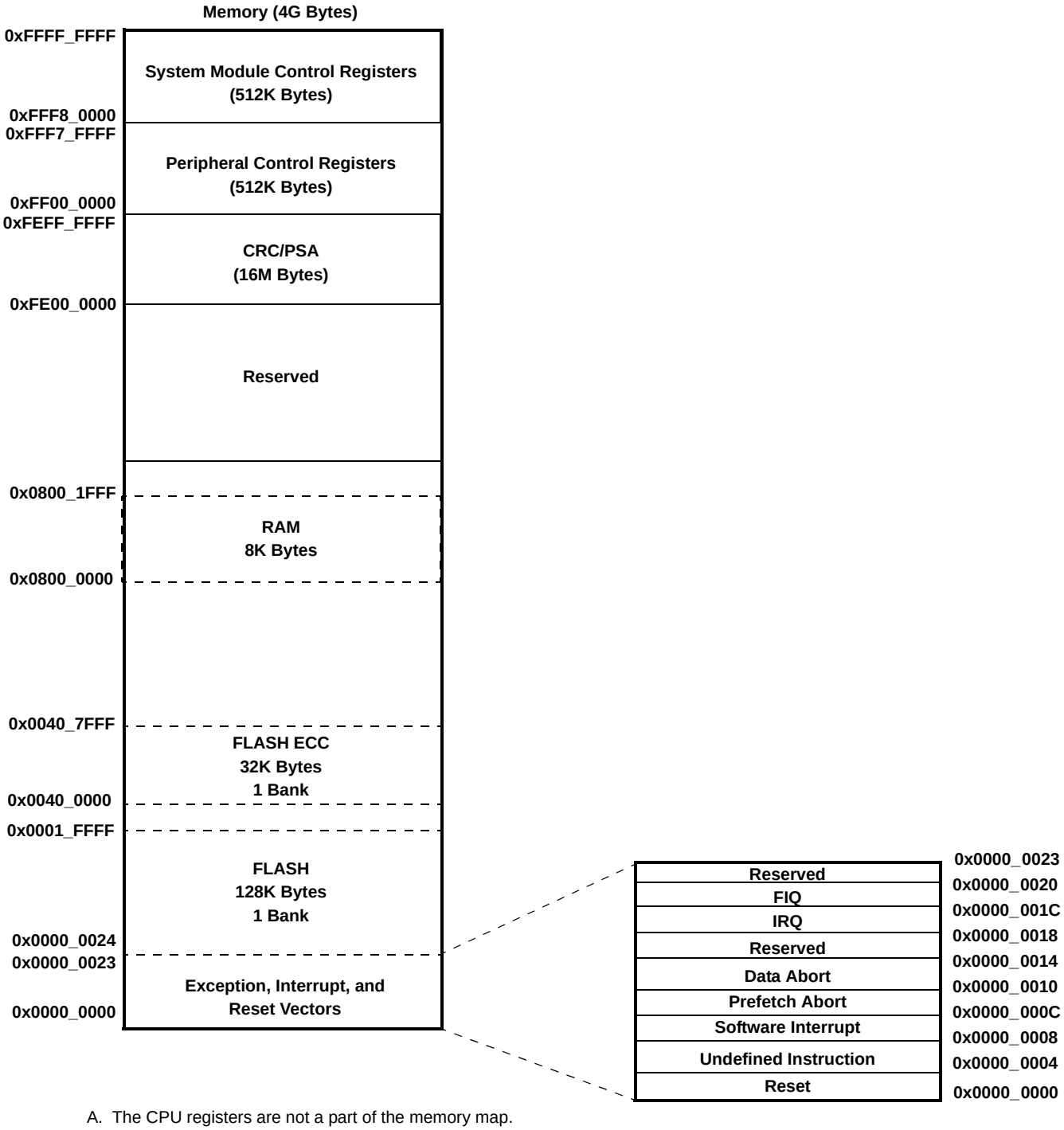
| TERMINAL NAME | PIN | INPUT VOLTAGE(1)(2) | OUTPUT CURRENT(1)(2) | INTERNAL PULLUP/ PULL-DOWN(3) | DESCRIPTION |
|---|---|---|---|---|---|
| **FLASH** | | | | | |
| FLTP2 | 134 | 5V | | | Flash test pad 2. **For proper operation, this pin must not be connected [no connect (NC)].** |
| $V_{CCP}$ | 132 | 5V PWR | | | Flash external pump voltage (5 V). This pin is required for both Flash read and Flash program and erase operations. |
| **SUPPLY VOLTAGE CORE (1.8 V)** | | | | | |
| $V_{CC}$ | 6<br>32<br>49<br>60<br>98<br>135 | 1.8-V PWR | | | VREG output voltage / Core logic supply voltage<br>The functionality of the Vcc pins are dependant upon the state of the REGDIS pin. If REGDIS pin is HIGH, the internal VREG is disabled and core logic voltage should be supplied through these pins. If REGDIS pin is LOW, the internal VREG is enabled and the VREG output voltage is output on these pins. |
| **SUPPLY VOLTAGE DIGITAL I/O AND REGULATOR (5 V)** | | | | | |
| $V_{CCIO}$ | 12<br>39<br>47 | 5-V PWR | | | Digital I/O supply voltage |
| $V_{CCIOR}$ | 56<br>92<br>103<br>115 | | | | Digital I/O and internal regulator supply voltage |
| **SUPPLY GROUND CORE** | | | | | |
| $V_{SS}$ | 3<br>33<br>50<br>61<br>99<br>133<br>136 | GND | | | Core supply ground reference |
| **SUPPLY GROUND DIGITAL I/O** | | | | | |
| $V_{SSIO}$ | 13<br>40<br>48<br>57<br>93<br>104<br>116 | GND | | | Digital I/O supply ground reference |

1 PWR = power, GND = ground, REF = reference voltage, NC = no connect
2 All I/O pins, except $\overline{RST}$, are configured as inputs while $\overline{PORRST}$ is low and immediately after $\overline{PORRST}$ goes high.
3 IPD = internal pulldown, IPU = internal pullup (all internal pullups and pulldowns are active on input pins, independent of the $\overline{PORRST}$ state.) Programmable IPU's/IPD's are disabled by default, except for I2C1SDA and I2C1SCL.

## PLF111 DEVICE-SPECIFIC INFORMATION

### memory map

Figure 1 shows the memory map of the PLF111 device.




A. The CPU registers are not a part of the memory map.

**Figure 1. TMS470PLF111 Memory Map**

## memory selects

Memories in the PLF111 device are located at fixed addresses. Tables below detail the mapping of the memory regions.

**Table 2. Memory Frame Assignment**

| MEMORY FRAME NAME | BASE ADDRESS | ENDING ADDRESS | MEMORY TYPE | ACTUAL MEMORY SIZE |
|---|---|---|---|---|
| nCS0 | 0x0000 0000 | 0x0001 FFFF | Flash | 128KBytes |
| | 0x0040 0000 | 0x0040 7FFF | Flash-ECC | 32KBytes |
| CSRAM0 | 0x0800 0000 | 0x0800 1FFF | Internal RAM | 8KBytes |

**Table 3. Peripheral Memory**

| PERIPHERAL MEMORY NAME | ADDRESS RANGE | | PERIPHERAL MEMORY CHIP SELECT | PERIPHERAL MEMORY POWERDOWN CONTROL REGISTER |
|---|---|---|---|---|
| | BASE ADDRESS | ENDING ADDRESS | | |
| CAN (SCC) RAM | 0xFF1E 0000 | 0xFF1F FFFF | PCS[15] | PCSPWRDWNSET0[15] |
| ADC RAM | 0xFF3E 0000 | 0xFF3F FFFF | PCS[31] | PCSPWRDWNSET0[31] |
| HET RAM | 0xFF46 0000 | 0xFF47 FFFF | PCS[35] | PCSPWRDWNSET1[3] |

**Table 4. Peripheral Select Map with Address Range**

| PERIPHERAL NAME | ADDRESS RANGE | | PERIPHERAL SELECT | PERIPHERAL POWERDOWN CONTROL REGISTER |
|---|---|---|---|---|
| | BASE ADDRESS | ENDING ADDRESS | | |
| SPI | 0xFFF7 F400 | 0xFFF7 F5FF | PS[2] | PSPWRDWNSET0[9:8] |
| LIN2 | 0xFFF7 E600 | 0xFFF7 E6FF | PS[6] | PSPWRDWNSET0[26] |
| LIN1 | 0xFFF7 E500 | 0xFFF7 E5FF | PS[6] | PSPWRDWNSET0[25] |
| SCC | 0xFFF7 DC00 | 0xFFF7 DCFF | PS[8] | PSPWRDWNSET1[0] |
| I2C | 0xFFF7 D400 | 0xFFF7 D4FF | PS[10] | PSPWRDWNSET1[8] |
| C2SI | 0xFFF7 D000 | 0xFFF7 D0FF | PS[11] | PSPWRDWNSET1[12] |
| MibADC | 0xFFF7 C000 | 0xFFF7 C1FF | PS[15] | PSPWRDWNSET1[29:28] |
| GIO | 0xFFF7 BC00 | 0xFFF7 BDFF | PS[16] | PSPWRDWNSET2[1:0] |
| HET | 0xFFF7 B800 | 0xFFF7 B8FF | PS[17] | PSPWRDWNSET2[4] |

**Table 5. System Peripheral Registers**

| FRAME NAME | BASE ADDRESS | ENDING ADDRESS |
|---|---|---|
| CRC/PSA | 0xFE00 0000 | 0xFEFF FFFF |
| VIM RAM | 0xFFF8 2000 | 0xFFF8 2FFF |
| Flash wrapper | 0xFFF8 7000 | 0xFFF8 7FFF |
| PCR Registers | 0xFFFF E000 | 0xFFFF E0FF |
| RTI | 0xFFFF FC00 | 0xFFFF FCFF |
| VIM Registers | 0xFFFF FE00 | 0xFFFF FEFF |
| System Registers | 0xFFFF FF00 | 0xFFFF FFFF |

## memory

### F05 flash

The F05 flash memory is a nonvolatile electrically erasable and programmable memory implemented with a 32-bit-wide data bus interface. The F05 flash has an external state machine for programming and erase functions.

The PLF111 flash memory and internal static RAM memory locations can be swapped by configuring the SYS module BMMCR1 register.

**NOTE**

**The flash external pump voltage ($V_{CCP}$) is required for all operations (program, erase, and read).**

#### *flash protection keys*

The PLF111 device provides flash protection keys. These four 32-bit protection keys prevent program/erase/compaction operations from occurring until after the four protection keys have been matched by the CPU loading the correct user keys into the FMPKEY control register. The protection keys on the PLF111 are located in the last 4 words of the first 8K sector.

#### *flash pipeline mode*

When in pipeline mode, the flash operates with a system clock frequency of up to 48 MHz (versus a system clock frequency of 24 MHz in normal mode). Flash in pipeline mode is capable of accessing 64-bit words and provides two 32-bit pipelined words to the CPU. Also, in pipeline mode the Flash can be read with no wait states when memory addresses are sequential (after the initial 1- or 2-wait-state reads).

**NOTE**

**After a system reset, pipeline mode is disabled (ENPIPE bit [FMREGOPT.0] is a "0"). In other words, the PLF111 device powers up and comes out of reset in non-pipeline mode with a default number of wait states set to 1.**

## memory (continued)

### *flash program and erase*

The PLF111 device flash contains one 128K-byte memory array (or bank) and consists of ten sectors. These ten sectors are sized as follows:

| SECTOR NO. | SEGMENT | LOW ADDRESS | HIGH ADDRESS | MEMORY ARRAYS (OR BANKS) |
|---|---|---|---|---|
| 0 | 8K Bytes | 0x0000_0000 | 0x0000_1FFF | BANK0 (128K Bytes) |
| 1 | 8K Bytes | 0x0000_2000 | 0x0000_3FFF | |
| 2 | 16K Bytes | 0x0000_4000 | 0x0000_7FFF | |
| 3 | 16K Bytes | 0x0000_8000 | 0x0000_BFFF | |
| 4 | 16K Bytes | 0x0000_C000 | 0x0000_FFFF | |
| 5 | 16K Bytes | 0x0001_0000 | 0x0001_3FFF | |
| 6 | 16K Bytes | 0x0001_4000 | 0x0001_7FFF | |
| 7 | 16K Bytes | 0x0001_8000 | 0x0001_BFFF | |
| 8 | 8K Bytes | 0x0001_C000 | 0x0001_DFFF | |
| 9 | 8K Bytes | 0x0001_E000 | 0x0001_FFFF | |

The minimum size for an erase operation is one sector. The maximum size for a program operation is one 16-bit word.

The PLF111 device also contains flash ECC memory. The flash ECC bank (BANK1) is 16 bits wide and cannot be reused for program storage and execution. Only sectors 0 and 1 are used for ECC. The bank is sized as follows:

| SECTOR NO. | SEGMENT | LOW ADDRESS | HIGH ADDRESS | MEMORY ARRAYS (OR BANKS) |
|---|---|---|---|---|
| 0 | 8K Bytes | 0x0040_0000 | 0x0040_1FFF | BANK1 (32K Bytes) |
| 1 | 8K Bytes | 0x0040_2000 | 0x0040_3FFF | |
| 2 | 8K Bytes | 0x0040_4000 | 0x0000_5FFF | |
| 3 | 8K Bytes | 0x0040_6000 | 0x0000_7FFF | |

**NOTE**

**The flash external pump voltage ($V_{CCP}$) is required for all operations (program, erase, and read).**

### interrupt priority (VIM)

The vectored interrupt module (VIM) provides a fully programmable priority scheme. Interrupt requests originating from the PLF111 peripheral modules (i.e., SPI; LIN1 or LIN2; RTI; etc.) are assigned to channels within the 32-channel VIM where, via programmable register mapping, the interrupt priority of the channels can be changed. Programming multiple interrupt sources to the same VIM channel effectively shares the VIM channel between sources.

The VIM request channels are maskable so that individual channels can be selectively disabled. All interrupt requests can be programmed in the VIM to be of either type:

- Fast interrupt request (FIQ)
- Normal interrupt request (IRQ)

The VIM prioritizes interrupts. The precedences of request channels decrease with ascending channel order in the VIM (0 [highest] and 31 [lowest] priority). For VIM default mapping, channel priorities, and their associated modules, see Table 6, Interrupt Priority (VIM).

**Table 6. Interrupt Priority (VIM)**

| MODULES | INTERRUPT SOURCES | DEFAULT VIM INTERRUPT REQUEST MAPPING |
|---|---|---|
| System | System error | 0 |
| System | SW interrupt (SSI) | 1 |
| RTI | RTI compare interrupt 0 | 2 |
| RTI | RTI compare interrupt 1 | 3 |
| RTI | RTI compare interrupt 2 | 4 |
| RTI | RTI compare interrupt 3 | 5 |
| RTI | RTI overflow interrupt 0 | 6 |
| RTI | RTI overflow interrupt 1 | 7 |
| RESERVED | | 8 |
| GIO | GIO interrupt A | 9 |
| GIO | GIO interrupt B | 10 |
| HET | HET level 0 interrupt | 11 |
| HET | HET level 1 interrupt | 12 |
| SPI1 | SPI1 level 0 interrupt | 13 |
| SPI1 | SPI1 level 1 interrupt | 14 |
| LIN2 | LIN2 level 0 interrupt | 15 |
| LIN2 | LIN2 level 1 interrupt | 16 |
| SCC | SCC level 0 interrupt | 17 |
| SCC | SCC level 1 interrupt | 18 |
| ADC | ADC level 0 interrupt | 19 |
| ADC | ADC level 1 interrupt | 20 |
| I2C | I2C level 0 interrupt | 21 |
| I2C | I2C level 1 interrupt | 22 |
| FLASH ECC | Flash ECC interrupt | 23 |
| RESERVED | | 24 |
| C2SIb | C2SIb interrupt | 25 |

## interrupt priority (VIM) (continued)

**Table 6, Interrupt Priority (VIM). Interrupt Priority (VIM) (Continued)**

| MODULES | INTERRUPT SOURCES | DEFAULT VIM INTERRUPT REQUEST MAPPING |
|---|---|---|
| LIN1 | LIN1 level 0 interrupt | 26 |
| LIN1 | LIN1 level 1 interrupt | 27 |
| RESERVED | | 28 |
| RESERVED | | 29 |
| RESERVED | | 30 |
| RESERVED | | 31 |

## MibADC

The multi-buffered analog-to-digital converter (MibADC) accepts an analog signal and converts the signal to a 10-bit digital value.

The PLF111 MibADC module stores its digital results in one of three FIFO buffers. There is one FIFO buffer for each conversion group [event, group1 (G1), and group2 (G2)], and the total MibADC FIFO on the device is divided amongst these three regions. The size of the individual group buffers are software programmable. MibADC buffers can be serviced by interrupts.

### MibADC event trigger capability

- All three conversion groups can be configured for event-triggered operation, providing up to three event-triggered groups.
- The trigger source and polarity can be selected individually for group 1, group 2 and the event group from the options identified in Table 7, MibADC Event Hookup Configuration.

**Table 7. MibADC Event Hookup Configuration**

| EVENT # | SOURCE SELECT BITS FOR G1, G2, OR EVENT (G1SRC[1:0], G2SRC[1:0], or EVSRC[1:0]) | SIGNAL PIN NAME |
|---|---|---|
| EVENT1 | 000 | ADEVT |
| EVENT2 | 001 | HET1 |
| EVENT3 | 010 | HET3 |
| EVENT4 | 011 | Reserved |
| EVENT5 | 100 | Reserved |
| EVENT6 | 101 | Reserved |
| EVENT7 | 110 | Reserved |
| EVENT8 | 111 | Reserved |

## development system support

Texas Instruments provides extensive hardware and software development support tools for the TMS470 family. These support tools include:

- Code Composer Studio™ Integrated Development Environment (IDE)
  - Fully integrated suite of software development tools
  - Includes Compiler/Assembler/Linker, Debugger, and Simulator
  - Supports Real-Time analysis, data visualization, and open API
- Optimizing C compiler
  - Supports high-level language programming
  - Full implementation of the standard ANSI C language
  - Powerful optimizer that improves code-execution speed and reduces code size
  - Extensive run-time support library included
  - TMS470 control registers easily accessible from the C program
  - Interfaces C functions and assembly functions easily
  - Establishes comprehensive, easy-to-use tool set for the development of high-performance microcontroller applications in C/C++
- Assembly language tools (assembler and linker)
  - Provides extensive macro capability
  - Allows high-speed operation
  - Allows extensive control of the assembly process using assembler directives
  - Automatically resolves memory references as C and assembly modules are combined

For more information on pricing and availability, contact the nearest TI field sales office or authorized distributor.

Code Composer Studio is a trademark of Texas Instruments.

## device numbering conventions

Figure 2 illustrates the numbering and symbol nomenclature for the TMS470 family.

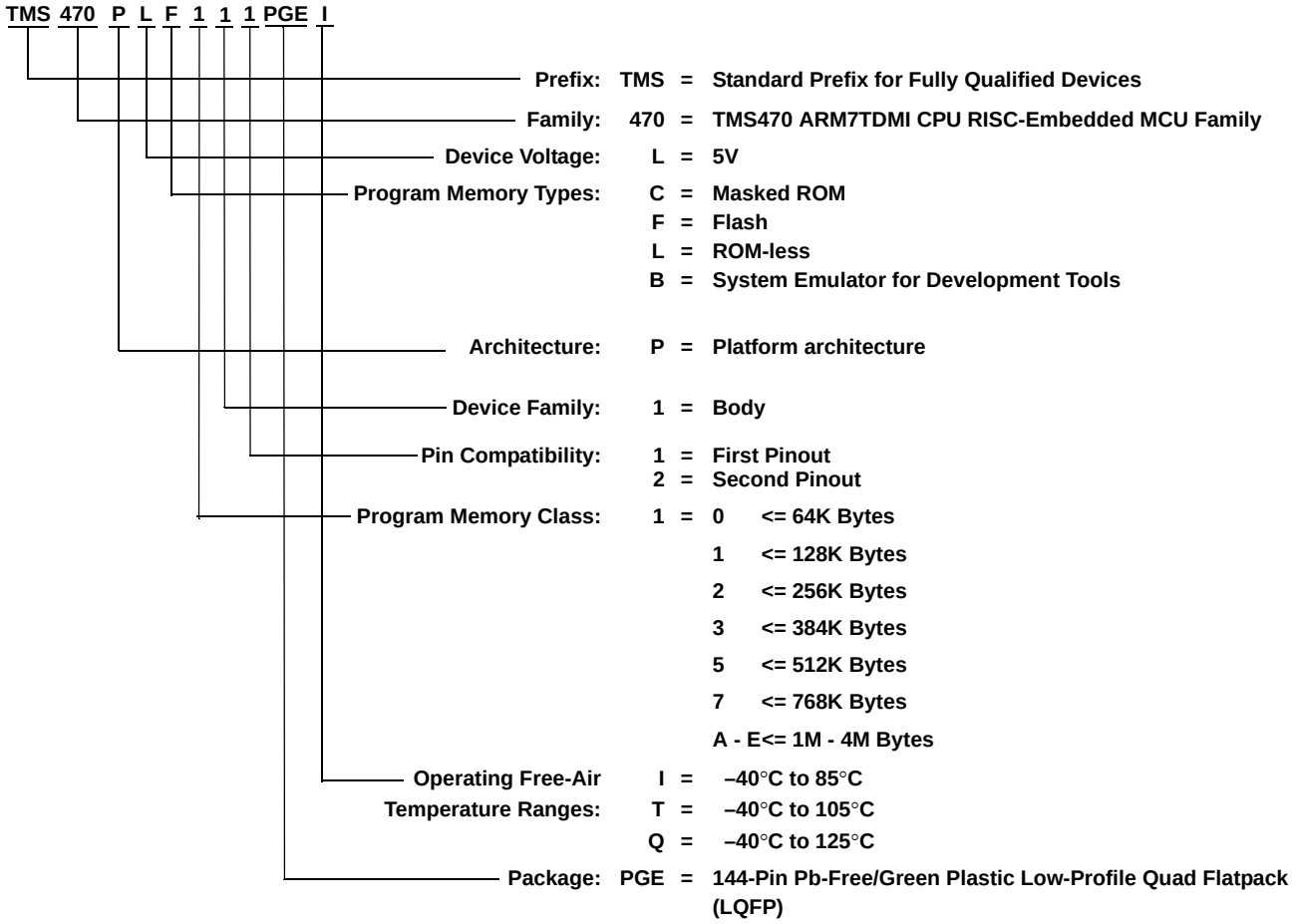



**Figure 2. TMS470 Family Nomenclature**

## device identification code register

The device identification code register identifies the coprocessor status, an assigned device-specific part number, the technology family (TF), the I/O voltage, whether or not parity is supported, the levels of flash and RAM erro detection, and the device version. The PLF111 device identification code register value is 0x0006_3405.

**Table 8. TMS470 Device ID Bit Allocation Register**

| | BIT 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | BIT 16 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| FFFF_FFF0 | CP15 | PART NUMBER | | | | | | | | | | | | | | TF |
| | R-K | R-K | | | | | | | | | | | | | | R-K |

| BIT 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | BIT 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| TF | | | I/O VOLT | PP | FLASH ECC | | RAM ECC | VERSION | | | | | 1 | 0 | 1 |
| R-K | | | R-K | R-K | R-K | | R-K | R-K | | | | | R-1 | R-0 | R-1 |

LEGEND:
R = Read only, -K = Value constant after $\overline{\text{RESET}}$

*Device ID Bit Allocation Register Field Descriptions*

| Bit | Name | Value | Description |
|---|---|---|---|
| 31 | CP15 | | This bit indicates the presence of coprocessor (CP15) |
| | | 0 | No coprocessor present in the device |
| | | 1 | Coprocessor present in the device |
| 30–17 | PART NUMBER | | These bits indicate the assigned device-specific part number. The assigned device-specific part number for the PLF111 device is 00000000000011 (0x3). |
| 16–13 | TF | | Technology family bit<br>These bits indicate the technology family (C05, F05, F035, C035). |
| | | 0001 | F05 |
| 12 | I/O VOLT | | I/O voltage bit<br>This bit identifies the core power supply: |
| | | 0 | 3.3 V |
| | | 1 | 5 V |
| 11 | PP | | Peripheral parity bit<br>This bit indicates whether parity is supported: |
| | | 0 | No parity on peripheral |
| | | 1 | Parity on peripheral |

*Device ID Bit Allocation Register Field Descriptions (Continued)*

| Bit | Name | Value | Description |
|---|---|---|---|
| 10–9 | FLASHECC | | Flash ECC bits<br>These bits indicate the level of error detection and correction on the flash memory: |
| | | 00 | No error detection/correction |
| | | 01 | Program memory with parity |
| | | 10 | Program memory with ECC |
| | | 11 | Reserved |
| 8 | RAMECC | | RAM ECC bits<br>This bit indicates the presence of error detection and correction on the CPU RAM: |
| | | 0 | RAM ECC not present |
| | | 1 | RAM ECC present |
| 7–3 | VERSION | | These bits identify the silicon version of the device. |
| 2–0 | 101 | | Bits 2:0 are set to 101 by default to indicate a platform device. |

## device part numbers

Table 9, Device Part Number lists all the available TMS470PLF111 devices.

**Table 9. Device Part Number**

| DEVICE PART NUMBER | PROGRAM MEMORY | | PACKAGE TYPE | | TEMPERATURE RANGES | | |
|---|---|---|---|---|---|---|---|
| | ROM | FLASH EEPROM | 100-PIN LQFP | 144-PIN LQFP | –40°C TO 85°C | –40°C TO 105°C | –40°C TO 125°C |
| TMS470PLF111PGEI | | X | | X | X | | |
| TMS470PLF111PGET | | X | | X | | X | |
| TMS470PLF111PGEQ | | X | | X | | | X |

## DEVICE ELECTRICAL SPECIFICATIONS AND TIMING PARAMETERS

### absolute maximum ratings over operating free-air temperature range, A version (unless otherwise noted)(1)

Supply voltage ranges: $V_{CC}$(2) . . . . . −0.5 V to 2.5 V
Supply voltage ranges: $V_{CCIO}$, $V_{CCAD}$, $V_{CCP}$ (flash pump)(2) . . . . . −0.5 V to 6 V
Input voltage range: All input pins . . . . . −0.5 V to 6 V
Input clamp current: ADIN[0:15] $I_{IK}$ ($V_I < 0$ or $V_I > V_{CCAD}$) . . . . . ±10 mA
All other pins $I_{IK}$ ($V_I < 0$ or $V_I > V_{CCIOR}$) . . . . . ±20 mA
Operating free-air temperature ranges, $T_A$: I version . . . . . −40°C to 85°C
T version . . . . . −40°C to 105°C
Q version . . . . . −40°C to 125°C
Operating junction temperature range, $T_J$ . . . . . −40°C to 150°C
Storage temperature range, $T_{stg}$ . . . . . −65°C to 150°C

1 Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2 All voltage values are with respect to their associated grounds.

### device recommended operating conditions(3)

| | | | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|---|
| $V_{CCIOR}$ | Digital I/O and internal regulator supply voltage | | 4.75 | 5 | 5.25 | V |
| $V_{CC}$ | Voltage regulator output voltage, internal regulator enabled | | 1.81 | 1.91 | 2.05 | V |
| $V_{CCAD}$ | MibADC supply voltage | | 4.75 | 5 | 5.25 | V |
| $V_{CCP}$ | Flash pump supply voltage | | 4.75 | 5 | 5.25 | V |
| $V_{SS}$ | Digital logic supply ground | | | 0 | | V |
| $V_{SSAD}$ | MibADC supply ground | | – 0.1 | | 0.1 | V |
| $T_A$ | Operating free-air temperature | I version | – 40 | | 85 | °C |
| | | T version | – 40 | | 105 | °C |
| | | Q version | – 40 | | 125 | °C |
| $T_J$ | Operating junction temperature | | – 40 | | 150 | °C |

3 All voltages are with respect to $V_{SS}$, except $V_{CCAD}$, which is with respect to $V_{SSAD}$.

## electrical characteristics over recommended operating free-air temperature range(1)

| PARAMETER | | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $V_{hys}$ | Input hysteresis | | | 0.5 | | | V |
| $V_{IL}$ | Low-level input voltage | All inputs(2) | | $V_{SS}$ – 0.5 | | $0.3V_{CCIOR}$ | V |
| $V_{IH}$ | High-level input voltage | All inputs | | $0.7V_{CCIOR}$ | | $V_{CCIOR}$ + 0.5 | V |
| $V_{OL}$ | Low-level output voltage(4) | | $I_{OL}$ = $I_{OL}$ MAX | | | 0.2 $V_{CCIOR}$ | V |
| | | | $I_{OL}$ = 50 µA | | | 0.2 | |
| $V_{OH}$ | High-level output voltage(4) | | $I_{OH}$ = $I_{OH}$ MAX | 0.8 $V_{CCIOR}$ | | | V |
| | | | $I_{OH}$ = 50 µA | $V_{CCIOR}$ – 0.2 | | | |
| $I_{IC}$ | Input clamp current (I/O pins)(5)(9) | | $V_I < V_{SSIO} - 0.3$ or $V_I > V_{CCIOR} + 0.3$ | –2 | | 2 | mA |
| $I_I$ | 20µA IPU/IPD | $I_{IL}$ Pulldown | $V_I = V_{SS}$ | –1 | | 1 | µA |
| | | $I_{IH}$ Pulldown | $V_I = V_{CCIOR}$ | 5 | | 40 | |
| | | $I_{IL}$ Pullup | $V_I = V_{SS}$ | –40 | | –5 | |
| | | $I_{IH}$ Pullup | $V_I = V_{CCIOR}$ | –1 | | 1 | |
| | 100µA IPU/IPD | $I_{IL}$ Pulldown | $V_I = V_{SS}$ | –1 | | 1 | |
| | | $I_{IH}$ Pulldown | $V_I = V_{CCIOR}$ | 23 | | 88 | |
| | | $I_{IL}$ Pullup | $V_I = V_{SS}$ | –204 | | –69 | |
| | | $I_{IH}$ Pullup | $V_I = V_{CCIOR}$ | –1 | | 1 | |
| | All other pins | No IPU/IPD | | –1 | | 1 | |
| $I_{OL}$ | Low-level output current | TDO, ECLK, AWD | $V_{OL}$ = $V_{OL}$ MAX | | | 8 | mA |
| | | $\overline{RST}$, SPICLK, SPISIMO, SPISOMI, CANSTX, C2SITX | | | | 4 | |
| | | All other output pins | | | | 2 | |
| $I_{OH}$ | High-level output current | TDO, ECLK, AWD | $V_{OH}$ = $V_{OH}$ MIN | –8 | | | mA |
| | | $\overline{RST}$, SPICLK, SPISIMO, SPISOMI, CANSTX, C2SITX | | –4 | | | |
| | | All other output pins | | –2 | | | |
| $C_I$ | Input capacitance | | | | 6 | | pF |
| $C_O$ | Output capacitance | | | | 7 | | pF |

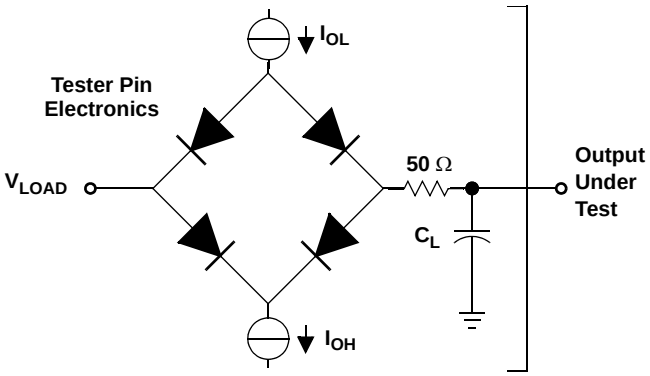
1 Source currents (out of the device) are negative while sink currents (into the device) are positive.
2 This does not apply to the $\overline{PORRST}$ pin. For $\overline{PORRST}$ exceptions, see the $\overline{RST}$ and $\overline{PORRST}$ timings section on page 40.
3 $V_{OL}$ and $V_{OH}$ are linear with respect to the amount of load current ($I_{OL}$/$I_{OH}$) applied.
4 Parameter does not apply to input-only or output-only pins.
5 I/O pins configured as inputs or outputs with no load. All pulldown inputs ≤ 0.2 V. All pullup inputs ≥ $V_{CCIO}$ – 0.2 V.
6 For flash banks/pumps in sleep mode.
7 The PLF111 device will enter low power mode only if the internal regulator is enabled. Low power modes are not supported when internal regulator is disabled.
8 Based on resistor of 5.3Ω and capacitor of 1µF in series with $V_{CCP}$.
9 The following pins do not have clamping diodes: nPORRST, REGDIS, TCK, nTRST and TEST. The application must not exceed an input current of +-2mA with an absolute maximum rating of +-20mA.

## electrical characteristics over recommended operating free-air temperature range(1) (continued)

| MODE | PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| Operating | $V_{CCIOR}$ regulator/IO supply current/Vcc digital supply current | HCLK = 48MHz, VCLK = 48 MHz, PLL enabled<br>$V_{CCIOR}$ = 5.25 V<br>Internal regulator enabled | | | 92 | mA |
| | $V_{CCIOR}$ regulator/IO supply current/Vcc digital supply current | HCLK = 24MHz, VCLK = 24 MHz, PLL enabled<br>$V_{CCIOR}$ = 5.25 V<br>Internal regulator enabled | | | 62 | mA |
| | $V_{CCIOR}$ regulator/IO supply current/Vcc digital supply current | HCLK = 8MHz, VCLK = 8 MHz, PLL disabled<br>$V_{CCIOR}$ = 5.25 V<br>Internal regulator enabled | | | 42 | mA |
| | $V_{CCAD}$ supply current | $V_{CCAD}$ = 5.25 V | | | 18 | mA |
| | $V_{CCP}$ pump supply current | $V_{CCP}$ = 5.25 V, read operation | | | 10 | mA |
| | $V_{CCP}$ pump supply current | $V_{CCP}$ = 5.25 V, peak program and erase operation | | | 30 | mA |
| | $V_{CCP}$ pump supply current | $V_{CCP}$ = 5.25 V, peak program and erase operation(8) | | | 18 | mA |
| | $V_{CCP}$ pump supply current | $V_{CCP}$ = 5.25 V, average program and erase operation (8) | | | 15 | mA |
| Doze(7) | $V_{CCIOR}$ regulator/IO supply current/Vcc digital supply current | I version (85°C)<br>OSCIN = 8 MHz, $V_{CCIOR}$ = 5.25 V | | | 660 | uA |
| | $V_{CCIOR}$ regulator/IO supply current/Vcc digital supply current | Q version (125°C)<br>OSCIN = 8 MHz, $V_{CCIOR}$ = 5.25 V | | | 850 | uA |
| | $V_{CCAD}$ supply current | $V_{CCAD}$ = 5.25 V(6) | | | 10 | uA |
| | $V_{CCP}$ pump supply current | $V_{CCP}$ = 5.25 V(6) | | | 10 | uA |
| Sleep(7) | $V_{CCIOR}$ regulator/IO supply current/Vcc digital supply current | I version (85°C)<br>$V_{CC}$ = 2.05 V | | | 110 | uA |
| | $V_{CCIOR}$ regulator/IO supply current/Vcc digital supply current | Q version (125°C)<br>$V_{CC}$ = 2.05 V | | | 350 | uA |
| | $V_{CCAD}$ supply current | $V_{CCAD}$ = 5.25 V(6) | | | 10 | uA |
| | $V_{CCP}$ pump supply current | $V_{CCP}$ = 5.25 V(6) | | | 10 | uA |

1Source currents (out of the device) are negative while sink currents (into the device) are positive.
2This does not apply to the $\overline{\text{PORRST}}$ pin. For $\overline{\text{PORRST}}$ exceptions, see the $\overline{\text{RST}}$ and $\overline{\text{PORRST}}$ timings section on page 40.
3$V_{OL}$ and $V_{OH}$ are linear with respect to the amount of load current ($I_{OL}$/$I_{OH}$) applied.
4Parameter does not apply to input-only or output-only pins.
5I/O pins configured as inputs or outputs with no load. All pulldown inputs ≤ 0.2 V. All pullup inputs ≥ $V_{CCIO}$ − 0.2 V.
6For flash banks/pumps in sleep mode.
7The PLF111 device will enter low power mode only if the internal regulator is enabled. Low power modes are not supported when internal regulator is disabled.
8 Based on the condition that a parallel capacitor of 1uF is placed on the VCCP line and series resistor of 5.3 Ohm is placed in the VCCP line
9The following pins do not have clamping diodes: nPORRST, REGDIS, TCK, nTRST and TEST. The application must not exceed an input current of +-2mA with an absolute maximum rating of +-20mA.

## PARAMETER MEASUREMENT INFORMATION




Where: $I_{OL}$ = $I_{OL}$ MAX for the respective pin(A)
$I_{OH}$ = $I_{OH}$ MIN for the respective pin(A)
$V_{LOAD}$ = 1.5 V
$C_L$ = 150-pF typical load-circuit capacitance(B)

NOTES: A. For these values, see the "electrical characteristics over recommended operating free-air temperature range" table.
B. All timing parameters measured using an external load capacitance of 150 pF unless otherwise noted.

**Figure 3. Test Load Circuit**

## timing parameter symbology

Timing parameter symbols have been created in accordance with JEDEC Standard 100. In order to shorten the symbols, some of the pin names and other related terminology have been abbreviated as follows:

| | | | |
|---|---|---|---|
| CM | Compaction, CMPCT | RD | Read |
| | | RST | Reset, $\overline{\text{RST}}$ |
| | | RX | SCInRX |
| VCLK | VBUS Interface clock | S | Slave mode |
| M | Master mode | SCC | SCInCLK |
| OSC | OSCIN | SIMO | SPInSIMO |
| | | SOMI | SPInSOMI |
| | | SPC | SPInCLK |
| | | SYS | System clock |
| | | TX | SCInTX |

Lowercase subscripts and their meanings are:

| | | | |
|---|---|---|---|
| a | access time | r | rise time |
| c | cycle time (period) | su | setup time |
| d | delay time | t | transition time |
| f | fall time | v | valid time |
| h | hold time | w | pulse duration (width) |

The following additional letters are used with these meanings:

| | | | |
|---|---|---|---|
| H | High | X | Unknown, changing, or don't care level |
| L | Low | Z | High impedance |
| V | Valid | | |

**device clock**

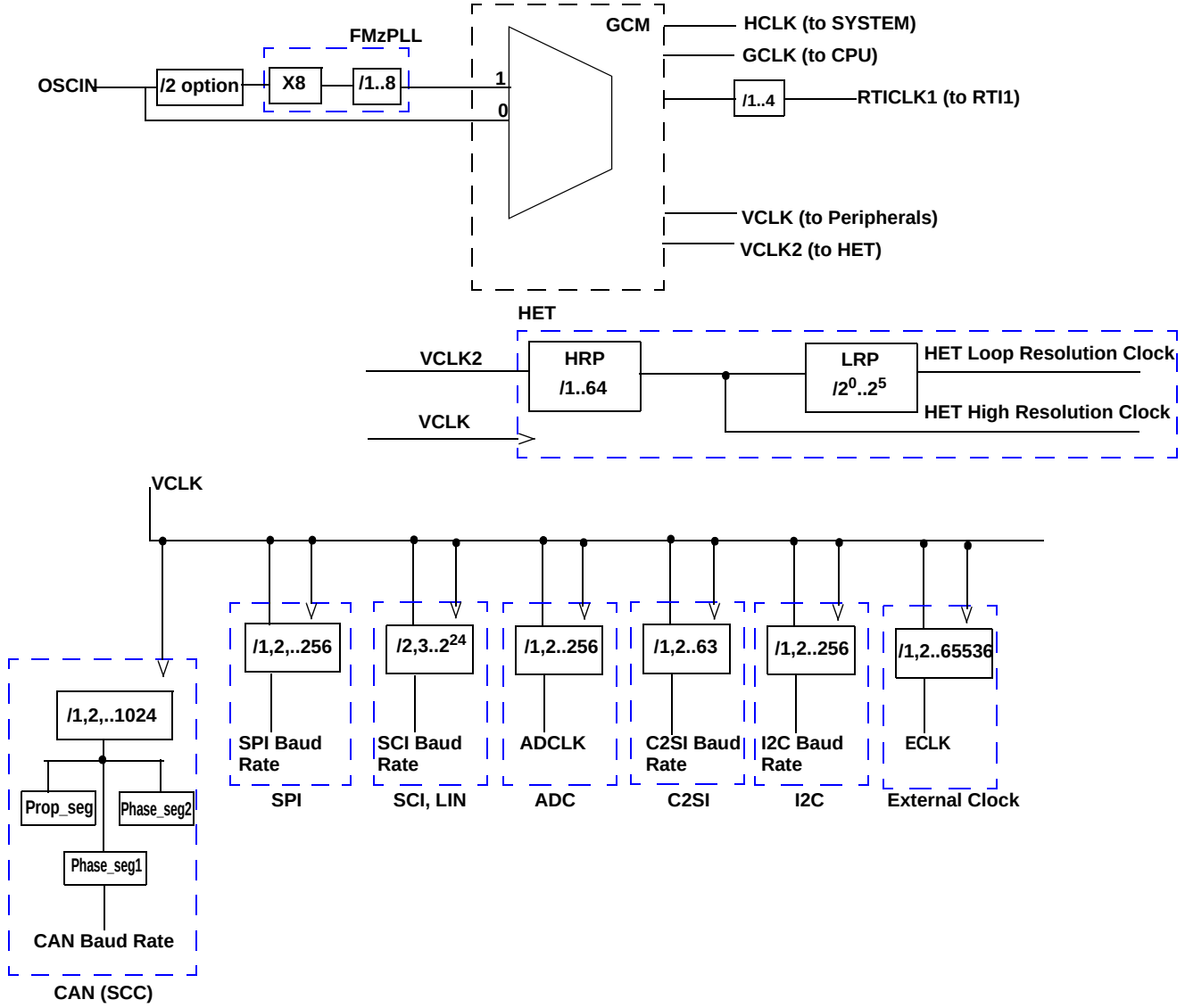



**Figure 4. TMS470 Platform Clock Domains Block Diagram**

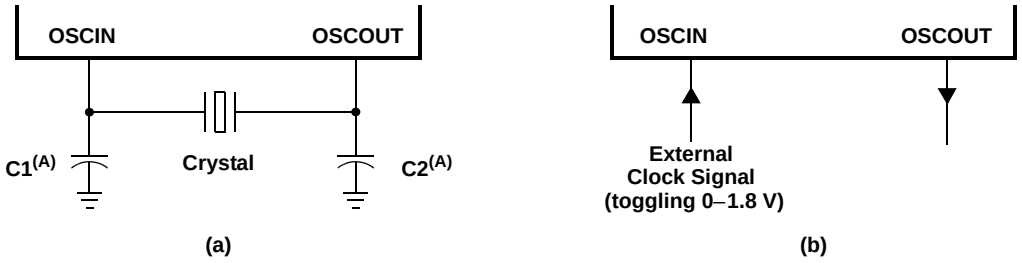
**Table 10. GCM Clock Source Assignments**

| GCM SOURCE NUMBER | CLOCK SOURCE |
|---|---|
| 0 | OSCIN |
| 1 | FMzPLL output |
| 2 | RESERVED |
| 3 | RESERVED |
| 4 | RESERVED |
| 5 | RESERVED |
| 6 | RESERVED |
| 7 | RESERVED |

### external reference resonator/crystal oscillator clock option

The oscillator is enabled by connecting the appropriate fundamental 4–20 MHz resonator/crystal and load capacitors across the external OSCIN and OSCOUT pins as shown in Figure 5a. The oscillator is a single-stage inverter held in bias by an integrated bias resistor. This resistor is disabled during leakage test measurement and HALT mode. **TI strongly encourages each customer to submit samples of the device to the resonator/crystal vendors for validation.** The vendors are equipped to determine what load capacitors will best tune their resonator/crystal to the microcontroller device for optimum start-up and operation over temperature/voltage extremes.

An external oscillator source can be used by connecting a 1.8 V clock signal to the OSCIN pin and leaving the OSCOUT pin unconnected (open) as shown in Figure 5b.




A. The values of C1 and C2 should be provided by the resonator/crystal vendor.

**Figure 5. Crystal/Clock Connection**

## FM$_Z$PLL and clock specifications

### input frequency increase for FM$_z$PLL

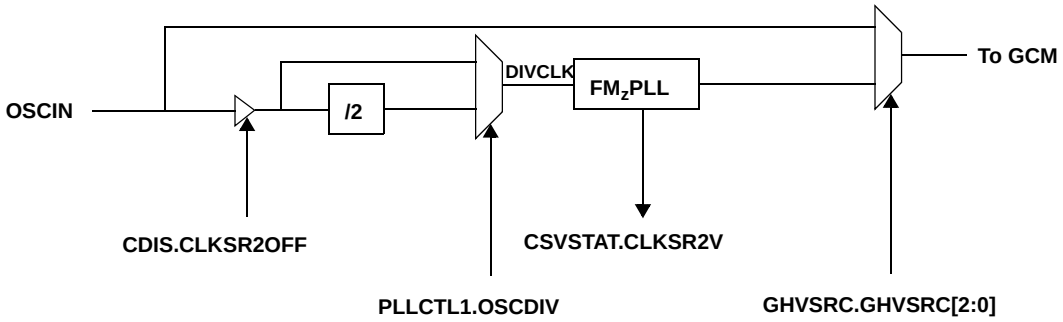



**Figure 6. FM$_Z$PLL Clock Input Circuitry**

The FM$_z$PLL has an input frequency (DIVCLK) range from 4MHz to 10MHz. In order to allow for input OSCIN frequencies higher than 10Mhz, the oscillator input must be divided down by 2 through a software programmable register bit PLLCTL1.OSCDIV. DIVCLK can be either OSCIN/1 or OSCIN/2. This is selectable via the OSC_DIV bit in the PLLCTL1 register. The default value for this bit is divide-by-1.

After reset, the system clock and CPU clock are driven by OSCIN, and CLKSR2OFF switches off DIVCLK to the PLL. Software must ensure that CLKSR2OFF (CSDIS) is only set to 1 if DIVCLK does not exceed the 10MHz maximum input frequency of the FM$_z$PLL. If CLKSR2OFF is set to one, the PLL will start its locking process. Once the PLL is locked it will signal this with the CLKSR2V bit (CSVSTAT) and the software can then switch to the PLL output clock with the GHVSRC[2:0] bits (GHVSRC). This is shown in Figure 6. For more information, please see the System Architecture specification.

The FM$_Z$PLL only supports a multiplication factor of 8 only.

### timing requirements for input clocks(1)

| | | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|
| $f_{(OSC)}$ | Input clock frequency | 4 | | 20 | MHz |
| $t_{c(OSC)}$ | Cycle time, OSCIN | 50 | | | ns |
| $t_{w(OSCIL)}$ | Pulse duration, OSCIN low | 15 | | | ns |
| $t_{w(OSCIH)}$ | Pulse duration, OSCIN high | 15 | | | ns |
| $f_{(OSCRST)}$(2) | OSC FAIL frequency | | 600 | | kHz |

1 Frequency modulation mode of the FMzPLL is not supported.
2 Causes a device reset (specifically a clock reset) by setting the OSC RST bit in SYSESR and the OSC FAIL flag bit in GLBSTAT as defined in the TMS470 Platform Architecture documentation.

## $FM_ZPLL$ and clock specifications (continued)

### switching characteristics over recommended operating conditions for clocks(1)(2)(3)

| PARAMETER | | TEST CONDITIONS(4) | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| $f_{(HCLK)}$ | System clock frequency(5) | Pipeline mode enabled | | 48 | MHz |
| | | Pipeline mode disabled | | 24 | MHz |
| $f_{(VCLK)}$ | Peripheral VBUS clock frequency | | | 48 | MHz |
| $f_{(VCLK2)}$ | HET clock frequency | | | 48 | MHz |
| $f_{(ECLK)}$ | External clock output frequency for ECP module | | | 48 | MHz |
| $f_{(DIVCLK)}$ | FMzPLL clock in frequency | | | 10 | MHz |
| $t_{c(HCLK)}$ | Cycle time, system clock | Pipeline mode enabled | 20.8 | | ns |
| | | Pipeline mode disabled | 41.6 | | ns |
| $t_{c(VCLK)}$ | Cycle time, peripheral VBUS clock | | 20.8 | | ns |
| $t_{c(VCLK2)}$ | Cycle time, HET clock | | 20.8 | | ns |
| $t_{c(ECLK)}$ | Cycle time, ECP module external clock output | | 20.8 | | ns |
| $t_{c(DIVCLK)}$ | Cycle time, FMzPLL clock in | | 100 | | ns |

1 $f_{(HCLK)} = M * f_{(OSC)} / R$, where M = 8, and R = {1,2,3,4,5,6,7,8}.
$f_{(VCLK)} = f_{(HCLK)} / X$, where X = {1,2,3,4,5,6,7,8,9,10,11,12,13,14,15,16}. X is the peripheral VBUS clock divider ratio.
2 $f_{(ECLK)} = f_{(VCLK)} / N$, where N = {1 to 65536}. N is the ECP prescale value defined by the ECPCTRL.[15:0] register bits in the ECP module.
3 Frequency modulation mode of the FMzPLL is not supported.
4 Pipeline mode enabled or disabled is determined by the ENPIPE bit (FMREGOPT.0).
5 Flash Vread must be set to 5Vand must always be set at 5V.

### sequence to wake up from doze mode

In doze mode, the HCLK, GCLK, VCLK, and VCLK2 are all turned off. Also, the main oscillator is the only clock source running while in doze mode. Please see the TMS470 Platform Architecture Specification (SPNU230) for more details on the doze mode. Doze mode is not supported if the internal voltage regulator is disabled.

The RTICLK1 is still active, which allows the RTI module to generate periodic wake up interrupts, if required. The other wakeup options are: external interrupts via GIO pins, CAN message, SCI/LIN, C2SI and I2C. The sequence for waking up from doze mode is described below:

Step 1. Wakeup request is received/generated. Figure 7 shows the CAN module generating the wakeup interrupt.
Step 2. This wakeup event causes the core VREG to wake up.
Step 3. Since the main oscillator is running already it is used as the clock source upon wakeup.
Step 4. The software runs using the main oscillator as the clock source. Also, now the PLL can be enabled.
Step 5. Once the PLL has acquired LOCK, the software can switch over to using the PLL output clock for normal operation.

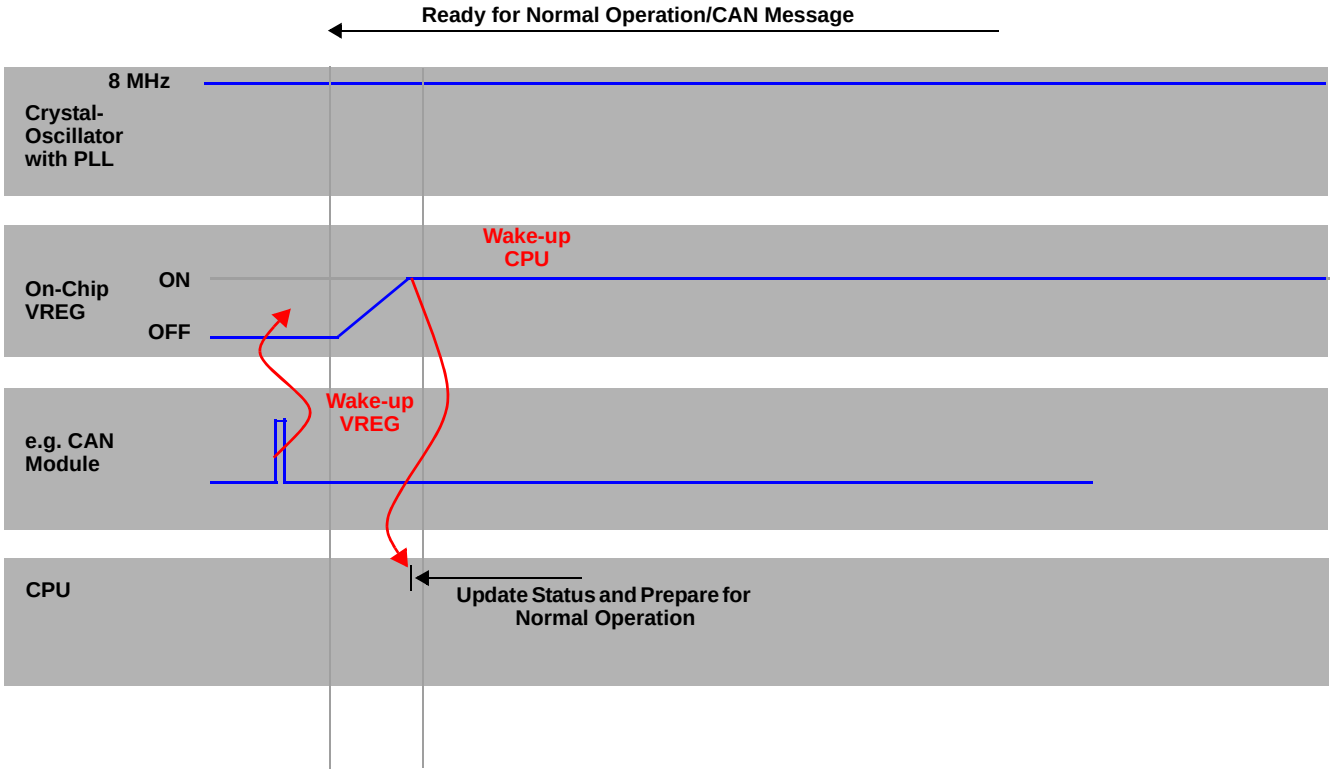



**Figure 7. Wake Up From Doze Mode**

### sequence to wake up from sleep mode

In sleep mode, ALL the clocks are turned off: HCLK, GCLK, VCLK, VCLK2, and RTICLK1. All the clock sources are also disabled. Please refer to the TMS470 Platform Architecture Specification (SPNU230) for more details on sleep mode. Sleep mode is not supported if the internal voltage regulator is disabled.

The wakeup options are: external interrupts via GIO pins, CAN, SCI/LIN, C2SI and I2C. The sequence for waking up from the sleep mode is described below:

Step 1. Wakeup request is received/generated. Figure 8 shows the CAN module generating the wakeup interrupt based on a message received.
Step 2. This wakeup event causes the on-chip VREG to wake up.
Step 3. Once the on-chip VREG wakes up, the CPU and the main oscillator start to wake up.
Step 4. Once the main oscillator output is valid, the software runs using the main oscillator as the clock source. The software can prepare for normal operation. Also, now the PLL can be enabled.
Step 5. Once the PLL has acquired LOCK, the software can switch over to using the PLL output clock for normal operation.

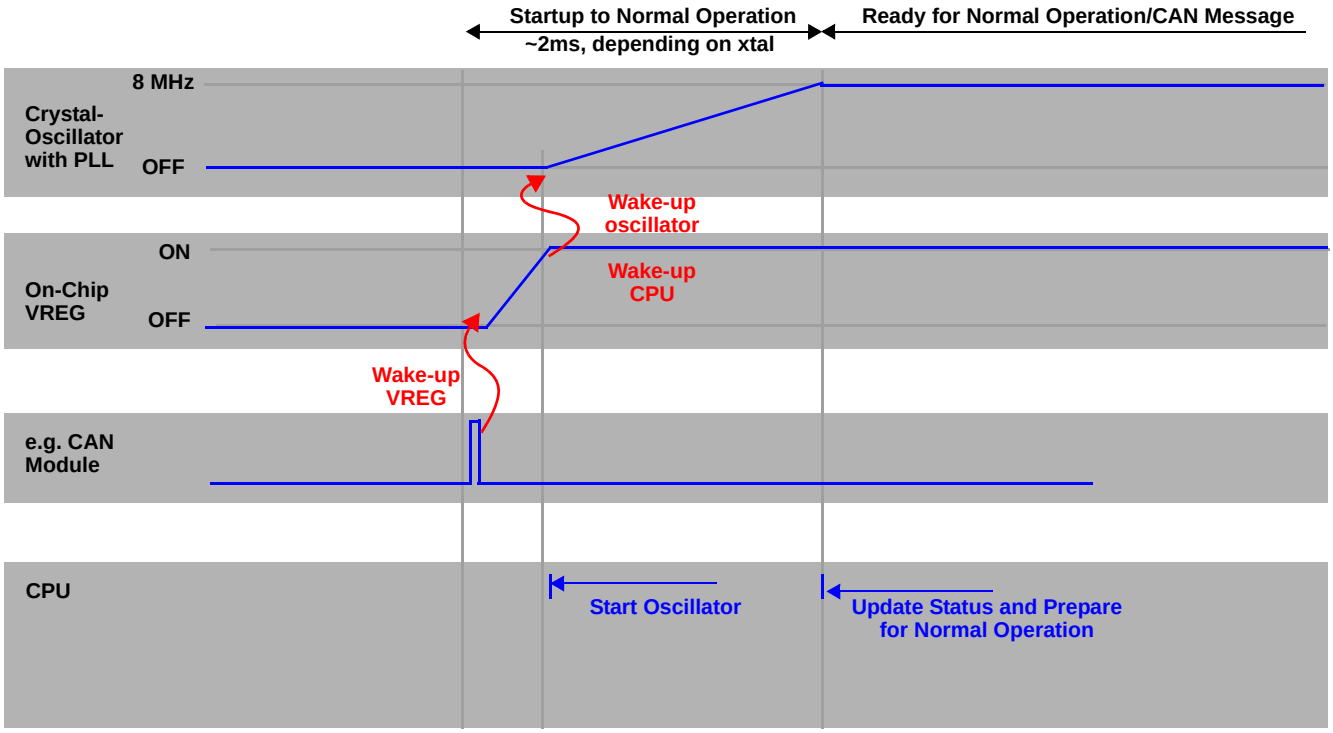



**Figure 8. Wake Up From Sleep Mode**

### summary of wakeup from low power modes

| MODE | CLOCK SOURCE ACTIVE | ACTIVE CLOCKS | WAKEUP OPTIONS | WAKEUP CLOCK SOURCE | WAKEUP TIMES |
|---|---|---|---|---|---|
| Doze | Oscillator | RTICLK1 | GIO interrupts, CAN Rx, SCI/LIN Rx, C2SI Rx, RTI, I2C SDA | Oscillator | VREG wakeup(1) + flash pump sleep(2) + flash pump standby(3) |
| Sleep | None | None | GIO interrupts, CAN Rx, SCI/LIN Rx, C2SI Rx, I2C SDA | Oscillator | VREG wakeup + Osc. startup + 1024 Osc. cycles + flash pump sleep + flash pump standby |

1 VREG wakeup = $t_{halt\text{-}normal}$. See page 39.

2 Flash pump sleep = minimum time for which the flash pump is in sleep mode before it enters standby mode = 2μs. The flash pump sleep2standby counter must be programmed such that the (counter value X wakeup clock source period) is at least 2μs.

3 Flash pump standby = minimum time for which the flash pump is in standby mode before it enters active mode = 1μs. The flash pump standby2active counter must be programmed such that the (counter value X wakeup clock source period) is at least 1μs.

4 Low power modes are not supported if the internal voltage regulator is disabled.

**Note:** The flash banks will wake up in parallel with the flash pump. The flash banks can wake up faster than the flash pump and therefore the overall flash module wake up time is determined by the pump wake up time.

## $FM_ZPLL$ and clock specifications (continued)

### switching characteristics over recommended operating conditions for external clocks (see Figure 9)[1]

| NO. | PARAMETER | | TEST CONDITIONS | MIN | MAX | UNIT |
|---|---|---|---|---|---|---|
| 3 | $t_{w(EOL)}$ | Pulse duration, ECLK low | | $0.5t_{c(ECLK)} - t_f$ | | ns |
| 4 | $t_{w(EOH)}$ | Pulse duration, ECLK high | | $0.5t_{c(ECLK)} - t_r$ | | ns |

1 $f_{(ECLK)} = f_{(VCLK)}/N$ where N = {1 to 65536}. N is the ECP prescale value defined by the ECPCTRL.[15:0] register bits in the system module.

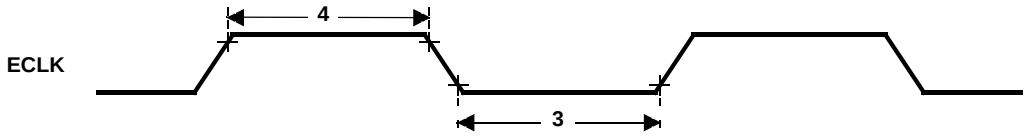
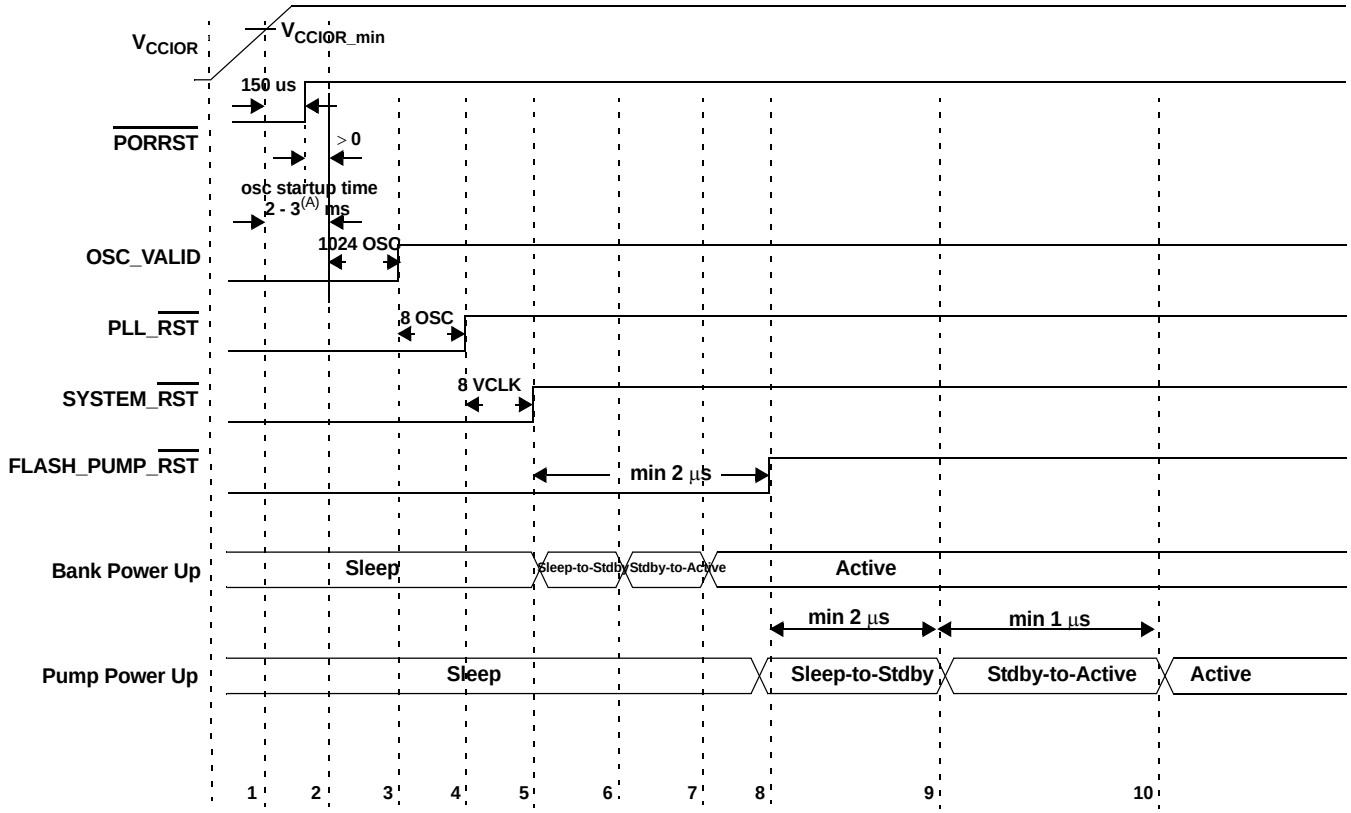



**Figure 9. ECLK Timing Diagram**

## power-up sequence

The power up sequence starts with the input voltage rising above $V_{CCIOR\_min}$ and the release of reset. The oscillator must first start and its amplitude grow to an acceptable level. Simultaneously, the flash pump and banks power up. Code can be executed from RAM any time after SYSTEM_$\overline{RST}$ is released; however, an access to flash will be held off until the flash is ready.




NOTE A: Oscillator startup time is highly influenced by the crystal, load capacitor values, temperature and voltage.

**Figure 10. Power-Up Sequencing**

Step 1. Power is turned on and $V_{CCIOR}$ starts to rise. The $\overline{PORRST}$ signal must be released (driven HIGH) no earlier than 150µs after the $V_{CCIOR}$ reaches 4.75V. OSC clock is still unstable. The oscillator start up time is typically 2-3ms from the time $V_{CCIOR\_min}$ is reached.

Step 2. Once the oscillator starts up, the PLL wrapper counts an additional 1024 OSC clocks before asserting OSC_VALID.

Step 3. After OSC_VALID is active, the global clock module (GCM) starts generating all domain clocks (GCLK, HCLK, VCLK, VCLK2). The PLL wrapper counts 8 OSC clocks before deasserting PLL_$\overline{RST}$.

**power-up sequence (continued)**

Step 4. After PLL_$\overline{\text{RST}}$ is deasserted, all flip flops will be in their reset state. The System module counts eight VCLK cycles and then releases the SYSTEM_$\overline{\text{RST}}$ to the rest of the device. The external $\overline{\text{RST}}$ pin is equivalent to the internal SYSTEM_$\overline{\text{RST}}$ signal. Asserting external $\overline{\text{RST}}$ will synchronously extend the internal SYSTEM_$\overline{\text{RST}}$.

Step 5. Flash bank(s) are now in standby mode. This transition occurs only when waking up from low power modes. The flash banks are already in an active state on power up.

Step 6. Flash bank(s) are now in active mode. No read access to bank yet -- only DC current.

Step 7. Reset to flash pumps is released.

Step 8. Flash pump module is now in standby mode.

Step 9. Flash pump module is now in active mode. no read access to bank yet -- only DC current.

Step 10. Flash wrapper generates the BANK_RDY signal and the flash access can now proceed.

## internal voltage regulator specifications

| PARAMETER | DESCRIPTION | MIN | MAX | UNIT |
|---|---|---|---|---|
| $t_{D(VCCIOR)0-3}$ | Delay time, 5V input supply to ramp from 0V to 4.75V(1) | 25 | | us |
| $t_{V(PORRST)L}$ | Valid time, $\overline{PORRST}$ active after 5V input supply becomes ≥ 4.75V | 150 | | us |
| $V_{CCIORmin(PORRST)f}$ | Minimum input voltage, when $\overline{PORRST}$ must be made active during power down or brown out | 4.75 | | V |
| $C_{min(VCC)core}$ | Capacitance distributed over all core VCC pins for voltage regulator stability | 10 | | uF |
| $ESR_{(max)core}$ | Total combined ESR of stabilization capacitors on core Vcc pins | 0 | 0.25 | Ω/pin |

1 Ramping at minimum $t_{D(VCCIOR)0-3}$ with large load capacitance $C_{min}$ can cause large transient currents (approximately 1.9 A).

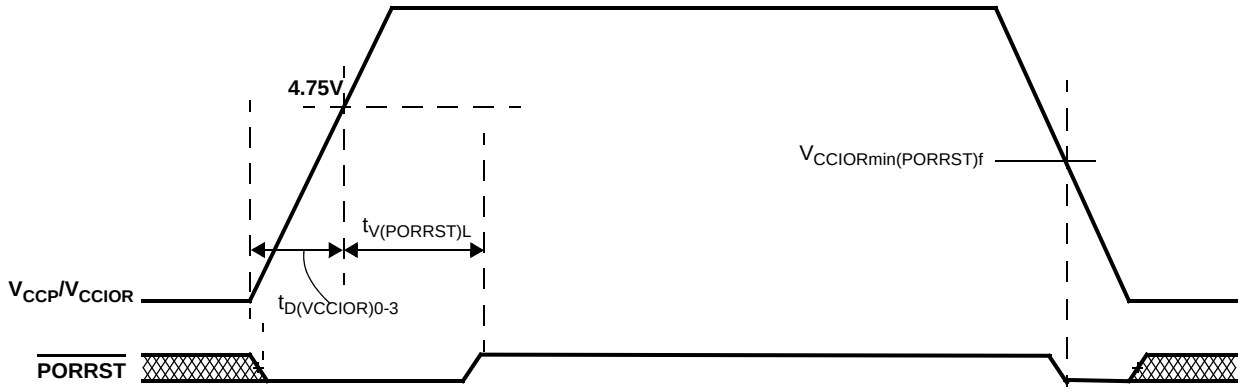



**Figure 11. $\overline{PORRST}$ Timing Requirements**

## VREG recommended operation conditions

| PARAMETER | | TEST CONDITIONS | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| $I_{CC}$ | $V_{CC}$ load rating | Normal mode, regulator active | 0 | 100 | mA |
| | | Halt mode, regulator active | | 3 | mA |

## VREG halt-mode timing characterisitics(2)(3)

| PARAMETER | | MIN | MAX | UNIT |
|---|---|---|---|---|
| $t_{normal-halt}$ | transition time between normal mode and halt mode | | 70 | nS |
| $t_{halt-normal}$ | transition time between halt mode and normal mode | | 20 | µS |

2 These times only reflect VREG transition times. Times for other components are not included.
3 Device low power modes are not supported when the VREG is disabled

## $\overline{\text{RST}}$ and $\overline{\text{PORRST}}$ timings

### switching characteristics over recommended operating conditions for $\overline{\text{RST}}$(1)

| PARAMETER | | MIN | MAX | UNIT |
|---|---|---|---|---|
| $t_{v(RST)}$ | Valid time, $\overline{\text{RST}}$ active after $\overline{\text{PORRST}}$ inactive | $1048t_{c(OSC)}$ | | ns |
| $t_{fsu}$ | Flash start up time, from $\overline{\text{RST}}$ inactive to fetch of first instruction from Flash (Flash pump stabilization time) | 5 | | µs |

1 Specified values do NOT include rise/fall times. For rise and fall timings, see the "switching characteristics for output timings versus load capacitance" table.

## JTAG scan interface timing (JTAG clock specification 10-MHz and 50-pF load on TDO output)

| NO. | | | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| 1 | $t_{c(JTAG)}$ | Cycle time, JTAG low and high period | 50 | | ns |
| 2 | $t_{su(TDI/TMS - TCKr)}$ | Setup time, TDI, TMS before TCK rise (TCKr) | 15 | | ns |
| 3 | $t_{h(TCKr -TDI/TMS)}$ | Hold time, TDI, TMS after TCKr | 15 | | ns |
| 4 | $t_{h(TCKf -TDO)}$ | Hold time, TDO after TCKf | 10 | | ns |
| 5 | $t_{d(TCKf -TDO)}$ | Delay time, TDO valid after TCK fall (TCKf) | | 45 | ns |

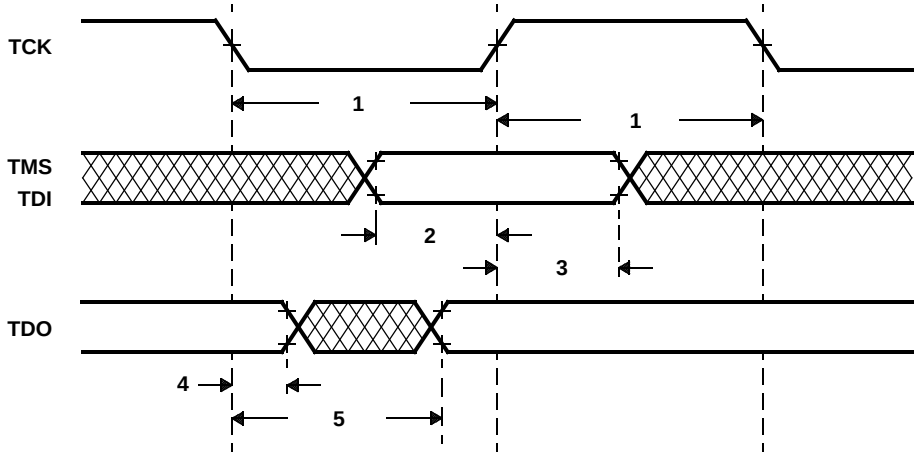



**Figure 12. JTAG Scan Timings**

## output timings

### switching characteristics for output timings versus load capacitance ($C_L$) (see Figure 13)

| PARAMETER | | | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| $t_r$ | Rise time, 8mA buffers | $C_L$ = 15 pF | 0.5 | 2.5 | ns |
| | | $C_L$ = 50 pF | 1.5 | 5.0 | |
| | | $C_L$ = 100 pF | 3.0 | 9.0 | |
| | | $C_L$ = 150 pF | 4.5 | 12.5 | |
| $t_f$ | Fall time, 8mA buffers | $C_L$ = 15 pF | 0.5 | 2.5 | ns |
| | | $C_L$ = 50 pF | 1.5 | 5.0 | |
| | | $C_L$ = 100 pF | 3.0 | 9.0 | |
| | | $C_L$ = 150 pF | 4.5 | 12.5 | |
| $t_r$ | Rise time, 4mA buffers | $C_L$ = 15 pF | 2.5 | 8 | ns |
| | | $C_L$ = 50 pF | 5 | 14 | |
| | | $C_L$ = 100 pF | 9 | 23 | |
| | | $C_L$ = 150 pF | 13 | 32 | |
| $t_f$ | Fall time, 4mA buffers | $C_L$ = 15 pF | 2.5 | 8 | ns |
| | | $C_L$ = 50 pF | 5 | 14 | |
| | | $C_L$ = 100 pF | 9 | 23 | |
| | | $C_L$ = 150 pF | 13 | 32 | |
| $t_r$ | Rise time, 2mA buffers | $C_L$ = 15 pF | 2.5 | 10 | ns |
| | | $C_L$ = 50 pF | 6.0 | 25 | |
| | | $C_L$ = 100 pF | 12 | 45 | |
| | | $C_L$ = 150 pF | 18 | 65 | |
| $t_f$ | Fall time, 2mA buffers | $C_L$ = 15 pF | 3 | 10 | ns |
| | | $C_L$ = 50 pF | 8.5 | 25 | |
| | | $C_L$ = 100 pF | 16 | 45 | |
| | | $C_L$ = 150 pF | 23 | 65 | |

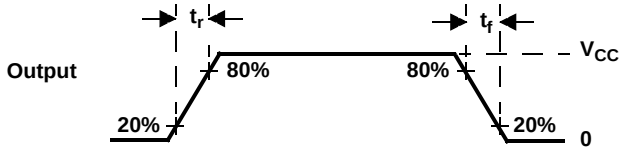



**Figure 13. CMOS-Level Outputs**

## input timings for general purpose input output pins

timing requirements for input timings[1][2]((see Figure 14)

| | | MIN | MAX | UNIT |
|---|---|---|---|---|
| $t_{pw}$ | Input minimum pulse width | $t_{c(VCLK)}$ + 10 | | ns |

1 $t_{c(VCLK)}$ = peripheral VBUS clock cycle time = $1/f_{(VCLK)}$
2 Applicable to peripheral pins in GPIO mode only.

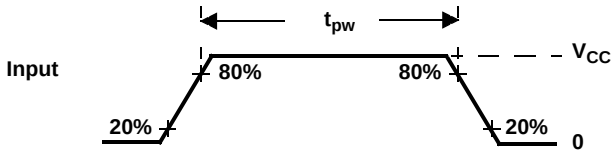



**Figure 14. CMOS-Level Inputs**

## flash timings

### timing requirements for program flash(1)

| | | | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $t_{acc\_delay}$ | Flash pump stabilization time | From sleep mode to standby mode | 2 | | | us |
| | | From standby mode to active mode | 1 | | | |
| | Flash bank stabilization time | From sleep mode to standby mode | 1.9 | | | us |
| | | From standby mode to active mode | 0.1 | | | |
| $t_{prog(16\text{-}bit)}$ | Half word (16-bit) programming time(2) | | 4 | 16 | 200 | µs |
| $t_{prog(Total)}$ | Total programming time(2)(3) | | | 1.3 | 15 | s |
| $t_{erase(sector)}$ | Sector erase time(2) | | | 2 | 15 | s |
| $t_{wec}$ | Write/erase cycles at $T_A$ = 85°C(2) | | | | 100 | cycles |
| $t_{fp(\overline{RST})}$ | Flash pump settling time from $\overline{RST}$ to SLEEP | | | $143t_{c(HCLK)}$ | | ns |
| $t_{fp(SLEEP)}$ | Initial flash pump settling time from SLEEP to STANDBY | | | $143t_{c(HCLK)}$ | | ns |
| $t_{fp(STANDBY)}$ | Initial flash pump settling time from STANDBY to ACTIVE | | | $72t_{c(HCLK)}$ | | ns |

1 For more detailed information on the flash core sectors, see the flash program and erase section of this data sheet.
2 Flash program/erase is specified only at a temperature range of -40C to 85C.
3The total programming time includes overhead of state machine, but does not include data transfer time.

## SPIn master mode timing parameters

### SPIn master mode external timing parameters (CLOCK PHASE = 0, SPInCLK = output, SPInSIMO = output, and SPInSOMI = input)(1)(2)(3)(see Figure 15)

| NO. | | | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| 1 | $t_{c(SPC)M}$ | Cycle time, SPInCLK (4) | 125 | $256t_{c(VCLK)}$ | ns |
| 2(5) | $t_{w(SPCH)M}$ | Pulse duration, SPInCLK high (clock polarity = 0) | $0.5t_{c(SPC)M} - t_r$ | $0.5t_{c(SPC)M} + 5$ | |
| | $t_{w(SPCL)M}$ | Pulse duration, SPInCLK low (clock polarity = 1) | $0.5t_{c(SPC)M} - t_f$ | $0.5t_{c(SPC)M} + 5$ | |
| 3(5) | $t_{w(SPCL)M}$ | Pulse duration, SPInCLK low (clock polarity = 0) | $0.5t_{c(SPC)M} - t_f$ | $0.5t_{c(SPC)M} + 5$ | |
| | $t_{w(SPCH)M}$ | Pulse duration, SPInCLK high (clock polarity = 1) | $0.5t_{c(SPC)M} - t_r$ | $0.5t_{c(SPC)M} + 5$ | |
| 4(5) | $t_{d(SPCH-SIMO)M}$ | Delay time, SPInCLK high to SPInSIMO valid (clock polarity = 0) | | 10 | |
| | $t_{d(SPCL-SIMO)M}$ | Delay time, SPInCLK low to SPInSIMO valid (clock polarity = 1) | | 10 | |
| 5(5) | $t_{v(SPCL-SIMO)M}$ | Valid time, SPInSIMO data valid after SPInCLK low (clock polarity = 0) | $t_{c(SPC)M} - 5 - t_f$ | | ns |
| | $t_{v(SPCH-SIMO)M}$ | Valid time, SPInSIMO data valid after SPInCLK high (clock polarity = 1) | $t_{c(SPC)M} - 5 - t_r$ | | |
| 6(5) | $t_{su(SOMI-SPCL)M}$ | Setup time, SPInSOMI before SPInCLK low (clock polarity = 0) | 6 | | ns |
| | $t_{su(SOMI-SPCH)M}$ | Setup time, SPInSOMI before SPInCLK high (clock polarity = 1) | 6 | | |
| 7(5) | $t_{v(SPCL-SOMI)M}$ | Valid time, SPInSOMI data valid after SPInCLK low (clock polarity = 0) | 6 | | ns |
| | $t_{v(SPCH-SOMI)M}$ | Valid time, SPInSOMI data valid after SPInCLK high (clock polarity = 1) | 6 | | |
| 8(5) | $t_{C2TDELAY}$ | Setup time CS active until SPICLK high (clock polarity = 0) | $C2TDELAY*t_{c(VCLK)} + 2*t_{c(VCLK)} - t_{f(SPICS)} + t_{r(SPICLK)}$ | | ns |
| | | Setup time CS active until SPICLK low (clock polarity = 1) | $C2TDELAY*t_{c(VCLK)} + 2*t_{c(VCLK)} - t_{f(SPICS)} + t_{f(SPICLK)}$ | | ns |
| 9(5) | $t_{T2CDELAY}$ | Hold time SPICLK low CS until inactive (clock polarity = 0) | | $0.5*t_{c(SPC)M} + T2CDELAY*t_{c(VCLK)} + t_{c(VCLK)} - t_{f(SPICLK)} + t_{r(SPICS)}$ | ns |
| | | Hold time SPICLK high until CS inactive (clock polarity = 1) | | $0.5*t_{c(SPC)M} + T2CDELAY*t_{c(VCLK)} + t_{c(VCLK)} - t_{r(SPICLK)} + t_{r(SPICS)}$ | ns |

1 The MASTER bit is set and the CLOCK PHASE bit is cleared.
2 $t_{c(VCLK)}$ = interface clock cycle time = $1/f_{(VCLK)}$
3 For rise and fall timings, see the "switching characteristics for output timings versus load capacitance" table.
4 When the SPI is in Master mode, the following must be true:
For PS values from 1 to 255:$t_{c(SPC)M} \geq (PS + 1)t_{c(VCLK)} \geq 100$ ns, where PS is the prescale value.
For PS values of 0:$t_{c(SPC)M} = 2t_{c(VCLK)} \geq 100$ ns.
5 The active edge of the SPInCLK signal referenced is controlled by the CLOCK POLARITY bit.

**SPIn master mode timing parameters (continued)**

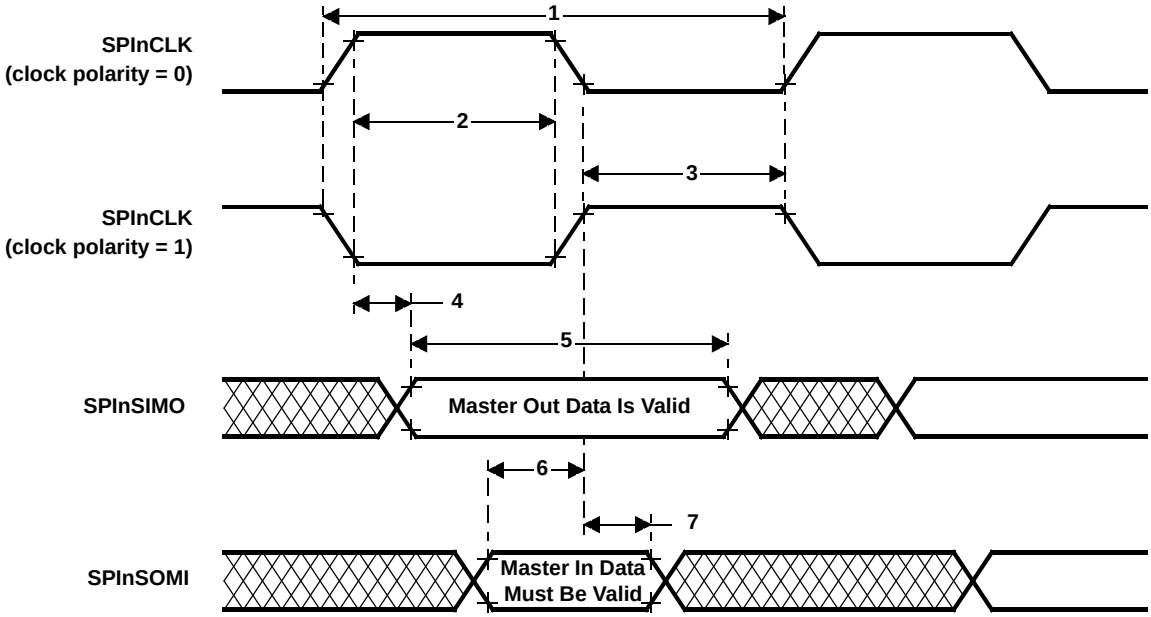



**Figure 15. SPIn Master Mode External Timing (CLOCK PHASE = 0)**

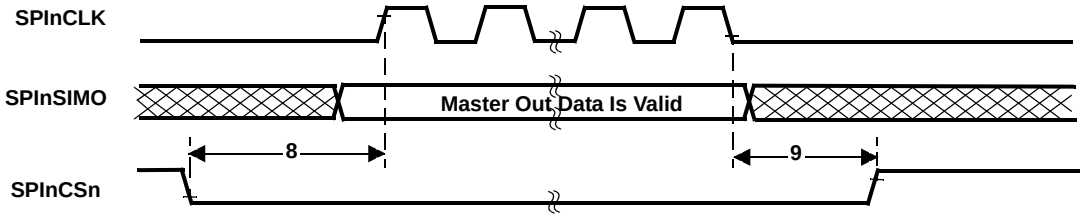



**Figure 16. SPI Master Mode Chip Select timing (CLOCK PHASE = 1; CLOCK POLARITY = 0)**

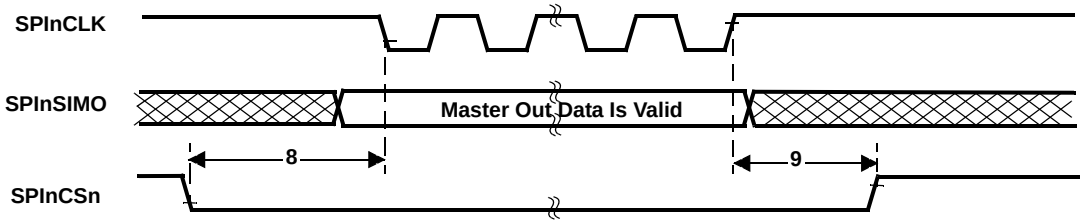



**Figure 17. SPI Master Mode Chip Select timing (CLOCK PHASE = 1; CLOCK POLARITY = 1)**

## SPIn master mode timing parameters (continued)

### SPIn master mode external timing parameters (CLOCK PHASE = 1, SPInCLK = output, SPInSIMO = output, and SPInSOMI = input)(1)(2)(3) (see Figure 18)

| NO. | | | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| 1 | $t_{c(SPC)M}$ | Cycle time, SPInCLK (4) | 125 | $256t_{c(VCLK)}$ | ns |
| 2(5) | $t_{w(SPCH)M}$ | Pulse duration, SPInCLK high (clock polarity = 0) | $0.5t_{c(SPC)M} - t_r$ | $0.5t_{c(SPC)M} + 5$ | |
| | $t_{w(SPCL)M}$ | Pulse duration, SPInCLK low (clock polarity = 1) | $0.5t_{c(SPC)M} - t_f$ | $0.5t_{c(SPC)M} + 5$ | |
| 3(5) | $t_{w(SPCL)M}$ | Pulse duration, SPInCLK low (clock polarity = 0) | $0.5t_{c(SPC)M} - t_f$ | $0.5t_{c(SPC)M} + 5$ | |
| | $t_{w(SPCH)M}$ | Pulse duration, SPInCLK high (clock polarity = 1) | $0.5t_{c(SPC)M} - t_r$ | $0.5t_{c(SPC)M} + 5$ | |
| 4(5) | $t_{v(SIMO-SPCH)M}$ | Valid time, SPInCLK high after SPInSIMO data valid (clock polarity = 0) | $0.5t_{c(SPC)M} - 10$ | | |
| | $t_{v(SIMO-SPCL)M}$ | Valid time, SPInCLK low after SPInSIMO data valid (clock polarity = 1) | $0.5t_{c(SPC)M} - 10$ | | |
| 5(5) | $t_{v(SPCH-SIMO)M}$ | Valid time, SPInSIMO data valid after SPInCLK high (clock polarity = 0) | $0.5t_{c(SPC)M} - 5 - t_r$ | | |
| | $t_{v(SPCL-SIMO)M}$ | Valid time, SPInSIMO data valid after SPInCLK low (clock polarity = 1) | $0.5t_{c(SPC)M} - 5 - t_f$ | | |
| 6(5) | $t_{su(SOMI-SPCH)M}$ | Setup time, SPInSOMI before SPInCLK high (clock polarity = 0) | 6 | | |
| | $t_{su(SOMI-SPCL)M}$ | Setup time, SPInSOMI before SPInCLK low (clock polarity = 1) | 6 | | |
| 7(5) | $t_{v(SPCH-SOMI)M}$ | Valid time, SPInSOMI data valid after SPInCLK high (clock polarity = 0) | 6 | | |
| | $t_{v(SPCL-SOMI)M}$ | Valid time, SPInSOMI data valid after SPInCLK low (clock polarity = 1) | 6 | | |

1 The MASTER bit is set and the CLOCK PHASE bit set.
2 $t_{c(VCLK)}$ = interface clock cycle time = $1/f_{(VCLK)}$
3 For rise and fall timings, see the "switching characteristics for output timings versus load capacitance" table.
4 When the SPI is in Master mode, the following must be true:
For PS values from 1 to 255:$t_{c(SPC)M} \geq (PS + 1)t_{c(VCLK)} \geq 100$ ns, where PS is the prescale value.
For PS values of 0:$t_{c(SPC)M} = 2t_{c(VCLK)} \geq 100$ ns.
5 The active edge of the SPInCLK signal referenced is controlled by the CLOCK POLARITY bit.

## SPIn master mode timing parameters (continued)

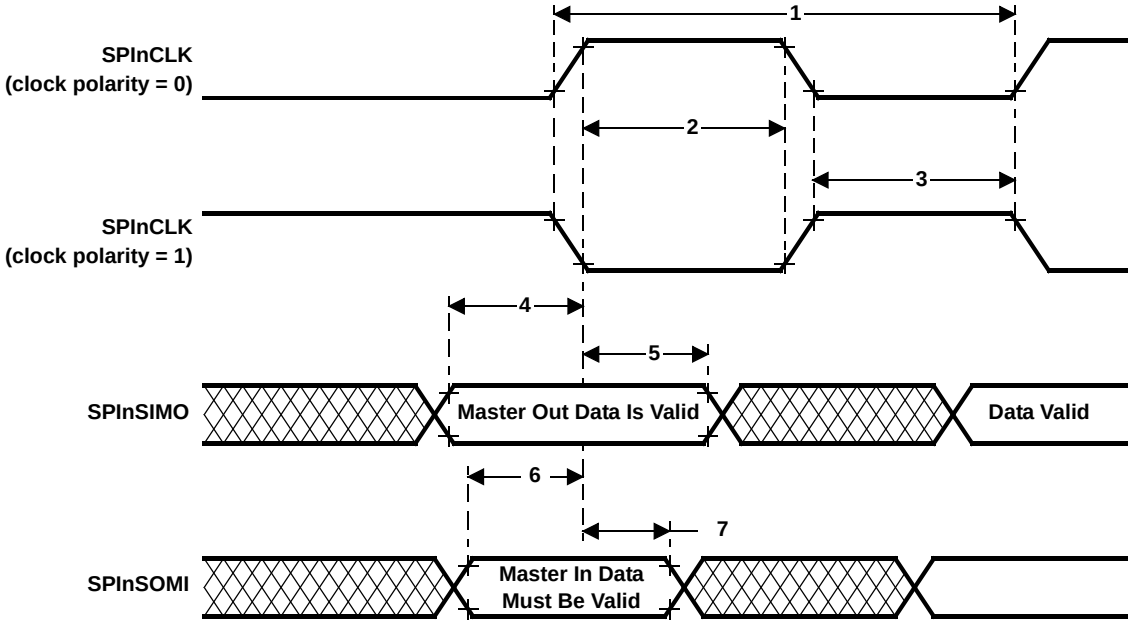



**Figure 18. SPIn Master Mode External Timing (CLOCK PHASE = 1)**

## SPIn slave mode timing parameters

### SPIn slave mode external timing parameters (CLOCK PHASE = 0, SPInCLK = input, SPInSIMO = input, and SPInSOMI = output)[1][2][3][4](see Figure 19)

| NO | | | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| 1 | $t_{c(SPC)S}$ | Cycle time, SPInCLK[5] | 100 | $256t_{c(VCLK)}$ | ns |
| 2[6] | $t_{w(SPCH)S}$ | Pulse duration, SPInCLK high (clock polarity = 0) | $0.5t_{c(SPC)S} - 0.25t_{c(VCLK)}$ | $0.5t_{c(SPC)S} + 0.25t_{c(VCLK)}$ | |
| | $t_{w(SPCL)S}$ | Pulse duration, SPInCLK low (clock polarity = 1) | $0.5t_{c(SPC)S} - 0.25t_{c(VCLK)}$ | $0.5t_{c(SPC)S} + 0.25t_{c(VCLK)}$ | |
| 3[6] | $t_{w(SPCL)S}$ | Pulse duration, SPInCLK low (clock polarity = 0) | $0.5t_{c(SPC)S} - 0.25t_{c(VCLK)}$ | $0.5t_{c(SPC)S} + 0.25t_{c(VCLK)}$ | |
| | $t_{w(SPCH)S}$ | Pulse duration, SPInCLK high (clock polarity = 1) | $0.5t_{c(SPC)S} - 0.25t_{c(VCLK)}$ | $0.5t_{c(SPC)S} + 0.25t_{c(VCLK)}$ | |
| 4[6] | $t_{d(SPCH-SOMI)S}$ | Delay time, SPInCLK high to SPInSOMI valid (clock polarity = 0) | $0.5t_{c(VCLK)}$ | $1.5t_{c(VCLK)}$ | |
| | $t_{d(SPCL-SOMI)S}$ | Delay time, SPInCLK low to SPInSOMI valid (clock polarity = 1) | $0.5t_{c(VCLK)}$ | $1.5t_{c(VCLK)}$ | |
| 5[6] | $t_{v(SPCH-SOMI)S}$ | Valid time, SPInSOMI data valid after SPInCLK high (clock polarity = 0) | $t_{c(SPC)S}-1.5t_{c(VCLK)}-t_f$ | | |
| | $t_{v(SPCL-SOMI)S}$ | Valid time, SPInSOMI data valid after SPInCLK low (clock polarity = 1) | $t_{c(SPC)S}-1.5t_{c(VCLK)}-t_r$ | | |
| 6[6] | $t_{su(SIMO-SPCL)S}$ | Setup time, SPInSIMO before SPInCLK low (clock polarity = 0) | 6 | | |
| | $t_{su(SIMO-SPCH)S}$ | Setup time, SPInSIMO before SPInCLK high (clock polarity = 1) | 6 | | |
| 7[6] | $t_{v(SPCL-SIMO)S}$ | Valid time, SPInSIMO data valid after SPInCLK low (clock polarity = 0) | 6 | | |
| | $t_{v(SPCH-SIMO)S}$ | Valid time, SPInSIMO data valid after SPInCLK high (clock polarity = 1) | 6 | | |

1 The MASTER bit is cleared and the CLOCK PHASE bit is cleared.
2 If the SPI is in slave mode, the following must be true: $t_{c(SPC)S} \geq (PS + 1)\ t_{c(VCLK)}$, where PS = prescale value.
3 For rise and fall timings, see the "switching characteristics for output timings versus load capacitance" table.
4 $t_{c(VCLK)}$ = interface clock cycle time = $1/f_{(VCLK)}$
5 When the SPIn is in Slave mode, the following must be true:
For PS values from 1 to 255:$t_{c(SPC)S} \geq (PS +1)t_{c(VCLK)} \geq 100$ ns, where PS is the prescale value.
For PS values of 0:$t_{c(SPC)S} = 2t_{c(VCLK)} \geq 100$ ns.
6 The active edge of the SPInCLK signal referenced is controlled by the CLOCK POLARITY bit.

## SPIn slave mode timing parameters (continued)

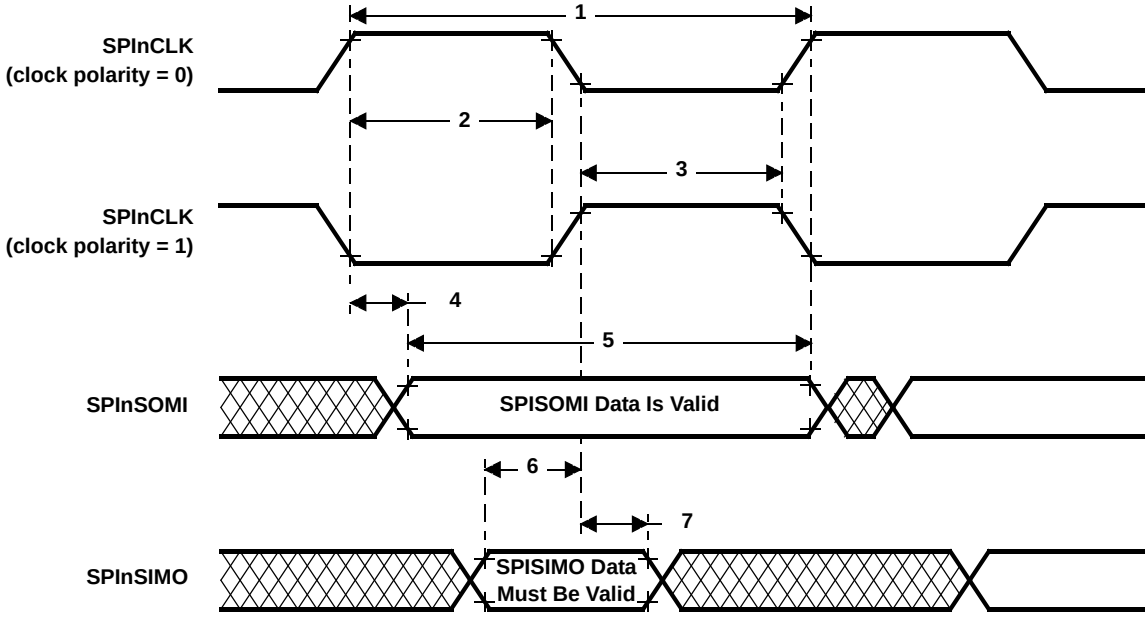



**Figure 19. SPIn Slave Mode External Timing (CLOCK PHASE = 0)**

## SPIn slave mode timing parameters (continued)

### SPIn slave mode external timing parameters (CLOCK PHASE = 1, SPInCLK = input, SPInSIMO = input, and SPInSOMI = output)(1)(2)(3)(4)(see Figure 20)

| NO | | | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| 1 | $t_{c(SPC)S}$ | Cycle time, SPInCLK(5) | 100 | $256t_{c(VCLK)}$ | ns |
| 2(6) | $t_{w(SPCH)S}$ | Pulse duration, SPInCLK high (clock polarity = 0) | $0.5t_{c(SPC)S}-0.25t_{c(VCLK)}$ | $0.5t_{c(SPC)S}+0.25t_{c(VCLK)}$ | |
| | $t_{w(SPCL)S}$ | Pulse duration, SPInCLK low (clock polarity = 1) | $0.5t_{c(SPC)S}-0.25t_{c(VCLK)}$ | $0.5t_{c(SPC)S}+0.25t_{c(VCLK)}$ | |
| 3(6) | $t_{w(SPCL)S}$ | Pulse duration, SPInCLK low (clock polarity = 0) | $0.5t_{c(SPC)S}-0.25t_{c(VCLK)}$ | $0.5t_{c(SPC)S}+0.25t_{c(VCLK)}$ | |
| | $t_{w(SPCH)S}$ | Pulse duration, SPInCLK high (clock polarity = 1) | $0.5t_{c(SPC)S}-0.25t_{c(VCLK)}$ | $0.5t_{c(SPC)S}+0.25t_{c(VCLK)}$ | |
| 4(6) | $t_{v(SOMI-SPCH)S}$ | Valid time, SPInCLK high after SPInSOMI data valid (clock polarity = 0) | $0.5t_{c(VCLK)}$ | $1.5t_{c(VCLK)}$ | |
| | $t_{v(SOMI-SPCL)S}$ | Valid time, SPInCLK low after SPInSOMI data valid (clock polarity = 1) | $0.5t_{c(VCLK)}$ | $1.5t_{c(VCLK)}$ | |
| 5(6) | $t_{v(SPCH-SOMI)S}$ | Valid time, SPInSOMI data valid after SPInCLK high (clock polarity = 0) | $t_{c(SPC)S}-1.5t_{c(VCLK)}-t_f$ | | |
| | $t_{v(SPCL-SOMI)S}$ | Valid time, SPInSOMI data valid after SPInCLK low (clock polarity = 1) | $t_{c(SPC)S}-1.5t_{c(VCLK)}-t_r$ | | |
| 6(6) | $t_{su(SIMO-SPCH)S}$ | Setup time, SPInSIMO before SPInCLK high (clock polarity = 0) | 6 | | |
| | $t_{su(SIMO-SPCL)S}$ | Setup time, SPInSIMO before SPInCLK low (clock polarity = 1) | 6 | | |
| 7(6) | $t_{v(SPCH-SIMO)S}$ | Valid time, SPInSIMO data valid after SPInCLK high (clock polarity = 0) | 6 | | |
| | $t_{v(SPCL-SIMO)S}$ | Valid time, SPInSIMO data valid after SPInCLK low (clock polarity = 1) | 6 | | |

1 The MASTER bit is cleared and the CLOCK PHASE bit is set.
2 If the SPI is in slave mode, the following must be true: $t_{c(SPC)S} \geq (PS + 1)\ t_{c(VCLK)}$, where PS = prescale value.
3 For rise and fall timings, see the "switching characteristics for output timings versus load capacitance" table.
4 $t_{c(VCLK)}$ = interface clock cycle time = $1/f_{(VCLK)}$
5 When the SPIn is in Slave mode, the following must be true:
For PS values from 1 to 255:$t_{c(SPC)S} \geq (PS +1)t_{c(VCLK)} \geq 100$ ns, where PS is the prescale value.
For PS values of 0:$t_{c(SPC)S} = 2t_{c(VCLK)} \geq 100$ ns.
6 The active edge of the SPInCLK signal referenced is controlled by the CLOCK POLARITY bit.

## SPIn slave mode timing parameters (continued)

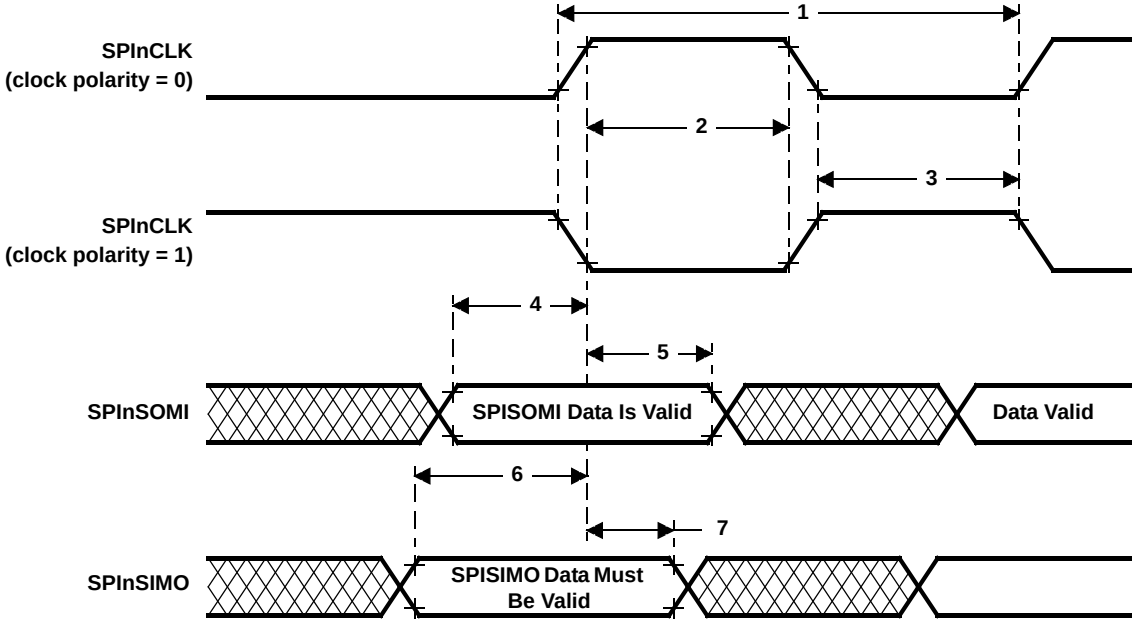



**Figure 20. SPIn Slave Mode External Timing (CLOCK PHASE = 1)**

NOTE : Data transmission/reception characteristics for isosynchronous mode with external clocking are similar to the asynchronous mode. Data transmission occurs on the SCICLK rising edge, and data reception on the SCICLK falling edge.

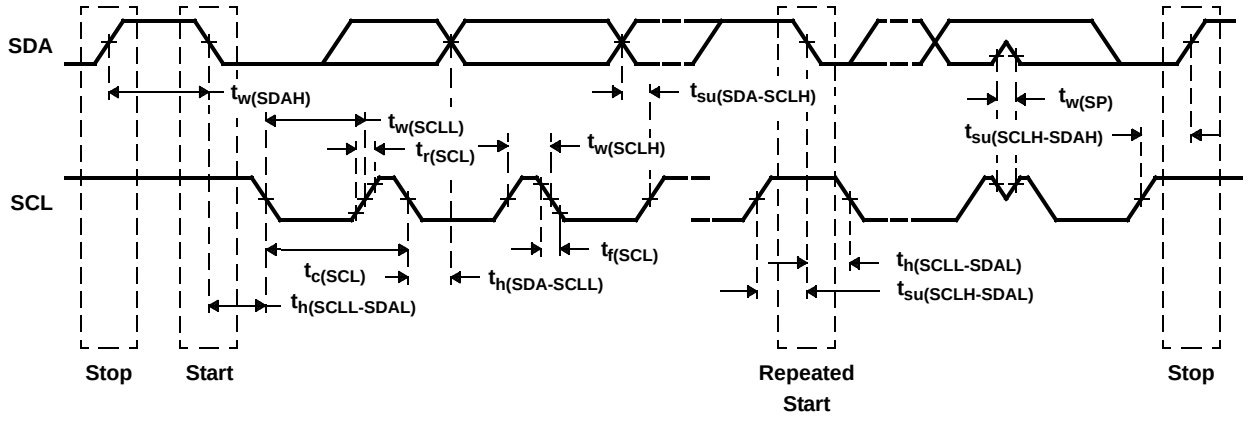
## I2C timing

Table 11, I2C Signals (SDA and SCL) Switching Characteristics(1) below assumes testing over recommended operating conditions.

**Table 11. I2C Signals (SDA and SCL) Switching Characteristics(1)**

| PARAMETER | | | STANDARD MODE | | FAST MODE | | UNIT |
|---|---|---|---|---|---|---|---|
| | | | MIN | MAX | MIN | MAX | |
| $t_{c(I2CCLK)}$ | Cycle time, I2C module clock | | 75 | 150 | 75 | 150 | ns |
| $t_{c(SCL)}$ | Cycle time, SCL | | 10 | | 2.5 | | µs |
| $t_{su(SCLH-SDAL)}$ | Setup time, SCL high before SDA low (for a repeated START condition) | | 4.7 | | 0.6 | | µs |
| $t_{h(SCLL-SDAL)}$ | Hold time, SCL low after SDA low (for a repeated START condition) | | 4 | | 0.6 | | µs |
| $t_{w(SCLL)}$ | Pulse duration, SCL low | | 4.7 | | 1.3 | | µs |
| $t_{w(SCLH)}$ | Pulse duration, SCL high | | 4 | | 0.6 | | µs |
| $t_{su(SDA-SCLH)}$ | Setup time, SDA valid before SCL high | | 250 | | 100 | | ns |
| $t_{h(SDA-SCLL)}$ | Hold time, SDA valid after SCL low | For I2C bus devices | 0 | 3.45(2) | 0 | 0.9 | µs |
| $t_{w(SDAH)}$ | Pulse duration, SDA high between STOP and START conditions | | 4.7 | | 1.3 | | µs |
| $t_{su(SCLH-SDAH)}$ | Setup time, SCL high before SDA high (for STOP condition) | | 4.0 | | 0.6 | | µs |
| $t_{w(SP)}$ | Pulse duration, spike (must be suppressed) | | | | 0 | 50 | ns |
| $C_b$(3) | Capacitive load for each bus line | | | 400 | | 400 | pF |

1 The I2C pins SDA and SCL do not feature fail-safe I/O buffers. These pins could potentially draw current when the device is powered down.
2 The maximum $t_{h(SDA-SCLL)}$ for I2C bus devices needs only be met if the device does not stretch the low period ($t_{w(SCLL)}$) of the SCL signal.
3 $C_b$ = The total capacitance of one bus line in pF.




NOTE:A device must internally provide a hold time of at least 300 ns for the SDA signal (referred to the $V_{IHmin}$ of the SCL signal) to bridge the undefined region of the falling edge of SCL.

NOTE:The maximum $t_{h(SDA-SCLL)}$ needs only be met if the device does not stretch the LOW period ($t_{w(SCLL)}$) of the SCL signal.

NOTE:A Fast-mode I2C-bus device can be used in a standard-mode I2C-bus system, but the requirement $t_{su(SDA-SCLH)} \geq 250$ ns must then be met. This will automatically be the case if the device does not stretch the LOW period of the SCL signal. If such a device does stretch the LOW period of the SCL signal, it must output the next data bit to the SDA line $t_r$ max + $t_{su(SDA-SCLH)}$.

NOTE:$C_b$ = total capacitance of one bus line in pF. If mixed with fast-mode devices, faster fall-times are allowed.

**Figure 21. I2C Timings**

## standard CAN controller (SCC) mode timings

### dynamic characteristics for the CANSTX and CANSRX pins

| PARAMETER | | MIN | MAX | UNIT |
|---|---|---|---|---|
| $t_d$(CANSTX) | Delay time, transmit shift register to CANSTX pin(1) | | 15 | ns |
| $t_d$(CANSRX) | Delay time, CANSRX pin to receive shift register | | 5 | ns |

1 These values do not include rise/fall times of the output buffer.

## high-end timer (HET) timings

### dynamic characteristics for the HET pins

| PARAMETER | | MIN | MAX | UNIT |
|---|---|---|---|---|
| $t_{opw}$(HET) | Output pulse width, this is the minimum pulse width that can be generated(1) | $1/f_{(VCLK2)}$ | | ns |
| $t_{ipw}$(HET) | Input pulse width, this is the minimum pulse width that can be captured(2) | $1/f_{(VCLK2)}$ | | ns |

1 $t_{opw}(HET) = HRP_{(min)} = hr_{(min)}$ / SYSCLK
2 $t_{ipw}(HET) = LRP_{(min)} = hr_{(min)} * lr_{(min)}$ / SYSCLK

## multi-buffered A-to-D converter (MibADC)

The multi-buffered A-to-D converter (MibADC) has a separate power bus for its analog circuitry that enhances the A-to-D performance by preventing digital switching noise on the logic circuitry which could be present on $V_{SS}$ and $V_{CC}$ from coupling into the A-to-D analog stage. All A-to-D specifications are given with respect to $AD_{REFLO}$ unless otherwise noted.

Resolution . . . . . 10 bits (1024 values)
Monotonic . . . . . Assured
Output conversion code . . . . . 00h to 3FFh [00 for $V_{AI} \leq AD_{REFLO}$; 3FF for $V_{AI} \geq AD_{REFHI}$]

### MibADC recommended operating conditions(1)

| | | MIN | MAX | UNIT |
|---|---|---|---|---|
| $AD_{REFHI}$ | A-to-D high -voltage reference source | $V_{SSAD}$ | $V_{CCAD}$ | V |
| $AD_{REFLO}$ | A-to-D low-voltage reference source | $V_{SSAD}$ | $V_{CCAD}$ | V |
| $V_{AI}$ | Analog input voltage | $V_{SSAD}$ – 0.3 | $V_{CCAD}$ + 0.3 | V |
| $I_{AIC}$ | Analog input clamp current(2) ($V_{AI} < V_{SSAD}$ – 0.3 or $V_{AI} > V_{CCAD}$ + 0.3) | – 2 | 2 | mA |

1 For $V_{CCAD}$ and $V_{SSAD}$ recommended operating conditions, see the "device recommended operating conditions" table.
2 Input currents into any ADC input channel outside the specified limits could affect conversion results of other channels.

### operating characteristics over full ranges of recommended operating conditions(3)(4)

| PARAMETER | | DESCRIPTION/CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $R_{MUX}$ | Analog input mux-on resistance | See Figure 22 | | 50 | 100 | Ω |
| $R_{ADC}$ | ADC sample switch on-resistance | See Figure 22 | | 250 | 500 | Ω |
| $C_{MUX}$ | Input mux capacitance | See Figure 22 | | | 24 | pF |
| $C_{ADC}$ | ADC sample switch-on capacitance | See Figure 22 | | | 7 | pF |
| $I_{AIL}$ | Analog input leakage current | | –1 | | 1 | µA |
| $I_{ADREFHI}$ | $AD_{REFHI}$ input current | $AD_{REFHI}$ = 3.6 V, $AD_{REFLO}$ = $V_{SSAD}$ | | | 5 | mA |
| CR | Conversion range over which specified accuracy is maintained | $AD_{REFHI}$ – $AD_{REFLO}$ | 4.75 | | 5.25 | V |
| $E_{DNL}$ | Differential nonlinearity error | Difference between the actual step width and the ideal value. (See Figure 23) | | | ±1.5 | LSB |
| $E_{INL}$ | Integral nonlinearity error | Maximum deviation from the best straight line through the MibADC. MibADC transfer characteristics, excluding the quantization error. (See Figure 24) | | | ±2.0 | LSB |
| $E_{TOT}$ | Total error/Absolute accuracy | Maximum value of the difference between an analog value and the ideal midstep value. (See Figure 25) | | | ±2 | LSB |

3 $V_{CCAD} = AD_{REFHI}$
4 1 LSB = $(AD_{REFHI} – AD_{REFLO})/2^{10}$ for the MibADC

### multi-buffered A-to-D converter (MibADC) (continued)

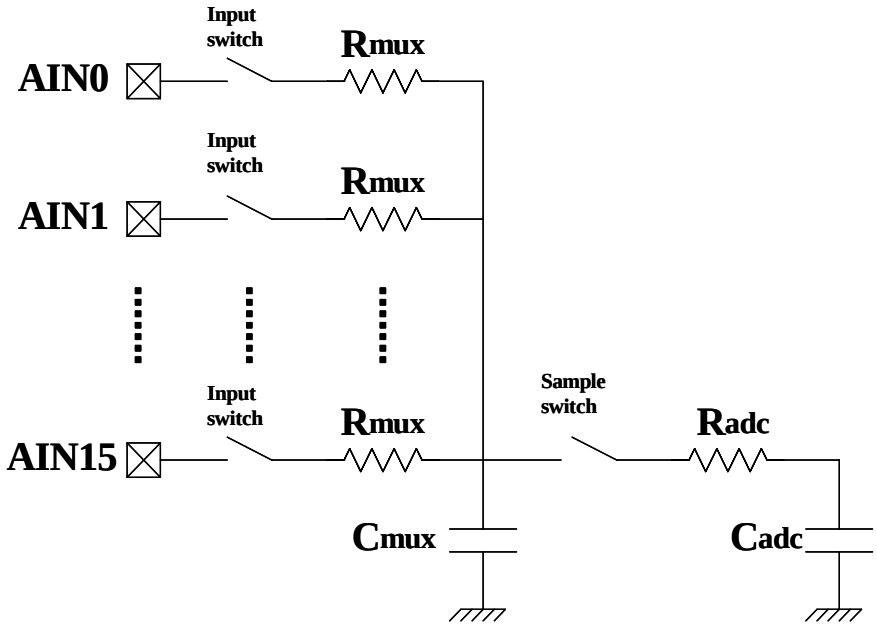



**Figure 22. MibADC Input Equivalent Circuit**

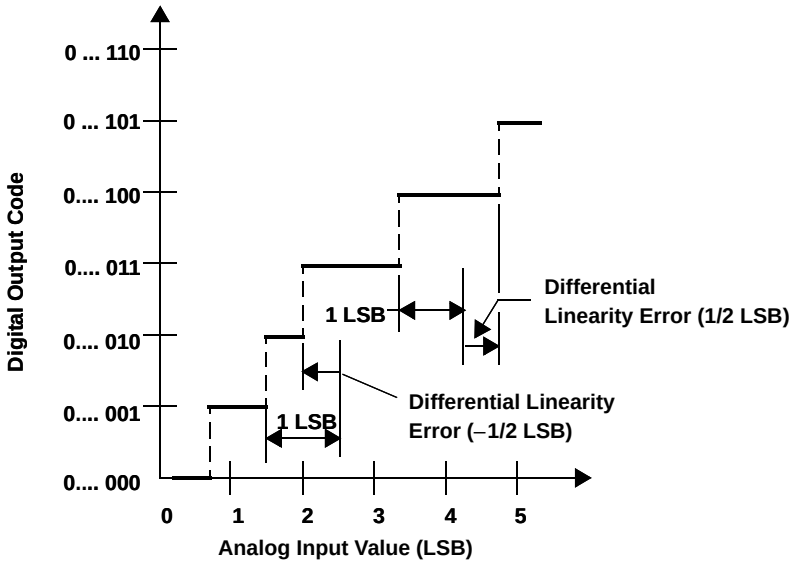
### multi-buffer adc timing requirements

| | | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|
| $t_{c(ADCLK)}$ | Cycle time, MibADC clock | 0.05 | | | µs |
| $t_{d(SH)}$ | Delay time, sample and hold time | 1 | | | µs |
| $t_{d(C)}$ | Delay time, conversion time | 0.55 | | | µs |
| $t_{d(SHC)}$ (1) | Delay time, total sample/hold and conversion time | 1.55 | | | µs |
| $t_{d(PU-ADV)}$ (1) | Delay time, ADC stable after exiting power-down mode | 0 | | | ns |

1 This is the minimum sample/hold and conversion time that can be achieved. These parameters are dependent on many factors.

## multi-buffered A-to-D converter (MibADC) (continued)

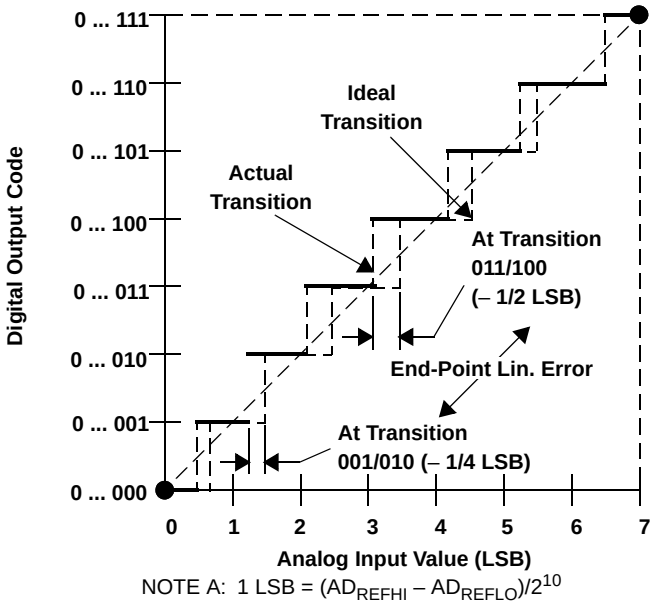
The differential nonlinearity error shown in Figure 23 (sometimes referred to as differential linearity) is the difference between an actual step width and the ideal value of 1 LSB.




NOTE A: 1 LSB = $(AD_{REFHI} – AD_{REFLO})/2^{10}$

**Figure 23. Differential Nonlinearity (DNL)**

The integral nonlinearity error shown in Figure 24 (sometimes referred to as linearity error) is the deviation of the values on the actual transfer function from a straight line.

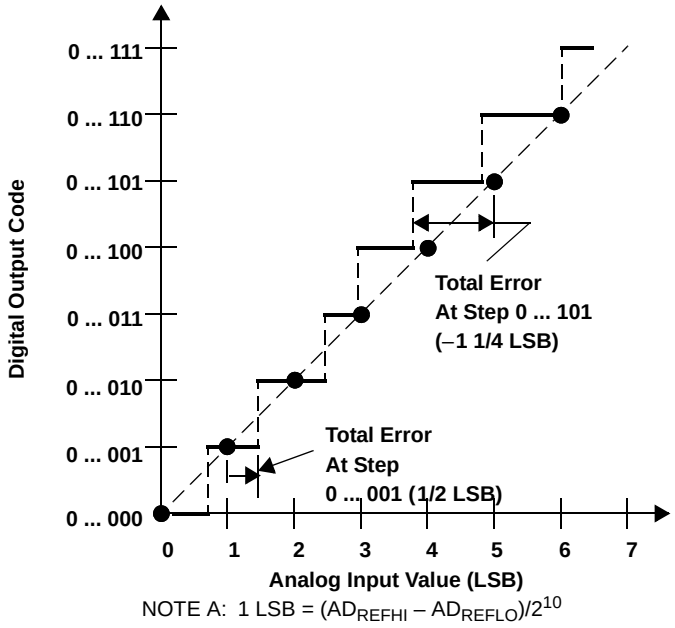



NOTE A: 1 LSB = $(AD_{REFHI} – AD_{REFLO})/2^{10}$

**Figure 24. Integral Nonlinearity (INL) Error**

## multi-buffer A-to-D converter (MibADC) (continued)

The absolute accuracy or total error of an MibADC as shown in Figure 25 is the maximum value of the difference between an analog value and the ideal midstep value.

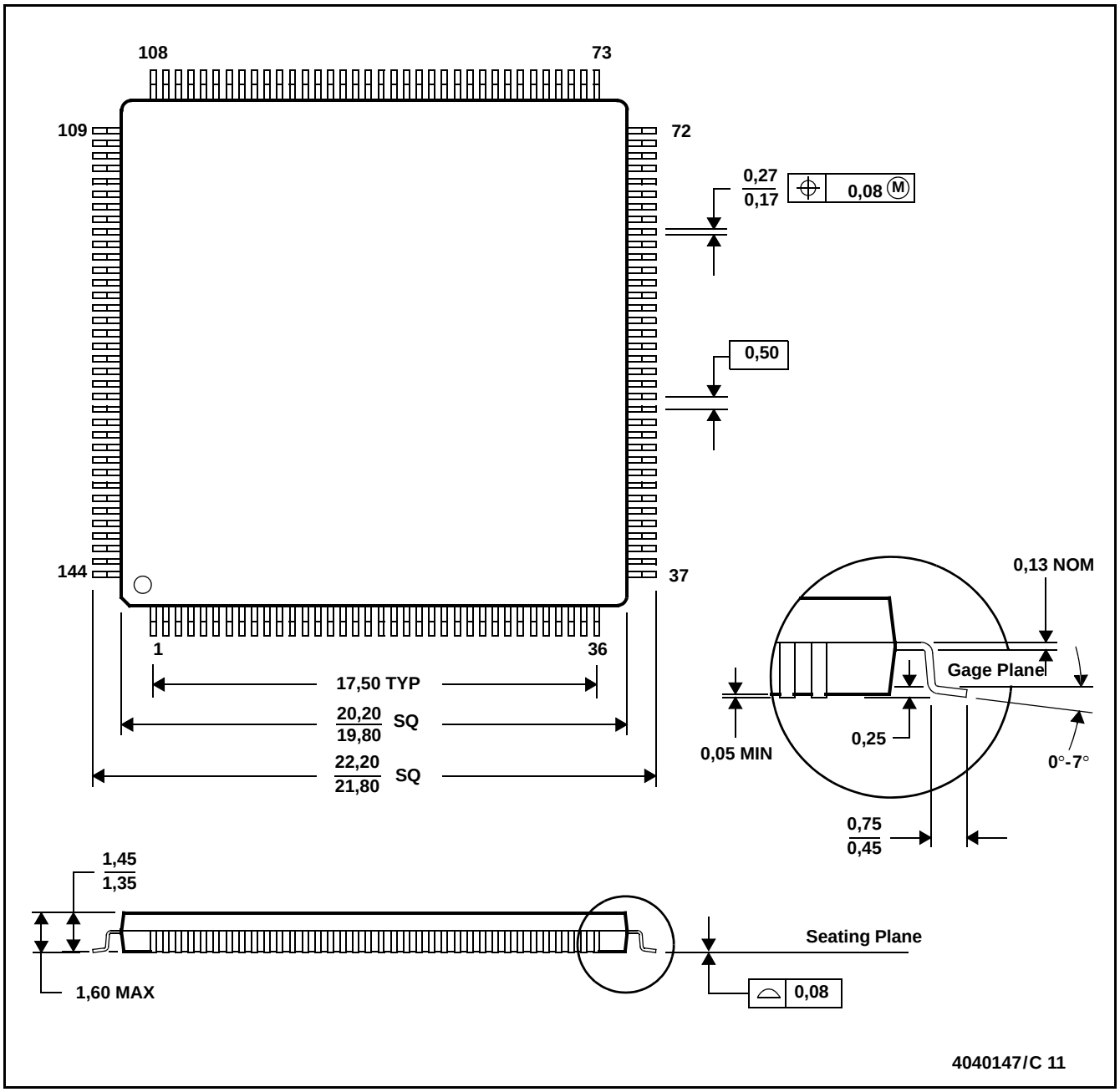



NOTE A: 1 LSB = $(AD_{REFHI} – AD_{REFLO})/2^{10}$

**Figure 25. Absolute Accuracy (Total) Error**

## MECHANICAL DATA

**PGE (S-PQFP-G144)** **PLASTIC QUAD FLATPACK**




NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS-026

**Thermal Resistance Characteristics**

| PARAMETER | °C/W |
|---|---|
| $R_{\Theta JA}$ | 98 |
| $R_{\Theta JB}$ | 43 |
| $R_{\Theta JC}$ | 22 |

**List of Figures**

**List of Tables**

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