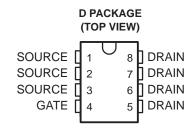
- Low  $r_{DS(on)} \dots 0.09 \Omega$  Typ at  $V_{GS} = -10 \text{ V}$
- 3 V Compatible
- Requires No External V<sub>CC</sub>
- TTL and CMOS Compatible Inputs
- V<sub>GS(th)</sub> = −1.5 V Max
- Available in Ultrathin TSSOP Package (PW)
- ESD Protection Up to 2 kV per MIL-STD-883C, Method 3015

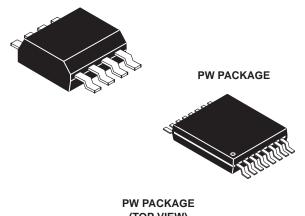
# description

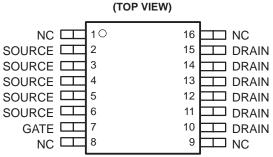
The TPS1101 is a single, low-r<sub>DS(on)</sub>, P-channel, enhancement-mode MOSFET. The device has been optimized for 3-V or 5-V power distribution in battery-powered systems by means of the Texas Instruments LinBiCMOS<sup>TM</sup> process. With a maximum V<sub>GS(th)</sub> of -1.5 V and an I<sub>DSS</sub> of only 0.5  $\mu$ A, the TPS1101 is the ideal high-side switch for low-voltage, portable battery-management systems where maximizing battery life is a primary concern. The low r<sub>DS(on)</sub> and excellent ac characteristics (rise time 5.5 ns typical) of the TPS1101 make it the logical choice for low-voltage switching applications such as power switches for pulse-width-modulated (PWM) controllers or motor/bridge drivers.

The ultrathin thin shrink small-outline package or TSSOP (PW) version fits in height-restricted places where other P-channel MOSFETs cannot. The size advantage is especially important where board height restrictions do not allow for an small-outline integrated circuit (SOIC) package. Such applications include notebook computers, personal digital assistants (PDAs), cellular



**D PACKAGE** 





NC - No internal connection

telephones, and PCMCIA cards. For existing designs, the D-packaged version has a pinout common with other P-channel MOSFETs in SOIC packages.

#### **AVAILABLE OPTIONS**

	PACKAGED	DEVICES†	CHIP FORM
TJ	SMALL OUTLINE (D)	TSSOP (PW)	(Y)
-40°C to 150°C	TPS1101D	TPS1101PWLE	TPS1101Y

<sup>&</sup>lt;sup>†</sup> The D package is available taped and reeled. Add an R suffix to device type (e.g., TPS1101DR). The PW package is only available left-end taped and reeled (indicated by the LE suffix on the device type; e.g., TPS1101PWLE). The chip form is tested at 25°C.

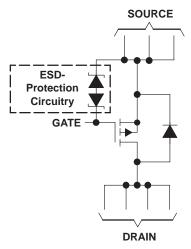


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LinBiCMOS is a trademark of Texas Instruments Incorporated.



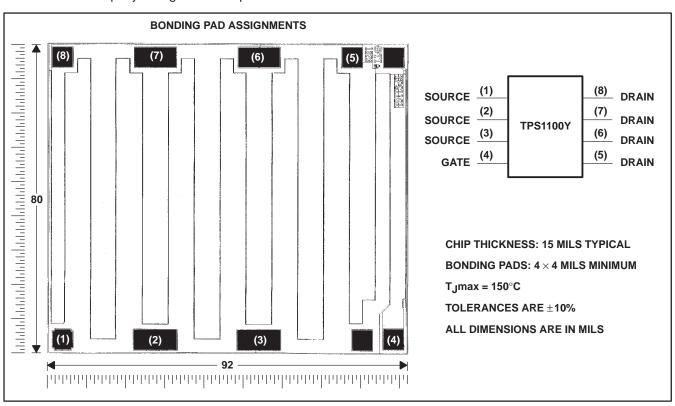
# schematic



NOTE A: For all applications, all source terminals should be connected and all drain terminals should be connected.

# **TPS1101Y** chip information

This chip, when properly assembled, displays characteristics similar to the TPS1101. Thermal compression or ultrasonic bonding may be used on the doped aluminum bonding pads. The chips may be mounted with conductive epoxy or a gold-silicon preform.





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# absolute maximum ratings over operating free-air temperature (unless otherwise noted)†

Drain-to-source voltage, V <sub>DS</sub> -15						
Gate-to-source voltage, VGS 2 or – 15						
		Danakasa	T <sub>A</sub> = 25°C	±0.62		
	V 27V	D package	T <sub>A</sub> = 125°C	±0.39		
	$V_{GS} = -2.7 \text{ V}$	PW package	T <sub>A</sub> = 25°C	±0.61		
		P vv package	T <sub>A</sub> = 125°C	±0.38		
		D package	T <sub>A</sub> = 25°C	±0.88		
	Vac - 2V	D раскаде	T <sub>A</sub> = 125°C	±0.47		
	V <sub>G</sub> S = −3 V	PW package	T <sub>A</sub> = 25°C	±0.86		
Continuous drain current (T <sub>J</sub> = 150°C), I <sub>D</sub> ‡		F vv package	T <sub>A</sub> = 125°C	±0.45	Α	
Continuous diam current (1) = 150 C), ID+	V <sub>GS</sub> = -4.5 V	D package	T <sub>A</sub> = 25°C	±1.52	A	
		Браскаде	T <sub>A</sub> = 125°C	±0.71		
		PW package	T <sub>A</sub> = 25°C	±1.44		
		P vv package	T <sub>A</sub> = 125°C	±0.67		
		Dipackago	T <sub>A</sub> = 25°C	±2.30		
	V <sub>GS</sub> = -10 V	D package	T <sub>A</sub> = 125°C	±1.04		
	VGS = -10 V	PW package	T <sub>A</sub> = 25°C	±2.18		
		P vv package	T <sub>A</sub> = 125°C	±0.98		
Pulsed drain current, ID <sup>‡</sup>			T <sub>A</sub> = 25°C	±10	Α	
Continuous source current (diode conduction), Is $T_A = 25^{\circ}C$ $-1.1$						
Storage temperature range, T <sub>Stg</sub> -55 to 150						
Operating junction temperature range, T <sub>J</sub> -40 to 150						
Operating free-air temperature range, T <sub>A</sub> -40 to 125						
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds 260						

<sup>†</sup> Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

#### **DISSIPATION RATING TABLE**

PACKAGE	$T_{\mbox{A}} \le 25^{\circ}\mbox{C}$ POWER RATING	DERATING FACTOR <sup>‡</sup> ABOVE T <sub>A</sub> = 25°C	T <sub>A</sub> = 70°C POWER RATING	T <sub>A</sub> = 85°C POWER RATING	T <sub>A</sub> = 125°C POWER RATING
D	791 mW	6.33 mW/°C	506 mW	411 mW	158 mW
PW	710 mW	5.68 mW/°C	454 mW	369 mW	142 mW

<sup>‡</sup> Maximum values are calculated using a derating factor based on  $R_{\theta JA} = 158^{\circ}\text{C/W}$  for the D package and  $R_{\theta JA} = 176^{\circ}\text{C/W}$  for the PW package. These devices are mounted on an FR4 board with no special thermal considerations.



<sup>\$\</sup>frac{1}{2}\$ Maximum values are calculated using a derating factor based on \$R\_{\theta JA} = 158^{\circ}C/W\$ for the D package and \$R\_{\theta JA} = 176^{\circ}C/W\$ for the PW package. These devices are mounted on an FR4 board with no special thermal considerations.

# TPS1101, TPS1101Y SINGLE P-CHANNEL ENHANCEMENT-MODE MOSFETS

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# electrical characteristics at $T_J = 25^{\circ}C$ (unless otherwise noted)

# static

	PARAMETER	TES	T CONDITION	NC.	7	ΓPS1101		TI	PS1101Y	′	UNIT
	FARAWIETER	TEST CONDITIONS			MIN	TYP	MAX	MIN	TYP	MAX	UNIT
V <sub>GS(th)</sub>	Gate-to-source threshold voltage	$V_{DS} = V_{GS}$ , $I_{D} = -250 \mu A$			-1	-1.25	-1.5		-1.25		V
V <sub>SD</sub>	Source-to-drain voltage (diode-forward voltage)†	I <sub>S</sub> = -1 A,	$S = -1 \text{ A}, \qquad V_{GS} = 0 \text{ V}$			-1.04			-1.04		V
IGSS	Reverse gate current, drain short circuited to source	V <sub>DS</sub> = 0 V,	V <sub>GS</sub> = -12	V			±100				nA
Inco	Zero-gate-voltage drain	$V_{DS} = -12 V$ ,	\/oo = 0 \/	T <sub>J</sub> = 25°C			-0.5				μΑ
IDSS	current	VDS = -12  V,	VGS = 0 V	T <sub>J</sub> = 125°C			-10				μΑ
		$V_{GS} = -10 \text{ V}$	$I_D = -2.5 A$			90			90		
	Static drain-to-source	$V_{GS} = -4.5 \text{ V}$	$I_D = -1.5 A$			134	190		134		<b>m</b> O
rDS(on)	on-state resistance†	$V_{GS} = -3 V$	L- 0.5 A			198	310		198		mΩ
		$V_{GS} = -2.7 \text{ V}$	$I_D = -0.5 A$			232	400		232		
9fs	Forward transconductance†	$V_{DS} = -10 \text{ V},$	I <sub>D</sub> = -2 A	I <sub>D</sub> = -2 A		4.3			4.3		S

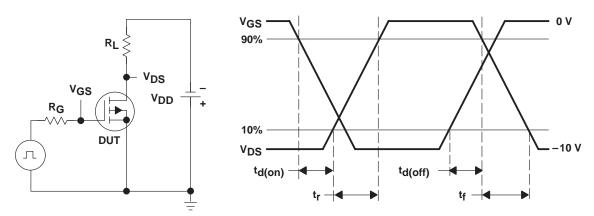
<sup>†</sup> Pulse test: pulse duration ≤ 300 μs, duty cycle ≤ 2%

# dynamic

	PARAMETER		TEST CONDITIONS			TPS1101, TPS1101Y			
	PARAINETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT		
Qg	Total gate charge					11.25			
Qgs	Gate-to-source charge	$V_{DS} = -10 V$ ,	$V_{GS} = -10 V$ ,	$I_{D} = -1 A$		1.5		nC	
Q <sub>gd</sub>	Gate-to-drain charge	1				2.6			
t <sub>d</sub> (on)	Turn-on delay time					6.5		ns	
td(off)	Turn-off delay time	$V_{DD} = -10 \text{ V},$		$I_{D} = -1 A$ ,		19		ns	
t <sub>r</sub>	Rise time	$R_G = 6 \Omega$	See Figures 1 and 2			5.5			
t <sub>f</sub>	Fall time					13		ns	
trr(SD)	Source-to-drain reverse recovery time	IF = 5.3 A,	di/dt = 100 A/μs			16			



# PARAMETER MEASUREMENT INFORMATION



**Figure 1. Switching-Time Test Circuit** 

Figure 2. Switching-Time Waveforms

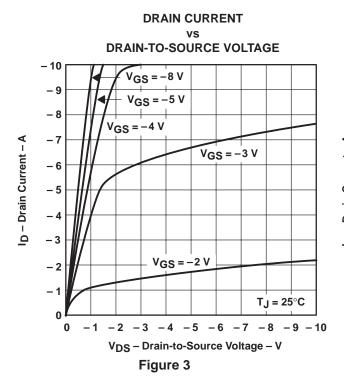
# **TYPICAL CHARACTERISTICS**

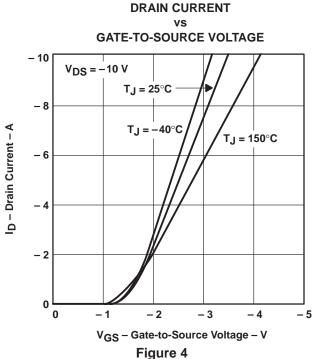
# **Table of Graphs**

		FIGURE
Drain current	vs Drain-to-source voltage	3
Drain current	vs Gate-to-source voltage	4
Static drain-to-source on-state resistance	vs Drain current	5
Capacitance	vs Drain-to-source voltage	6
Static drain-to-source on-state resistance (normalized)	vs Junction temperature	7
Source-to-drain diode current	vs Source-to-drain voltage	8
Static drain-to-source on-state resistance	vs Gate-to-source voltage	9
Gate-to-source threshold voltage	vs Junction temperature	10
Gate-to-source voltage	vs Gate charge	11

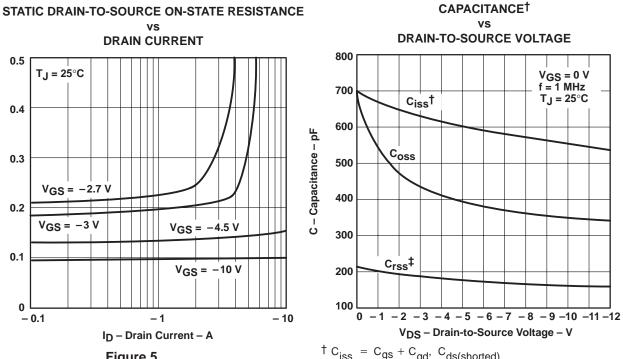


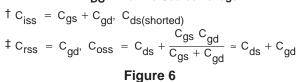
# TYPICAL CHARACTERISTICS





# **DRAIN CURRENT** 0.5 T<sub>J</sub> = 25°C <sup>r</sup> DS(on) - Static Drain-to-Source On-State 0.4 Resistance – Ω 0.3 $V_{GS} = -2.7 V$ 0.2 $V_{GS} = -4.5 V$ 0.1 $V_{GS} = -10 V$ 0 - 0.1 I<sub>D</sub> – Drain Current – A Figure 5

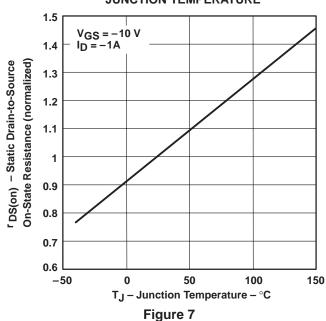




# TYPICAL CHARACTERISTICS

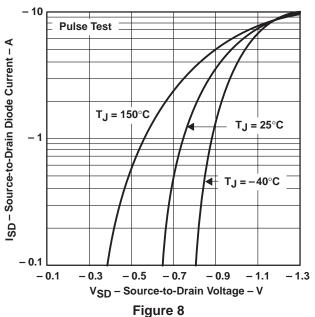
# STATIC DRAIN-TO-SOURCE ON-STATE RESISTANCE (NORMALIZED)

# JUNCTION TEMPERATURE



# SOURCE-TO-DRAIN DIODE CURRENT vs

# SOURCE-TO-DRAIN VOLTAGE



# STATIC DRAIN-TO-SOURCE ON-STATE RESISTANCE

### VS

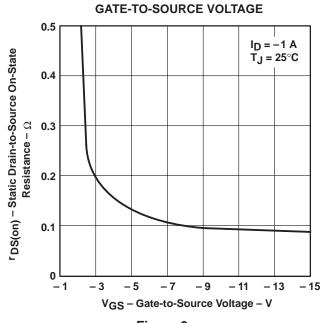


Figure 9

# GATE-TO-SOURCE THRESHOLD VOLTAGE

### VS

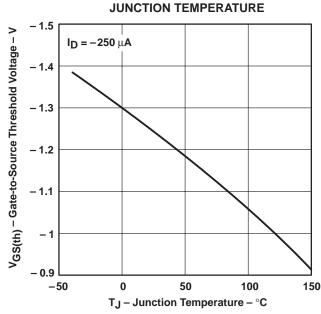


Figure 10

# TYPICAL CHARACTERISTICS

# GATE-TO-SOURCE VOLTAGE vs

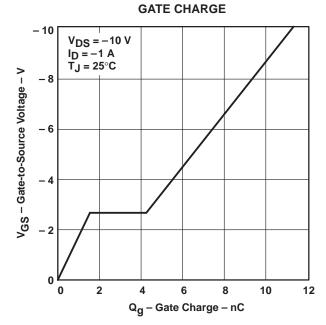


Figure 11

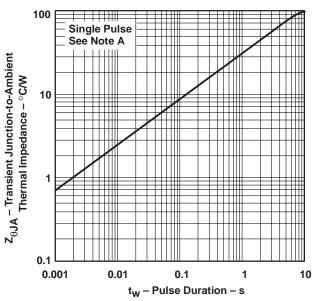
# THERMAL INFORMATION

# **DRAIN CURRENT** vs **DRAIN-TO-SOURCE VOLTAGE** - 100 Single Pulse See Note A -10 0.001 sI<sub>D</sub> – Drain Current – A 0.01 s 0.1 s1 s 10 s - 0.1 DC T<sub>J</sub> = 150°C TA = 25°C -0.01- 0.1 - 10 - 100 V<sub>DS</sub> - Drain-to-Source Voltage - V

NOTE A: Values are for the D package and are FR4-board-mounted only.

Figure 12

# TRANSIENT JUNCTION-TO-AMBIENT THERMAL IMPEDANCE vs PULSE DURATION



NOTE A: Values are for the D package and are FR4-board-mounted only.

Figure 13

# **APPLICATION INFORMATION**

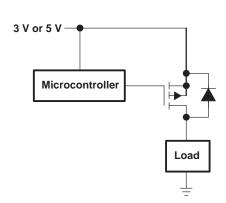


Figure 14. Notebook Load Management

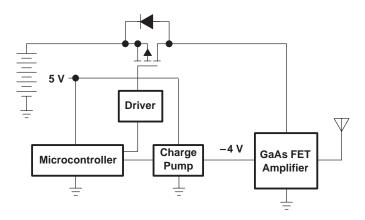


Figure 15. Cellular Phone Output Drive







i.com 6-Dec-2006

# **PACKAGING INFORMATION**

Orderable Device	Status <sup>(1)</sup>	Package Type	Package Drawing	Pins	Package Qty	e Eco Plan <sup>(2)</sup>	Lead/Ball Finish	MSL Peak Temp <sup>(3)</sup>
TPS1101D	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS1101DG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS1101DR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS1101DRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS1101PWLE	OBSOLETE	TSSOP	PW	16		TBD	Call TI	Call TI
TPS1101PWR	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS1101PWRG4	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free** (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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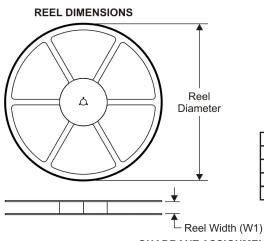
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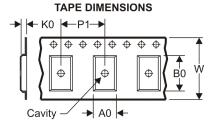




11-Mar-2008

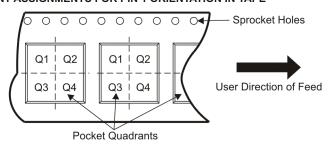
# TAPE AND REEL INFORMATION





Α0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

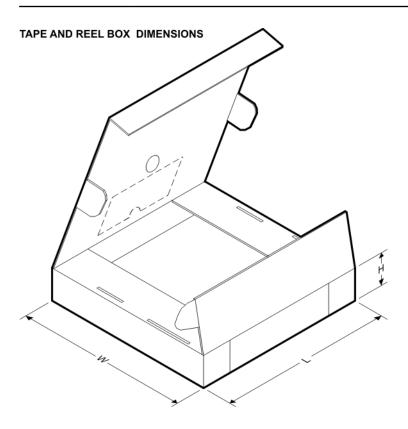


\*All dimensions are nominal

	Device	Package Type	Package Drawing			Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
	TPS1101DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
I	TPS1101PWR	TSSOP	PW	16	2000	330.0	12.4	7.0	5.6	1.6	8.0	12.0	Q1

# PACKAGE MATERIALS INFORMATION

11-Mar-2008



## \*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS1101DR	SOIC	D	8	2500	346.0	346.0	29.0
TPS1101PWR	TSSOP	PW	16	2000	346.0	346.0	29.0

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