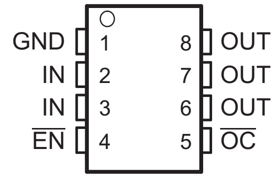
POWER-DISTRIBUTION SWITCHES

Check for Samples: TPS2020-Q1, TPS2021-Q1, TPS2022-Q1, TPS2024-Q1

FEATURES

- **Qualified for Automotive Applications**
- **33-mΩ (5-V Input) High-Side MOSFET Switch**
- **Short-Circuit and Thermal Protection**
- **Overcurrent Logic Output**
- **Operating Range: 2.7 V to 5.5 V**
- **Logic-Level Enable Input**
- **Typical Rise Time: 6.1 ms**
- **Undervoltage Lockout**
- **Maximum Standby Supply Current: 10 µA**
- **No Drain-Source Back-Gate Diode**
- **Available in 8-Pin SOIC Package**
- **Ambient Temperature Range: –40°C to 85°C**
- **ESD Protection: 2-kV Human-Body Model, 200-V Machine Model**
- **UL Listed - File No. E169910**

D PACKAGE
(TOP VIEW)



DESCRIPTION

The TPS202x family of power distribution switches is intended for applications where heavy capacitive loads and short circuits are likely to be encountered. These devices are 50-mΩ N-channel MOSFET high-side power switches. The switch is controlled by a logic enable compatible with 5-V logic and 3-V logic. Gate drive is provided by an internal charge pump designed to control the power-switch rise times and fall times to minimize current surges during switching. The charge pump requires no external components and allows operation from supplies as low as 2.7 V.

When the output load exceeds the current-limit threshold or a short is present, the TPS202x limits the output current to a safe level by switching into a constant-current mode, pulling the overcurrent (OC) logic output low. When continuous heavy overloads and short circuits increase the power dissipation in the switch, causing the junction temperature to rise, a thermal protection circuit shuts off the switch to prevent damage. Recovery from a thermal shutdown is automatic once the device has cooled sufficiently. Internal circuitry ensures the switch remains off until valid input voltage is present.

The TPS202x devices differ only in short-circuit current threshold. The TPS2020 limits at 0.3-A load, the TPS2021 at 0.9-A load, the TPS2022 at 1.5-A load, and the TPS2024 at 3-A load. The TPS202x is available in an 8-pin small-outline integrated-circuit (SOIC) package and operates over a junction temperature range of –40°C to 125°C.

GENERAL SWITCH CATALOG

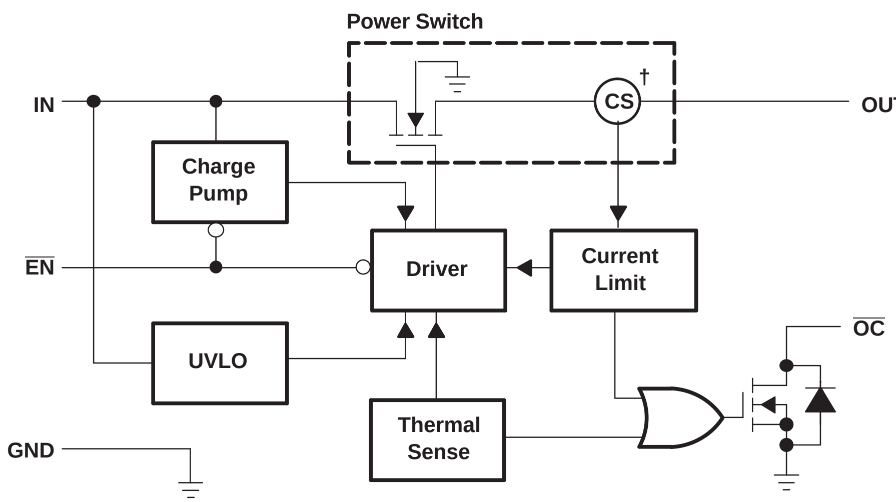
33 mΩ, Single	80 mΩ, Single	80 mΩ, Dual	80 mΩ, Dual	80 mΩ, Triple	80 mΩ, Quad	80 mΩ, Quad
TPS201xA 0.2 A to 2 A TPS202x 0.2 A to 2 A TPS203x 0.2 A to 2 A	TPS2014 600 mA TPS2015 1 A TPS2041B 500 mA TPS2051B 500 mA TPS2045A 250 mA TPS2049 100 mA TPS2055A 250 mA TPS2061 1 A TPS2065 1 A TPS2068 1.5 A TPS2069 1.5 A	TPS2042B 500 mA TPS2052B 500 mA TPS2046B 250 mA TPS2056 250 mA TPS2062 1 A TPS2066 1 A TPS2060 1.5 A TPS2064 1.5 A	TPS2080 500 mA TPS2081 500 mA TPS2082 500 mA TPS2090 250 mA TPS2091 250 mA TPS2092 250 mA	TPS2043B 500 mA TPS2053B 500 mA TPS2047B 250 mA TPS2057A 250 mA TPS2063 1 A TPS2067 1 A	TPS2044B 500 mA TPS2054B 500 mA TPS2048A 250 mA TPS2058 250 mA	TPS2085 500 mA TPS2086 500 mA TPS2087 500 mA TPS2095 250 mA TPS2096 250 mA TPS2097 250 mA

ORDERING INFORMATION(1)

T_A	ENABLE	RECOMMENDED MAXIMUM CONTINUOUS LOAD CURRENT (A)	TYPICAL SHORT-CIRCUIT CURRENT LIMIT AT 25°C (A)	PACKAGED DEVICES(2) SMALL OUTLINE (D)
–40°C to 85°C	Active low	0.2	0.3	TPS2020IDRQ1
		0.6	0.9	TPS2021IDRQ1
		1	1.5	TPS2022DRQ1
		2	3	TPS2024IDRQ1

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.
(2) Package drawings, thermal data, and symbolization are available at www.ti.com/packaging.

FUNCTIONAL BLOCK DIAGRAM



†Current Sense

TERMINAL FUNCTIONS

TERMINAL		I/O	DESCRIPTION
NAME	NO.		
$\overline{EN}$	4	I	Enable input. Logic-low turns on power switch.
GND	1	I	Ground
IN	2, 3	I	Input voltage
$\overline{OC}$	5	O	Overcurrent. Logic output, active-low
OUT	6, 7, 8	O	Power-switch output

DETAILED DESCRIPTION

Power Switch

The power switch is an N-channel MOSFET with a maximum on-state resistance of 50 mΩ ($V_{I(IN)}$ = 5 V). Configured as a high-side switch, the power switch prevents current flow from OUT to IN and IN to OUT when disabled.

Charge Pump

An internal charge pump supplies power to the driver circuit and provides the necessary voltage to pull the gate of the MOSFET above the source. The charge pump operates from input voltages as low as 2.7 V and requires very little supply current.

Driver

The driver controls the gate voltage of the power switch. To limit large current surges and reduce the associated electromagnetic interference (EMI) produced, the driver incorporates circuitry that controls the rise times and fall times of the output voltage. The rise and fall times are typically in the 2-ms to 9-ms range.

Enable ($\overline{EN}$)

The logic enable disables the power switch, the bias for the charge pump, driver, and other circuitry to reduce the supply current to less than 10 μA when a logic-high is present on $\overline{EN}$. A logic-zero input on $\overline{EN}$ restores bias to the drive and control circuits and turns the power on. The enable input is compatible with both TTL and CMOS logic levels.

Overcurrent ($\overline{OC}$)

The $\overline{OC}$ open drain output is asserted (active low) when an overcurrent or overtemperature condition is encountered. The output remains asserted until the overcurrent or overtemperature condition is removed.

Current Sense

A sense FET monitors the current supplied to the load. The sense FET measures current more efficiently than conventional resistance methods. When an overload or short circuit is encountered, the current-sense circuitry sends a control signal to the driver. The driver, in turn, reduces the gate voltage and drives the power FET into its saturation region, which switches the output into a constant-current mode and holds the current constant while varying the voltage on the load.

Thermal Sense

An internal thermal-sense circuit shuts off the power switch when the junction temperature rises to approximately 140°C. Hysteresis is built into the thermal sense circuit. After the device has cooled approximately 20°C, the switch turns back on. The switch continues to cycle off and on until the fault is removed.

Undervoltage Lockout

A voltage sense circuit monitors the input voltage. When the input voltage is below approximately 2 V, a control signal turns off the power switch.

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted)[1]

$V_{I(IN)}$ [2]	Input voltage range		–0.3 V to 6 V
$V_{O(OUT)}$ [2]	Output voltage range		–0.3 V to $V_{I(IN)}$ + 0.3 V
$V_{I(EN)}$	Input voltage range		–0.3 V to 6 V
$I_{O(OUT)}$	Continuous output current		Internally limited
	Continuous total power dissipation		See Dissipation Rating Table
T_J	Operating virtual junction temperature range		–40°C to 125°C
T_{stg}	Storage temperature range		–65°C to 150°C
ESD	Electrostatic discharge protection	Human body model	2 kV
		Machine model	200 V
		Charged device model (CDM)	750 V

(1) Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under recommended operating conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltages are with respect to GND.

DISSIPATION RATINGS

PACKAGE	$T_A \leq 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING
D	725 mW	5.8 mW/°C	464 mW	377 mW

RECOMMENDED OPERATING CONDITIONS

			MIN	MAX	UNIT
$V_{I(IN)}$	Input voltage		2.7	5.5	V
$V_{I(\overline{EN})}$			0	5.5	V
I_O	Continuous output current	TPS2020	0	0.2	A
		TPS2021	0	0.6	
		TPS2022	0	1	
		TPS2024	0	2	
T_J	Operating virtual junction temperature		–40	125	°C

ELECTRICAL CHARACTERISTICS

over recommended operating junction temperature range, $V_{I(IN)}$ = 5.5 V, I_O = rated current, $\overline{EN}$ = 0 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS[1]		T_J[2]	MIN	TYP	MAX	UNIT
Power Switch								
$r_{DS(on)}$	Static drain-source on-state resistance	$V_{I(IN)}$ = 5 V, I_O = 1.8 A		25°C		33	43.5	mΩ
				85°C		38	57.5	
				125°C		44	62.5	
		$V_{I(IN)}$ = 3.3 V, I_O = 1.8 A		25°C		37	48.5	
				85°C		43	68.5	
				125°C		51	87	
		$V_{I(IN)}$ = 5 V, I_O = 1 A		25°C		30	43.5	
				125°C		43	62.5	
		$V_{I(IN)}$ = 3.3 V, I_O = 1 A		25°C		31	48.5	
				125°C		48	87	
		$V_{I(IN)}$ = 5 V, I_O = 0.18 A		25°C		30	34	
				85°C		35	41	
				125°C		39	47	
		$V_{I(IN)}$ = 3.3 V, I_O = 0.18 A		25°C		33	37	
				85°C		39	46	
				125°C		44	56	
		$V_{I(IN)}$ = 5 V, I_O = 0.6 A	TPS2021	25°C		33	36	
				125°C		44	48	
		$V_{I(IN)}$ = 3.3 V, I_O = 0.6 A	TPS2021	25°C		37	40	
				125°C		51	59	
t_r	Rise time, output	$V_{I(IN)}$ = 5.5 V, C_L = 1 μF, R_L = 10 Ω		25°C		6.1		ms
		$V_{I(IN)}$ = 2.7 V, C_L = 1 μF, R_L = 10 Ω				8.6		
t_f	Fall time, output	$V_{I(IN)}$ = 5.5 V, C_L = 1 μF, R_L = 10 Ω		25°C		3.4		ms
		$V_{I(IN)}$ = 2.7 V, C_L = 1 μF, R_L = 10 Ω				3		
Enable Input ($\overline{EN}$)								
V_{IH}	High-level input voltage	2.7 V ≤ $V_{I(IN)}$ ≤ 5.5 V		Full range	2			V
V_{IL}	Low-level input voltage	4.5 V ≤ $V_{I(IN)}$ ≤ 5.5 V		Full range			0.8	V
		2.7 V ≤ $V_{I(IN)}$ ≤ 4.5 V		Full range			0.5	
I_I	Input current	$\overline{EN}$ = 0 V or $\overline{EN}$ = $V_{I(IN)}$		Full range	–0.5		0.5	μA
t_{on}	Turnon time	C_L = 100 μF, R_L= 10 Ω		Full range			20	ms
t_{off}	Turnoff time	C_L = 100 μF, R_L= 10 Ω		Full range			40	
Current Limit								
I_{OS}	Short-circuit output current	V_I = 5.5 V, OUT connected to GND, Device enabled into short circuit	TPS2020	25°C	0.22	0.3	0.4	A
			TPS2021		0.66	0.9	1.1	
			TPS2022		1.1	1.5	1.8	
			TPS2024		2	3	4.2	

(1) Pulse-testing techniques maintain junction temperature close to ambient temperature; thermal effects must be taken into account separately.
(2) Full range T_J = -40°C to 125°C

ELECTRICAL CHARACTERISTICS (continued)

over recommended operating junction temperature range, $V_{I(IN)}$ = 5.5 V, I_O = rated current, $\overline{EN}$ = 0 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS[1]	T_J[2]	MIN	TYP	MAX	UNIT
Supply Current							
	Supply current, low-level output	No load on OUT, $\overline{EN}$ = $V_{I(IN)}$	25°C		0.3	1	µA
			Full range			10	
	Supply current, high-level output	No load on OUT, $\overline{EN}$ = 0 V	25°C		58	75	µA
			Full range		75	100	
	Leakage current	OUT connected to ground, $\overline{EN}$ = $V_{I(IN)}$	Full range		10		µA
Undervoltage Lockout							
Low-level input voltage			Full range	2		2.5	V
Hysteresis			25°C		100		mV
Overcurrent ($\overline{OC}$)							
Output low voltage		I_O = 10 mA, $V_{OL(\overline{OC})}$	Full range			0.4	V
Off-state current[3]		V_O = 5 V, V_O = 3.3 V	Full range			1	µA

(3) Specified by design.

PARAMETER MEASURMENT INFORMATION

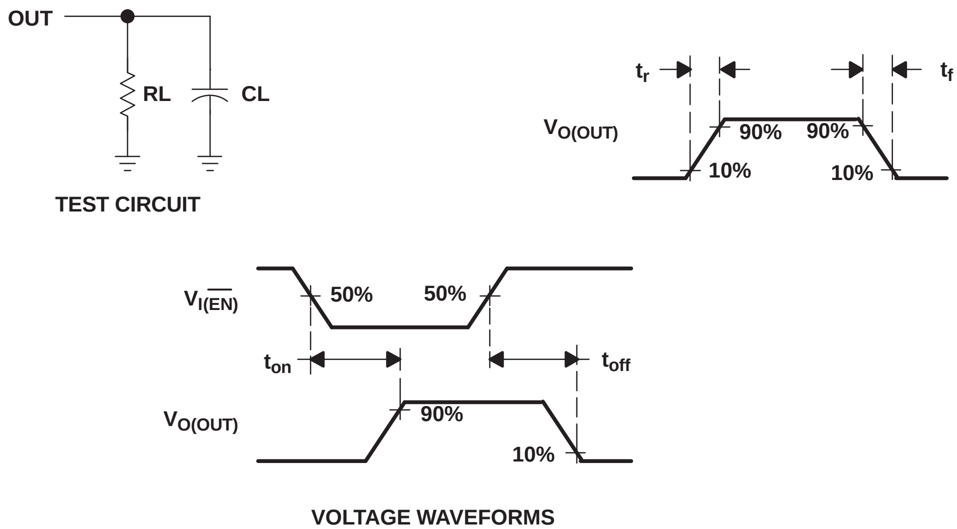


Figure 1. Test Circuit and Voltage Waveforms

Table 1. Timing Diagrams

	FIGURE
Turnon Delay and Rise TIme	2
Turnoff Delay and Fall Time	3
Turnon Delay and Rise TIme with 1-µF Load	4
Turnoff Delay and Rise TIme with 1-µF Load	5
Device Enabled into Short	6
TPS2020 Ramped Load on Enabled Device	7
TPS2021 Ramped Load on Enabled Device	8
TPS2022 Ramped Load on Enabled Device	9
TPS2024 Ramped Load on Enabled Device	10
TPS2024, Inrush Current	11
7.9-Ω Load Connected to an Enabled TPS2020 Device	12
3.7-Ω Load Connected to an Enabled TPS2020 Device	13
3.7-Ω Load Connected to an Enabled TPS2021 Device	14
2.6-Ω Load Connected to an Enabled TPS2021 Device	15
2.6-Ω Load Connected to an Enabled TPS2022 Device	16
1.2-Ω Load Connected to an Enabled TPS2022 Device	17
0.9-Ω Load Connected to an Enabled TPS2024 Device	18
0.5-Ω Load Connected to an Enabled TPS2024 Device	19

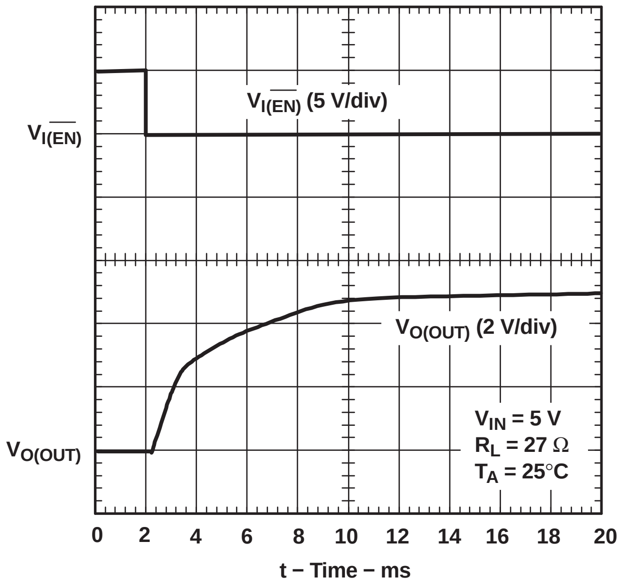


Figure 2. Turnon Delay and Rise Time

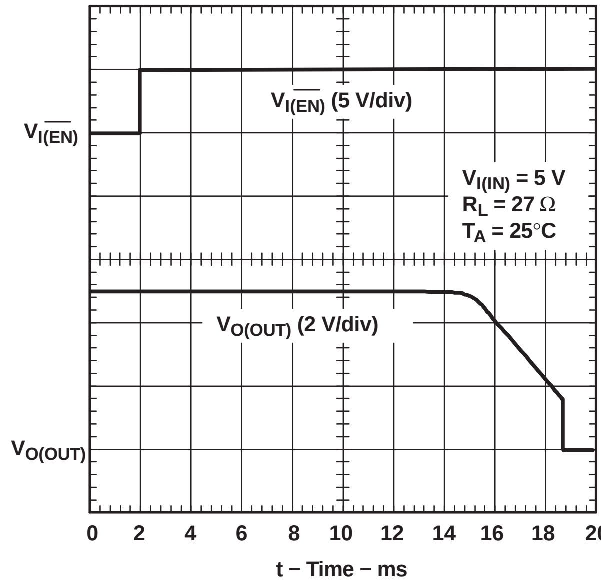


Figure 3. Turnoff Delay and Fall Time

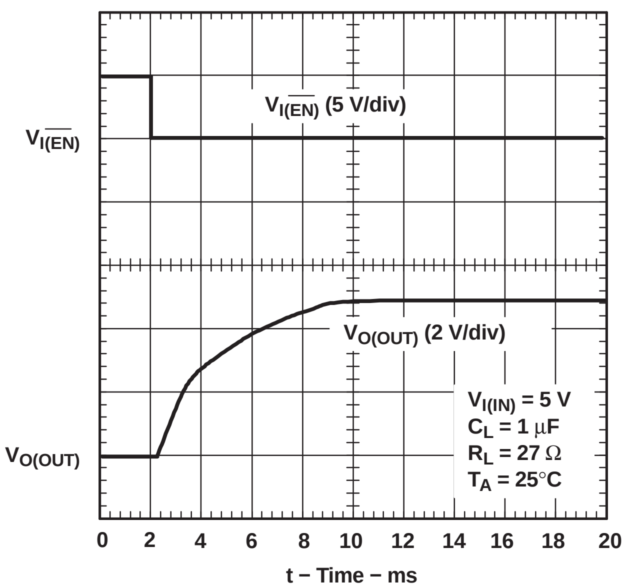


Figure 4. Turnon Delay and Rise Time with 1-μF Load

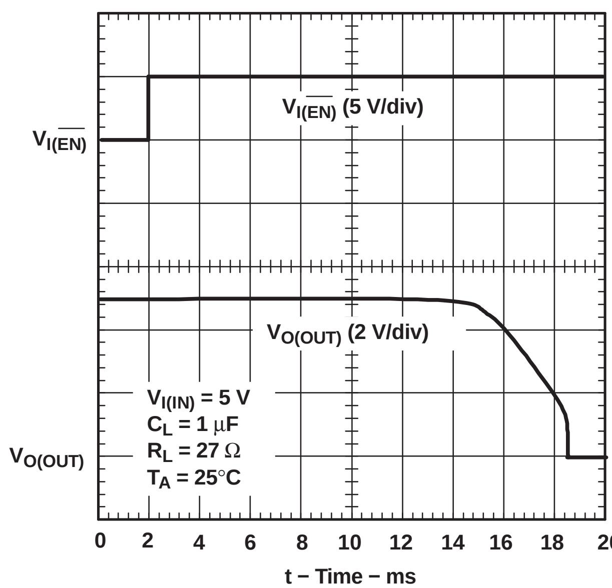


Figure 5. Turnoff Delay and Fall Time with 1-μF Load

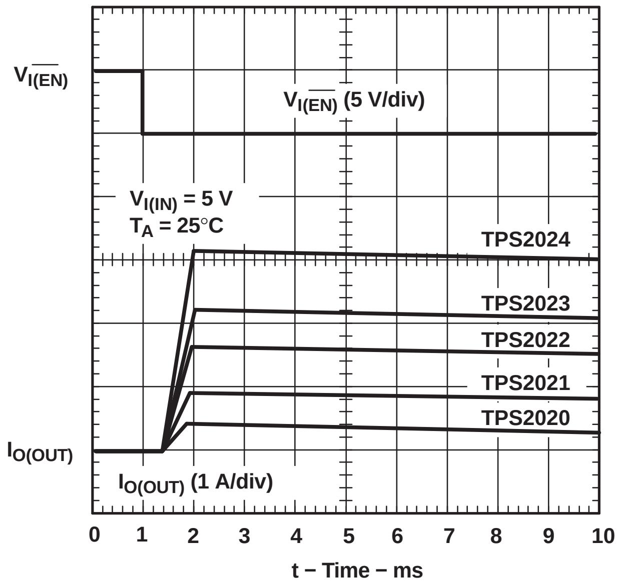


Figure 6. Device Enabled Into Short

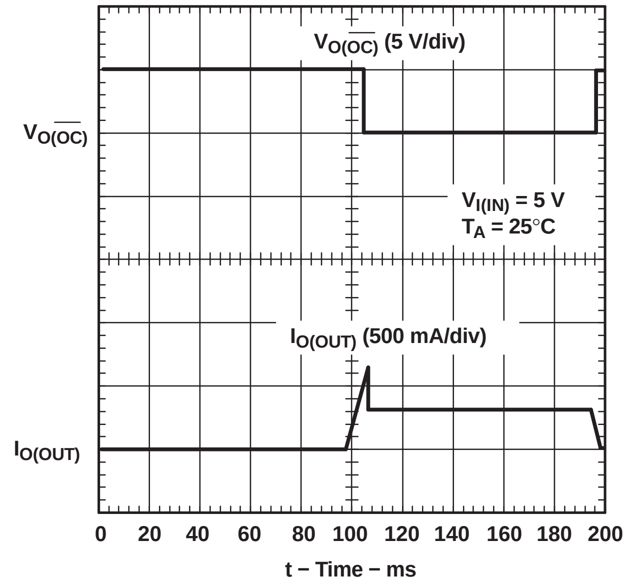


Figure 7. TPS2020, Ramped Load on Enabled Device

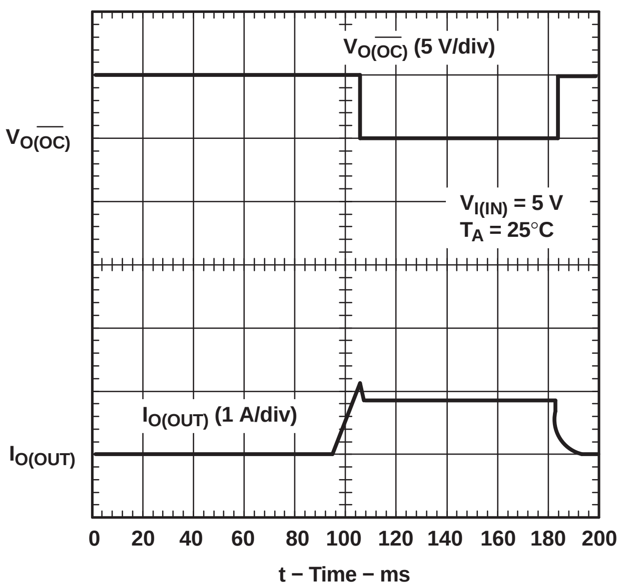


Figure 8. TPS2021, Ramped Load on Enabled Device

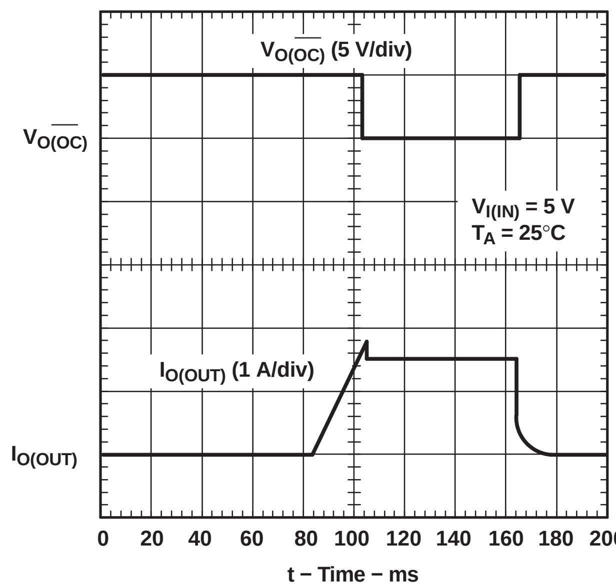


Figure 9. TPS2022, Ramped Load on Enabled Device

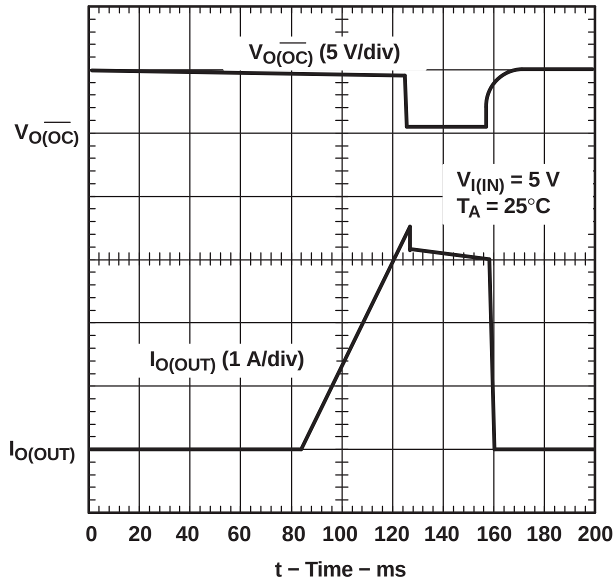


Figure 10. TPS2024, Ramped Load on Enabled Device

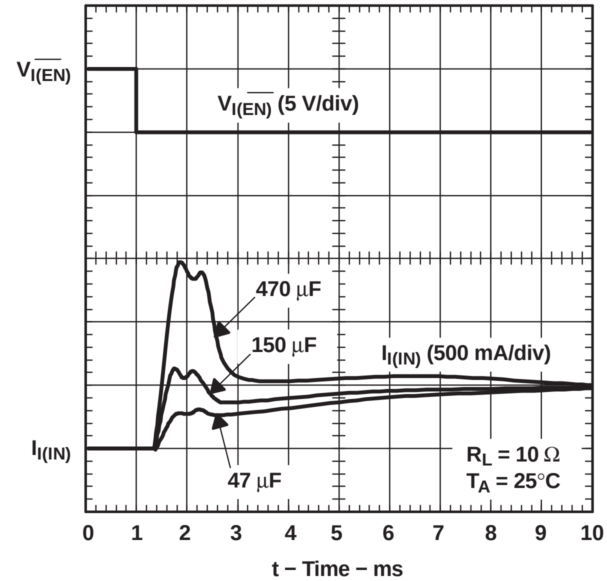


Figure 11. TPS2024, Inrush Current

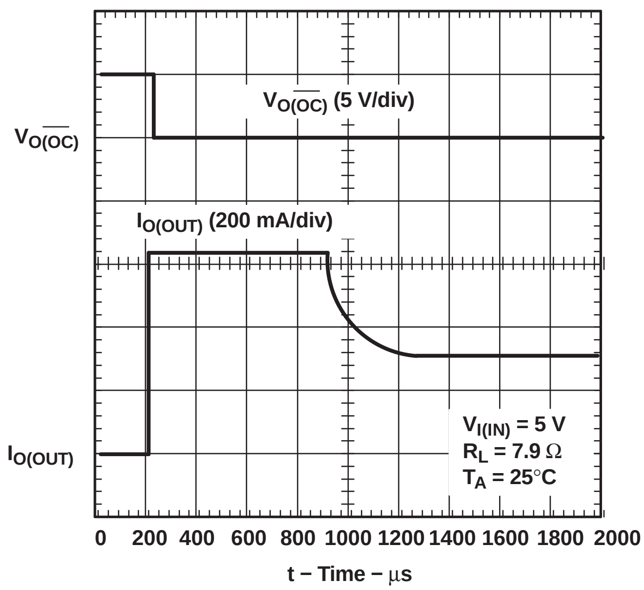


Figure 12. 7.9-Ω Load Connected to an Enabled TPS2020 Device

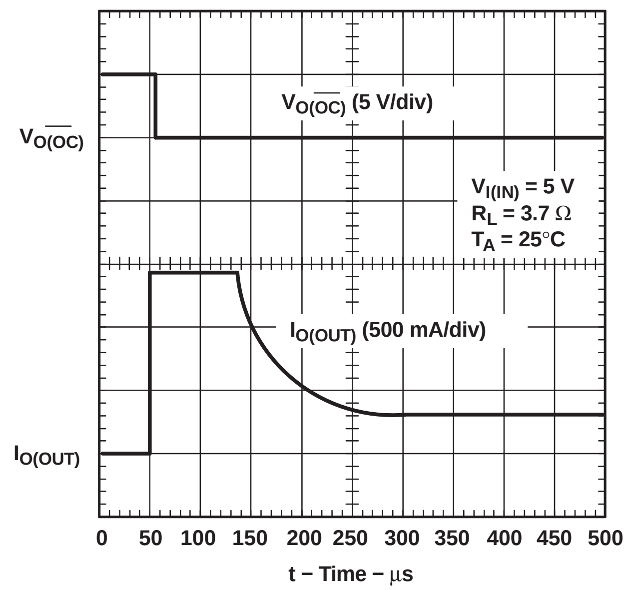


Figure 13. 3.7-Ω Load Connected to an Enabled TPS2020 Device

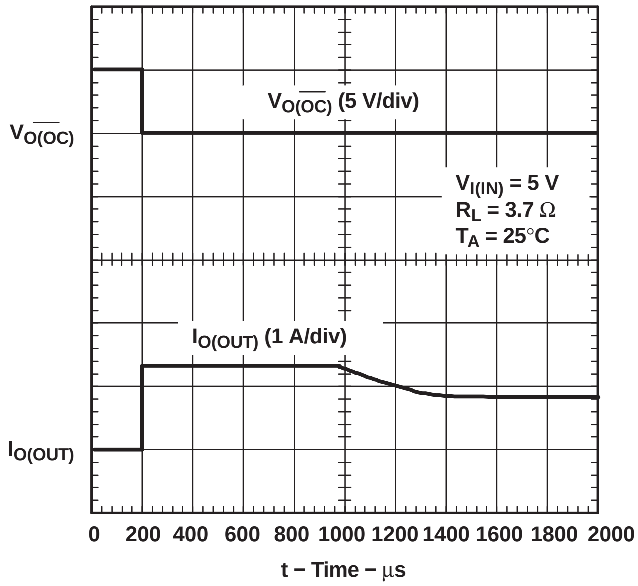


Figure 14. 3.7-Ω Load Connected to an Enabled TPS2021 Device

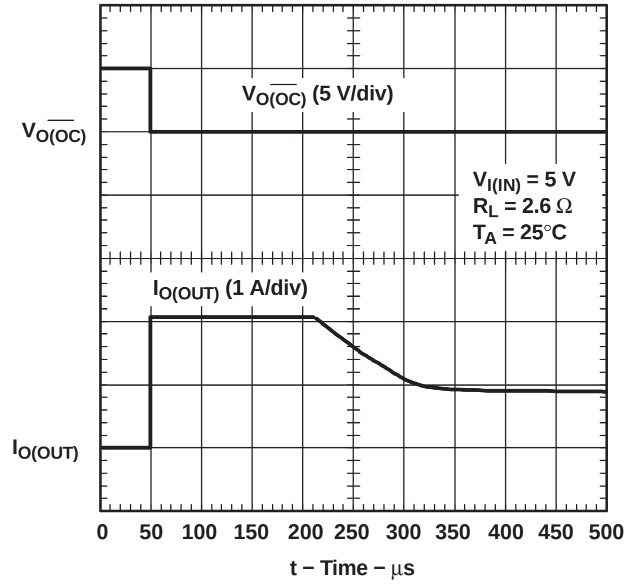


Figure 15. 2.6-Ω Load Connected to an Enabled TPS2021 Device

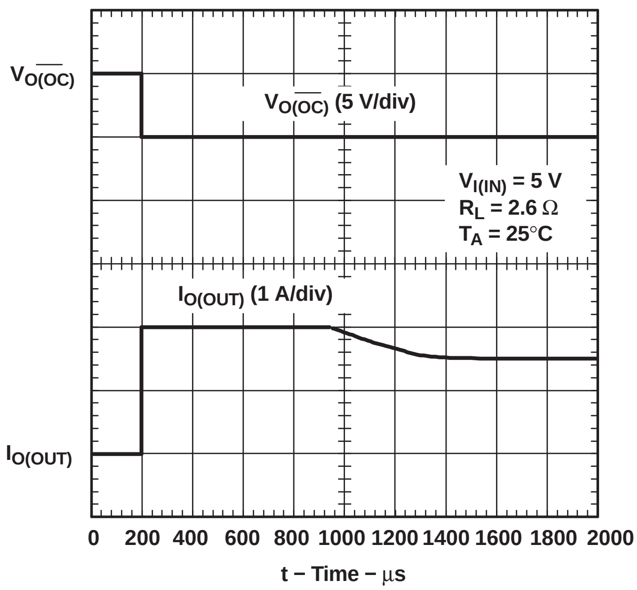


Figure 16. 2.6-Ω Load Connected to an Enabled TPS2022 Device

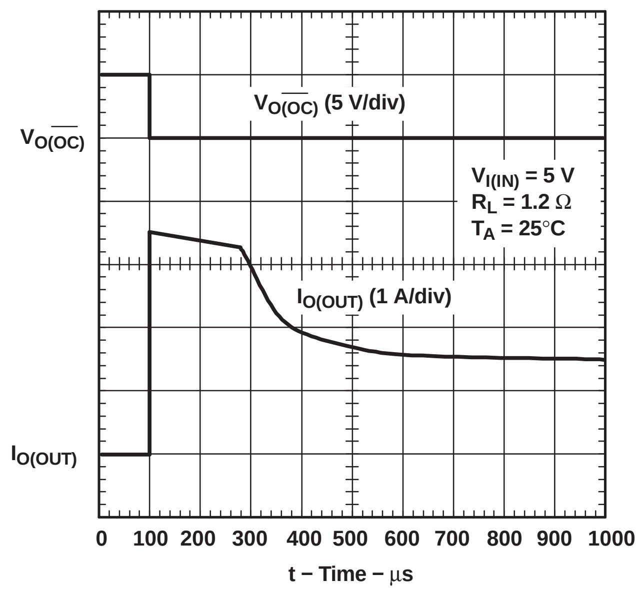


Figure 17. 1.2-Ω Load Connected to an Enabled TPS2022 Device

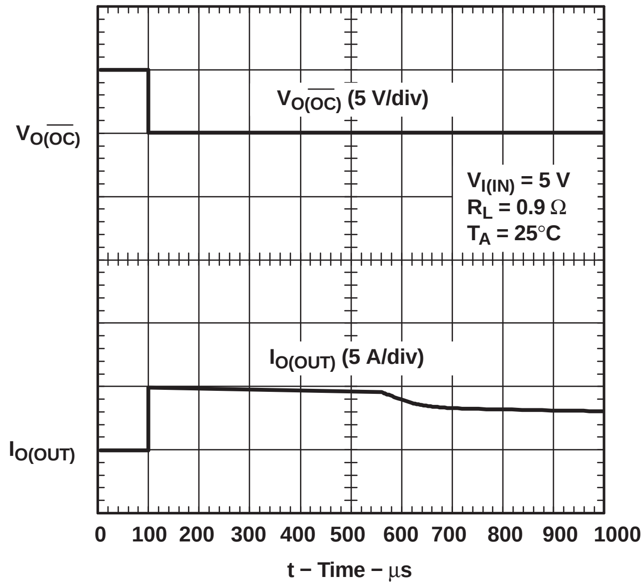


Figure 18. 0.9-Ω Load Connected to an Enabled TPS2024 Device

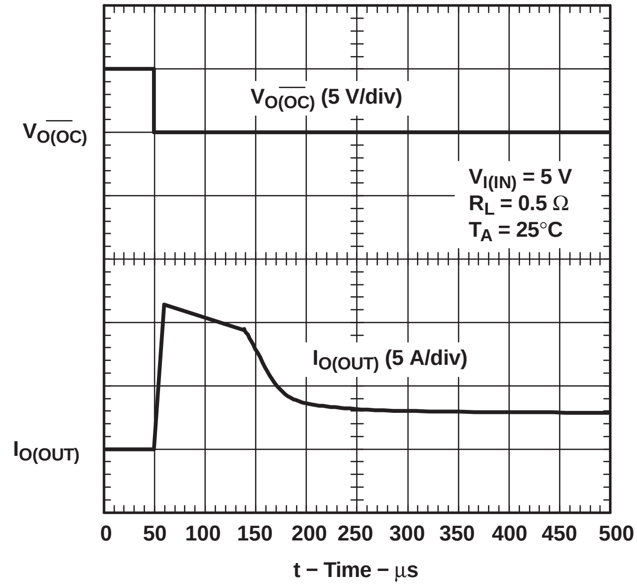


Figure 19. 0.5-Ω Load Connected to an Enabled TPS2024 Device

TYPICAL CHARACTERISTICS

Table 2. Typical Characteristics Graphs

			FIGURE
$t_{d(on)}$	Turnon delay time	vs Output voltage	23
$t_{d(off)}$	Turnoff delay time	vs Input voltage	24
t_r	Rise time	vs Load current	25
t_f	Fall time	vs Load current	26
	Supply current (enabled)	vs Junction temperature	27
	Supply current (disabled)	vs Junction temperature	28
	Supply current (enabled)	vs Input voltage	29
	Supply current (disabled)	vs Input voltage	30
I_{OS}	Short-circuit current limit	vs Input voltage	31
		vs Junction temperature	32
$r_{DS(on)}$	Static drain-source on-state resistance	vs Input voltage	33
		vs Junction temperature	34
		vs Input voltage	35
		vs Junction temperature	36
V_I	Input voltage	Undervoltage lockout	37

TURNON DELAY TIME
vs
OUTPUT VOLTAGE

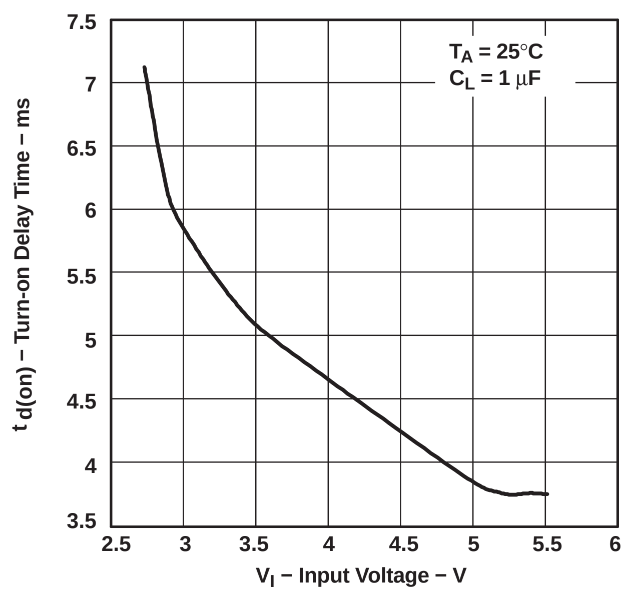


Figure 20.

TURNOFF DELAY TIME
vs
INPUT VOLTAGE

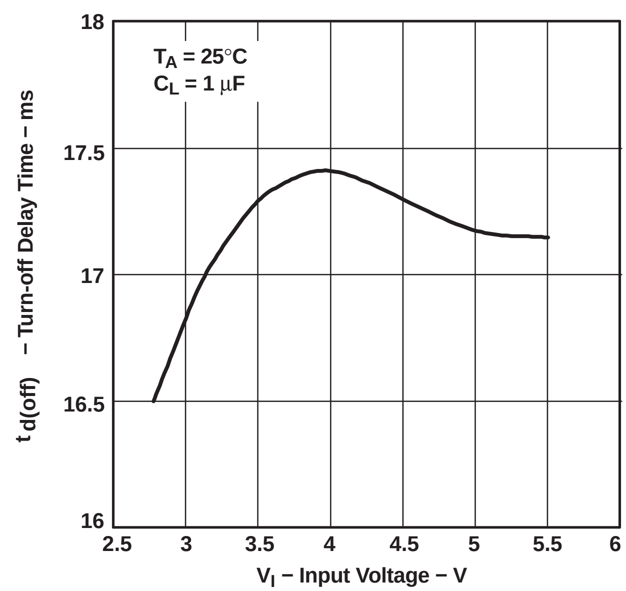


Figure 21.

RISE TIME vs LOAD CURRENT

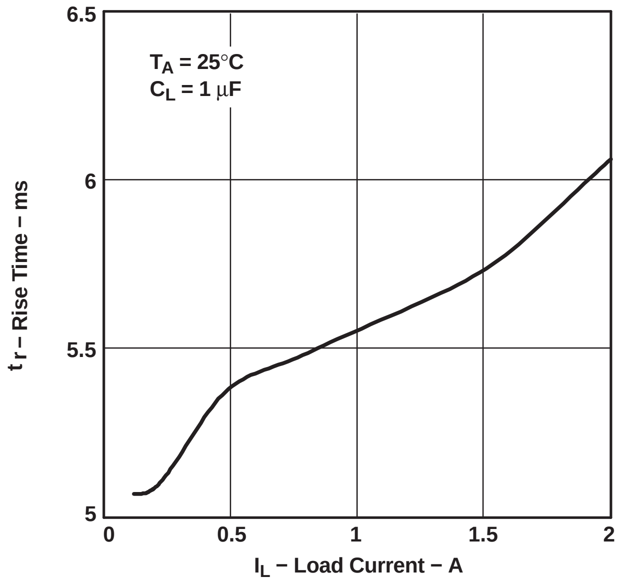


Figure 22.

FALL TIME vs LOAD CURRENT

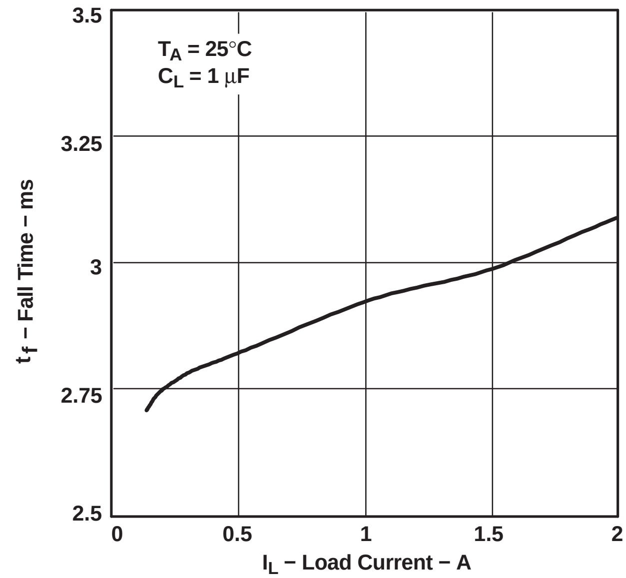


Figure 23.

SUPPLY CURRENT (ENABLED) vs JUNCTION TEMPERATURE

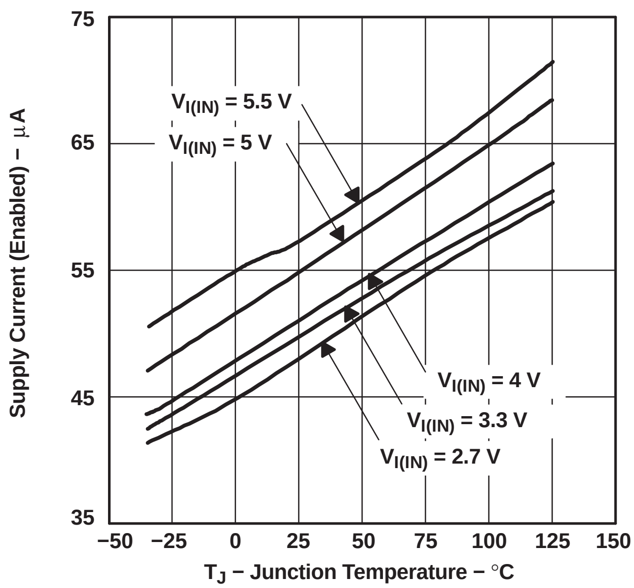


Figure 24.

SUPPLY CURRENT (DISABLED) vs JUNCTION TEMPERATURE

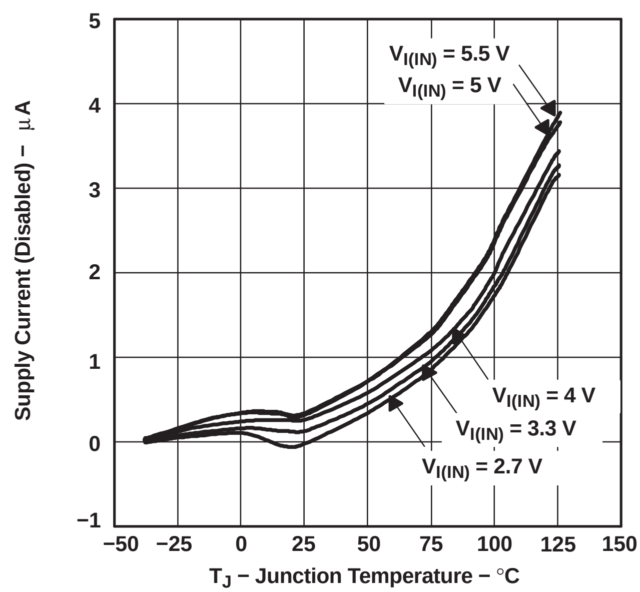


Figure 25.

SUPPLY CURRENT (ENABLED)
vs
INPUT VOLTAGE

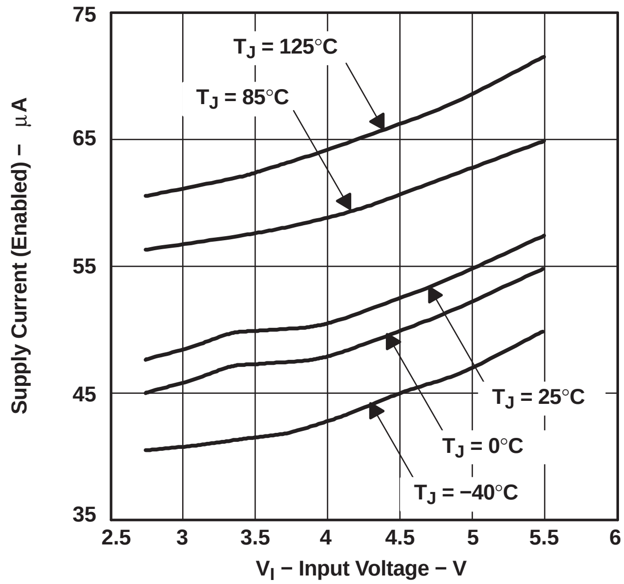


Figure 26.

SUPPLY CURRENT (DISABLED)
vs
INPUT VOLTAGE

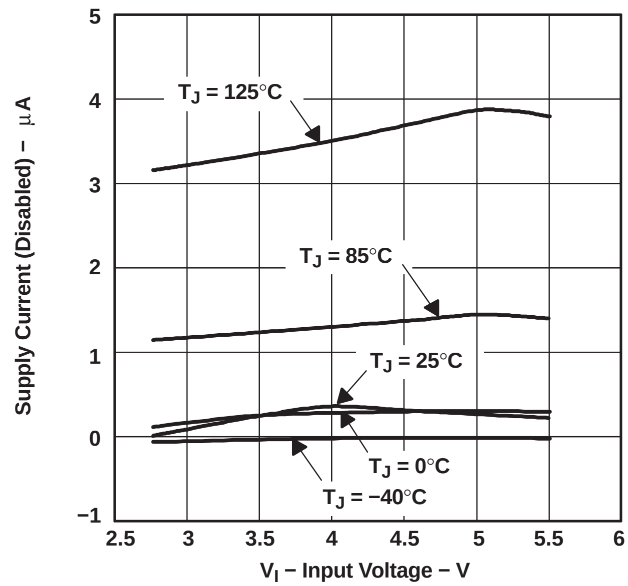


Figure 27.

SHORT-CIRCUIT CURRENT LIMIT
vs
INPUT VOLTAGE

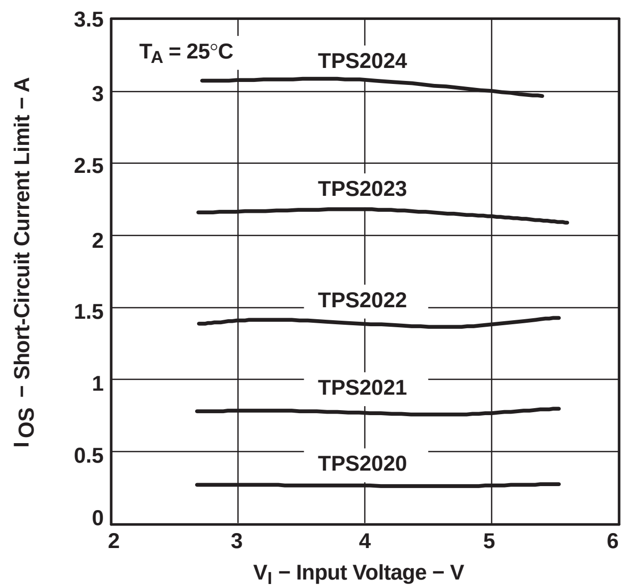


Figure 28.

SHORT-CIRCUIT CURRENT LIMIT
vs
JUNCTION TEMPERATURE

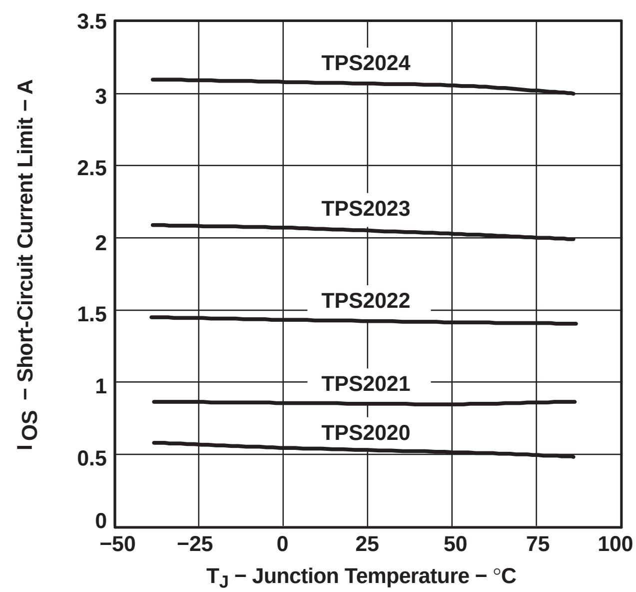


Figure 29.

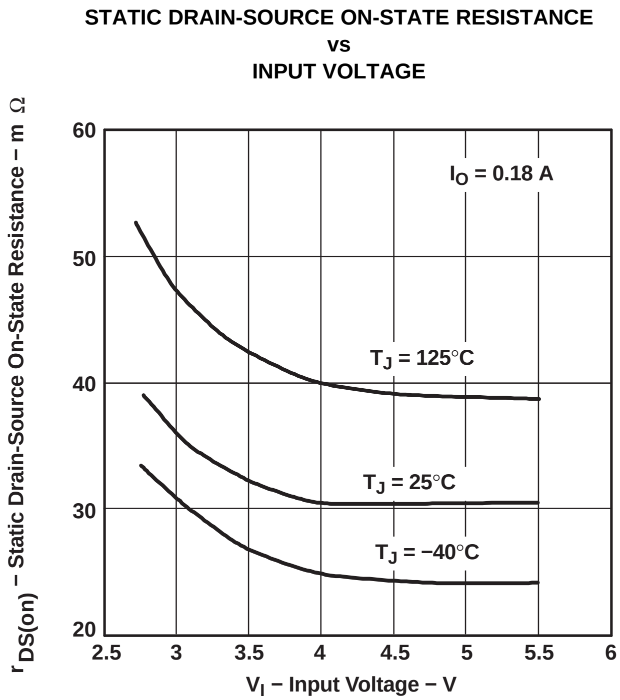


Figure 30.

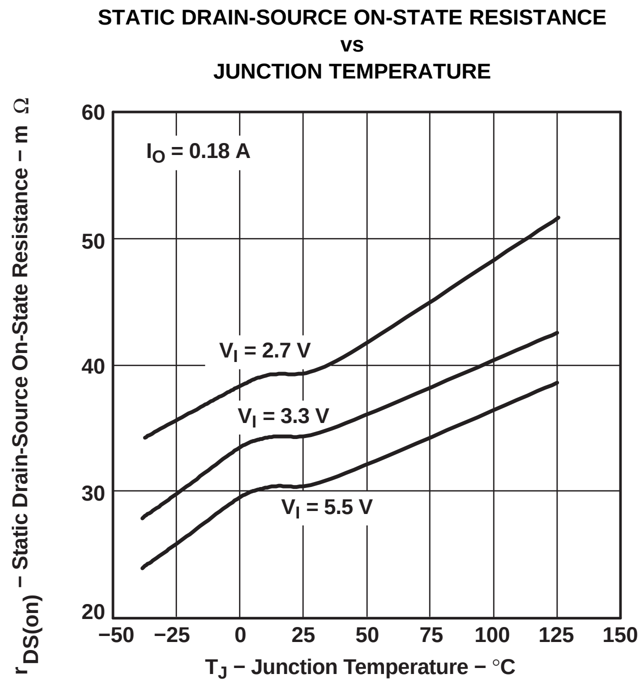


Figure 31.

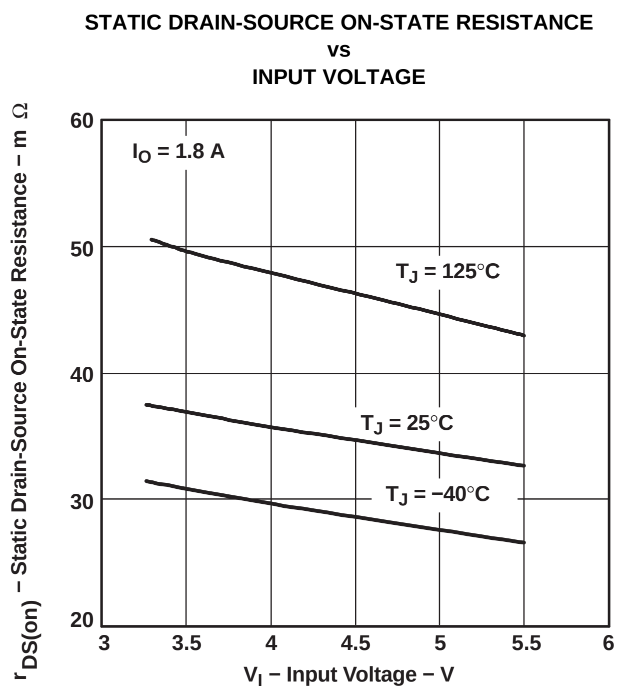


Figure 32.

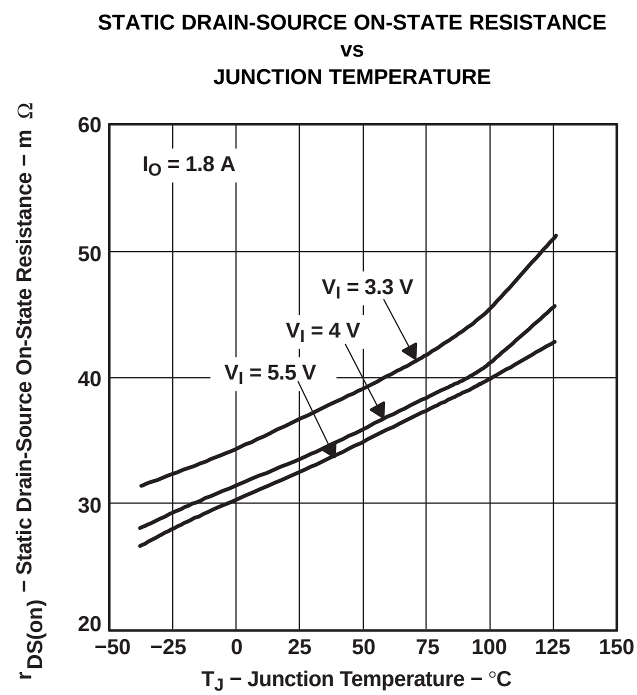


Figure 33.

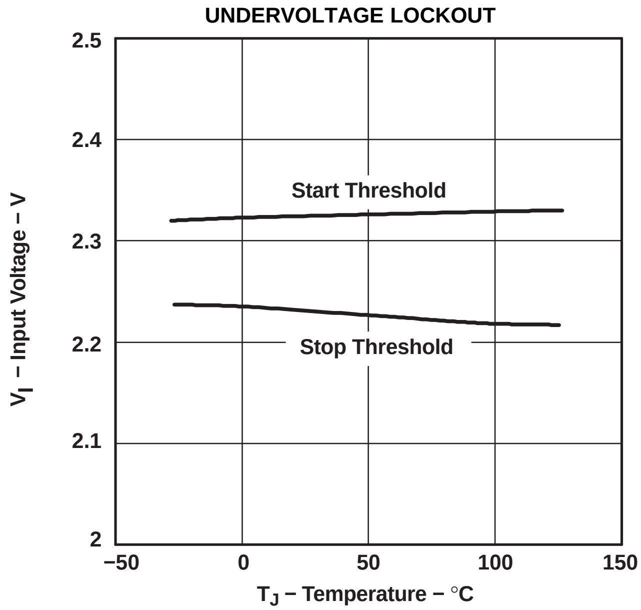

UNDERVOLTAGE LOCKOUT
2.5
2.4
2.3
2.2
2.1
2
−50
0
50
100
150
Start Threshold
Stop Threshold
VI − Input Voltage − V
TJ − Temperature − °C

Figure 34.

APPLICATION INFORMATION

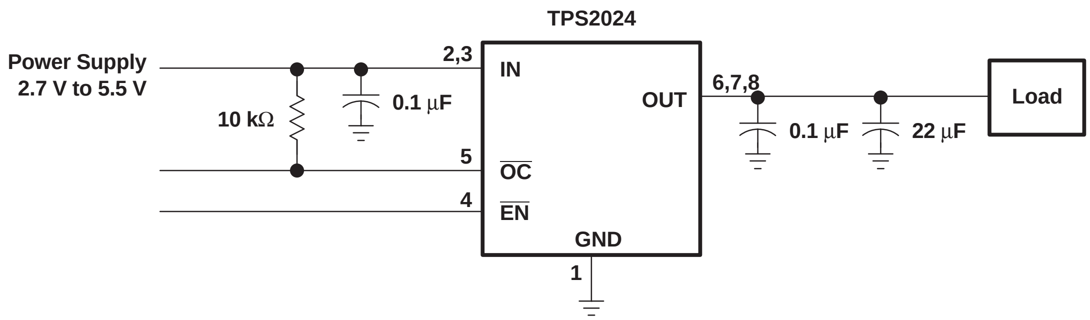


Figure 35. Typical Application

Power Supply Considerations

A 0.01-µF to 0.1-µF ceramic bypass capacitor between IN and GND, close to the device, is recommended. Placing a high-value electrolytic capacitor on the output and input pins is recommended when the output load is heavy. This precaution reduces power supply transients that may cause ringing on the input. Additionally, bypassing the output with a 0.01-µF to 0.1-µF ceramic capacitor improves the immunity of the device to short-circuit transients.

Overcurrent

A sense FET checks for overcurrent conditions. Unlike current-sense resistors, sense FETs do not increase the series resistance of the current path. When an overcurrent condition is detected, the device maintains a constant output current and reduces the output voltage accordingly. Complete shutdown occurs only if the fault is present long enough to activate thermal limiting.

Three possible overload conditions can occur. In the first condition, the output has been shorted before the device is enabled or before $V_{I(IN)}$ has been applied, see Figure 6. The TPS202x senses the short and immediately switches into a constant-current output.

In the second condition, the excessive load occurs while the device is enabled. At the instant the excessive load occurs, very high currents may flow for a short time before the current-limit circuit can react (see Figures 13–22). After the current-limit circuit has tripped (reached the overcurrent trip threshhold) the device switches into constant-current mode.

In the third condition, the load has been gradually increased beyond the recommended operating current. The current is permitted to rise until the current-limit threshold is reached or until the thermal limit of the device is exceeded (see Figures 7–11). The TPS202x is capable of delivering current up to the current-limit threshold without damaging the device. Once the threshold has been reached, the device switches into its constant-current mode.

$\overline{\text{OC}}$ Response

The $\overline{\text{OC}}$ open-drain output is asserted (active low) when an overcurrent or overtemperature condition is encountered. The output remains asserted until the overcurrent or overtemperature condition is removed. Connecting a heavy capacitive load to an enabled device can cause momentary false overcurrent reporting from the inrush current flowing through the device, charging the downstream capacitor. An RC filter can be connected to the $\overline{\text{OC}}$ pin to reduce false overcurrent reporting. Using low-ESR electrolytic capacitors on the output lowers the inrush current flow through the device during hot-plug events by providing a low impedance energy source, thereby reducing erroneous overcurrent reporting.

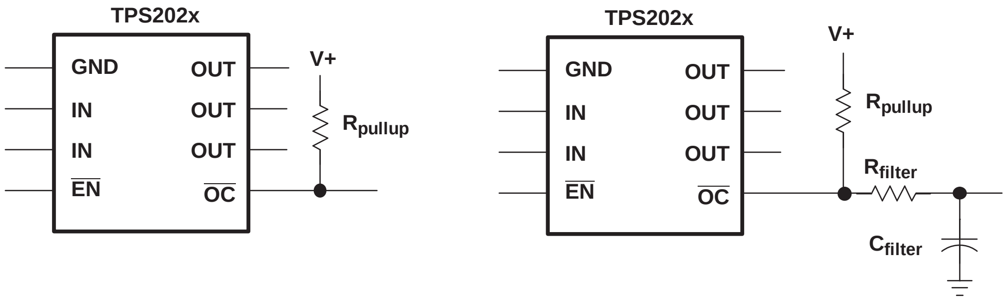


Figure 36. Typical Circuit for $\overline{OC}$ Pin and RC Filter for Damping Inrush $\overline{OC}$ Responses

Power Dissipation and Junction Temperature

The low on-resistance on the n-channel MOSFET allows small surface-mount packages, such as SOIC, to pass large currents. The thermal resistances of these packages are high compared to those of power packages; it is good design practice to check power dissipation and junction temperature. The first step is to find $r_{DS(on)}$ at the input voltage and operating temperature. As an initial estimate, use the highest operating ambient temperature of interest and read $r_{DS(on)}$ from Figures 33–36. Next, calculate the power dissipation using:

$$P_D = r_{DS(on)} \times I^2 \tag{1}$$

Finally, calculate the junction temperature:

$$T_J = P_D \times R_{\theta JA} + T_A \tag{2}$$

where:

T_A = Ambient temperature °C

$R_{\theta JA}$ = Thermal resistance—SOIC = 172°C/W, PDIP = 106°C/W

Compare the calculated junction temperature with the initial estimate. If they do not agree within a few degrees, repeat the calculation, using the calculated value as the new estimate. Two or three iterations are generally sufficient to get an acceptable answer.

Thermal Protection

Thermal protection prevents damage to the IC when heavy-overload or short-circuit faults are present for extended periods of time. The faults force the TPS202x into constant current mode, which causes the voltage across the high-side switch to increase; under short-circuit conditions, the voltage across the switch is equal to the input voltage. The increased dissipation causes the junction temperature to rise to high levels. The protection circuit senses the junction temperature of the switch and shuts it off. Hysteresis is built into the thermal sense circuit, and after the device has cooled approximately 20 degrees, the switch turns back on. The switch continues to cycle in this manner until the load fault or input power is removed.

Undervoltage Lockout (UVLO)

An undervoltage lockout ensures that the power switch is in the off state at powerup. Whenever the input voltage falls below approximately 2 V, the power switch is quickly turned off. This facilitates the design of hot-insertion systems where it is not possible to turn off the power switch before input power is removed. The UVLO also keeps the switch from being turned on until the power supply has reached at least 2 V, even if the switch is enabled. Upon reinsertion, the power switch is turned on, with a controlled rise time to reduce EMI and voltage overshoots.

Generic Hot-Plug Applications

In many applications it may be necessary to remove modules or pc boards while the main unit is still operating. These are considered hot-plug applications (see Figure 37). Such implementations require the control of current surges seen by the main power supply and the card being inserted. The most effective way to control these surges is to limit and slowly ramp the current and voltage being applied to the card, similar to the way in which a power supply normally turns on. Because of the controlled rise times and fall times of the TPS202x series, these devices can be used to provide a softer start-up to devices being hot-plugged into a powered system. The UVLO feature of the TPS202x also ensures the switch is off after the card has been removed, and the switch remains off during the next insertion. The UVLO feature ensures a soft start with a controlled rise time for every insertion of the card or module.

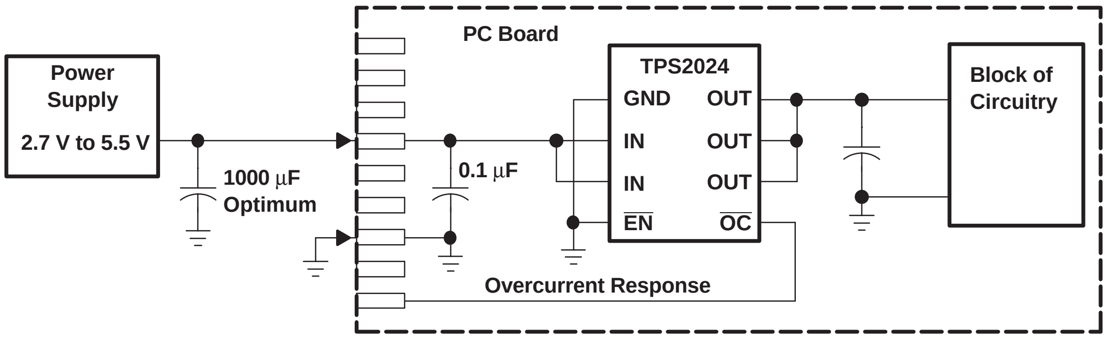


Figure 37. Typical Hot-Plug Implementation

By placing the TPS202x between the V_{CC} input and the rest of the circuitry, the input power reaches this device first after insertion. The typical rise time of the switch is approximately 9 ms, providing a slow voltage ramp at the output of the device. This implementation controls system surge currents and provides a hot-plugging mechanism for any device.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/ Ball Finish	MSL Peak Temp (3)	Samples (Requires Login)
TPS2020IDRQ1	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	Request Free Samples
TPS2021IDRQ1	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	Request Free Samples
TPS2022DRG4Q1	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	Request Free Samples
TPS2022DRQ1	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	Purchase Samples
TPS2024IDRG4Q1	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	Purchase Samples
TPS2024IDRQ1	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	Purchase Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF TPS2020-Q1, TPS2021-Q1, TPS2022-Q1, TPS2024-Q1 :

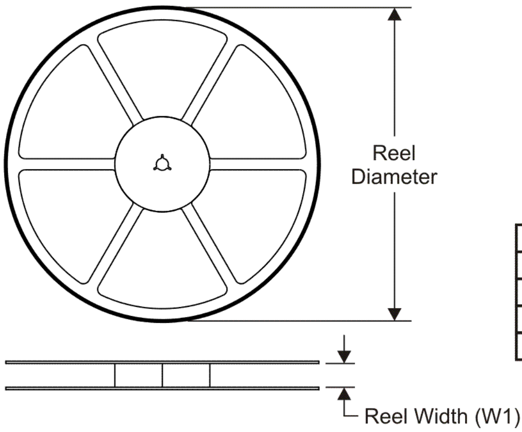
- Catalog: TPS2020, TPS2021, TPS2022, TPS2024

NOTE: Qualified Version Definitions:

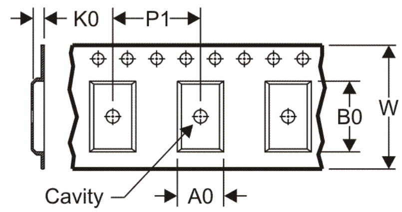
- Catalog - TI's standard catalog product

TAPE AND REEL INFORMATION

REEL DIMENSIONS

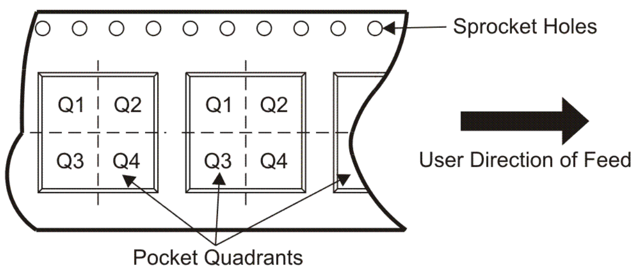


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

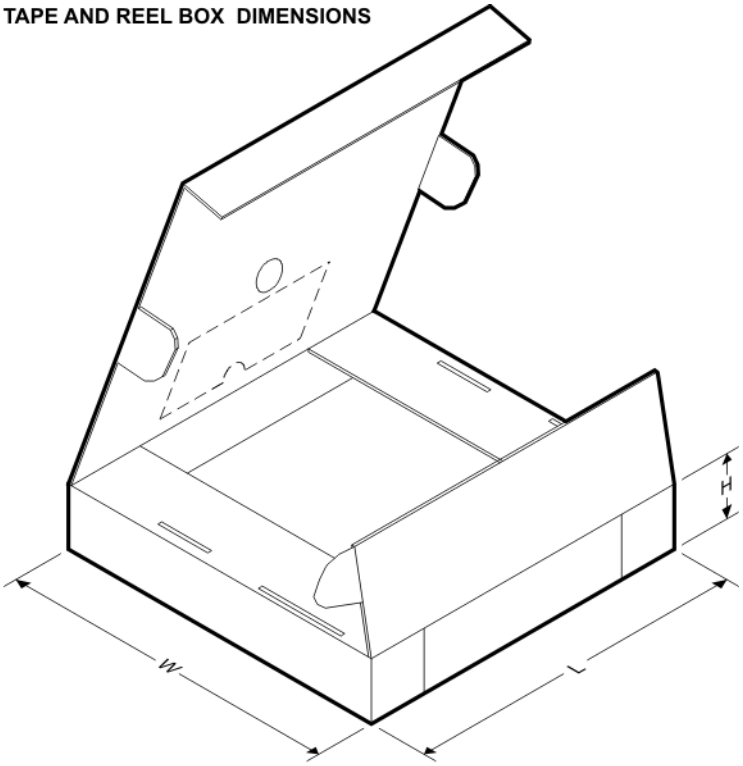
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS2020IDRQ1	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

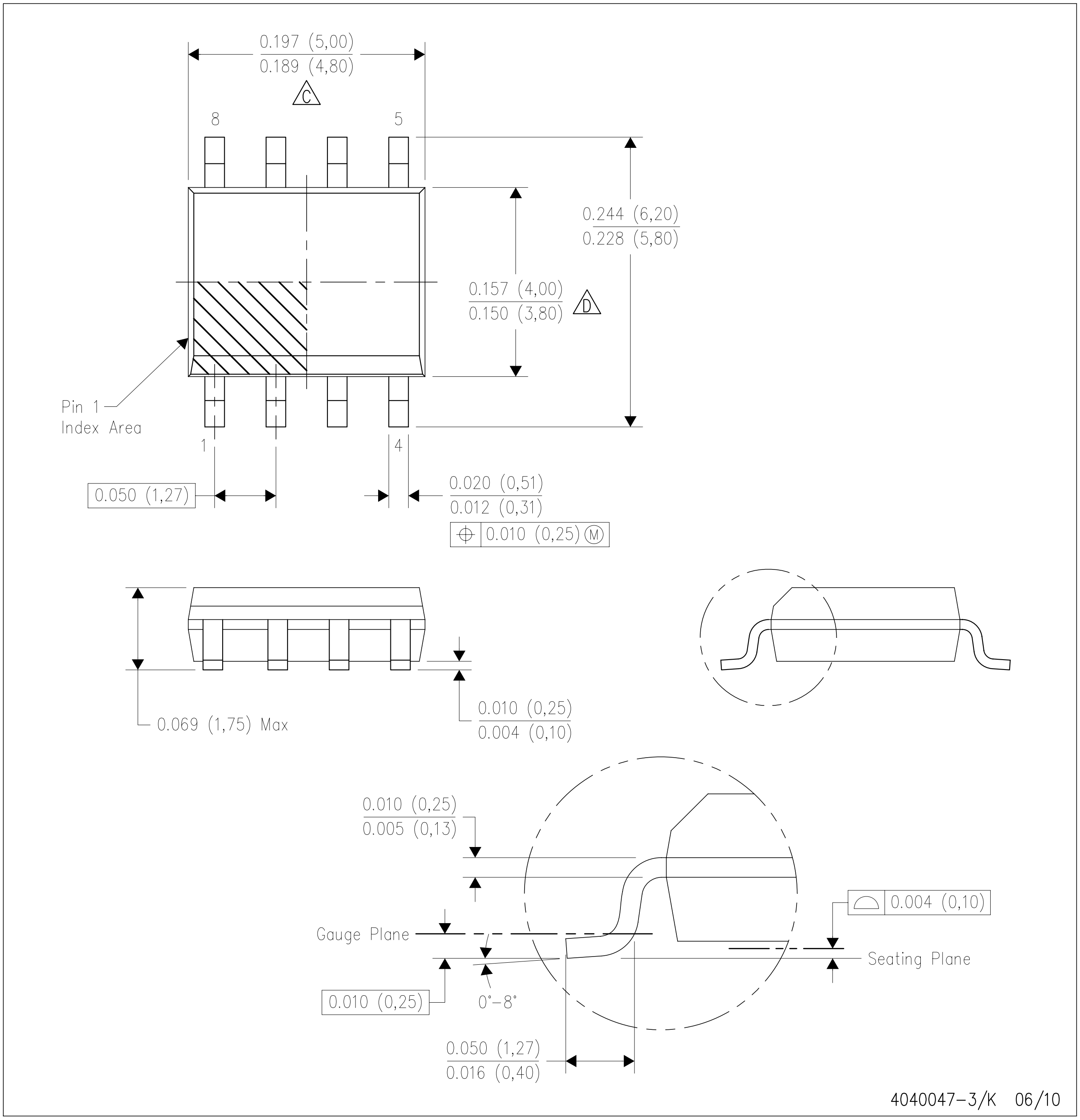
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

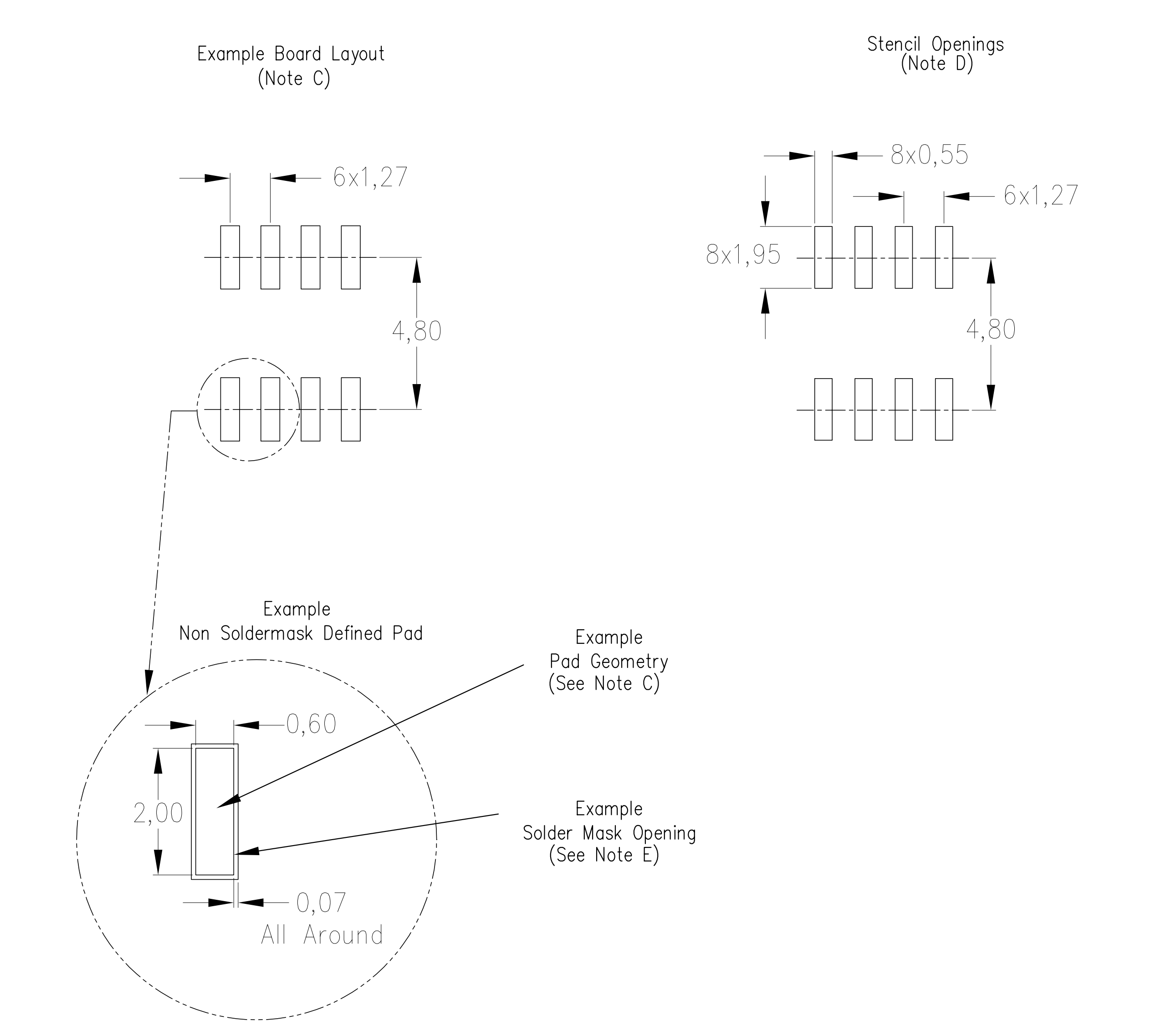
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS2020IDRQ1	SOIC	D	8	2500	340.5	338.1	20.6

D (R-PDSO-G8) PLASTIC SMALL-OUTLINE PACKAGE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 (0,15) per end.
D. Body width does not include interlead flash. Interlead flash shall not exceed .017 (0,43) per side.
E. Reference JEDEC MS-012 variation AA.

D (R-PDSO-G8) PLASTIC SMALL OUTLINE



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NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC-7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.