**TEXAS INSTRUMENTS**

D–8    DGN–8    D–16

**TPS2062-1**
**TPS2065-1**
**TPS2066-1**

www.ti.com                                                   SLVS714A−FEBRUARY 2007−REVISED MARCH 2009
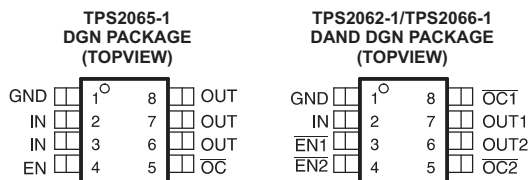
# CURRENT-LIMITED, POWER-DISTRIBUTION SWITCHES

## FEATURES

- **Output Discharge Function**
- **70-mΩ High-Side MOSFET**
- **1-A Continuous Current**
- **Thermal and Short-Circuit Protection**
- **Accurate Current Limit (1.1 A min, 1.9 A max)**
- **Operating Range: 2.7 V to 5.5 V**
- **0.6-ms Typical Rise Time**
- **Undervoltage Lockout**
- **Deglitched Fault Report ($\overline{OC}$)**
- **No $\overline{OC}$ Glitch During Power Up**
- **1-A Maximum Standby Supply Current**
- **Ambient Temperature Range: -40°C to 85°C**
- **ESD Protection**

## APPLICATIONS

- **Heavy Capacitive Loads**
- **Short-Circuit Protections**

**TPS2065-1**
**DGN PACKAGE**
**(TOPVIEW)**

| | | |
|---|---|---|
| GND | 1 | 8 OUT |
| IN | 2 | 7 OUT |
| IN | 3 | 6 OUT |
| EN | 4 | 5 $\overline{OC}$ |

**TPS2062-1/TPS2066-1**
**DAND DGN PACKAGE**
**(TOPVIEW)**

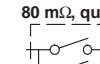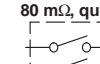| | | |
|---|---|---|
| GND | 1 | 8 $\overline{OC1}$ |
| IN | 2 | 7 OUT1 |
| $\overline{EN1}$ | 3 | 6 OUT2 |
| $\overline{EN2}$ | 4 | 5 $\overline{OC2}$ |

## DESCRIPTION

The TPS206x-1 power-distribution switches are intended for applications where heavy capacitive loads and short-circuits are likely to be encountered. This device incorporates 70-mΩ N-channel MOSFET power switches for power-distribution systems that require multiple power switches in a single package. Each switch is controlled by a logic enable input. Gate drive is provided by an internal charge pump designed to control the power-switch rise times and fall times to minimize current surges during switching. The charge pump requires no external components and allows operation from supplies as low as 2.7 V.

These switches provide a discharge function that provides a controlled discharge of the output voltage stored on the output capacitor.

When the output load exceeds the current-limit threshold or a short is present, the device limits the output current to a safe level by switching into a constant-current mode, pulling the overcurrent ($\overline{OCx}$) logic output low. When continuous heavy overloads and short-circuits increase the power dissipation in the switch, causing the junction temperature to rise, a thermal protection circuit shuts off the switch to prevent damage. Recovery from a thermal shutdown is automatic once the device has cooled sufficiently. Internal circuitry ensures that the switch remains off until valid input voltage is present. This power-distribution switch is designed to set current limit at 1.5 A typically.

**GENERAL SWITCH CATALOG**

| 33 mΩ, single | | | 80 mΩ, dual | | 80 mΩ, dual | | 80 mΩ, triple | | 80 mΩ, quad | | 80 mΩ, quad | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | TPS201xA | 0.2 A – 2 A | | TPS2042B | 500 mA | | | | | | | |
| | TPS202x | 0.2 A – 2 A | | TPS2052B | 500 mA | | | | | | | |
| | TPS203x | 0.2 A – 2 A | | TPS2046 | 250 mA | | | | | | | |
| | | | | TPS2056 | 250 mA | | | | | | | |
| | | | | TPS2062 | 1 A | TPS2080 | 500 mA | | | | | |
| | | | | TPS2066 | 1 A | TPS2081 | 500 mA | TPS2043B | 500 mA | | | TPS2085 | 500 mA |
| | | | | TPS2060 | 1.5 A | TPS2082 | 500 mA | TPS2053B | 500 mA | TPS2044B | 500 mA | TPS2086 | 500 mA |
| | | | | TPS2064 | 1.5 A | TPS2090 | 250 mA | TPS2047 | 250 mA | TPS2054B | 500 mA | TPS2087 | 500 mA |
| **80 mΩ, single** | | | **260 mΩ** | | TPS2091 | 250 mA | TPS2057 | 250 mA | TPS2048 | 250 mA | TPS2095 | 250 mA |
| | TPS2014 | 600 mA | IN1 | TPS2100/1 | TPS2092 | 250 mA | | | TPS2058 | 250 mA | TPS2096 | 250 mA |
| | TPS2015 | 1 A | IN2 | IN1 500 mA | | | | | | | TPS2097 | 250 mA |
| | TPS2041B | 500 mA | OUT | IN2 10 mA | | | | | | | | |
| | TPS2051B | 500 mA | **1.3 Ω** | TPS2102/3/4/5 | | | | | | | | |
| | TPS2045 | 250 mA | | IN1 500 mA | | | | | | | | |
| | TPS2055 | 250 mA | | IN2 100 mA | | | | | | | | |
| | TPS2061 | 1 A | | | | | | | | | | |
| | TPS2065 | 1 A | | | | | | | | | | |

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

## AVAILABLE OPTION AND ORDERING INFORMATION[1]

| $T_A$ | ENABLE | RECOMMENDED MAXIMUM CONTINUOUS LOAD CURRENT | TYPICAL SHORT-CIRCUIT CURRENT LIMIT AT 25°C | NUMBER OF SWITCHES | PACKAGED DEVICES [2] | |
|---|---|---|---|---|---|---|
| | | | | | MSOP (DGN) | SOIC(D) |
| −40°C to 85°C | Active high | 1 A | 1.5 A | Single | TPS2065DGN-1 | |
| | Active low | | | Dual | | TPS2062D-1 |
| | Active high | | | Dual | TPS2066DGN-1 | |

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.
(2) The package is available taped and reeled. Add an R suffix to device types (e.g., TPS2062-1DR).

## ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range unless otherwise noted[1]

| | | UNIT |
|---|---|---|
| Input voltage range, $V_{I(IN)}$[2] | | −0.3 V to 6 V |
| Output voltage range, $V_{O(OUT)}$[2], $V_{O(OUTx)}$ | | -0.3 V to 6 V |
| Input voltage range, $V_{I(\overline{EN})}$, $V_{I(EN)}$, $V_{I(\overline{ENx})}$, $V_{I(ENx)}$ | | −0.3 V to 6 V |
| Voltage range, $V_{I(\overline{OC})}$, $V_{I(\overline{OCx})}$ | | −0.3 V to 6 V |
| Continuous output current, $I_{O(OUT)}$, $I_{O(OUTx)}$ | | Internally limited |
| Continuous total power dissipation | | See Dissipation Rating Table |
| Operating virtual junction temperature range, $T_J$ | | -40°C to 125°C |
| Storage temperature range, $T_{stg}$ | | −65°C to 150°C |
| Electrostatic discharge (ESD) protection | Human body model MIL-STD-883C | 2 kV |
| | Charge device model (CDM) | 500 V |

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltages are with respect to GND.

## DISSIPATING RATING TABLE

| PACKAGE | $T_A \leq 25°C$ POWER RATING | DERATING FACTOR ABOVE $T_A = 25°C$ | $T_A = 70°C$ POWER RATING | $T_A = 85°C$ POWER RATING |
|---|---|---|---|---|
| D-8 | 585.82 mW | 5.8582 mW/°C | 322.20 mW | 234.32 mW |
| DGN-8 | 1712.3 mW | 17.123 mW/°C | 941.78 mW | 684.33 mW |

## RECOMMENDED OPERATING CONDITIONS

| | MIN | MAX | UNIT |
|---|---|---|---|
| Input voltage, $V_{I(IN)}$ | 2.7 | 5.5 | V |
| Input voltage, $V_{I(\overline{EN})}$, $V_{I(EN)}$, $V_{I(\overline{ENx})}$, $V_{I(ENx)}$ | 0 | 5.5 | V |
| Continuous output current, $I_{O(OUT)}$, $I_{O(OUTx)}$ | 0 | 1 | A |
| Steady state current through discharge. Device disabled, measured through output pin(s) | | 8 | mA |
| Operating virtual junction temperature, $T_J$ | -40 | 125 | °C |

## ELECTRICAL CHARACTERISTICS

over recommended operating junction temperature range, $V_{I(IN)}$ = 5.5 V, $I_O$ = 1 A, $V_{I(/ENx)}$ = 0 V, or $V_{I(ENx)}$ = 5.5 V (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS[1] | | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| **POWER SWITCH** | | | | | | | |
| $r_{DS(on)}$ | Static drain-source on-state resistance, 5-V operation and 3.3-V operation | $V_{I(IN)}$ = 5 V or 3.3 V, $I_O$ = 1 A, −40°C ≤ $T_J$ ≤ 125°C | | | 70 | 135 | mΩ |
| | Static drain-source on-state resistance, 2.7-V operation [2] | $V_{I(IN)}$ = 2.7 V, $I_O$ = 1 A, -40°C ≤ $T_J$ ≤ 125°C | | | 75 | 150 | mΩ |
| $t_r$ [2] | Rise time, output | $V_{I(IN)}$ = 5.5 V | $C_L$ = 1 μF, $R_L$ = 5 Ω, $T_J$ = 25°C | | 0.6 | 1.5 | ms |
| | | $V_{I(IN)}$ = 2.7 V | | | 0.4 | 1 | |
| $t_f$ [2] | Fall time, output | $V_{I(IN)}$ = 5.5 V | | 0.05 | | 0.5 | |
| | | $V_{I(IN)}$ = 2.7 V | | 0.05 | | 0.5 | |
| **ENABLE INPUT $\overline{EN}$ OR EN** | | | | | | | |
| $V_{IH}$ | High-level input voltage | 2.7 V ≤ $V_{I(IN)}$ ≤5.5 V | | 2 | | | V |
| $V_{IL}$ | Low-level input voltage | 2.7 V ≤ $V_{I(IN)}$ ≤ 5.5 V | | | | 0.8 | |
| $I_I$ | Input current | $V_{I(\overline{ENx})}$ = 0 V or 5.5 V, $V_{I(ENx)}$ = 0 V or 5.5 V | | -0.5 | | 0.5 | μA |
| $t_{on}$ [3] | Turnon time | $C_L$ = 100 μF, $R_L$ = 5 Ω | | | | 3 | ms |
| $t_{off}$ [3] | Turnoff time | $C_L$ = 100 μF, $R_L$ = 5 Ω | | | | 10 | |
| **CURRENT LIMIT** | | | | | | | |
| $I_{OS}$ | Short-circuit output current | $V_{I(IN)}$ = 5 V, OUT connected to GND, device enabled into short-circuit | $T_J$ = 25°C | 1.1 | 1.5 | 1.9 | A |
| | | | -40°C ≤ $T_J$ ≤ 125°C | 1.1 | 1.5 | 2.1 | |
| $I_{OC\_TRIP}$ [3] | Overcurrent trip threshold | $V_{I(IN)}$ = 5 V, current ramp (≤ 100 A/s) on OUT | | | 2.4 | 3 | A |
| **SUPPLY CURRENT (TPS2065-1)** | | | | | | | |
| Supply current, low-level output | | No load on OUT, $V_{I(\overline{ENx})}$ = 5.5 V, or $V_{I(ENx)}$ = 0 V | $T_J$ = 25°C | | 0.5 | 1 | μA |
| | | | -40°C ≤ $T_J$ ≤ 125°C | | 0.5 | 10 | |
| Supply current, high-level output | | No load on OUT, $V_{I(\overline{ENx})}$ = 0 V, or $V_{I(ENx)}$ = 5.5 V | $T_J$ = 25°C | | 43 | 60 | μA |
| | | | -40°C ≤ $T_J$ ≤ 125°C | | 43 | 70 | |
| Reverse leakage current | | $V_{I(OUTx)}$ = 5.5 V, IN = ground[3] | $T_J$ = 25°C | | 0 | | μA |
| **SUPPLY CURRENT (TPS2062-1, TPS2066-1)** | | | | | | | |
| Supply current, low-level output | | No load on OUT, $V_{I(\overline{ENx})}$ = 5.5 V, or $V_{I(ENx)}$ = 0 V | $T_J$ = 25°C | | 0.5 | 1 | μA |
| | | | -40°C ≤ $T_J$ ≤ 125°C | | 0.5 | 20 | |
| Supply current, high-level output | | No load on OUT, $V_{I(\overline{ENx})}$ = 0 V, or $V_{I(ENx)}$ = 5.5 V | $T_J$ = 25°C | | 50 | 70 | μA |
| | | | -40°C ≤ $T_J$ ≤ 125°C | | 50 | 90 | |
| Reverse leakage current | | $V_{I(OUTx)}$ = 5.5 V, IN = ground[3] | $T_J$ = 25°C | | 0.2 | | μA |

(1) Pulse-testing techniques maintain junction temperature close to ambient temperature; thermal effects must be taken into account separately.
(2) Not tested in production, specified by design.
(3) Not tested in production, specified by design.

## ELECTRICAL CHARACTERISTICS (continued)

over recommended operating junction temperature range, $V_{I(IN)}$ = 5.5 V, $I_O$ = 1 A, $V_{I(/ENx)}$ = 0 V, or $V_{I(ENx)}$ = 5.5 V (unless otherwise noted)

| PARAMETER | TEST CONDITIONS[1] | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|
| **UNDERVOLTAGE LOCKOUT** | | | | | |
| Low-level input voltage, IN | | 2 | | 2.5 | V |
| Hysteresis, IN | $T_J$ = 25°C | | 75 | | mV |
| **OVERCURRENT $\overline{OC1}$ and $\overline{OC2}$** | | | | | |
| Output low voltage, $V_{OL(OCx)}$ | $I_{O(\overline{OCx})}$ = 5 mA | | | 0.4 | V |
| Off-state current[4] | $V_{O(\overline{OCx})}$ = 5 V or 3.3 V | | | 1 | µA |
| $\overline{OC}$ deglitch[4] | $\overline{OCx}$ assertion or deassertion | 4 | 8 | 15 | ms |
| Discharge resistance | $V_{CC}$ = 5 V, disabled, $I_O$ = 1 mA | | 100 | | Ω |
| **THERMAL SHUTDOWN[5]** | | | | | |
| Thermal shutdown threshold[4] | | 135 | | | °C |
| Recovery from thermal shutdown[4] | | 125 | | | °C |
| Hysteresis[4] | | | 10 | | °C |

(4)  Not tested in production, specified by design.
(5)  The thermal shutdown only reacts under overcurrent conditions.

## DEVICE INFORMATION

### Pin Functions

| | PIN | | | I/O | DESCRIPTION |
|---|---|---|---|---|---|
| NAME | TPS2065-1 | TPS2062-1 | TPS2066-1 | | |
| EN | 4 | – | – | I | Enable input, logic high turns on power switch |
| $\overline{EN1}$ | – | 3 | – | I | Enable input, logic low turns on channel 1 |
| $\overline{EN2}$ | – | 4 | – | I | Enable input, logic high turns on channel 2 |
| EN1 | – | – | 3 | I | Enable input, logic high turns on channel 1 |
| EN2 | – | – | 4 | I | Enable input, logic high turns on channel 2 |
| GND | 1 | 1 | 1 | | Ground connection |
| IN | 2, 3 | 2 | 2 | I | Input voltage; connect a 0.1 µF or greater ceramic capacitor from IN to GND as close to the IC as possible |
| $\overline{OC}$ | 5 | – | – | O | Active-low open-drain output, asserted during over-current |
| $\overline{OC1}$ | – | 8 | 8 | O | Active-low open-drain output, asserted during over-current for channel 1 |
| $\overline{OC2}$ | | 5 | 5 | O | Active-low open-drain output, asserted during over-current for channel 2 |
| OUT | 6, 7, 8 | – | – | O | Power-switch output |
| OUT1 | – | 7 | 7 | O | Power-switch output for channel 1 |
| OUT2 | – | 6 | 6 | O | Power-switch output for channel 2 |

## FUNCTIONAL BLOCK DIAGRAM (TPS2065-1)
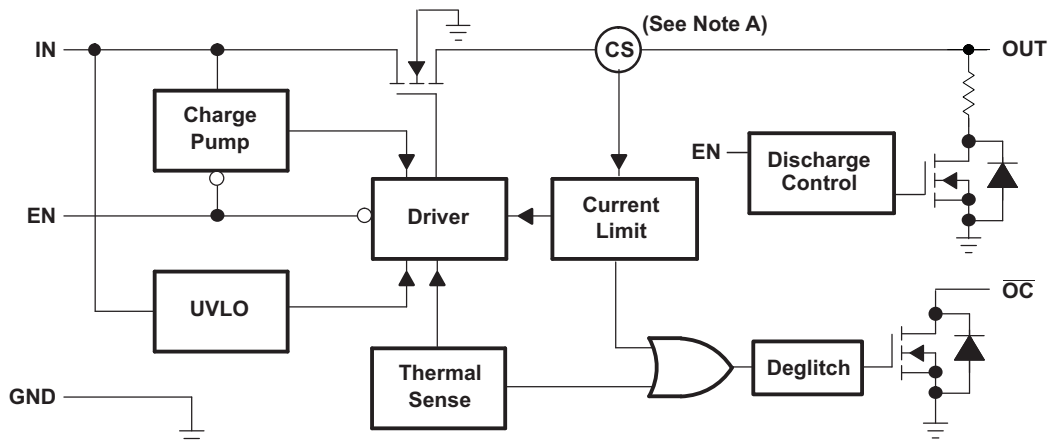


Note A: Current sense

## FUNCTIONAL BLOCK DIAGRAM (TPS2062-1 and TPS2066-1)
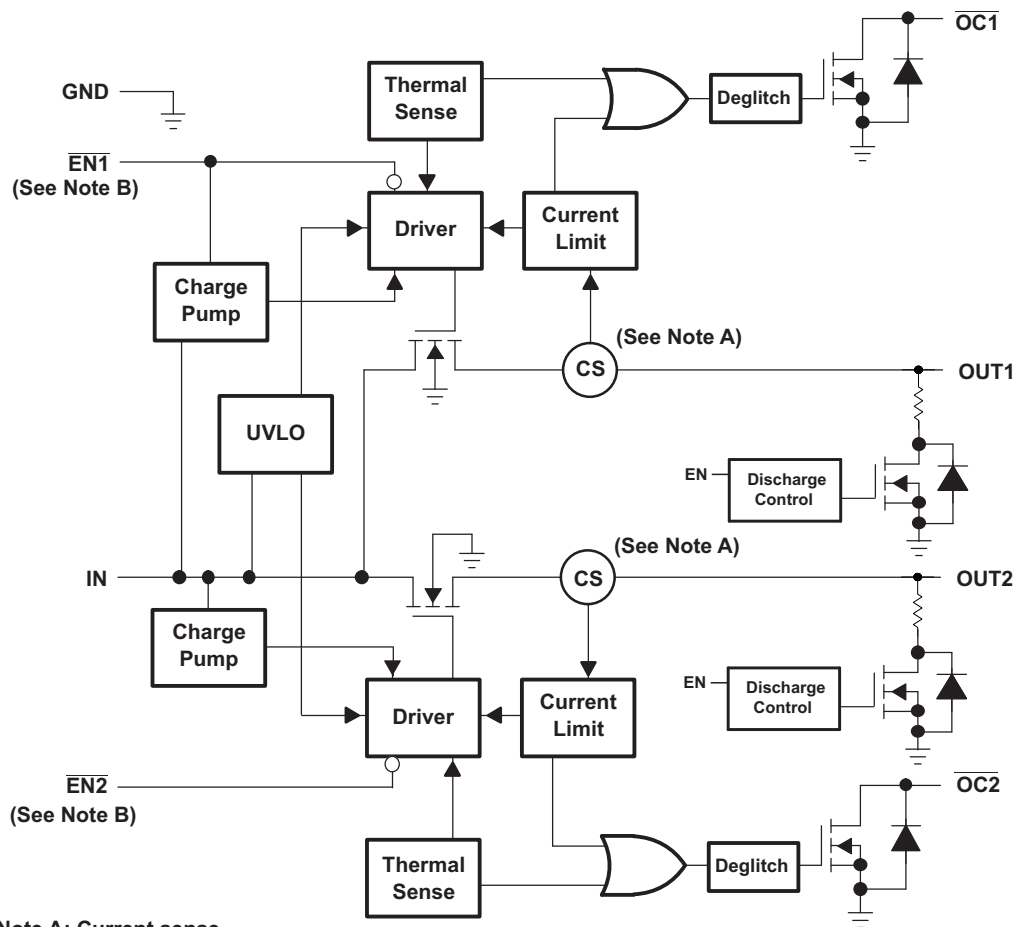


Note A: Current sense
Note B: Active low ($\overline{EN}$x) for TPS2062. Active high ($\overline{EN}$x) for TPS2066
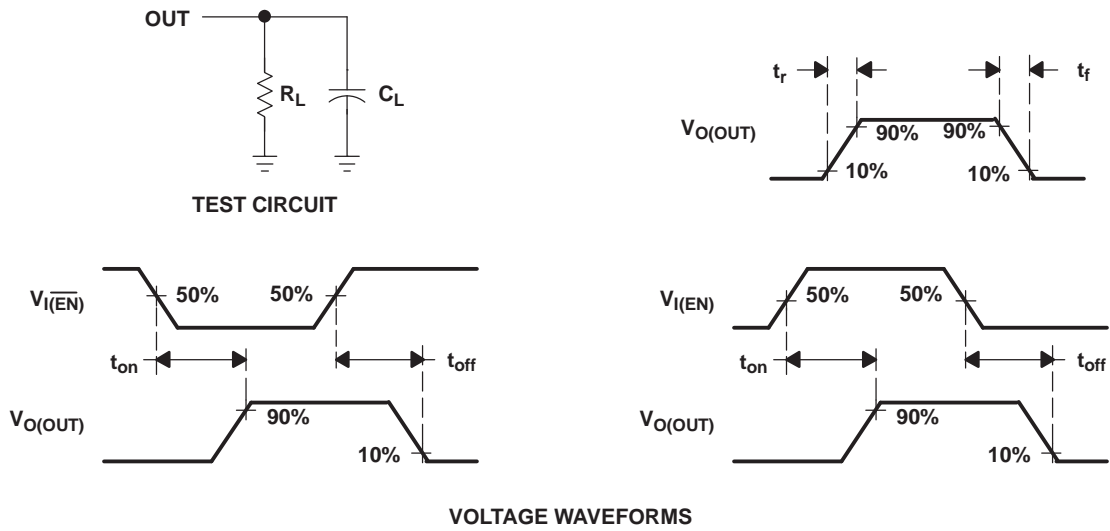
## PARAMETER MEASUREMENT INFORMATION

OUT

$R_L$   $C_L$

**TEST CIRCUIT**

$t_r$   $t_f$

$V_{O(OUT)}$   90%   90%
10%   10%

$V_{I(\overline{EN})}$   50%   50%

$t_{on}$   $t_{off}$

$V_{O(OUT)}$   90%
10%

$V_{I(EN)}$   50%   50%

$t_{on}$   $t_{off}$

$V_{O(OUT)}$   90%
10%

**VOLTAGE WAVEFORMS**

**Figure 1. Test Circuit and Voltage Waveforms**

$V_{I(EN)}$
5 V/div

$R_L = 5\ \Omega$,
$C_L = 1\ \mu F$
$T_A = 25°C$

$V_{O(OUT)}$
2 V/div

t – Time – 500 μs/div
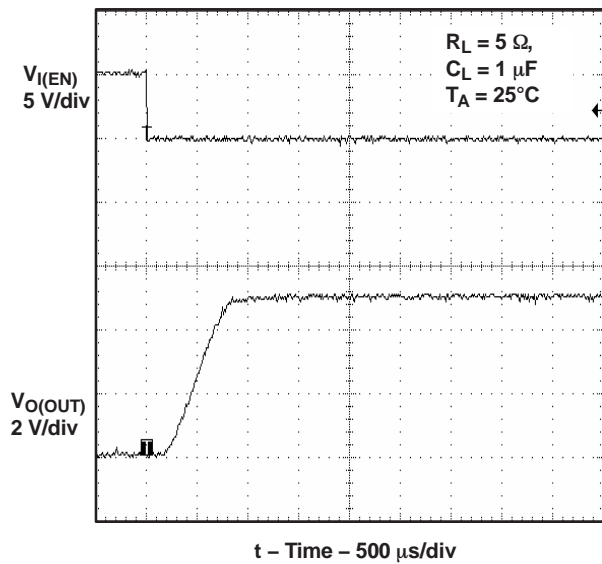
**Figure 2. Turnon Delay and Rise Time With 1-μF Load**

$V_{I(EN)}$
5 V/div

$V_{O(OUT)}$
2 V/div

$R_L = 5\ \Omega$,
$C_L = 1\ \mu F$
$T_A = 25°C$

t – Time – 500 μs/div
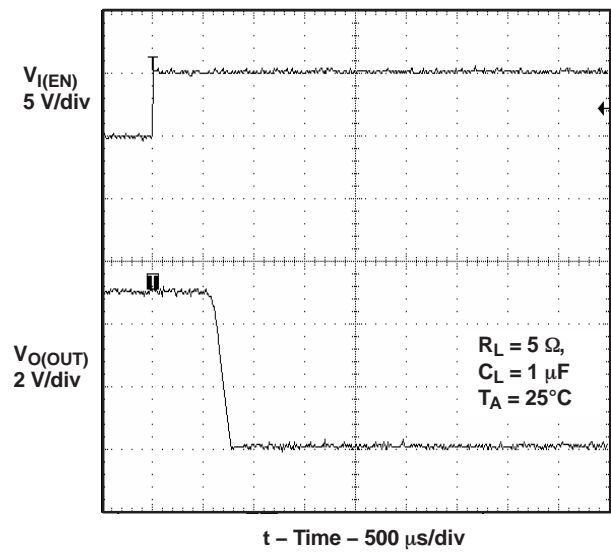
**Figure 3. Turnoff Delay and Fall Time With 1-μF Load**

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TPS2065-1
TPS2066-1

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## PARAMETER MEASUREMENT INFORMATION (continued)

$V_{I(EN)}$
5 V/div

$R_L = 5 \, \Omega,$
$C_L = 100 \, \mu F$
$T_A = 25°C$

$V_{O(OUT)}$
2 V/div

t − Time − 500 μs/div
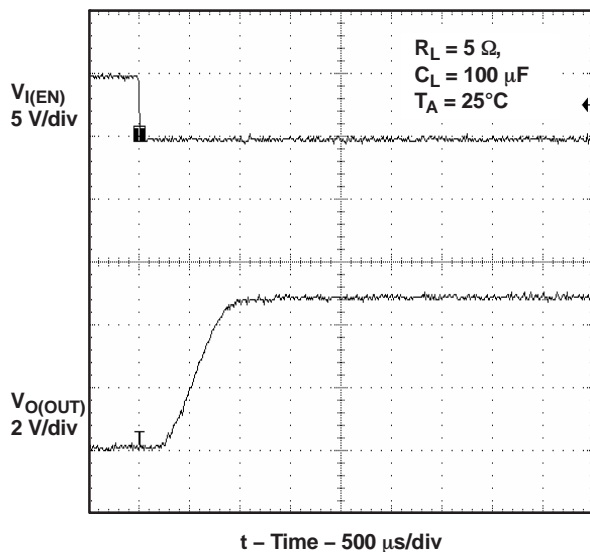
**Figure 4. Turnon Delay and Rise Time With 100-μF Load**

$V_{I(EN)}$
5 V/div

$V_{O(OUT)}$
2 V/div

$R_L = 5 \, \Omega,$
$C_L = 100 \, \mu F$
$T_A = 25°C$

t − Time − 500 μs/div
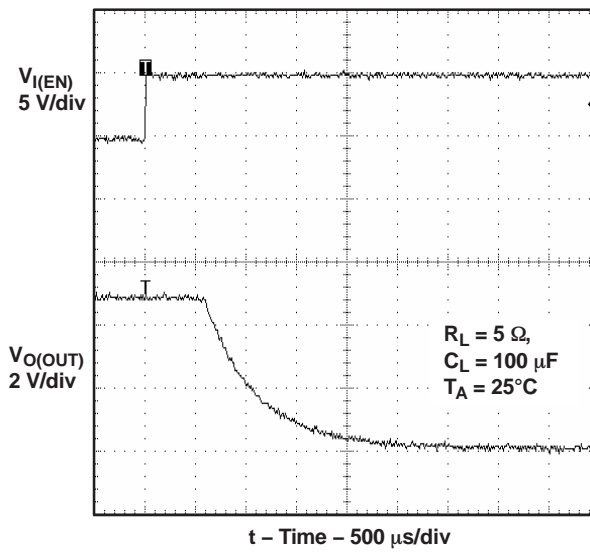
**Figure 5. Turnoff Delay and Fall Time With 100-μF Load**

$V_{I(EN)}$
5 V/div

$I_{O(OUT)}$
500 mA/div

t − Time − 500 μs/div
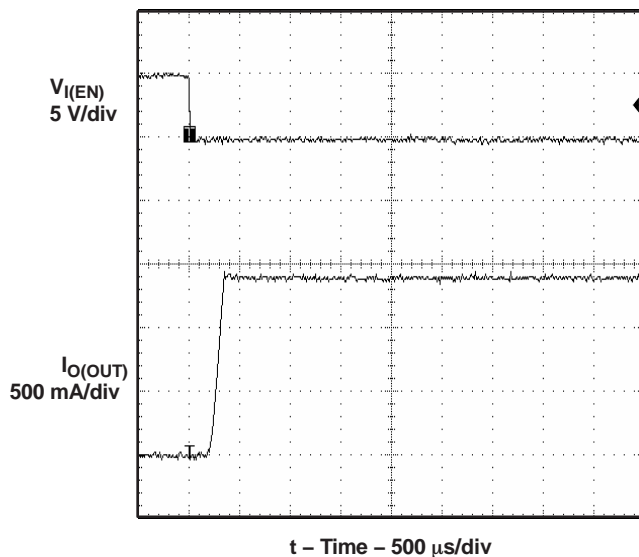
**Figure 6. Short-Circuit Current,
Device Enabled Into Short**

$V_{I(EN)}$
5 V/div

$V_{IN} = 5 \, V$
$R_L = 5 \, \Omega,$
$T_A = 25°C$

220 μF

470 μF

$I_{O(OUT)}$
500 mA/div

100 μF

t − Time − 1 ms/div
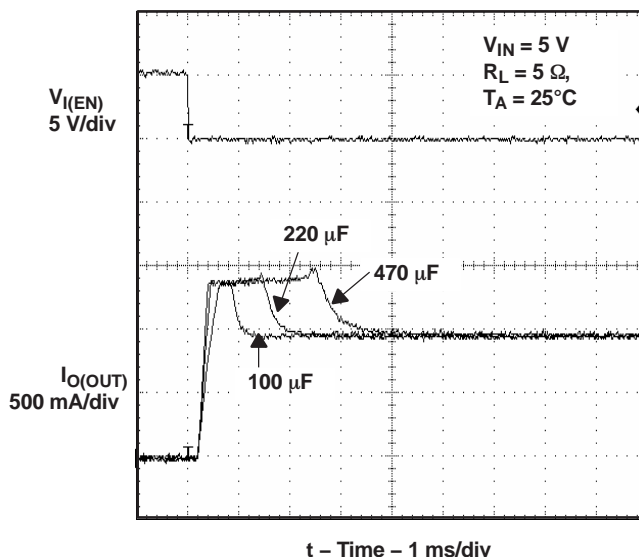
**Figure 7. Inrush Current With Different
Load Capacitance**

Product Folder Link(s): TPS2062-1 TPS2065-1 TPS2066-1

## PARAMETER MEASUREMENT INFORMATION (continued)



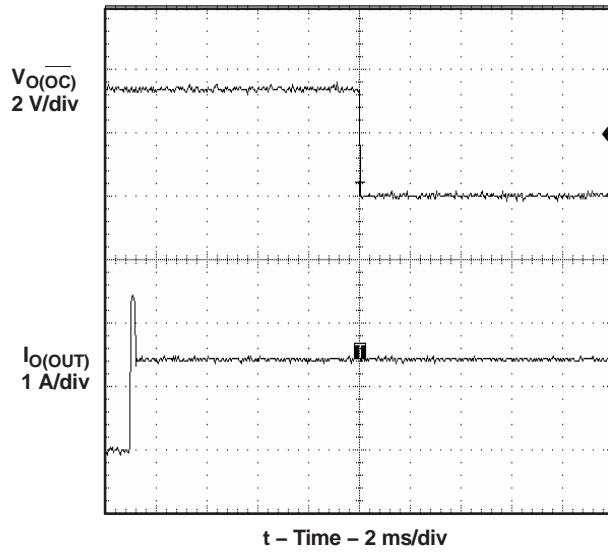**Figure 8. 2-Ω Load Connected to Enabled Device**
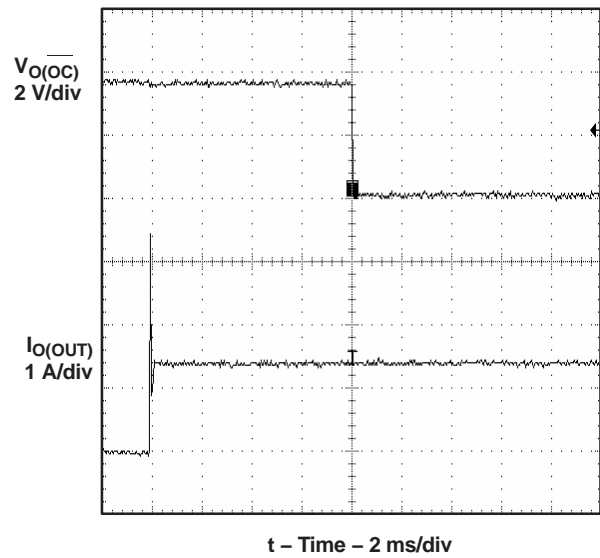


**Figure 9. 1-Ω Load Connected to Enabled Device**

## TYPICAL CHARACTERISTICS
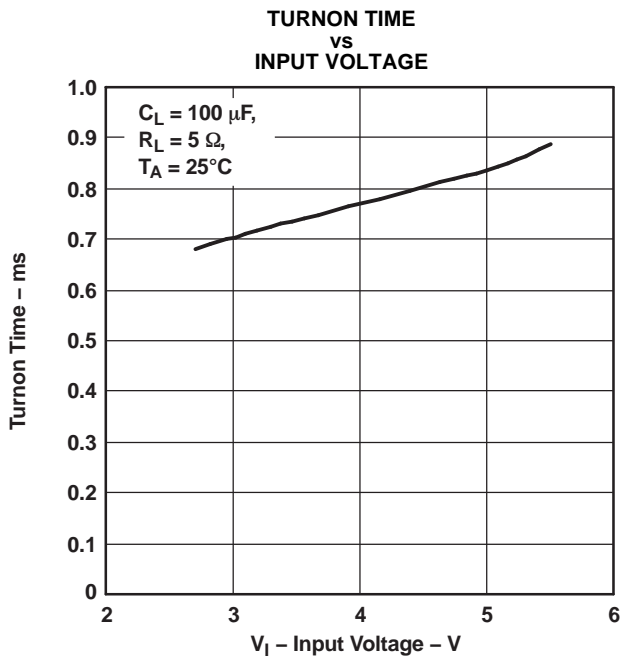
**TURNON TIME**
**vs**
**INPUT VOLTAGE**

$C_L = 100\ \mu F$,
$R_L = 5\ \Omega$,
$T_A = 25°C$

Turnon Time – ms

$V_I$ – Input Voltage – V

**Figure 10.**

**TURNOFF TIME**
**vs**
**INPUT VOLTAGE**

$C_L = 100\ \mu F$,
$R_L = 5\ \Omega$,
$T_A = 25°C$

Turnoff Time – mS

$V_I$ – Input Voltage – V

**Figure 11.**

**RISE TIME**
**vs**
**INPUT VOLTAGE**

$C_L = 1\ \mu F$,
$R_L = 5\ \Omega$,
$T_A = 25°C$

Rise Time – ms

$V_I$ – Input Voltage – V

**Figure 12.**

**FALL TIME**
**vs**
**INPUT VOLTAGE**

$C_L = 1\ \mu F$,
$R_L = 5\ \Omega$,
$T_A = 25°C$

Fall Time – ms

$V_I$ – Input Voltage – V

**Figure 13.**

*Submit Documentation Feedback*

9

Product Folder Link(s): TPS2062-1 TPS2065-1 TPS2066-1

**TPS2062-1**
**TPS2065-1**
**TPS2066-1**

TEXAS
INSTRUMENTS

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# TYPICAL CHARACTERISTICS (continued)

**TPS2061, TPS2065-1**
**SUPPLY CURRENT, OUTPUT ENABLED**
**vs**
**JUNCTION TEMPERATURE**



$V_I$ = 5.5 V

$V_I$ = 5 V

$V_I$ = 3.3 V

$V_I$ = 2.7 V

$I_{I (IN)}$ – Supply Current, Output Enabled – $\mu$A

$T_J$ – Junction Temperature – °C

Figure 14.

**TPS2062-1, TPS2066-1**
**SUPPLY CURRENT, OUTPUT ENABLED**
**vs**
**JUNCTION TEMPERATURE**



$V_I$ = 5.5 V

$V_I$ = 5 V

$V_I$ = 3.3 V

$V_I$ = 2.7 V

$I_{I (IN)}$ – Supply Current, Output Enabled – $\mu$A

$T_J$ – Junction Temperature – °C

Figure 15.

**TPS2065-1**
**SUPPLY CURRENT, OUTPUT DISABLED**
**vs**
**JUNCTION TEMPERATURE**



I – Off-State Current – $\mu$A

$T_J$ – Junction Temperature – °C

Figure 16.

**TPS2062-1, TPS2066-1**
**SUPPLY CURRENT, OUTPUT DISABLED**
**vs**
**JUNCTION TEMPERATURE**



I – Off-State Current – $\mu$A

$T_J$ – Junction Temperature – °C

Figure 17.

*Submit Documentation Feedback*

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## TYPICAL CHARACTERISTICS (continued)

STATIC DRAIN-SOURCE ON-STATE RESISTANCE
vs
JUNCTION TEMPERATURE

Figure 18.

SHORT-CIRCUIT OUTPUT CURRENT
vs
JUNCTION TEMPERATURE

Figure 19.

THRESHOLD TRIP CURRENT
vs
INPUT VOLTAGE

Figure 20.

UNDERVOLTAGE LOCKOUT
vs
JUNCTION TEMPERATURE
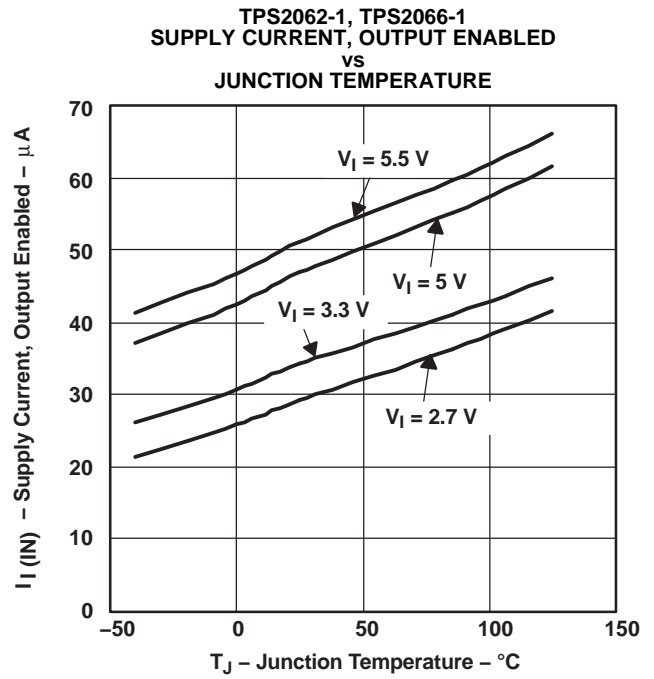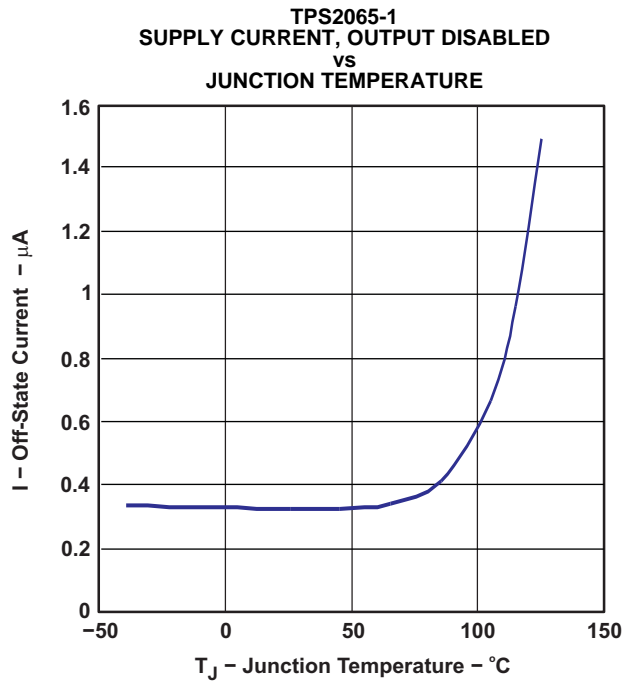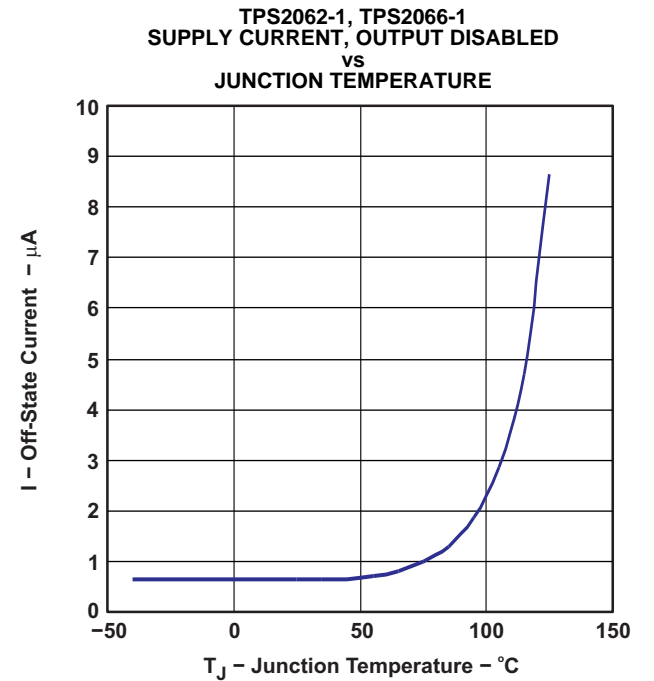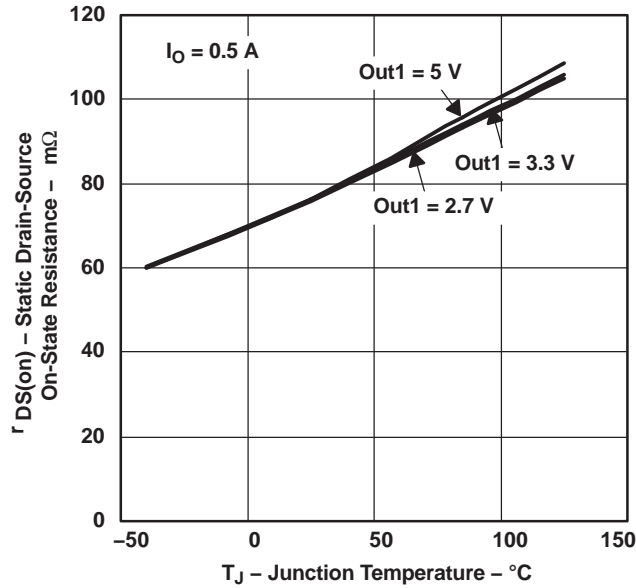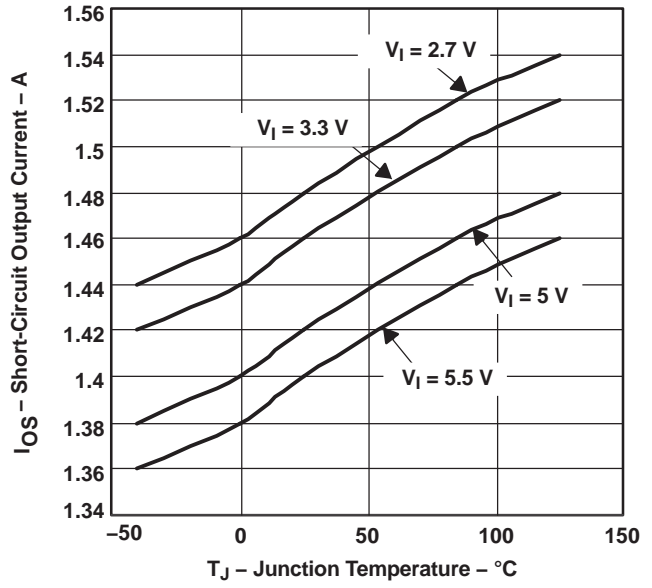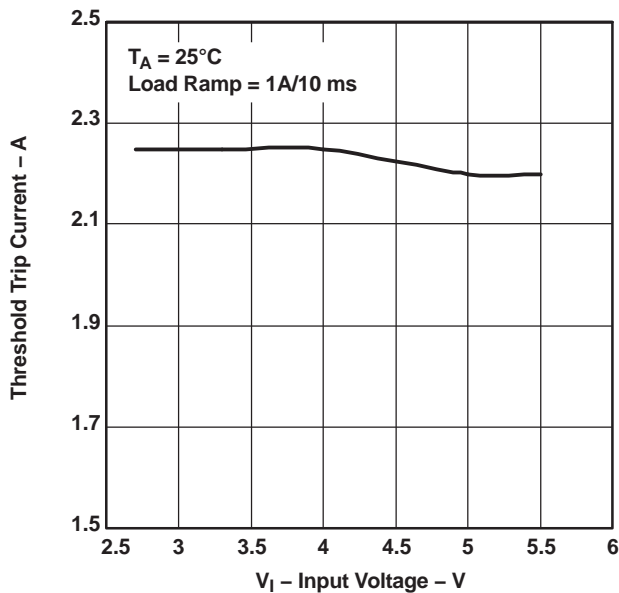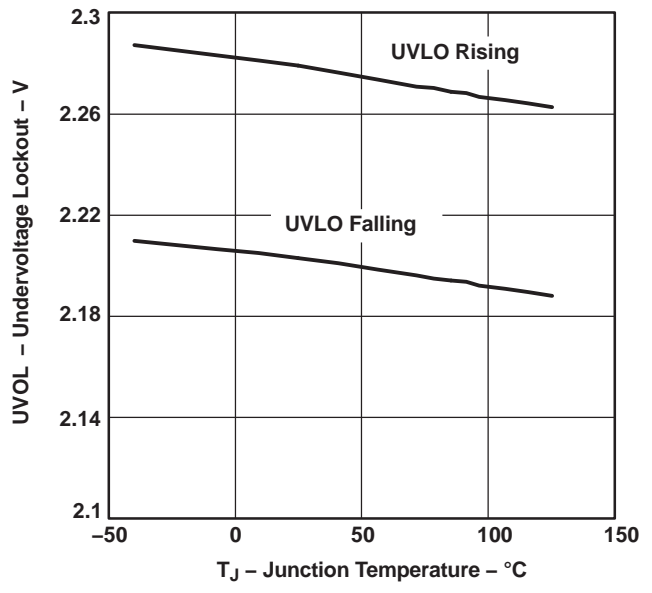
Figure 21.

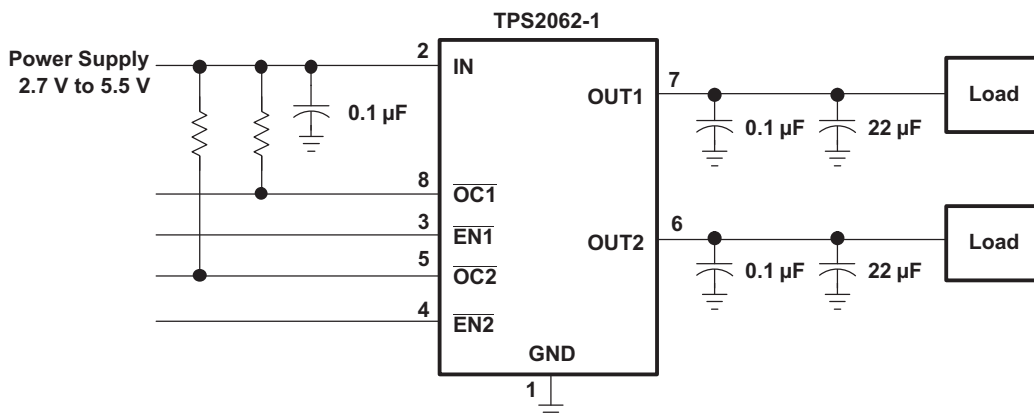Product Folder Link(s): TPS2062-1 TPS2065-1 TPS2066-

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## TYPICAL CHARACTERISTICS (continued)

**CURRENT-LIMIT RESPONSE**
**vs**
**PEAK CURRENT**



Figure 22.

Product Folder Link(s): *TPS2062-1 TPS2065-1 TPS2066-1*
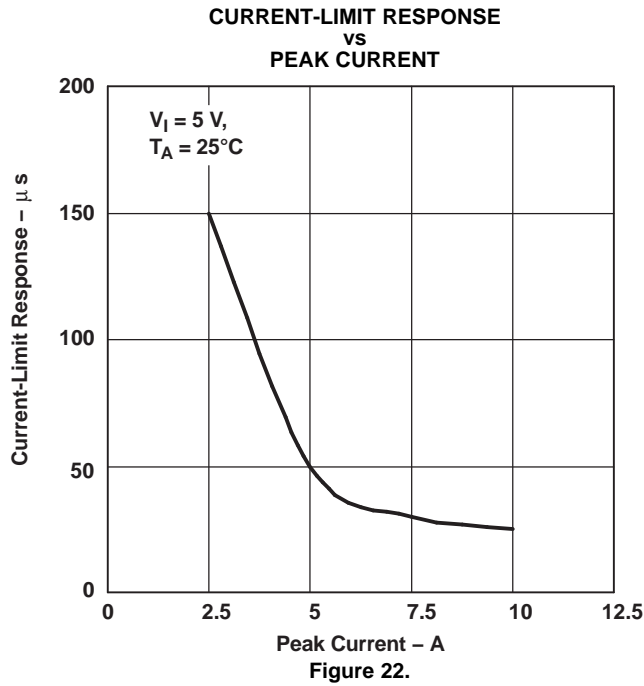
**APPLICATION INFORMATION**

## POWER-SUPPLY CONSIDERATIONS



**Figure 23. Typical Application**

A 0.01-μF to 0.1-μF ceramic bypass capacitor between IN and GND, close to the device, is recommended. Placing a high-value electrolytic capacitor on the output pin(s) is recommended when the output load is heavy. This precaution reduces power-supply transients that may cause ringing on the input. Additionally, bypassing the output with a 0.01-μF to 0.1-μF ceramic capacitor improves the immunity of the device to short-circuit transients.

## OVERCURRENT

A sense FET is employed to check for overcurrent conditions. Unlike current-sense resistors, sense FETs do not increase the series resistance of the current path. When an overcurrent condition is detected, the device maintains a constant output current and reduces the output voltage accordingly. Complete shutdown occurs only if the fault is present long enough to activate thermal limiting.

Three possible overload conditions can occur. In the first condition, the output has been shorted before the device is enabled or before $V_{I(IN)}$ has been applied (see Figure 15). The TPS206x-1 senses the short and immediately switches into a constant-current output.

In the second condition, a short or an overload occurs while the device is enabled. At the instant the overload occurs, high currents may flow for a short period of time before the current-limit circuit can react. After the current-limit circuit has tripped (reached the overcurrent trip threshold), the device switches into constant-current mode.

In the third condition, the load has been gradually increased beyond the recommended operating current. The current is permitted to rise until the current-limit threshold is reached or until the thermal limit of the device is exceeded (see Figure 17). The TPS206x-1 is capable of delivering current up to the current-limit threshold without damaging the device. Once the threshold has been reached, the device switches into its constant-current mode.

## $\overline{OC}$ RESPONSE

The $\overline{OCx}$ open-drain output is asserted (active low) when an overcurrent or overtemperature shutdown condition is encountered after a 10-ms deglitch timeout. The output remains asserted until the overcurrent or overtemperature condition is removed. Connecting a heavy capacitive load to an enabled device can cause a momentary overcurrent condition; however, no false reporting on $\overline{OCx}$ occurs due to the 10-ms deglitch circuit. The TPS206x-1 is designed to eliminate false overcurrent reporting. The internal overcurrent deglitch eliminates the need for external components to remove unwanted pulses. $\overline{OCx}$ is not deglitched when the switch is turned off due to an overtemperature shutdown.

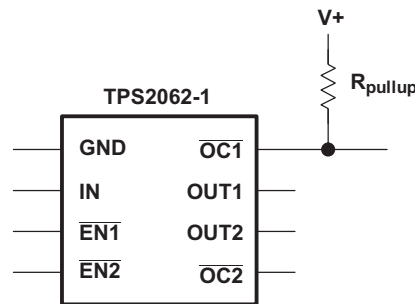www.BDTIC.com/TI

**TPS2062-1**
**TPS2065-1**
**TPS2066-1**

SLVS714A−FEBRUARY 2007−REVISED MARCH 2009

**TEXAS INSTRUMENTS**

www.ti.com

**Figure 24. Typical Circuit for the $\overline{\text{OC}}$ Pin**

## POWER DISSIPATION AND JUNCTION TEMPERATURE

The low on-resistance on the N-channel MOSFET allows the small surface-mount packages to pass large currents. The thermal resistances of these packages are high compared to those of power packages; it is good design practice to check power dissipation and junction temperature. Begin by determining the $r_{DS(on)}$ of the N-channel MOSFET relative to the input voltage and operating temperature. As an initial estimate, use the highest operating ambient temperature of interest and read $r_{DS(on)}$ from Figure 18. Using this value, the power dissipation per switch can be calculated by:

$$P_D = r_{DS(on)} \times I^2$$

Multiply this number by the number of switches being used. This step renders the total power dissipation from the N-channel MOSFETs.

Finally, calculate the junction temperature:

$$T_J = P_D \times R_{\theta JA} + T_A$$

Where:

$T_A$ = Ambient temperature °C

$R_{\theta JA}$ = Thermal resistance

$P_D$ = Total power dissipation based on number of switches being used.

Compare the calculated junction temperature with the initial estimate. If they do not agree within a few degrees, repeat the calculation, using the calculated value as the new estimate. Two or three iterations are generally sufficient to get a reasonable answer.

## THERMAL PROTECTION

Thermal protection prevents damage to the IC when heavy-overload or short-circuit faults are present for extended periods of time. The TPS206x-1 implements a thermal sensing to monitor the operating junction temperature of the power distribution switch. In an overcurrent or short-circuit condition, the junction temperature rises due to excessive power dissipation. Once the die temperature rises to approximately 140°C due to overcurrent conditions, the internal thermal sense circuitry turns the power switch off, thus preventing the power switch from damage. Hysteresis is built into the thermal sense circuit, and after the device has cooled approximately 10°C, the switch turns back on. The switch continues to cycle in this manner until the load fault or input power is removed. The $\overline{\text{OCx}}$ open-drain output is asserted (active low) when an overtemperature shutdown or overcurrent occurs.

## UNDERVOLTAGE LOCKOUT (UVLO)

An undervoltage lockout ensures that the power switch is in the off state at power up. Whenever the input voltage falls below approximately 2 V, the power switch is quickly turned off. This facilitates the design of hot-insertion systems where it is not possible to turn off the power switch before input power is removed. The UVLO also keeps the switch from being turned on until the power supply has reached at least 2 V, even if the switch is enabled. On reinsertion, the power switch is turned on, with a controlled rise time to reduce EMI and voltage overshoots.

## UNIVERSAL SERIAL BUS (USB) APPLICATIONS

The universal serial bus (USB) interface is a 12-Mb/s, or 1.5-Mb/s, multiplexed serial bus designed for low-to-medium bandwidth PC peripherals (e.g., keyboards, printers, scanners, and mice). The four-wire USB interface is conceived for dynamic attach-detach (hot plug-unplug) of peripherals. Two lines are provided for differential data, and two lines are provided for 5-V power distribution.

USB data is a 3.3-V level signal, but power is distributed at 5 V to allow for voltage drops in cases where power is distributed through more than one hub across long cables. Each function must provide its own regulated 3.3 V from the 5-V input or its own internal power supply.

The USB specification defines the following five classes of devices, each differentiated by power-consumption requirements:

- Hosts/self-powered hubs (SPH)
- Bus-powered hubs (BPH)
- Low-power, bus-powered functions
- High-power, bus-powered functions
- Self-powered functions

SPHs and BPHs distribute data and power to downstream functions. The TPS206x-1 has higher current capability than required by one USB port; so, it can be used on the host side and supplies power to multiple downstream ports or functions.

## HOST/SELF-POWERED AND BUS-POWERED HUBS

Hosts and SPHs have a local power supply that powers the embedded functions and the downstream ports (see Figure 25). This power supply must provide from 5.25 V to 4.75 V to the board side of the downstream connection under full-load and no-load conditions. Hosts and SPHs are required to have current-limit protection and must report overcurrent conditions to the USB controller. Typical SPHs are desktop PCs, monitors, printers, and stand-alone hubs.
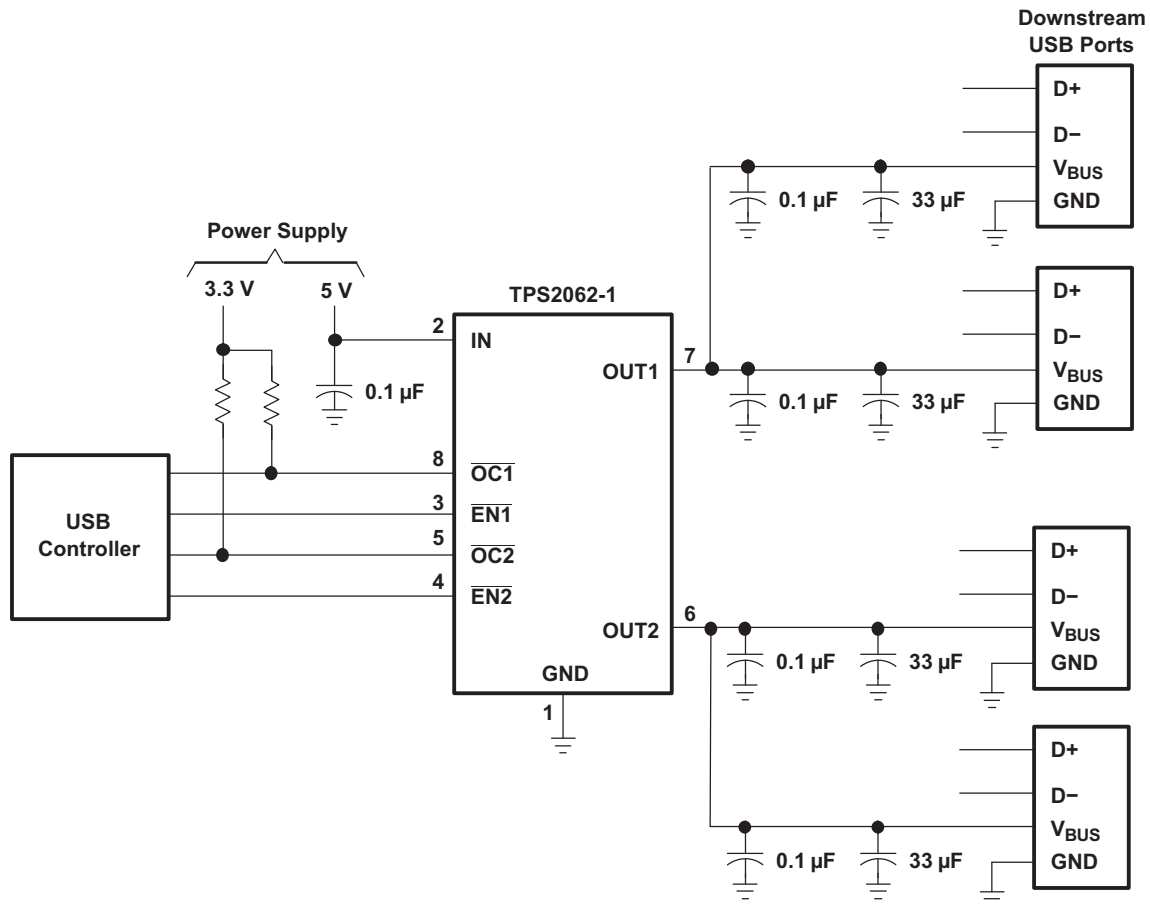
**Figure 25. Typical Four-Port USB Host / Self-Powered Hub**

BPHs obtain all power from upstream ports and often contain an embedded function. The hubs are required to power up with less than one unit load. The BPH usually has one embedded function, and power is always available to the controller of the hub. If the embedded function and hub require more than 100 mA on power up, the power to the embedded function may need to be kept off until enumeration is completed. This can be accomplished by removing power or by shutting off the clock to the embedded function. Power switching the embedded function is not necessary if the aggregate power draw for the function and controller is less than one unit load. The total current drawn by the bus-powered device is the sum of the current to the controller, the embedded function, and the downstream ports, and it is limited to 500 mA from an upstream port.

## LOW-POWER BUS-POWERED AND HIGH-POWER BUS-POWERED FUNCTIONS

Both low-power and high-power bus-powered functions obtain all power from upstream ports; low-power functions always draw less than 100 mA; high-power functions must draw less than 100 mA at power up and can draw up to 500 mA after enumeration. If the load of the function is more than the parallel combination of 44 Ω and 10 µF at power up, the device must implement inrush current limiting (see Figure 26). With TPS206x-1, the internal functions could draw more than 500 mA, which fits the needs of some applications such as motor driving circuits.
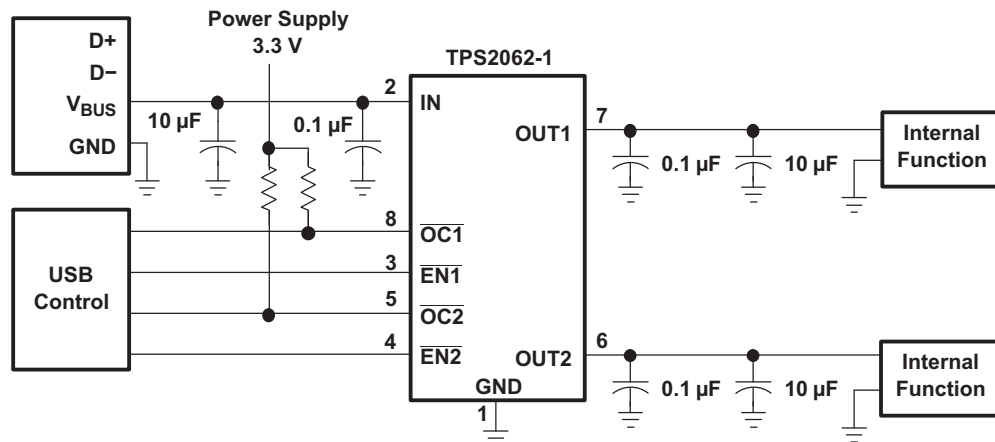
**Figure 26. High-Power Bus-Powered Function**

## USB POWER-DISTRIBUTION REQUIREMENTS

USB can be implemented in several ways, and, regardless of the type of USB device being developed, several power-distribution features must be implemented.

- Hosts/SPHs must:
  - Current-limit downstream ports
  - Report overcurrent conditions on USB $V_{BUS}$
- BPHs must:
  - Enable/disable power to downstream ports
  - Power up at <100 mA
  - Limit inrush current (<44 Ω and 10 µF)
- Functions must:
  - Limit inrush currents
  - Power up at <100 mA

The feature set of the TPS206x-1 allows them to meet each of these requirements. The integrated current-limiting and overcurrent reporting is required by hosts and self-powered hubs. The logic-level enable and controlled rise times meet the need of both input and output ports on bus-powered hubs, as well as the input ports for bus-powered functions (see Figure 27).
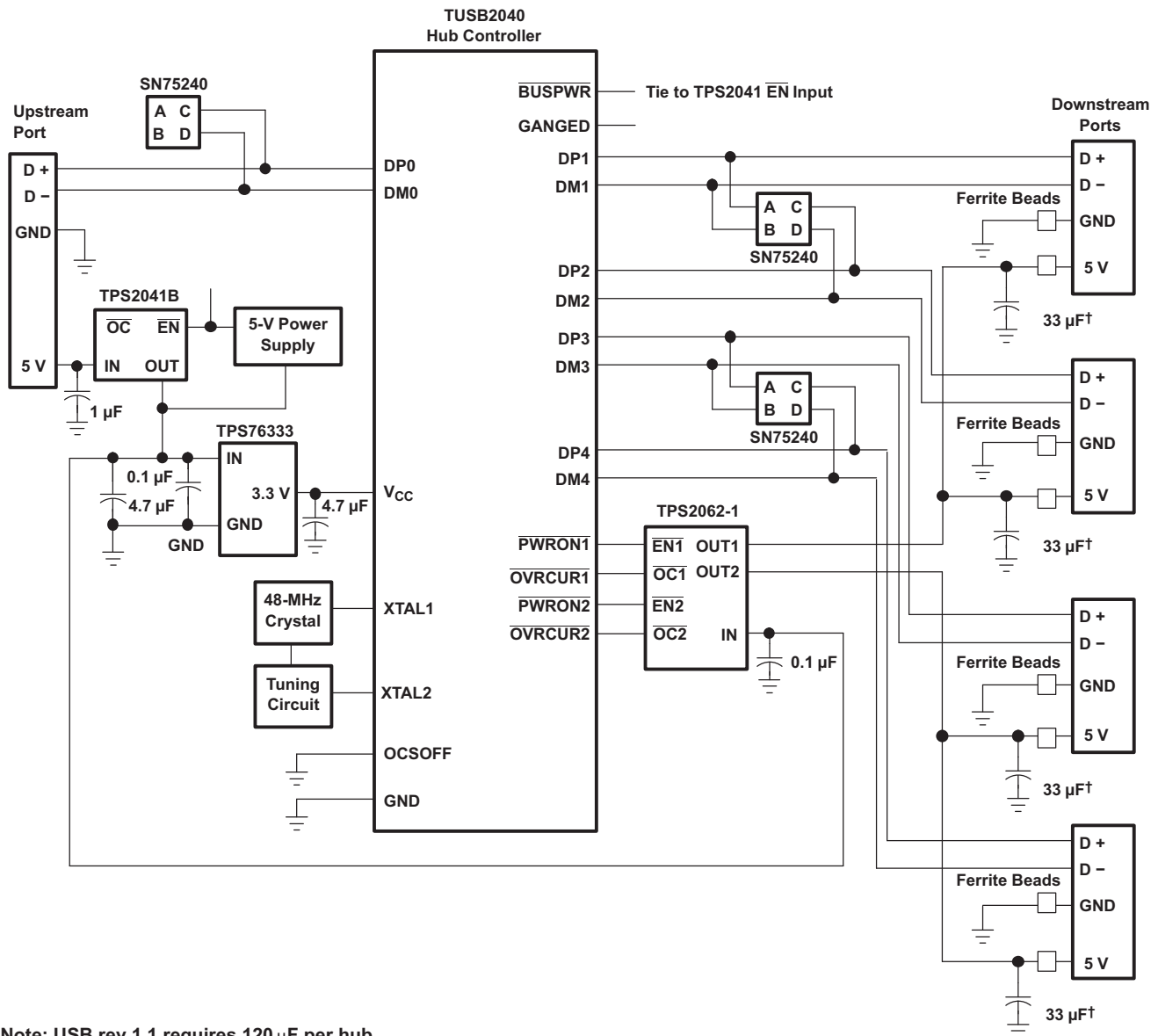
**Note: USB rev 1.1 requires 120 μF per hub.**

**Figure 27. Hybrid Self / Bus-Powered Hub Implementation**

## GENERIC HOT-PLUG APPLICATIONS

In many applications it may be necessary to remove modules or pc boards while the main unit is still operating. These are considered hot-plug applications. Such implementations require the control of current surges seen by the main power supply and the card being inserted. The most effective way to control these surges is to limit and slowly ramp the current and voltage being applied to the card, similar to the way in which a power supply normally turns on. Due to the controlled rise times and fall times of the TPS206x-1, these devices can be used to provide a softer start-up to devices being hot-plugged into a powered system. The UVLO feature of the TPS206x-1 also ensures that the switch is off after the card has been removed, and that the switch is off during the next insertion. The UVLO feature insures a soft start with a controlled rise time for every insertion of the card or module.
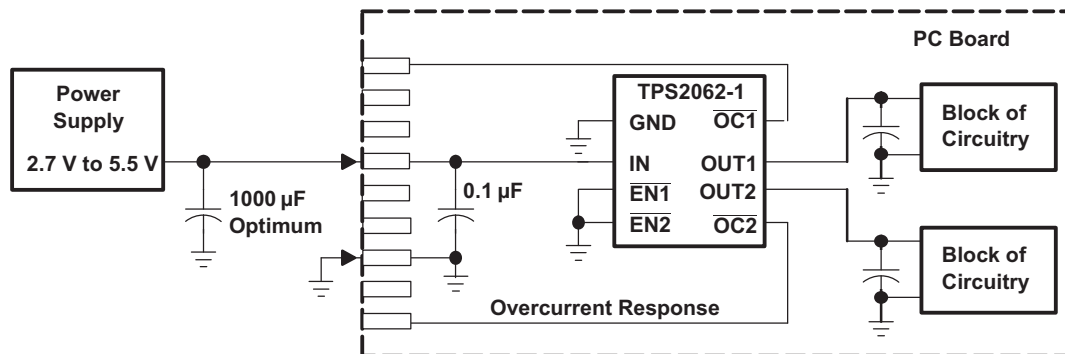
Product Folder Link(s): *TPS2062-1 TPS2065-1 TPS2066-1*

**Figure 28. Typical Hot-Plug Implementation**

By placing the TPS206x-1 between the $V_{CC}$ input and the rest of the circuitry, the input power reaches these devices first after insertion. The typical rise time of the switch is approximately 1 ms, providing a slow voltage ramp at the output of the device. This implementation controls system surge currents and provides a hot-plugging mechanism for any device.

## DETAILED DESCRIPTION

### Power Switch

The power switch is an N-channel MOSFET with a low on-state resistance. Configured as a high-side switch, the power switch prevents current flow from OUT to IN and IN to OUT when disabled. The power switch supplies a minimum current of 1 A.

### Charge Pump

An internal charge pump supplies power to the driver circuit and provides the necessary voltage to pull the gate of the MOSFET above the source. The charge pump operates from input voltages as low as 2.7 V and requires little supply current.

### Driver

The driver controls the gate voltage of the power switch. To limit large current surges and reduce the associated electromagnetic interference (EMI) produced, the driver incorporates circuitry that controls the rise times and fall times of the output voltage.

### Enable ($\overline{\text{ENx}}$ or ENx)

The logic enable disables the power switch and the bias for the charge pump, driver, and other circuitry to reduce the supply current. The supply current is reduced to less than 1 µA when a logic high is present on $\overline{\text{ENx}}$, or when a logic low is present on ENx. A logic zero input on $\overline{\text{ENx}}$, or a logic high input on ENx restores bias to the drive and control circuits and turns the switch on. The enable input is compatible with both TTL and CMOS logic levels.

### Overcurrent ($\overline{\text{OCx}}$)

The $\overline{\text{OCx}}$ open-drain output is asserted (active low) when an overcurrent or overtemperature condition is encountered. The output remains asserted until the overcurrent or overtemperature condition is removed. A 10-ms deglitch circuit prevents the $\overline{\text{OCx}}$ signal from oscillation or false triggering. If an overtemperature shutdown occurs, the $\overline{\text{OCx}}$ is asserted instantaneously.

Product Folder Link(s): TPS2062-1 TPS2065-1 TPS2066-

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## Current Sense

A sense FET monitors the current supplied to the load. The sense FET measures current more efficiently than conventional resistance methods. When an overload or short circuit is encountered, the current-sense circuitry sends a control signal to the driver. The driver in turn reduces the gate voltage and drives the power FET into its saturation region, which switches the output into a constant-current mode and holds the current constant while varying the voltage on the load.

## Thermal Sense

The TPS206x-1 implements a thermal sensing to monitor the operating temperature of the power distribution switch. In an overcurrent or short-circuit condition the junction temperature rises. When the die temperature rises to approximately 140°C due to overcurrent conditions, the internal thermal sense circuitry turns off the switch, thus preventing the device from damage. Hysteresis is built into the thermal sense, and after the device has cooled approximately 10 degrees, the switch turns back on. The switch continues to cycle off and on until the fault is removed. The open-drain false reporting output ($\overline{OCx}$) is asserted (active low) when an overtemperature shutdown or overcurrent occurs.

## Undervoltage Lockout

A voltage sense circuit monitors the input voltage. When the input voltage is below approximately 2 V, a control signal turns off the power switch.

## Discharge Function

When the device is disabled (when enable is deasserted or during power-up power-down when $V_I$ < UVLO) the discharge function is active. The discharge function offers a resistive discharge path for the external storage capacitor. This is suitable only to discharge filter capacitors for limited time and cannot dissipate steady state currents greater than 8 ma.

## PACKAGING INFORMATION

| Orderable Device | Status [1] | Package Type | Package Drawing | Pins | Package Qty | Eco Plan [2] | Lead/Ball Finish | MSL Peak Temp [3] |
|---|---|---|---|---|---|---|---|---|
| TPS2062D-1 | ACTIVE | SOIC | D | 8 | 75 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| TPS2062D-1G4 | ACTIVE | SOIC | D | 8 | 75 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| TPS2062DR-1 | ACTIVE | SOIC | D | 8 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| TPS2062DR-1G4 | ACTIVE | SOIC | D | 8 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| TPS2065DGN-1 | ACTIVE | MSOP-Power PAD | DGN | 8 | 80 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| TPS2065DGN-1G4 | ACTIVE | MSOP-Power PAD | DGN | 8 | 80 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| TPS2065DGNR-1 | ACTIVE | MSOP-Power PAD | DGN | 8 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| TPS2065DGNR-1G4 | ACTIVE | MSOP-Power PAD | DGN | 8 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| TPS2066DGN-1 | ACTIVE | MSOP-Power PAD | DGN | 8 | 80 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| TPS2066DGN-1G4 | ACTIVE | MSOP-Power PAD | DGN | 8 | 80 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| TPS2066DGNR-1 | ACTIVE | MSOP-Power PAD | DGN | 8 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| TPS2066DGNR-1G4 | ACTIVE | MSOP-Power PAD | DGN | 8 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |

[1] The marketing status values are defined as follows:
**ACTIVE:** Product device recommended for new designs.
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
**OBSOLETE:** TI has discontinued the production of the device.

[2] Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
**TBD:** The Pb-Free/Green conversion plan has not been defined.
**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

[3] MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder

temperature.

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# PACKAGE MATERIALS INFORMATION

## TAPE AND REEL INFORMATION

**REEL DIMENSIONS**

**TAPE DIMENSIONS**

| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**

*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| TPS2062DR-1 | SOIC | D | 8 | 2500 | 330.0 | 12.4 | 6.4 | 5.2 | 2.1 | 8.0 | 12.0 | Q1 |
| TPS2065DGNR-1 | MSOP-Power PAD | DGN | 8 | 2500 | 330.0 | 12.4 | 5.3 | 3.3 | 1.3 | 8.0 | 12.0 | Q1 |
| TPS2066DGNR-1 | MSOP-Power PAD | DGN | 8 | 2500 | 330.0 | 12.4 | 5.3 | 3.3 | 1.3 | 8.0 | 12.0 | Q1 |

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**TAPE AND REEL BOX  DIMENSIONS**



*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|--------|--------------|-----------------|------|-----|-------------|------------|-------------|
| TPS2062DR-1 | SOIC | D | 8 | 2500 | 340.5 | 338.1 | 20.6 |
| TPS2065DGNR-1 | MSOP-PowerPAD | DGN | 8 | 2500 | 346.0 | 346.0 | 35.0 |
| TPS2066DGNR-1 | MSOP-PowerPAD | DGN | 8 | 2500 | 346.0 | 346.0 | 35.0 |

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DGN (S−PDSO−G8)        PowerPAD™ PLASTIC SMALL−OUTLINE PACKAGE



Thermal Pad
(See Note D)

Gauge Plane

0°−8°

Seating Plane

1,10 MAX
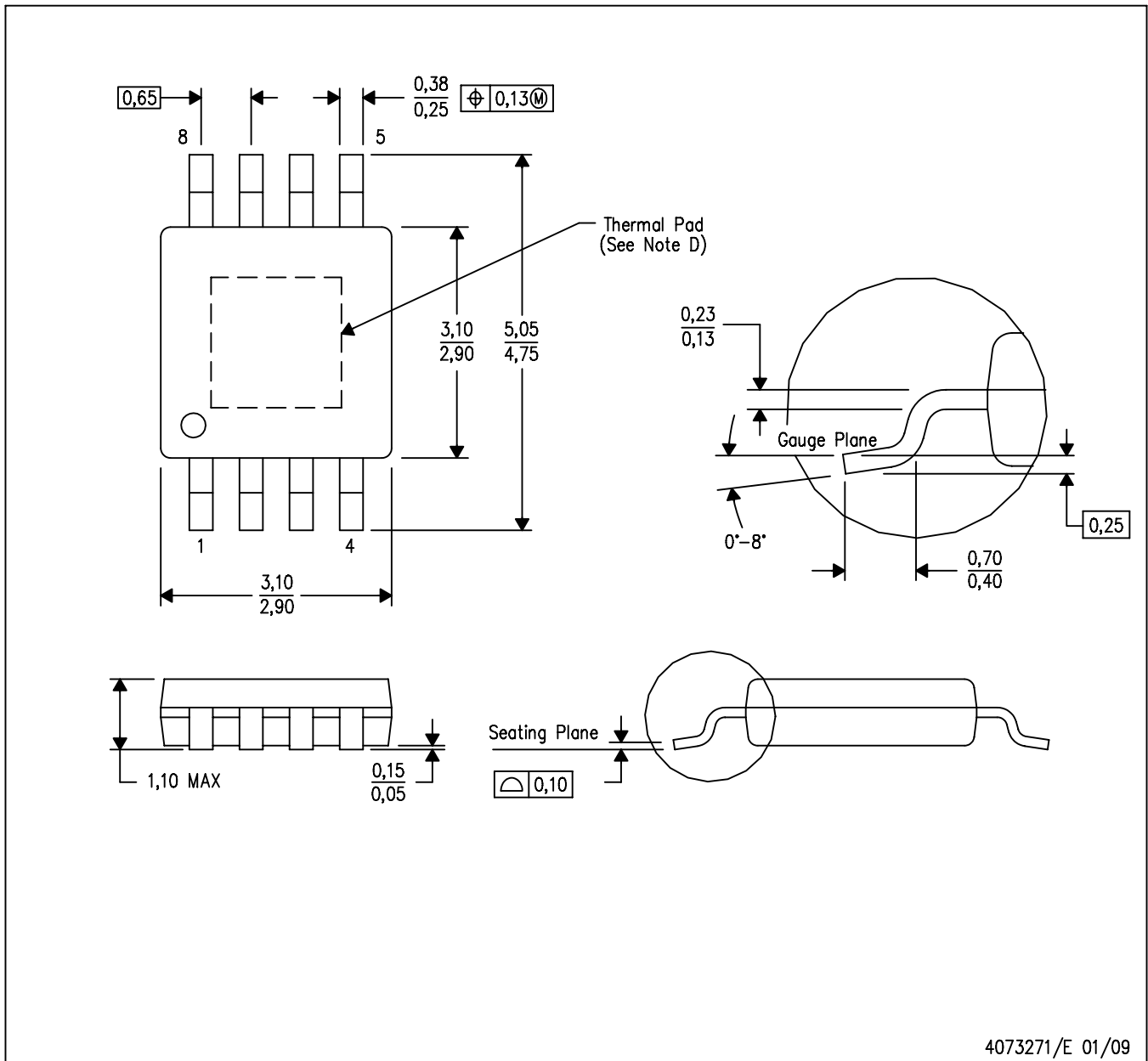
4073271/E 01/09

NOTES:    A.  All linear dimensions are in millimeters.
          B.  This drawing is subject to change without notice.
          C.  Body dimensions do not include mold flash or protrusion.
          D.  This package is designed to be soldered to a thermal pad on the board.  Refer to Technical Brief, PowerPad
              Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding
              recommended board layout.  This document is available at www.ti.com <http://www.ti.com>.
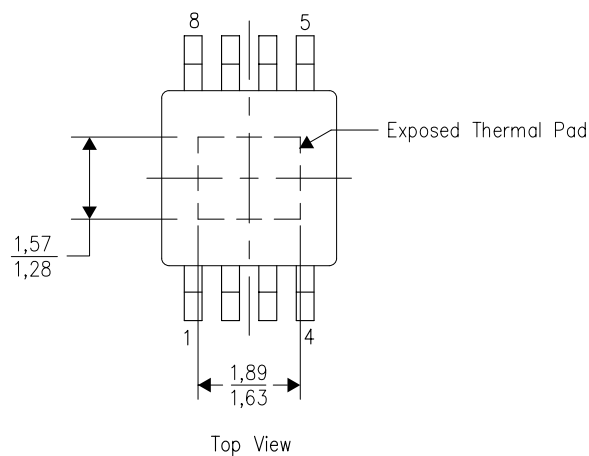          E.  Falls within JEDEC MO−187 variation AA−T

**PowerPAD is a trademark of Texas Instruments.**

## THERMAL INFORMATION

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached to a printed circuit board (PCB). The thermal pad must be soldered directly to the PCB. After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD Made Easy, Texas Instruments Literature No. SLMA004. Both documents are available at www.ti.com.
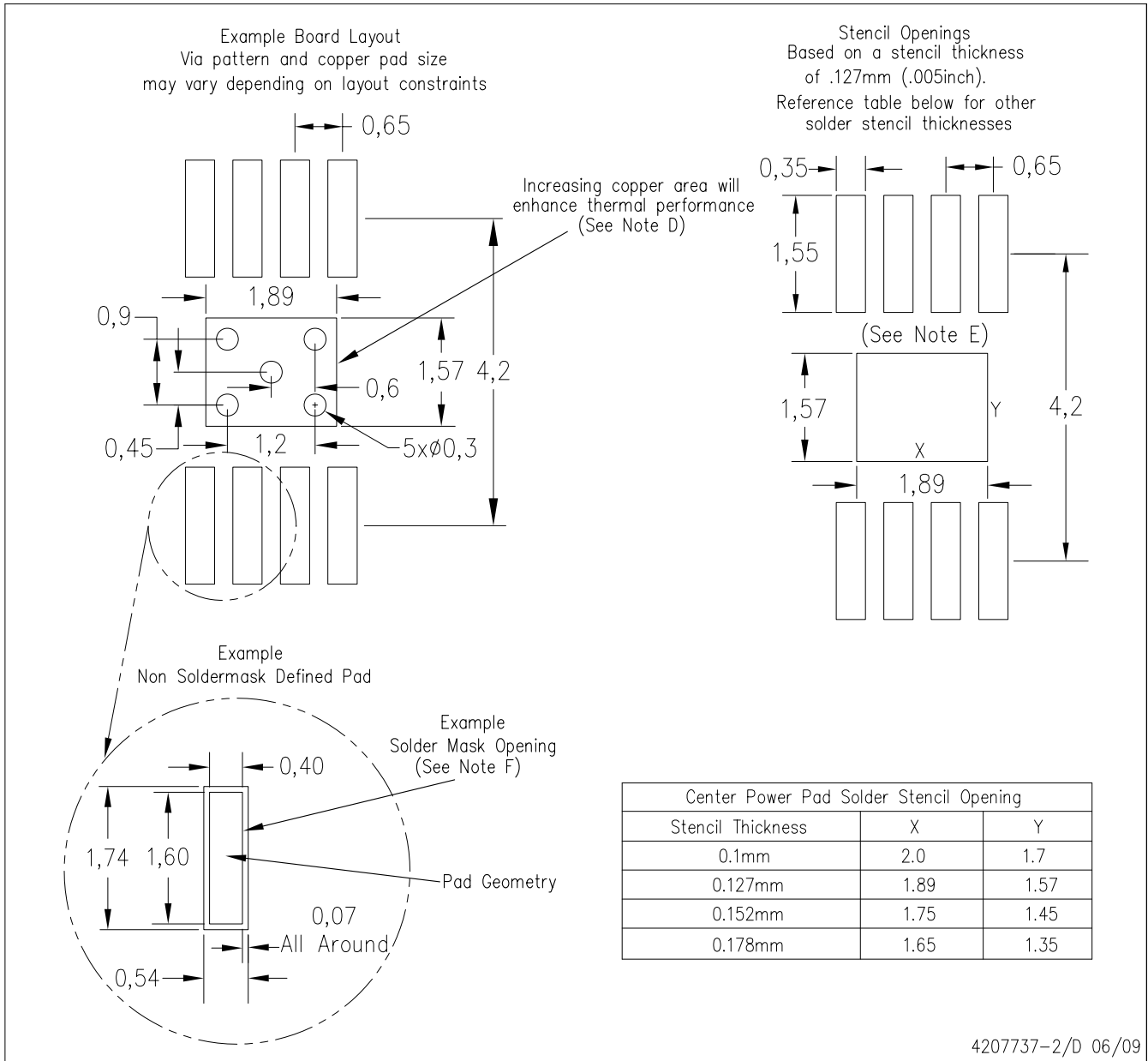
The exposed thermal pad dimensions for this package are shown in the following illustration.



Top View

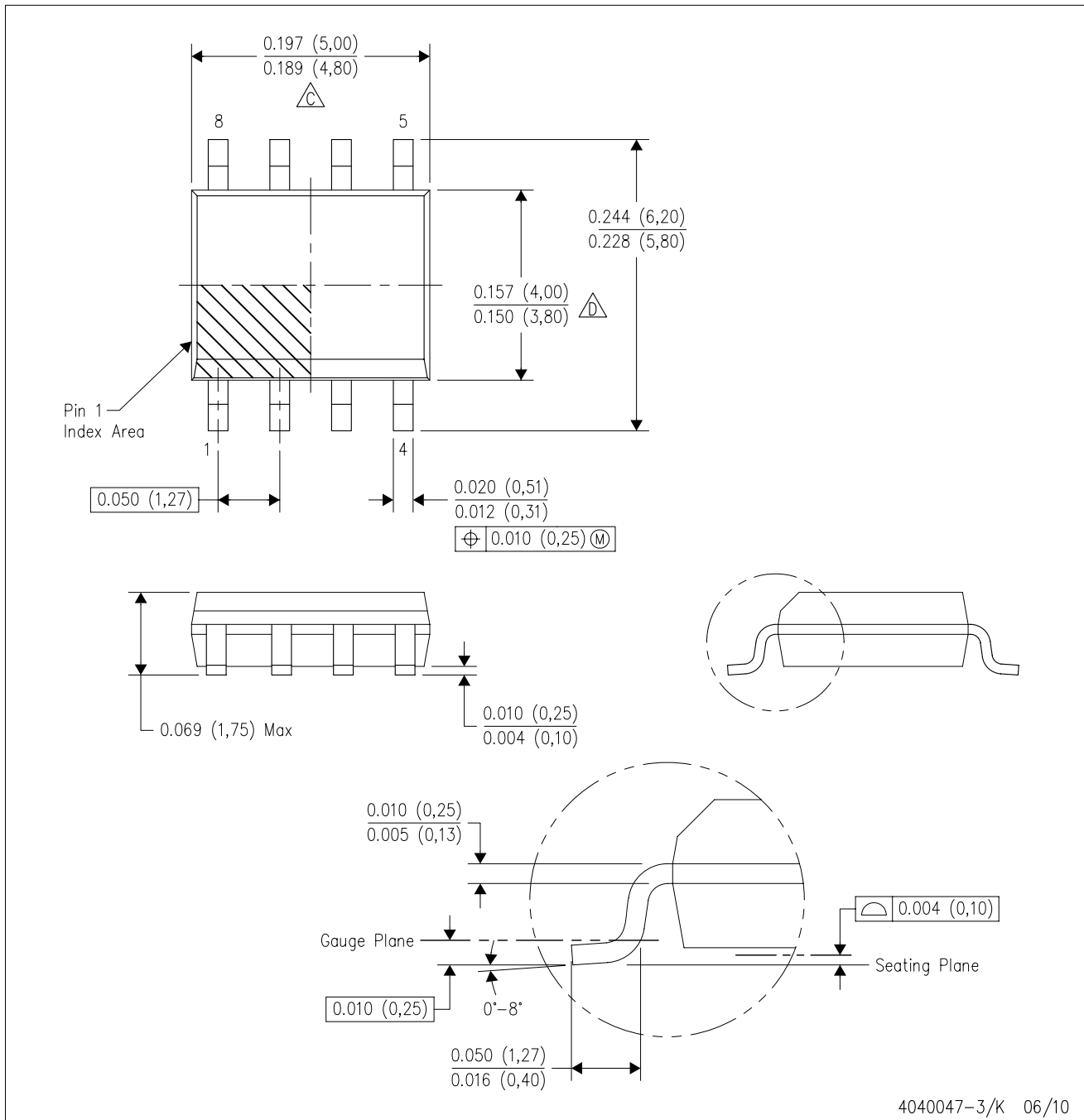NOTE:   All linear dimensions are in millimeters

Exposed Thermal Pad Dimensions

DGN (R-PDSO-G8)  PowerPAD™

Example Board Layout
Via pattern and copper pad size
may vary depending on layout constraints

0,65

Increasing copper area will
enhance thermal performance
(See Note D)

1,89

0,9

1,57  4,2

0,6

0,45     1,2

5x⌀0,3

Stencil Openings
Based on a stencil thickness
of .127mm (.005inch).
Reference table below for other
solder stencil thicknesses

0,35          0,65

1,55

(See Note E)

1,57                Y        4,2

X

1,89

Example
Non Soldermask Defined Pad

Example
Solder Mask Opening
(See Note F)

0,40

1,74  1,60

Pad Geometry

0,07

All Around

0,54

| Center Power Pad Solder Stencil Opening | | |
|---|---|---|
| Stencil Thickness | X | Y |
| 0.1mm | 2.0 | 1.7 |
| 0.127mm | 1.89 | 1.57 |
| 0.152mm | 1.75 | 1.45 |
| 0.178mm | 1.65 | 1.35 |

4207737-2/D 06/09

NOTES:  A.  All linear dimensions are in millimeters.
B.  This drawing is subject to change without notice.
C.  Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
D.  This package is designed to be soldered to a thermal pad on the board.  Refer to Technical Brief, PowerPad
Thermally Enhanced Package, Texas Instruments Literature No. SLMA002, SLMA004, and also the Product Data Sheets
for specific thermal information, via requirements, and recommended board layout.  These documents are available at
www.ti.com <http://www.ti.com>.  Publication IPC-7351 is recommended for alternate designs.
E.  Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release.  Customers should
contact their board assembly site for stencil design recommendations.  Example stencil design based on a 50% volumetric
metal load solder paste.  Refer to IPC-7525 for other stencil recommendations.
F.  Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.
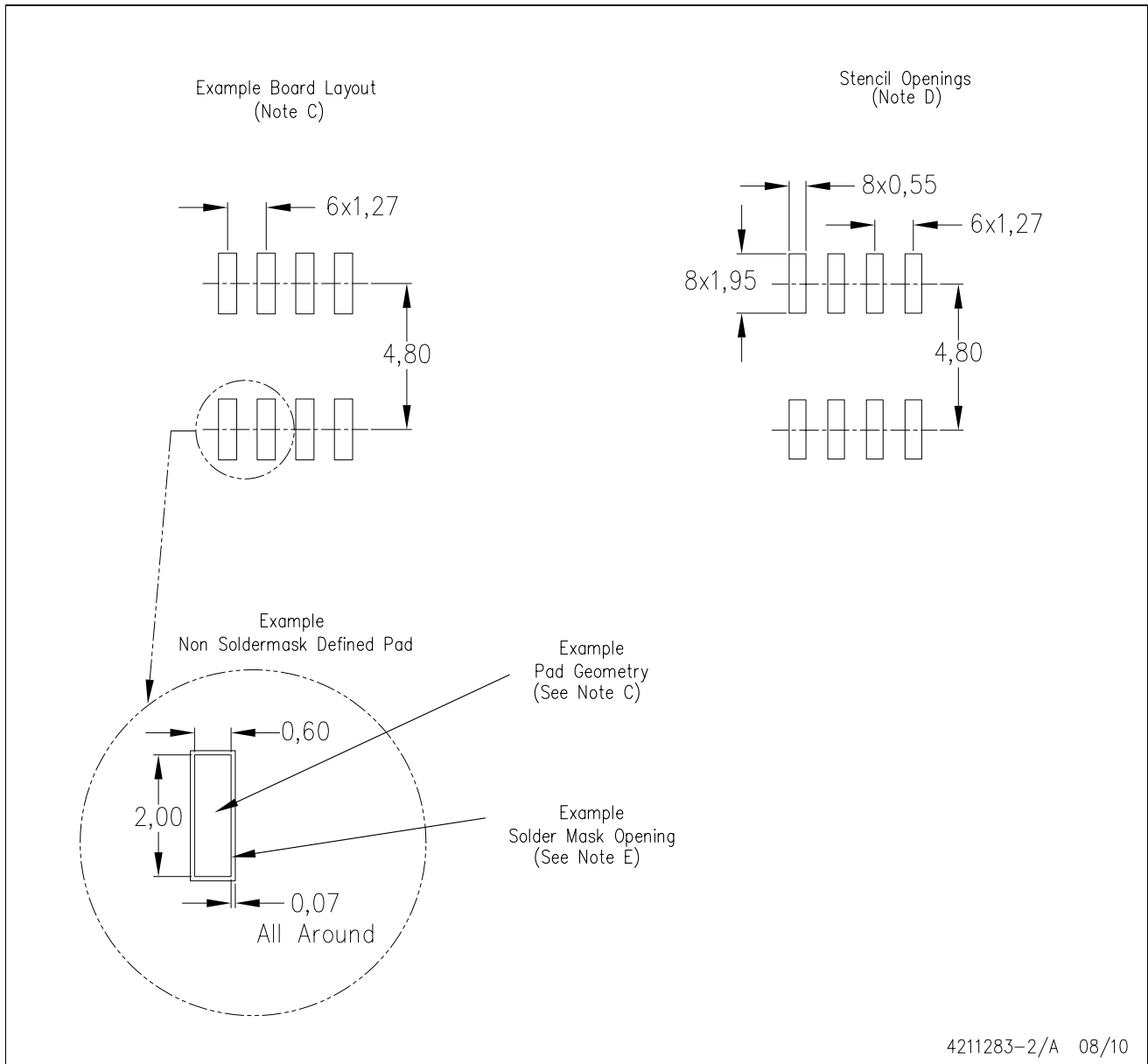
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D (R−PDSO−G8)                    PLASTIC SMALL−OUTLINE PACKAGE

0.197 (5,00)
0.189 (4,80)
C

8        5

0.244 (6,20)
0.228 (5,80)

0.157 (4,00)
0.150 (3,80)
D

Pin 1
Index Area

1        4

0.050 (1,27)

0.020 (0,51)
0.012 (0,31)

⊕ 0.010 (0,25) Ⓜ

0.069 (1,75) Max

0.010 (0,25)
0.004 (0,10)

0.010 (0,25)
0.005 (0,13)

Gauge Plane

0.004 (0,10)

Seating Plane

0.010 (0,25)

0°−8°

0.050 (1,27)
0.016 (0,40)

4040047−3/K   06/10

NOTES:    A.   All linear dimensions are in inches (millimeters).
          B.   This drawing is subject to change without notice.
          C.   Body length does not include mold flash, protrusions, or gate burrs.  Mold flash, protrusions, or gate burrs shall
               not exceed .006 (0,15) per end.
          D.   Body width does not include interlead flash.  Interlead flash shall not exceed .017 (0,43) per side.
          E.   Reference JEDEC MS−012 variation AA.

D (R−PDSO−G8)                    PLASTIC SMALL OUTLINE

Example Board Layout
(Note C)

Stencil Openings
(Note D)

6x1,27

8x0,55

6x1,27

8x1,95

4,80

4,80

Example
Non Soldermask Defined Pad

Example
Pad Geometry
(See Note C)

0,60

2,00

Example
Solder Mask Opening
(See Note E)

0,07
All Around

4211283−2/A   08/10

NOTES:   A.  All linear dimensions are in millimeters.
         B.  This drawing is subject to change without notice.
         C.  Publication IPC−7351 is recommended for alternate designs.
         D.  Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release.  Customers should
             contact their board assembly site for stencil design recommendations. Refer to IPC−7525 for other stencil recommendations.
         E.  Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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