

## FOUR-PORT USB HUB POWER CONTROLLERS

### FEATURES

- Complete USB Hub Power Solution
- Meets USB Specifications 1.1 and 2.0
- Independent Thermal and Short-Circuit Protection
- 3.3-V Regulator for USB Hub Controller
- Overcurrent Logic Outputs
- 4.5-V to 5.5-V Operating Range
- CMOS- and TTL-Compatible Enable Inputs
- 185  $\mu$ A Bus-Power Supply Current
- Available in 32-Pin HTSSOP PowerPAD™ Package
- –40°C to 85°C Ambient Temperature Range

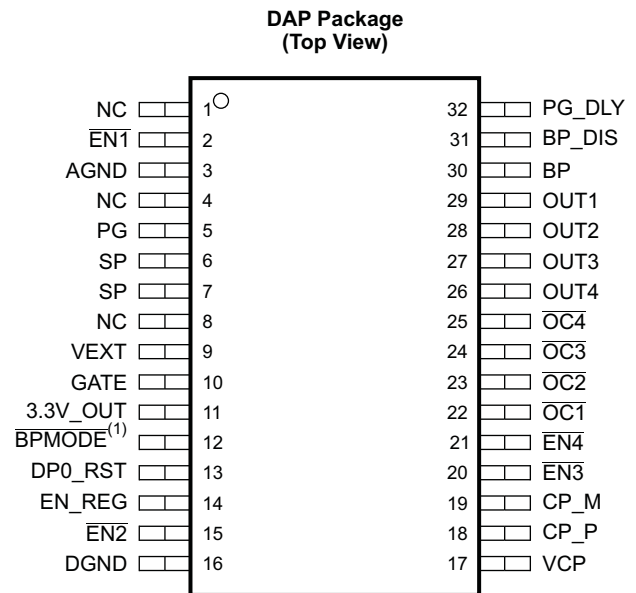
### DESCRIPTION

The TPS2070 and TPS2071 provide a complete USB hub power solution by incorporating four major functions: current-limited power switches for four ports, a 3.3-V 100-mA regulator, a 5-V regulator controller for self-power, and a DP0 line control to signal attach/detach of the hub.

These devices are designed to meet bus-powered and self-powered hub requirements. These devices are also designed for hybrid hub implementations and allow for automatic switching from self-powered mode to bus-powered mode if loss of self-power is experienced (can be disabled by applying a logic high to BP\_DIS).

Each port has a current-limited 107-m $\Omega$  N-channel MOSFET high-side power switch for 500-mA self-powered operation. Each port also has a current-limited 560-m $\Omega$  N-channel MOSFET high-side power switch for 100-mA bus-powered operation. All the N-channel MOSFETs are designed without parasitic diodes, preventing current backflow into the inputs.

For applications not requiring a 5-V regulator controller, use the TPS2074 or TPS2075 device.



NC - No internal connection

P0073-01

- (1) Pin 12 is active-low ( $\overline{\text{BPMODE}}$ ) for TSS2070 and active-high (BPMODE) for TPS2071.<sup>(1)</sup>

GENERAL SWITCH CATALOG						
33 m $\Omega$ , Single 	80 m $\Omega$ , Single 	80 m $\Omega$ , Dual 	80 m $\Omega$ , Dual 	80 m $\Omega$ , Triple 	80 m $\Omega$ , Quad 	80 m $\Omega$ , Quad 
TPS201xA 0.2 A to 2 A TPS202x 0.2 A to 2 A TPS203x 0.2 A to 2 A	TPS2014 600 mA TPS2015 1 A TPS2041B 500 mA TPS2051B 500 mA TPS2045A 250 mA TPS2049 100 mA TPS2055A 250 mA TPS2061 1 A TPS2065 1 A TPS2068 1.5 A TPS2069 1.5 A	TPS2042B 500 mA TPS2052B 500 mA TPS2046B 250 mA TPS2056 250 mA TPS2062 1 A TPS2066 1 A TPS2060 1.5 A TPS2064 1.5 A	TPS2080 500 mA TPS2081 500 mA TPS2082 500 mA TPS2090 250 mA TPS2091 250 mA TPS2092 250 mA	TPS2043B 500 mA TPS2053B 500 mA TPS2047B 250 mA TPS2057A 250 mA TPS2063 1 A TPS2067 1 A	TPS2044B 500 mA TPS2054B 500 mA TPS2048A 250 mA TPS2058 250 mA	TPS2085 500 mA TPS2086 500 mA TPS2087 500 mA TPS2095 250 mA TPS2096 250 mA TPS2097 250 mA



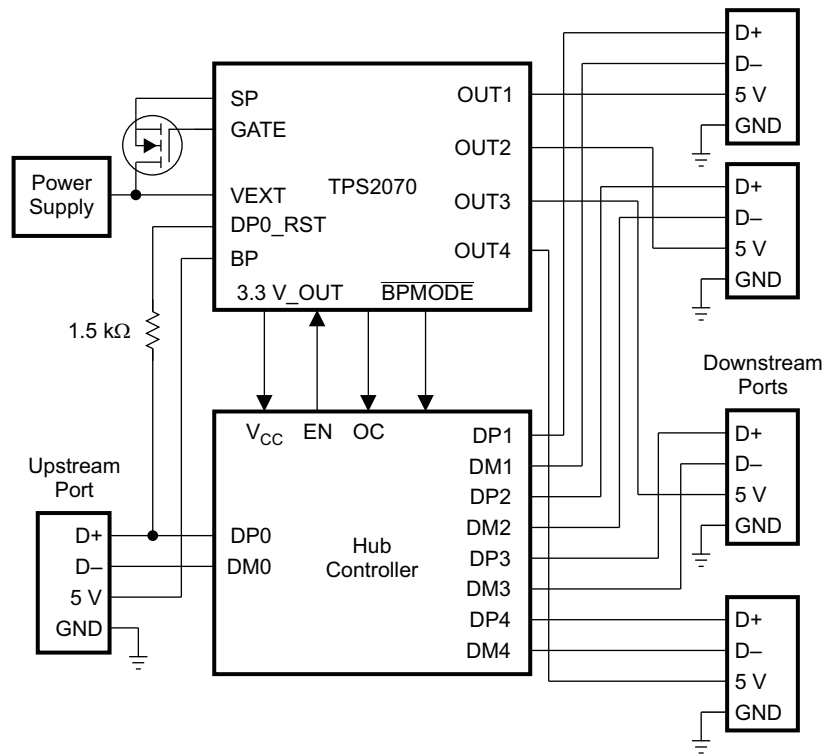
Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

PowerPAD is a trademark of Texas Instruments.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of the Texas Instruments standard warranty. Production process may not necessarily include testing of all parameters.

Copyright © 2000–2007 Texas Instruments Incorporated

Simplified Hybrid-Hub Diagram<sup>(1)</sup>



B0269-01

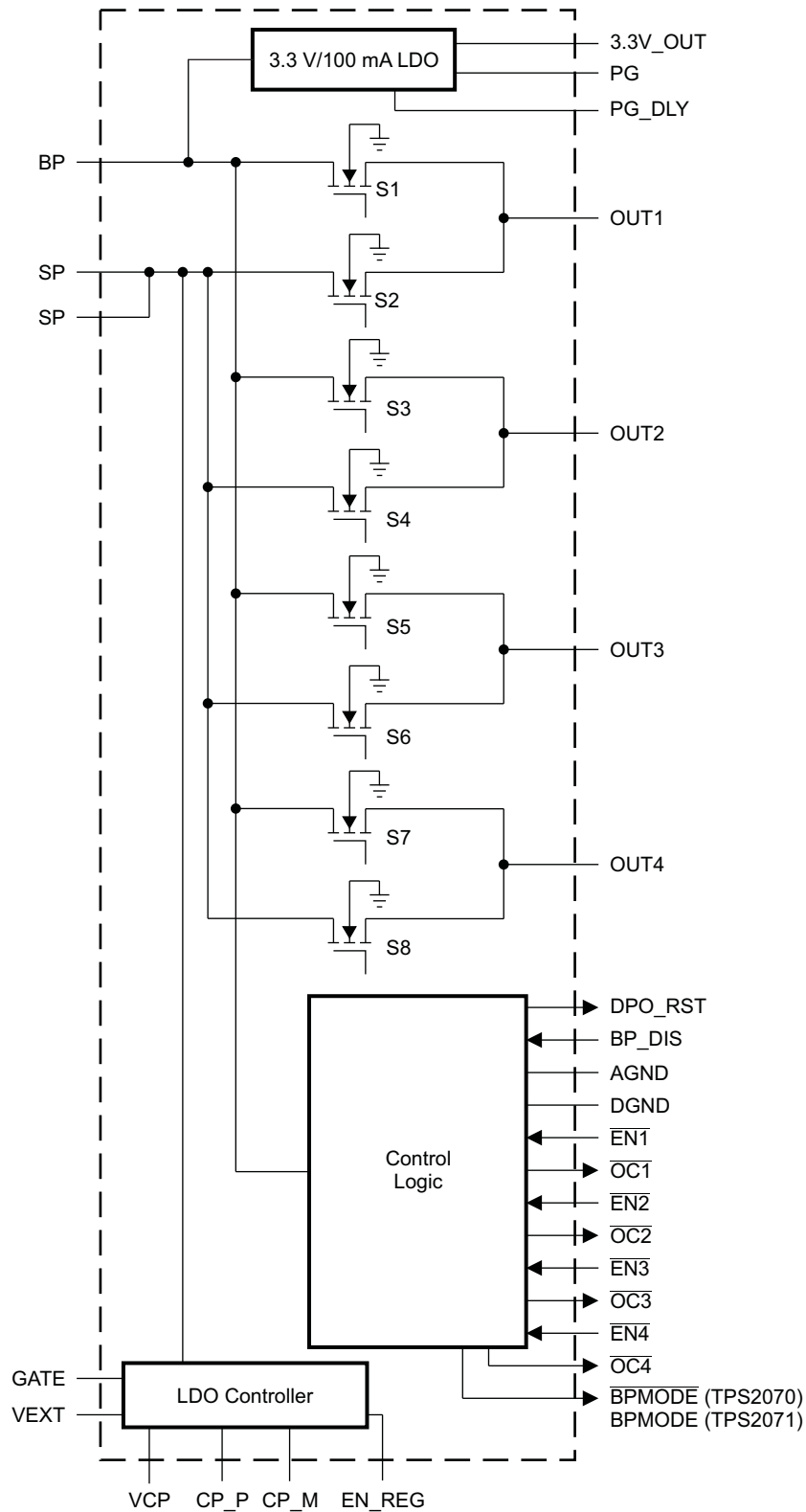
(1) See Figure 38 for complete implementation.

SELECTION GUIDE

T <sub>A</sub>	USB HUB POWER CONTROLLERS	PACKAGED DEVICES			
		PIN COUNT	BP MODE	HTSSOP (DAP) <sup>(1)</sup>	SSOP (DB)
–40°C to 85°C	Four-port with internal LDO controller	32	Active low	TPS2070DAP	—
			Active high	TPS2071DAP	—
	Four-port without internal LDO controller	24	Active low	—	TPS2074DB
			Active high	—	TPS2075DB

(1) The DAP package is available taped and reeled. Add an R suffix to the device type (e.g., TPS2070DAPR).

FUNCTIONAL BLOCK DIAGRAM



B0270-01

## TERMINAL FUNCTIONS

TERMINAL		I/O	DESCRIPTION
NAME	NO.		
3.3V_OUT	11	O	3.3-V internal voltage regulator output
AGND	3		Analog ground
BP	30	I	Bus power voltage input, connect to V <sub>BUS</sub>
BP_DIS	31	I	Active-high logic input, disables autoswitch to bus power when self-power is disconnected. Connect to BP or GND
$\overline{\text{BPMODE}}$ <sup>(1)</sup>	12	O	A logic signal that indicates if the outputs source from the bus-powered supply. $\overline{\text{BPMODE}}$ (TPS2070) or BPMODE (TPS2071) can be used to signal hub controller.
CP_M	19		Charge-pump-capacitor connection from CP_P. Recommend 0.01- $\mu\text{F}$ between CP_P and CP_M.
CP_P	18		Charge-pump-capacitor connection from CP_M. Recommend 0.01- $\mu\text{F}$ between CP_P and CP_M.
DGND	16		Digital ground
DP0_RST	13	O	Connects to DP signal from upstream hub/host through an external 1.5-k $\Omega$ resistor
$\overline{\text{EN1}}$	2	I	Active-low enable for OUT1
$\overline{\text{EN2}}$	15	I	Active-low enable for OUT2
$\overline{\text{EN3}}$	20	I	Active-low enable for OUT3
$\overline{\text{EN4}}$	21	I	Active-low enable for OUT4
EN_REG	14	I	Active-high enable, enables external voltage regulator. Connect to BP or GND
GATE	10	O	Output gate drive for an external N-channel MOSFET
NC	1, 4, 8		No internal connection
$\overline{\text{OC1}}$	22	O	Logic output, overcurrent response for OUT1
$\overline{\text{OC2}}$	23	O	Logic output, overcurrent response for OUT2
$\overline{\text{OC3}}$	24	O	Logic output, overcurrent response for OUT3
$\overline{\text{OC4}}$	25	O	Logic output, overcurrent response for OUT4
OUT1	29	O	Power switch output for downstream ports
OUT2	28	O	Power switch output for downstream ports
OUT3	27	O	Power switch output for downstream ports
OUT4	26	O	Power switch output for downstream ports
PG	5	O	Logic output, power good
PG_DLY <sup>(2)</sup>	32		Adjusts the PG time delay with a capacitor to ground. Adjust the pulse duration to fit the application.
SP	6, 7	I	Self-power voltage input, connects to local power supply
VCP	17		Charge-pump output, source for an external voltage-regulator driver. Recommend 0.1- $\mu\text{F}$ capacitor to DGND.
VEXT	9	I	Input voltage for the external voltage regulator

(1) Pin 12 is active-low for TPS2070 and active-high for TPS2071.

(2) Use the following formula to calculate the capacitance needed:  $C = (\text{desired pulse duration} \times 3 \times 10^{-6})/1.22$

## DETAILED DESCRIPTION

### BP

The bus-powered supply input (BP) serves as the source for the internal 3.3-V LDO and for all logic functions in the device. In bus-powered mode, BP also serves as the source for all the outputs (OUTx). If BP is below the undervoltage threshold, all power switches turn off and the LDO is disabled. BP must be connected to a voltage source for the device to operate.

### SP

The self-powered supply input (SP) serves as the source for all the outputs (OUTx) in self-powered mode. The enable logic for the SP switches requires that BP be connected to a voltage source.

### OUT1, OUT2, OUT3, OUT4

OUTx are the outputs of the integrated power switches.

### 3.3V\_OUT

The internal 3.3-V LDO output can be used to supply up to 100 mA of current to low-power functions, such as hub controllers.

### VEXT

VEXT is used to generate a 5-V source for the SP input by using the internal LDO controller and an external N-channel MOSFET. This pin connects to a 6-V to 9-V power supply and to the drain of the MOSFET if the external LDO is needed.

### GATE

GATE is the output of the 5-V LDO controller and connects to the gate of the external MOSFET.

### EN\_REG

The active-high input, EN\_REG, is used to enable the 5-V regulator controller. EN\_REG is compatible with TTL and CMOS logic levels.

### DP0\_RST

DP0\_RST functions as a hub reset when a 1.5-k $\Omega$  resistor is connected between DP0\_RST and the upstream DP0 data line in a hub system. To provide a clean attach signal on the DP0 data line, the DP0\_RST output goes low momentarily (because of the upstream pulldown resistor) to discharge any parasitic charge on the cable, then goes to the high-impedance state and finally outputs a high signal. The low and Hi-Z pulse durations are adjustable using a capacitor between PG\_DLY and ground, and are approximately 50% of the power-good time delay. Detachment is signaled by a Hi-Z on DP0\_RST. Both DP0\_RST and PG transition high at the same time.

### Power Good (PG)

The power-good (PG) function serves as a reset for a USB hub controller. PG is asserted low when the output voltage on the internal voltage regulator is below a fixed threshold. A time delay to ensure a stable output voltage before PG goes high is adjustable using a small-value ceramic capacitor from PG\_DLY to ground.

### PG\_DLY

PG\_DLY connects to an external capacitor to adjust the time delay for PG and DP0\_RST. For USB applications, a 0.1- $\mu$ F capacitor is recommended; however, see the USB hub controller data sheet to determine the required pulse-duration criteria.

### BP\_DIS

BP\_DIS is used to enable or disable the autoswitching function between bus-powered mode and self-powered mode. When BP\_DIS is connected low and the voltage on SP is greater than the undervoltage-lockout (UVLO) threshold, the device switches to self-powered operation automatically; if the SP voltage falls lower than the UVLO threshold, the device switches to bus-powered operation. When BP\_DIS is connected high, the autoswitching function is disabled and the device does not autoswitch to bus-powered operation if the SP voltage is below the UVLO threshold.

### BPMODE or BPMODE

BPMODE (TPS2070) or BPMODE (TPS2071) is an output that signals when the device is in bus-powered mode. The logic state is set according to the voltages on BP, SP, and BP\_DIS. For the TPS2070, BPMODE outputs a low signal to indicate bus-powered mode or a high signal to indicate self-powered mode. For the TPS2071, BPMODE outputs a high signal to indicate bus-powered mode or a low signal to indicate self-powered mode. This output can be used to inform a USB hub controller to configure for bus-powered mode or self-powered mode.

## $\overline{OC1}$ , $\overline{OC2}$ , $\overline{OC3}$ , $\overline{OC4}$

$\overline{OCx}$  is an output signal that is asserted (active low) when an overcurrent or overtemperature condition is encountered for the corresponding channel.  $\overline{OCx}$  remains asserted until the overcurrent or overtemperature condition is removed.

## $\overline{EN1}$ , $\overline{EN2}$ , $\overline{EN3}$ , $\overline{EN4}$

The active-low logic input  $\overline{ENx}$  enables or disables the power switches in the device. The enable input is compatible with both TTL and CMOS logic levels. The switches do not turn on until 3.3V\_OUT is above the PG threshold.

## ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted)<sup>(1) (2)</sup>

		VALUE	UNIT
Input voltage range	$V_{I(BP)}$ , $V_{I(SP)}$ , $V_{I(ENx)}$ , $V_{I(EN\_REG)}$ , $V_{I(BP\_DIS)}$	–0.3 to 6	V
	$V_{I(VEXT)}$	–0.3 to 10	V
Output voltage range	$V_{O(OUTx)}$ , $V_{O(3.3V\_OUT)}$ , $V_{O(PG\_DLY)}$ , $V_{O(OCx)}$ , $V_{O(BPMODE)}$ , $V_{O(DP0\_RST)}$ , $V_{O(PG)}$	–0.3 to 6	V
	$V_{O(GATE)}$ , $V_{O(CP\_M)}$ , $V_{O(CP\_P)}$ , $V_{O(VCP)}$	–0.3 to 15	V
Continuous output current	$I_{O(OUTx)}$	Internally limited	
	$I_{O(3.3V\_OUT)}$	Internally limited	
Maximum output current	$I_{O(VCP)}$	±30	mA
	$I_{O(BPMODE)}$ or $I_{O(BPMODE)}$ , $I_{O(DP0\_RST)}$ , $I_{O(PG)}$ , $I_{O(OCx)}$	±10	mA
	$I_{O(GATE)}$ , sourcing	700	µA
	$I_{O(GATE)}$ , sinking	–2.2	mA
Continuous total power dissipation		See Dissipation Rating Table	
Operating virtual junction temperature range, $T_J$		–40 to 125	°C
Storage temperature range, $T_{stg}$		–65 to 150	°C
Lead temperature (soldering), 1.6 mm (1/16 inch) from case for 10 seconds		260	°C

- (1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) All voltages are with respect to GND.

## DISSIPATION RATINGS

PACKAGE	$T_A \leq 25^\circ\text{C}$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25^\circ\text{C}$	$T_A = 70^\circ\text{C}$ POWER RATING	$T_A = 85^\circ\text{C}$ POWER RATING
32-DAP	1162.8 mW	11.6 mW/°C	639.5 mW	465.1 mW
32-DAP <sup>(1)</sup>	4255.3 mW	42.5 mW/°C	2340.4 mW	1702.1 mW

- (1) Using thermal pad as heatsink.

## RECOMMENDED OPERATING CONDITIONS

			MIN	MAX	UNIT
$V_{I(BP)}$	Input voltage		4.5	5.5	V
$V_{I(SP)}$			0	5.5	
$V_{I(VEXT)}$			0	9	
$V_{I(BP\_DIS)}$			0	5.5	
$V_{I(EN\bar{x})}$			0	5.5	
$V_{I(EN\_REG)}$			0	5.5	
$I_O$	Continuous output current	BP to OUTx (per switch)		100	mA
		SP to OUTx (per switch)		500	
		BP to 3.3V_OUT		100	
$T_J$	Operating virtual junction temperature		-40	125	°C

## ELECTRICAL CHARACTERISTICS

over recommended operating junction temperature range,  $4.5\text{ V} \leq V_{I(\text{BP})} \leq 5.5\text{ V}$ ,  $4.85\text{ V} \leq V_{I(\text{SP})} \leq 5.5\text{ V}$ ,  $6\text{ V} \leq V_{I(\text{VEXT})} \leq 9\text{ V}$ ,  $\overline{\text{EN}}\text{x} = 0\text{ V}$ ,  $\text{EN\_REG} = 0\text{ V}$ ,  $\text{BP\_DIS} = 0\text{ V}$  (unless otherwise noted)

PARAMETER		TEST CONDITIONS <sup>(1)</sup>		MIN	TYP	MAX	UNIT	
<b>INPUT CURRENT</b>								
$I_{I(\text{BP})}$	Input current at BP, switches disabled	No load on OUTx and 3.3V_OUT, $\overline{\text{EN}}\text{x} = V_{I(\text{BP})}$	$V_{I(\text{SP})} = \text{Hi-Z}$	185	240	$\mu\text{A}$		
			$V_{I(\text{SP})} = 0\text{ V}$	185	240			
			$V_{I(\text{SP})} = 5\text{ V}$	175	210			
	Input current at BP, switches enabled	No load on OUTx and 3.3V_OUT, $\overline{\text{EN}}\text{x} = 0\text{ V}$	$V_{I(\text{SP})} = \text{Hi-Z}$	185	240	$\mu\text{A}$		
			$V_{I(\text{SP})} = 0\text{ V}$	185	240			
			$V_{I(\text{SP})} = 5\text{ V}$	175	210			
$I_{I(\text{SP})}$	Input current at SP, switches disabled	No load on OUTx and 3.3V_OUT, $\overline{\text{EN}}\text{x} = V_{I(\text{SP})}$	$V_{I(\text{SP})} = \text{Hi-Z}$	90	115	$\mu\text{A}$		
			$V_{I(\text{SP})} = 0\text{ V}$	90	115			
			$V_{I(\text{SP})} = 5\text{ V}$	115	140			
	Input current at SP, switches enabled	No load on OUTx and 3.3V_OUT, $\overline{\text{EN}}\text{x} = 0\text{ V}$	$V_{I(\text{SP})} = \text{Hi-Z}$	90	115	$\mu\text{A}$		
			$V_{I(\text{SP})} = 0\text{ V}$	90	115			
			$V_{I(\text{SP})} = 5\text{ V}$	115	140			
$I_{I(\text{VEXT})}$	Input current at VEXT, LDO controller disabled	$V_{I(\text{EN\_REG})} = 0\text{ V}$ or Hi-Z, $V_{I(\text{BP})} = 5\text{ V}$ , $V_{I(\text{SP})} = \text{Hi-Z}$		200	360	$\mu\text{A}$		
	Input current, at VEXT, LDO controller enabled	$V_{I(\text{EN\_REG})} = 5\text{ V}$ , $V_{I(\text{BP})} = 5\text{ V}$ , $V_{I(\text{SP})} = \text{Hi-Z}$			10	$\text{mA}$		
<b>POWER SWITCHES</b>								
$r_{\text{DS(on)}}$	Static drain-source on-state resistance	SP to OUTx	$V_{I(\text{SP})} = V_{I(\text{BP})} = 5\text{ V}$ , $I_{\text{Ox}} = 0.5\text{ A}$	$T_{\text{A}} = 25^{\circ}\text{C}$	107	$\text{m}\Omega$		
			$T_{\text{A}} = 70^{\circ}\text{C}$	125	160			
		BP to OUTx	$V_{I(\text{BP})} = 4.5\text{ V}$ , $V_{I(\text{SP})} = \text{open}$ , $I_{\text{Ox}} = 0.1\text{ A}$	$T_{\text{A}} = 25^{\circ}\text{C}$	560			
			$T_{\text{A}} = 70^{\circ}\text{C}$	630	900			
$I_{\text{lk}}(\text{OUTx})$	Leakage current at OUTx			$\overline{\text{EN}}\text{x} = V_{I(\text{BP})} = 5.5\text{ V}$ , $V_{I(\text{SP})} = \text{Hi-Z}$ , OUTx connected to ground, $V_{I(\text{VIN})} = \text{Hi-Z}$ , no load on 3.3V_OUT	$T_{\text{J}} = 25^{\circ}\text{C}$	0.5	10	
				$\overline{\text{EN}}\text{x} = V_{I(\text{BP})} = V_{I(\text{SP})} = 5.5\text{ V}$ , OUTx connected to ground, $V_{I(\text{VEXT})} = \text{Hi-Z}$ , no load on 3.3V_OUT	$T_{\text{J}} = 25^{\circ}\text{C}$	0.5	10	
				$\overline{\text{EN}}\text{x} = V_{I(\text{BP})} = \text{Hi-Z}$ or $0\text{ V}$ , $V_{I(\text{VEXT})} = V_{I(\text{SP})} = V_{I(\text{OUTx})} = 5.5\text{ V}$ , no load on 3.3V_OUT	$T_{\text{J}} = 25^{\circ}\text{C}$	0.5	10	
				$\overline{\text{EN}}\text{x} = V_{I(\text{BP})} = V_{I(\text{SP})} = \text{Hi-Z}$ or $0\text{ V}$ , $V_{I(\text{VEXT})} = V_{I(\text{OUTx})} = 5.5\text{ V}$ , no load on 3.3V_OUT	$T_{\text{J}} = 25^{\circ}\text{C}$	0.5	10	
				$\overline{\text{EN}}\text{x} = V_{I(\text{BP})} = V_{I(\text{SP})} = V_{I(\text{VEXT})} = \text{Hi-Z}$ or $0\text{ V}$ , $V_{I(\text{OUTx})} = 5.5\text{ V}$ , no load on 3.3V_OUT	$T_{\text{J}} = 25^{\circ}\text{C}$	0.5	10	
$I_{\text{OS}}$	Short-circuit output current <sup>(1)</sup>			$V_{I(\text{BP})} = V_{I(\text{SP})} = 5\text{ V}$ , OUTx connected to GND, device enabled into short circuit		0.6	0.9	1.2
				$V_{I(\text{BP})} = 5\text{ V}$ , $V_{I(\text{SP})} = \text{open}$ , OUTx connected to GND, device enabled into short circuit		0.12	0.2	0.3

(1) Pulse-testing techniques maintain junction temperature close to ambient temperature; thermal effects must be taken into account separately.



## ELECTRICAL CHARACTERISTICS

over recommended operating junction temperature range,  $4.5\text{ V} \leq V_{I(\text{BP})} \leq 5.5\text{ V}$ ,  $4.85\text{ V} \leq V_{I(\text{SP})} \leq 5.5\text{ V}$ ,  $6\text{ V} \leq V_{I(\text{VEXT})} \leq 9\text{ V}$ ,  $\overline{\text{EN}}\text{x} = 0\text{ V}$ ,  $\text{EN\_REG} = 0\text{ V}$ ,  $\text{BP\_DIS} = 0\text{ V}$  (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
<b>INPUT SIGNALS (<math>\overline{\text{EN}}\text{x}</math>, <math>\text{EN\_REG}</math>, <math>\text{BP\_DIS}</math>)</b>						
$V_{\text{IH}}$	High-level input voltage		2			V
$V_{\text{IL}}$	Low-level input voltage				0.8	
$I_{\text{i}}$	Input current	Pullup	$\overline{\text{EN}}\text{x}$ (active-low)	$V_{I(\overline{\text{EN}}\text{x})} = 0\text{ V}$		5
		Pulldown	$\text{EN\_REG}$ (active-high)	$V_{I(\text{EN\_REG})} = 5\text{ V}$		5
			$\text{BP\_DIS}$ (active-high)	$V_{I(\text{BP\_DIS})} = 5\text{ V}$		5

## ELECTRICAL CHARACTERISTICS

over recommended operating junction temperature range,  $4.5\text{ V} \leq V_{I(\text{BP})} \leq 5.5\text{ V}$ ,  $4.85\text{ V} \leq V_{I(\text{SP})} \leq 5.5\text{ V}$ ,  $6\text{ V} \leq V_{I(\text{VEXT})} \leq 9\text{ V}$ ,  $\overline{\text{EN}}\text{x} = 0\text{ V}$ ,  $\text{EN\_REG} = 0\text{ V}$ ,  $\text{BP\_DIS} = 0\text{ V}$  (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
<b>OUTPUT SIGNALS (<math>\overline{\text{BPMODE}}</math> or <math>\text{BPMODE}</math>, <math>\overline{\text{OC}}\text{x}</math>, <math>\text{DPO\_RST}</math>)</b>						
$V_{\text{OH}}$	High-level output voltage	$\overline{\text{BPMODE}}$	$4.25\text{ V} \leq V_{I(\text{BP})} \leq 5.5\text{ V}$ , $4.5\text{ V} \leq V_{I(\text{SP})} \leq 5.5\text{ V}$	$I_{\text{O}} = 2\text{ mA}$	2.4	V
		$\text{BPMODE}$	$4.25\text{ V} \leq V_{I(\text{BP})} \leq 5.5\text{ V}$ , $V_{I(\text{SP})} < 4\text{ V}$		2.4	
		$\overline{\text{OC}}\text{x}$	$4.25\text{ V} \leq V_{I(\text{BP})} \leq 5.5\text{ V}$ , $V_{I(\overline{\text{EN}}\text{x})} = 3.3\text{ V}$ or Hi-Z		2.4	
		$\text{DPO\_RST}$	$4.25\text{ V} \leq V_{I(\text{BP})} \leq 5.5\text{ V}$ , $V_{I(\text{PG\_DLY})} = 3.3\text{ V}$		2.4	
$V_{\text{OL}}$	Low-level output voltage	$\overline{\text{BPMODE}}$	$4.25\text{ V} \leq V_{I(\text{BP})} \leq 5.5\text{ V}$ , $V_{I(\text{SP})} < 4\text{ V}$	$I_{\text{O}} = 3.2\text{ mA}$		0.4
		$\text{BPMODE}$	$4.25\text{ V} \leq V_{I(\text{BP})} \leq 5.5\text{ V}$ , $4.5\text{ V} \leq V_{I(\text{SP})} \leq 5.5\text{ V}$			0.4
		$\overline{\text{OC}}\text{x}$	$4.25\text{ V} \leq V_{I(\text{BP})} \leq 5.5\text{ V}$ , $\text{OUTx} = 0\text{ V}$		$I_{\text{O}(\overline{\text{OC}}\text{x})} = 3.2\text{ mA}$	
$V_{I(\text{BP})}$	Minimum input voltage at BP for low-level output		$I_{\text{O}} = 300\text{ }\mu\text{A}$ , $V_{\text{O}(\overline{\text{BPMODE}})} \leq 0.4\text{ V}$			1.5
			$I_{\text{O}} = 300\text{ }\mu\text{A}$ , $V_{\text{O}(\overline{\text{BPMODE}})} \leq 0.4\text{ V}$ , $V_{I(\text{SP})} = 5\text{ V}$			1.5
$I_{\text{ikg}}$	Hi-Z leakage current at $\text{DPO\_RST}$		$0\text{ V} \leq V_{I(\text{DPO\_RST})} \leq 3.3\text{ V}$ , $V_{I(\text{SP})} = 0\text{ V}$ , $V_{I(\text{BP})} = 5.5\text{ V}$ , $V_{I(\text{PG\_DLY})} = 0.9\text{ V}$		-5	5
$t_{\text{d}}$	Overcurrent response delay time <sup>(1)</sup>				1	10
<b>UNDERVOLTAGE LOCKOUT (SP, BP, VEXT)</b>						
Start threshold	SP					4.5
	BP	$V_{I(\text{SP})} = \text{Hi-Z}$				4.25
	VEXT					3
Stop threshold	SP				4	V
	BP				3.75	
	VEXT				2.5	
$V_{\text{hys}}$	Hysteresis voltage <sup>(1)</sup>	SP				300
		BP				300
		VEXT				150

(1) Specified by design, not tested in production.

## ELECTRICAL CHARACTERISTICS

over recommended operating junction temperature range,  $4.5\text{ V} \leq V_{I(\text{BP})} \leq 5.5\text{ V}$ ,  $4.85\text{ V} \leq V_{I(\text{SP})} \leq 5.5\text{ V}$ ,  $6\text{ V} \leq V_{I(\text{VEXT})} \leq 9\text{ V}$ ,  $\overline{\text{EN}}_x = 0\text{ V}$ ,  $\text{EN\_REG} = 0\text{ V}$ ,  $\text{BP\_DIS} = 0\text{ V}$ ,  $C_{L(3.3V\_OUT)} = 10\text{ }\mu\text{F}$  (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
<b>INTERNAL VOLTAGE REGULATOR</b>						
$V_O$	Output voltage, dc	$V_{I(\text{BP})} = 4.25\text{ V to } 5.5\text{ V}$ , $I_O = 5\text{ mA to } 100\text{ mA}$	3.2	3.3	3.4	V
	Dropout voltage	$I_O = 100\text{ mA}$		0.6		V
	Line regulation	$V_{I(\text{BP})} = 4.25\text{ V to } 5.25\text{ V}$ , $I_O = 5\text{ mA}$			0.1	%/V
	Load regulation	$V_{I(\text{BP})} = 4.25\text{ V}$ , $I_O = 5\text{ mA to } 100\text{ mA}$			0.6%	
$I_{OS}$	Short-circuit current limit <sup>(1)</sup>	$V_{I(\text{BP})} = 4.25\text{ V}$ , 3.3V_OUT connected to GND	0.12	0.2	0.3	A
	Pulldown current through transistor at 3.3V_OUTPUT <sup>(2)</sup>	$V_{I(3.3V\_OUT)} = 3.3\text{ V}$	10			mA
		$V_{I(3.3V\_OUT)} = 1\text{ V}$	5			
PSRR	Power-supply ripple rejection <sup>(2)</sup>	$f = 1\text{ kHz}$ , $C_{L(3.3V\_OUT)} = 4.7\text{ }\mu\text{F}$ , $\text{ESR} = 0.25\text{ }\Omega$ , $I_O = 5\text{ mA}$ , $V_{I(\text{BP})\text{PP}} = 100\text{ mV}$	40			dB
	Low-level trip threshold voltage at PG		2.88	2.94	3	V
$V_{\text{hys}}$	Hysteresis voltage at PG <sup>(2)</sup>		50		100	mV
$V_{OH}$	High-level output voltage at PG	$4.25\text{ V} \leq V_{I(\text{BP})} \leq 5.25\text{ V}$ , $I_O = 2\text{ mA}$	2.4			V
$V_{OL}$	Low-level output voltage at PG	$4.25\text{ V} \leq V_{I(\text{BP})} \leq 5.25\text{ V}$ , $I_O = 3.2\text{ mA}$			0.4	V
$V_{\text{ref}}$	Reference voltage at PG_DLY			1.22		V
	Charge current at PG_DLY			3		$\mu\text{A}$
$t_d$	Delay time at PG <sup>(2) (3)</sup>	$C_{L(\text{PG\_DLY})} = 0.47\text{ }\mu\text{F}$		190		ms

(1) Pulse-testing techniques maintain junction temperature close to ambient temperature; thermal effects must be taken into account separately.

(2) Specified by design, not tested in production.

(3) The PG delay time ( $t_d$ ) is calculated using the PG\_DLY reference voltage and charge current:

$$t_d = \frac{C_{L(\text{PG\_DLY})} \times V_{\text{ref}}}{\text{Charge Current}}$$

## ELECTRICAL CHARACTERISTICS

over recommended operating junction temperature range,  $4.5\text{ V} \leq V_{I(\text{BP})} \leq 5.5\text{ V}$ ,  $4.85\text{ V} \leq V_{I(\text{SP})} \leq 5.5\text{ V}$ ,  $6\text{ V} \leq V_{I(\text{VEXT})} \leq 9\text{ V}$ ,  $\overline{\text{EN}}_x = 0\text{ V}$ ,  $\text{EN\_REG} = 3.3\text{ V}$ ,  $\text{BP\_DIS} = 0\text{ V}$ ,  $C_{L(\text{SP})} = 220\text{ }\mu\text{F}$  (unless otherwise noted))

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
<b>VOLTAGE REGULATOR CONTROLLER</b>						
$V_{O(\text{CP})}$	Output voltage, charge pump	$V_{I(\text{VEXT})} = 6\text{ V}$ , $I_{O(\text{VCP})} = 5\text{ mA}$ , $C_{(\text{CP\_P})} = 10\text{ nF}$ , $C_{(\text{VCP})} = 100\text{ nF}$	10			V
$f_{\text{osc}}$	Oscillator frequency <sup>(1)</sup>	$6\text{ V} \leq V_{I(\text{VEXT})} \leq 9\text{ V}$ , $I_{O(\text{VCP})} = 5\text{ mA}$ , $V_{O(\text{VCP})} = 10\text{ V}$		850		kHz
Gate drive current	Sourcing	$V_{I(\text{VCP})} = 9\text{ V}$ , $V_{O(\text{GATE})} = 7.5\text{ V}$ , $V_{I(\text{SP})} = 4.5\text{ V}$	500			$\mu\text{A}$
	Sinking	$V_{I(\text{VCP})} = 9\text{ V}$ , $V_{O(\text{GATE})} = 5.5\text{ V}$ , $V_{I(\text{SP})} = 5.5\text{ V}$	1.5			mA
	Open-loop gain <sup>(1)</sup>	$V_{I(\text{VEXT})} = 6\text{ V}$ , $0.5\text{ V} \leq V_{O(\text{GATE})} \leq 9\text{ V}$		80		dB
	Reference voltage at $V_{I(\text{SP})}$ , using external regulator	$V_{I(\text{VEXT})} = 6\text{ V to } 9\text{ V}$ , IRLZ24N FET	4.9	5.1	5.25	V
	Gate clamp voltage	Gate to SP		10		V

(1) Specified by design, not tested in production.

## POWER SWITCH TIMING REQUIREMENTS

PARAMETER		TEST CONDITIONS <sup>(1)</sup>	MIN	TYP	MAX	UNIT
t <sub>on</sub> Turnon time <sup>(2)</sup>	BP to OUTx switch	V <sub>I(BP)</sub> = 5 V, V <sub>I(SP)</sub> = open, T <sub>A</sub> = 25°C, C <sub>L</sub> = 100 μF, R <sub>L</sub> = 50 Ω		4.5		ms
	SP to OUTx switch	V <sub>I(SP)</sub> = V <sub>I(BP)</sub> = 5 V, T <sub>A</sub> = 25°C, C <sub>L</sub> = 100 μF, R <sub>L</sub> = 10 Ω		4.5		
t <sub>off</sub> Turnoff time <sup>(2)</sup>	BP to OUTx switch	V <sub>I(BP)</sub> = 5 V, V <sub>I(SP)</sub> = open, T <sub>A</sub> = 25°C, C <sub>L</sub> = 100 μF, R <sub>L</sub> = 50 Ω		15		ms
	SP to OUTx switch	V <sub>I(SP)</sub> = V <sub>I(BP)</sub> = 5 V, T <sub>A</sub> = 25°C, C <sub>L</sub> = 100 μF, R <sub>L</sub> = 10 Ω		10		
t <sub>r</sub> Rise time, output <sup>(2)</sup>	BP to OUTx switch	V <sub>I(BP)</sub> = 5 V, V <sub>I(SP)</sub> = open, T <sub>A</sub> = 25°C, C <sub>L</sub> = 100 μF, R <sub>L</sub> = 50 Ω		4		ms
	SP to OUTx switch	V <sub>I(SP)</sub> = V <sub>I(BP)</sub> = 5 V, T <sub>A</sub> = 25°C, C <sub>L</sub> = 100 μF, R <sub>L</sub> = 10 Ω		3		
t <sub>f</sub> Fall time, output <sup>(2)</sup>	BP to OUTx switch	V <sub>I(BP)</sub> = 5 V, V <sub>I(SP)</sub> = open, T <sub>A</sub> = 25°C, C <sub>L</sub> = 100 μF, R <sub>L</sub> = 50 Ω		10		ms
	SP to OUTx switch	V <sub>I(SP)</sub> = V <sub>I(BP)</sub> = 5 V, T <sub>A</sub> = 25°C, C <sub>L</sub> = 100 μF, R <sub>L</sub> = 10 Ω		3		

(1) Pulse-testing techniques maintain junction temperature close to ambient temperature; thermal effects must be taken into account separately.

(2) Specified by design, not tested in production.

## THERMAL SHUTDOWN

over operating free-air temperature range (unless otherwise noted)

PARAMETER			MIN	TYP	MAX	UNIT
T <sub>J</sub>	Thermal shutdown	First		140		°C
		Second		150		
	Hysteresis	First		15		°C
		Second		25		

PARAMETER MEASUREMENT INFORMATION

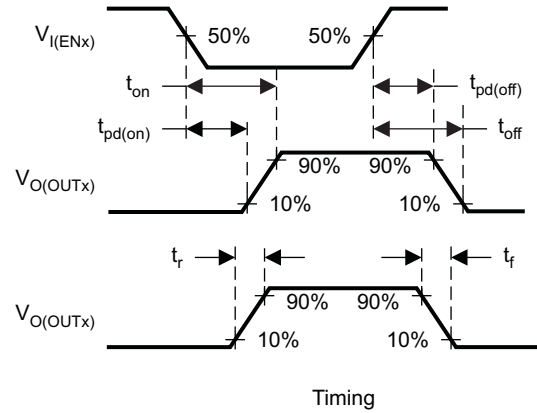
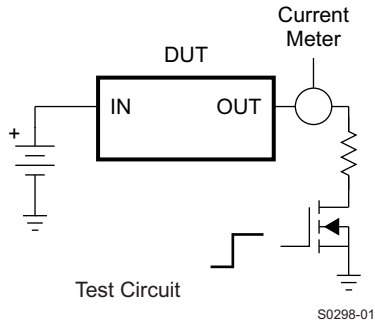


Figure 1. Current Limit Response

Figure 2. Timing and Internal Voltage Regulator Transition Waveforms

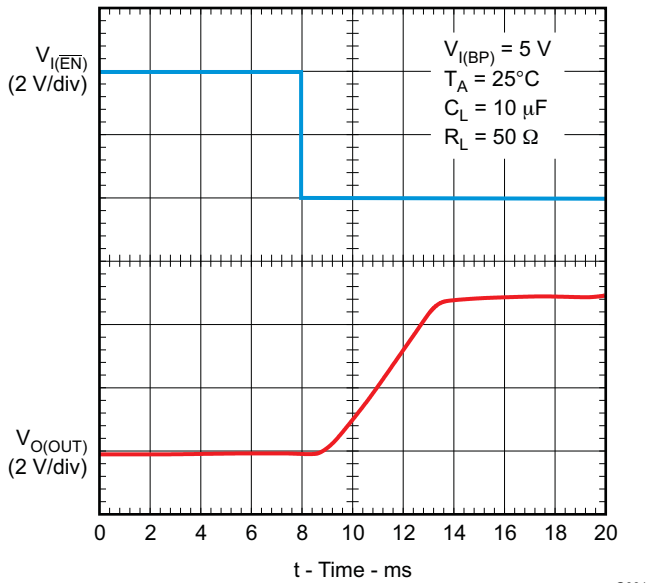


Figure 3. Turnon Delay and Rise Time (BP Switch)

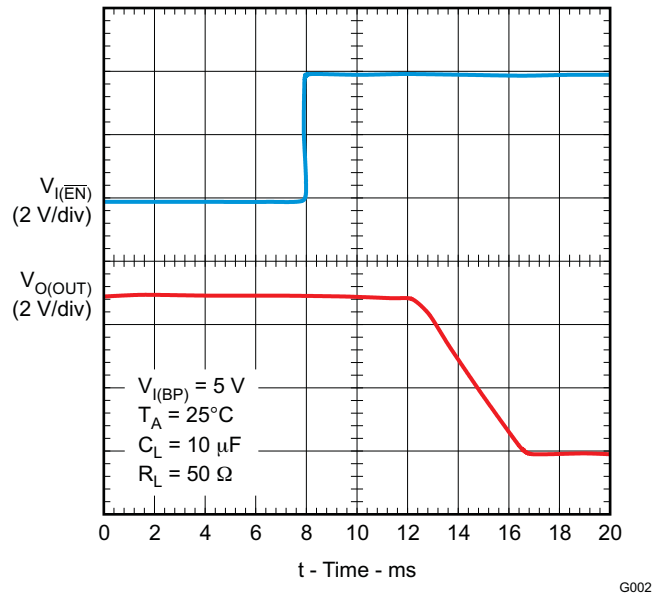
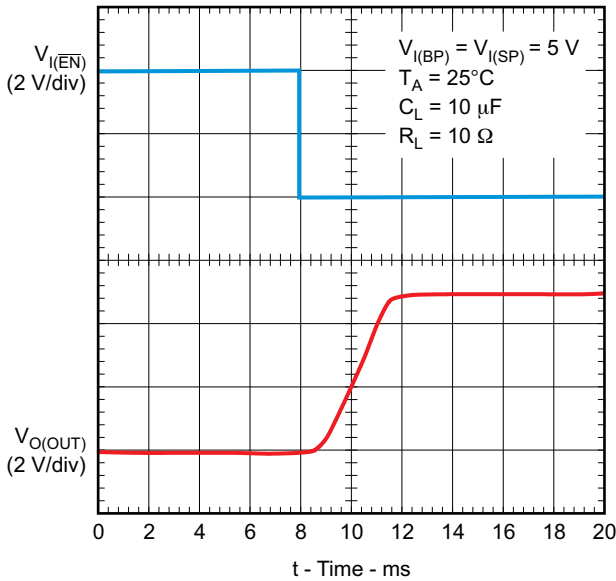


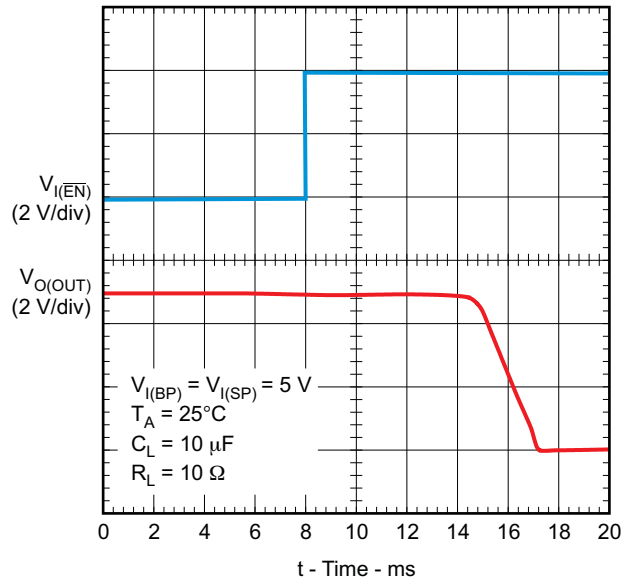
Figure 4. Turnoff Delay and Fall Time (BP Switch)

PARAMETER MEASUREMENT INFORMATION (continued)



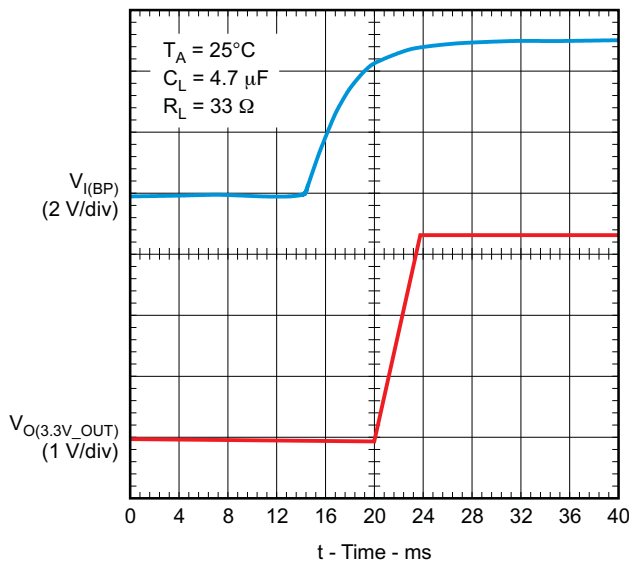
G003

Figure 5. Turnon Delay and Rise Time (SP Switch)



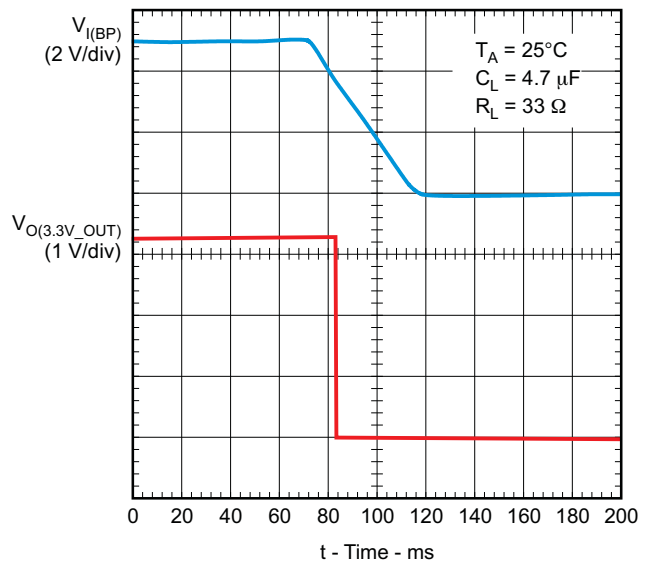
G004

Figure 6. Turnoff Delay and Fall Time (SP Switch)



G005

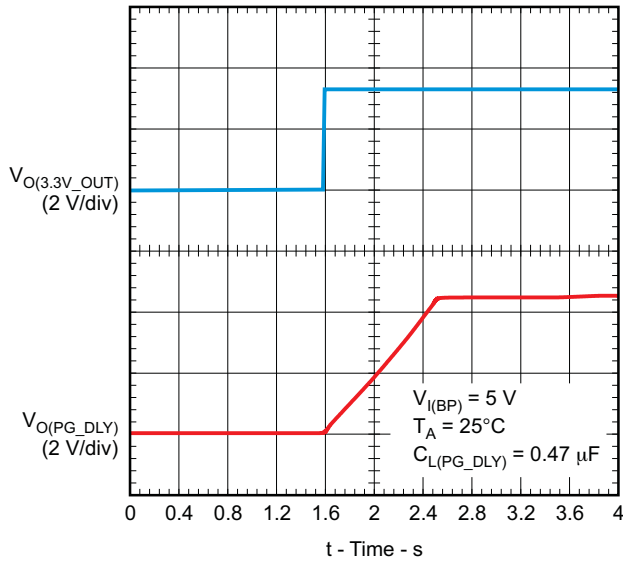
Figure 7. Turnon Delay and Rise Time (3.3V\_OUT)



G006

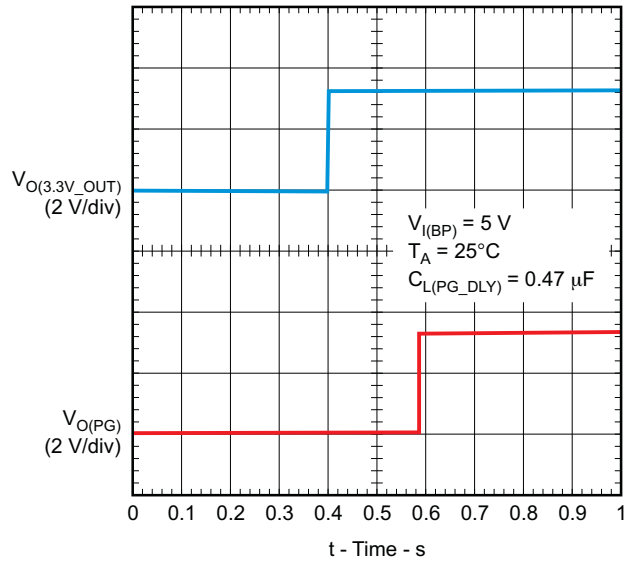
Figure 8. Turnoff Delay and Fall Time (3.3V\_OUT)

PARAMETER MEASUREMENT INFORMATION (continued)



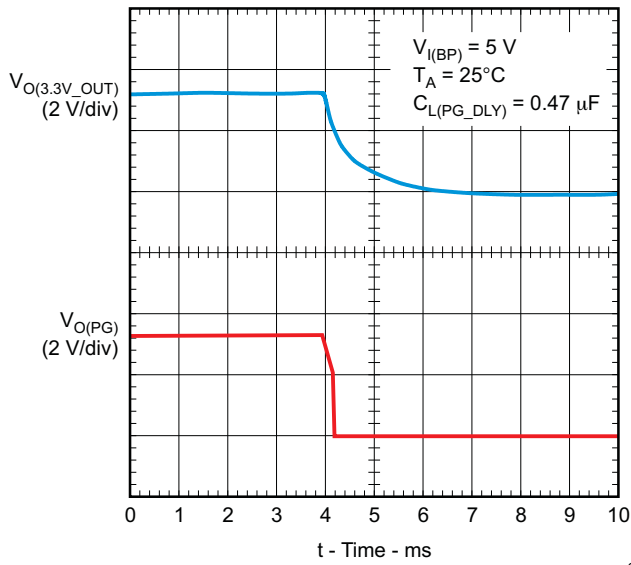
G007

Figure 9. PG\_DLY Rise Time With a 0.47-µF Capacitor



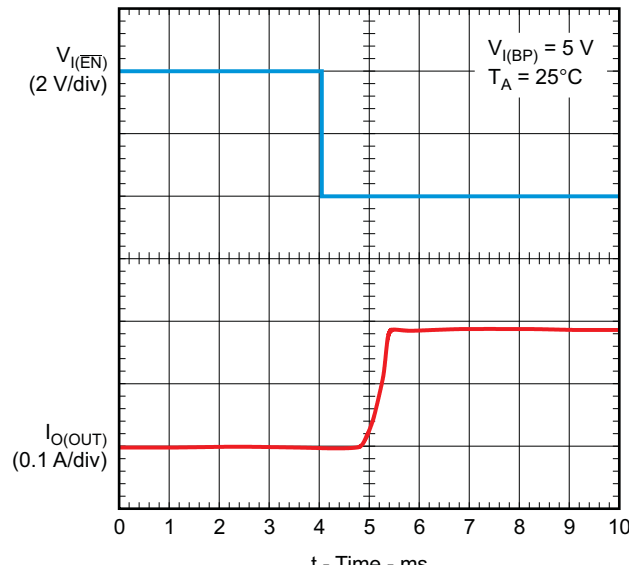
G008

Figure 10. Turnon Delay (3.3V\_OUT to PG)



G009

Figure 11. Turnoff Time (3.3V\_OUT to PG)



G010

Figure 12. Short-Circuit Current (BP Switch), Device Enabled Into Short

PARAMETER MEASUREMENT INFORMATION (continued)

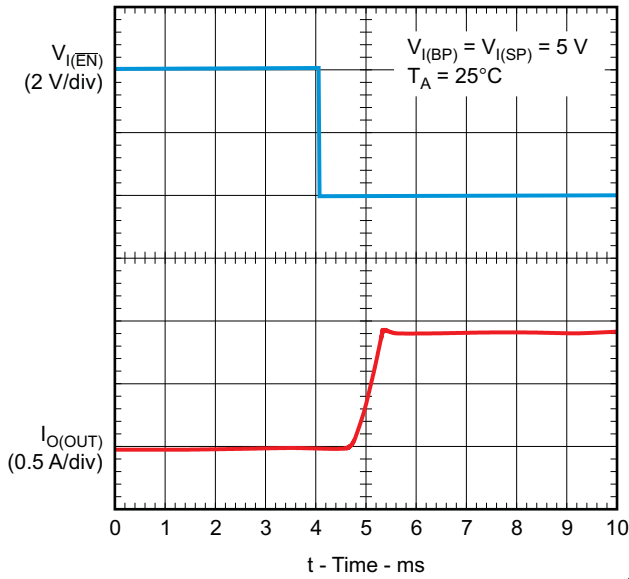


Figure 13. Short-Circuit Current (SP Switch), Device Enabled Into Short

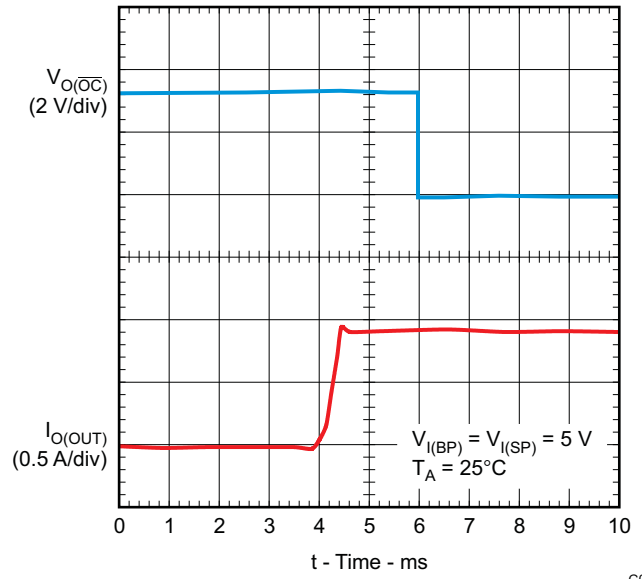


Figure 14.  $\overline{OC}$  Response (SP Switch), Device Enabled Into Short

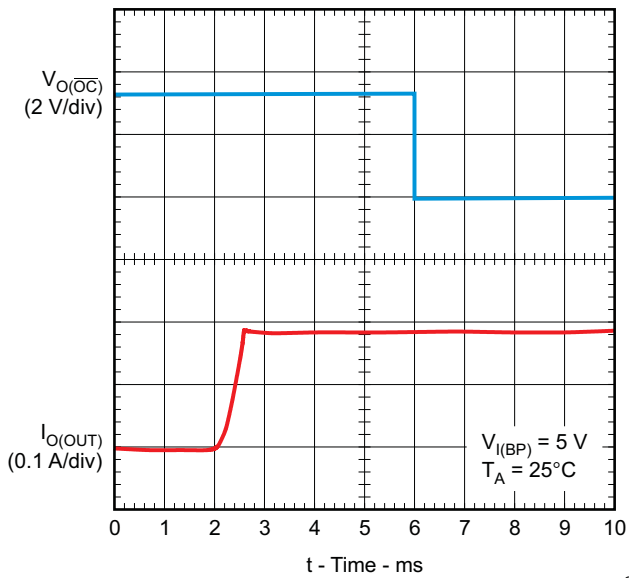


Figure 15.  $\overline{OC}$  Response (BP Switch), Device Enabled Into Short

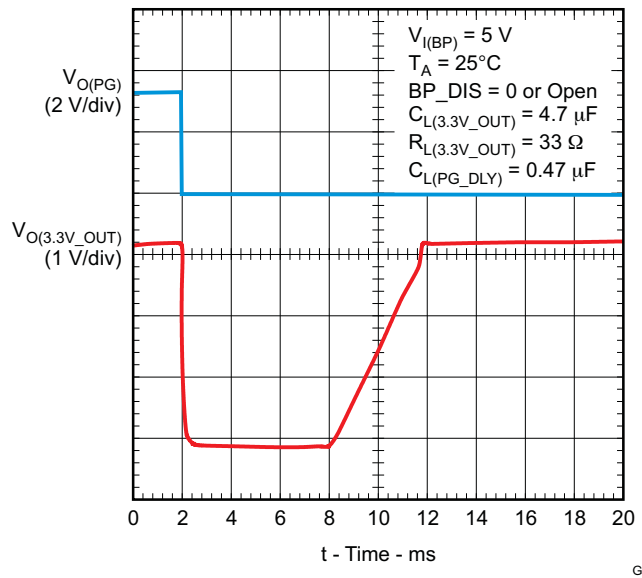


Figure 16. SP to BP Automatic Switchover Enabled

PARAMETER MEASUREMENT INFORMATION (continued)

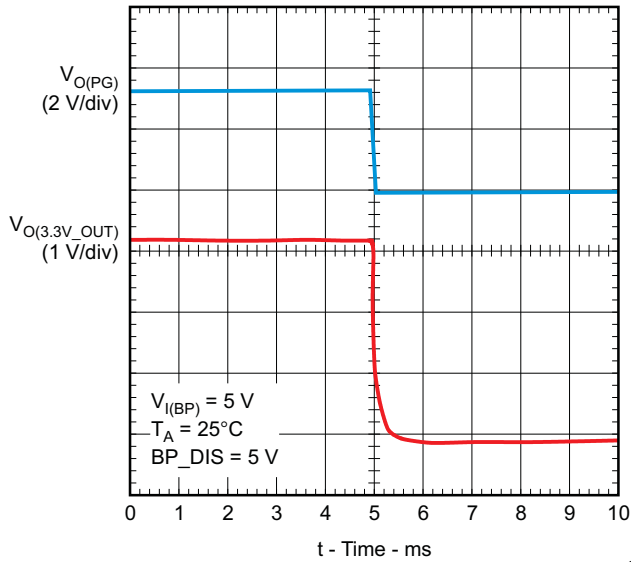


Figure 17. SP to BP Automatic Switchover Disabled

G015

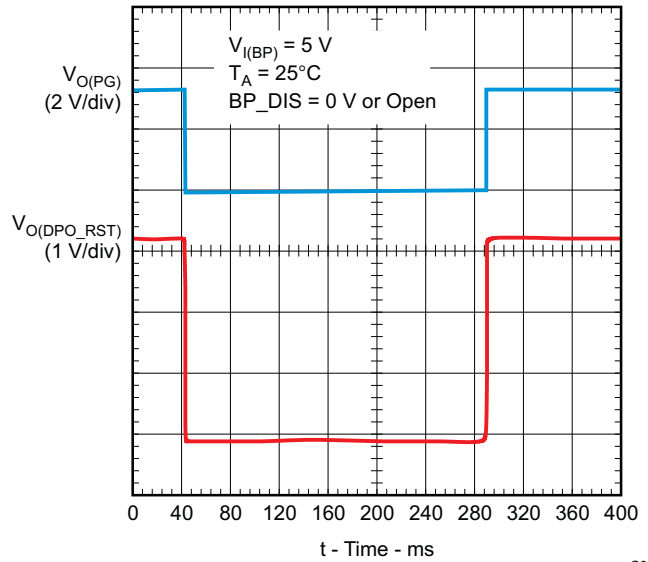


Figure 18. SP to BP Automatic Switchover Enabled

G016

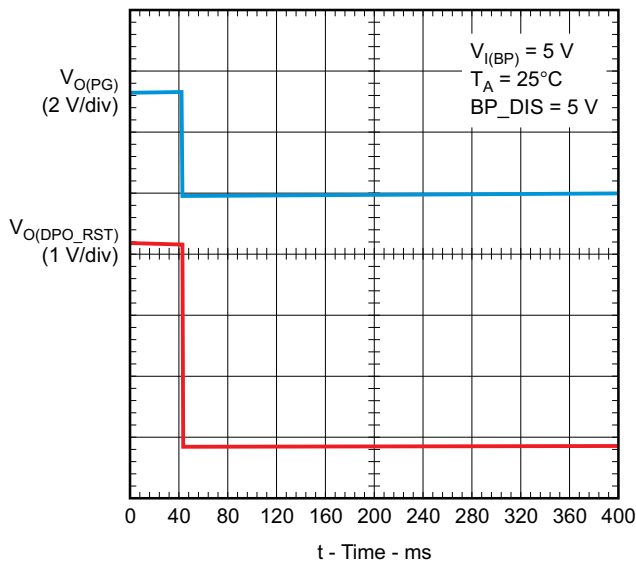


Figure 19. SP to BP Automatic Switchover Disabled

G017

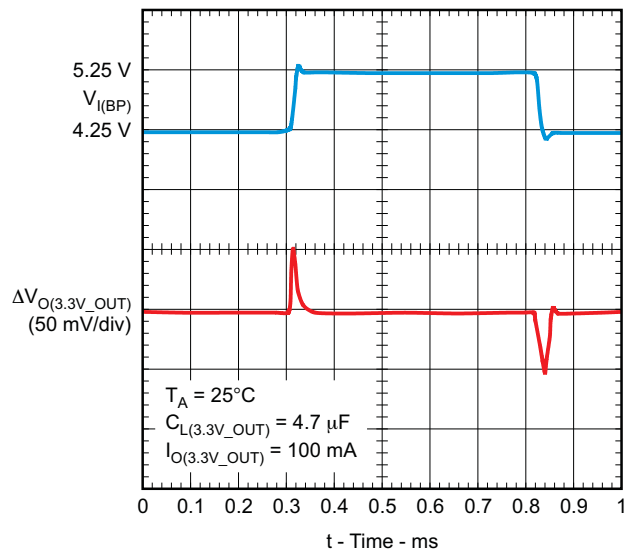


Figure 20. Line Transient Response

G018



PARAMETER MEASUREMENT INFORMATION (continued)

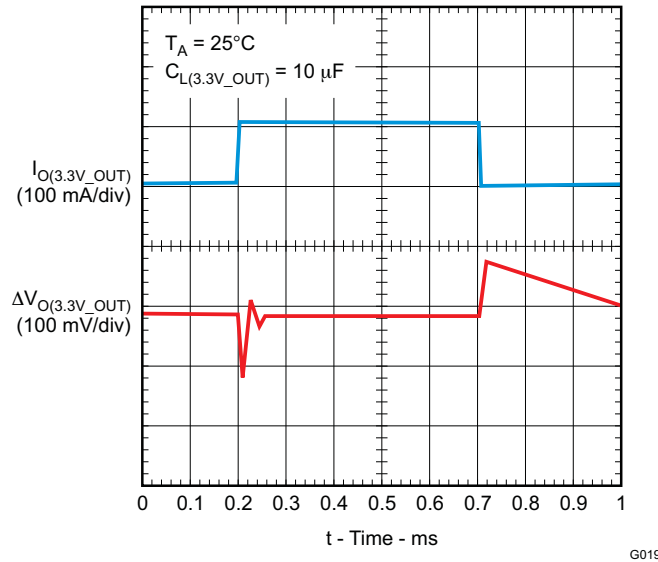


Figure 21. Load Transient Response

TYPICAL CHARACTERISTICS

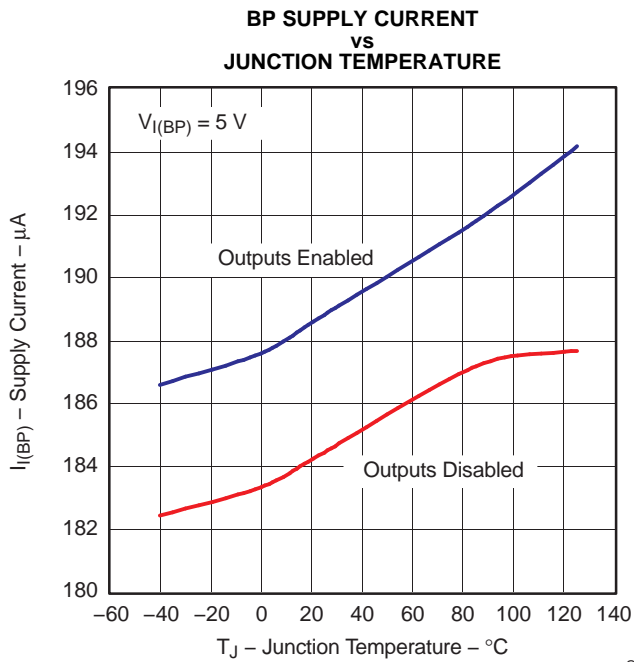


Figure 22.

G020

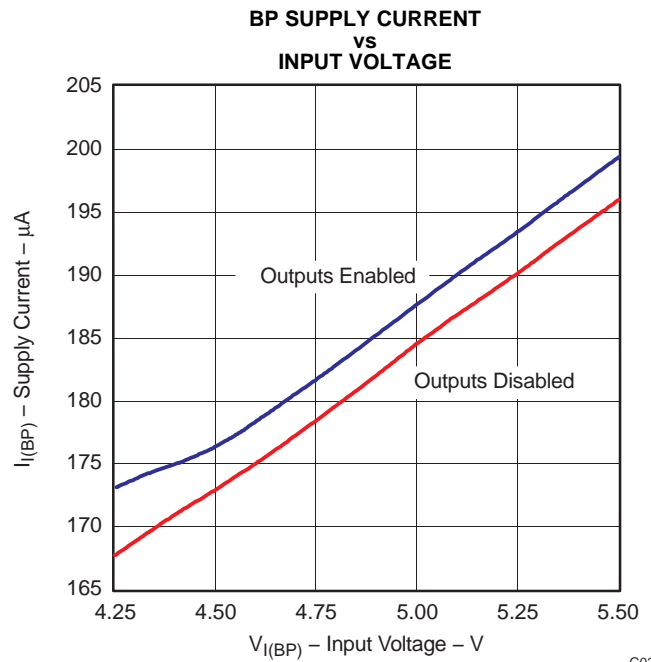


Figure 23.

G021

TYPICAL CHARACTERISTICS (continued)

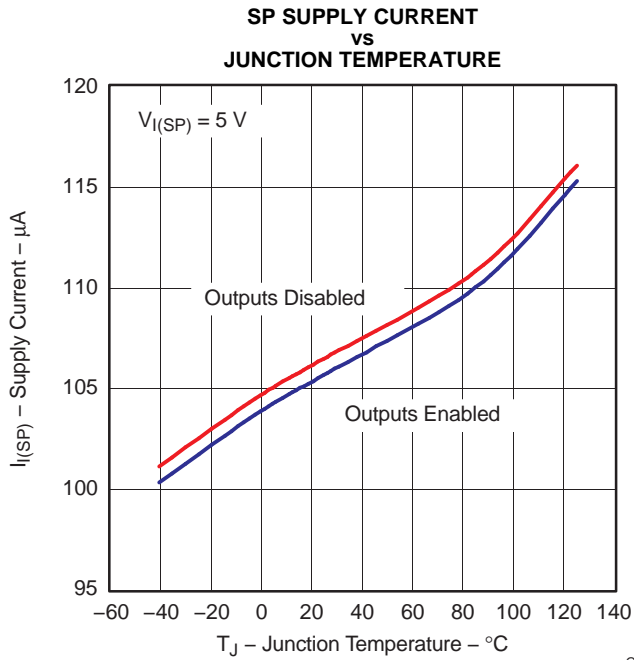


Figure 24.

G022

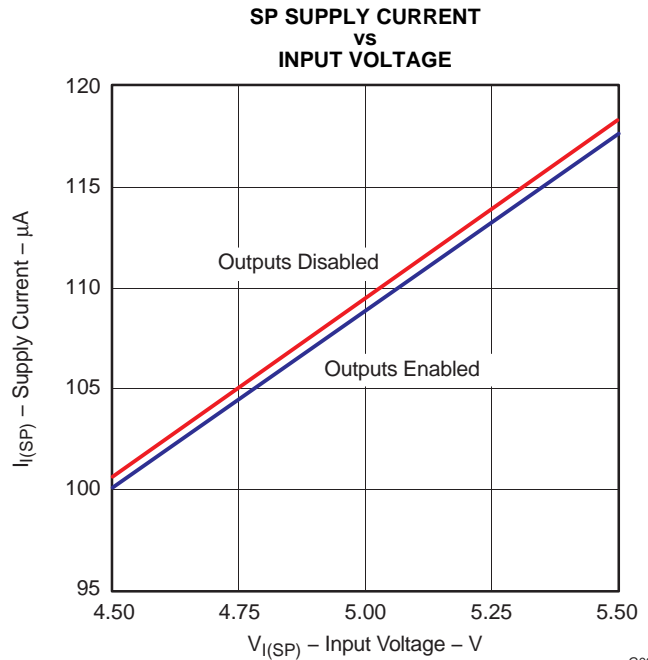


Figure 25.

G023

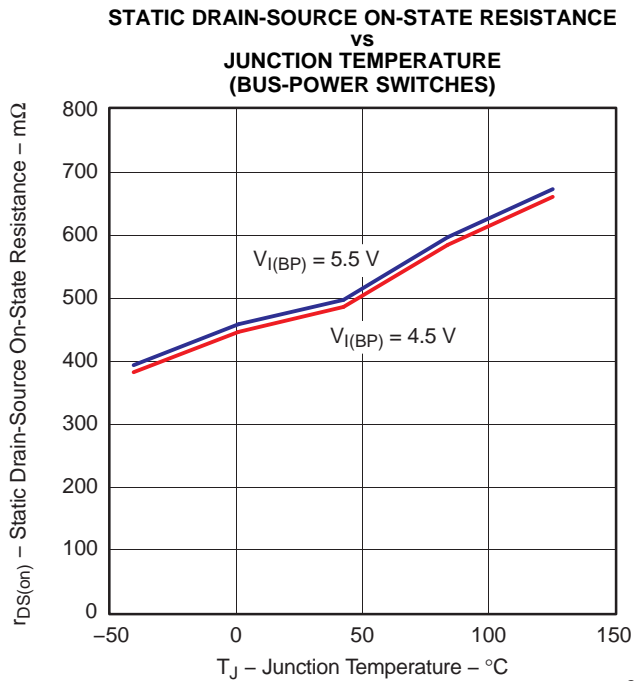


Figure 26.

G025

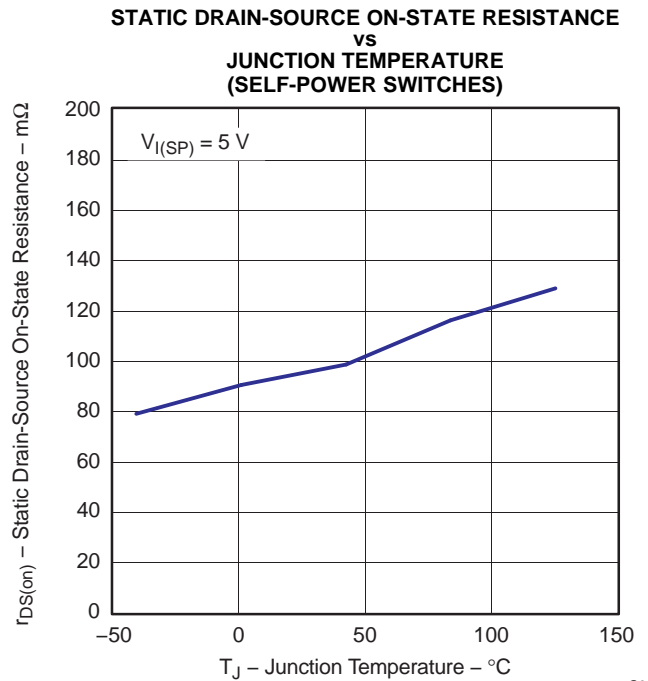


Figure 27.

G024

TYPICAL CHARACTERISTICS (continued)

SHORT-CIRCUIT OUTPUT CURRENT  
vs  
JUNCTION TEMPERATURE  
(BUS-POWER SWITCHES)

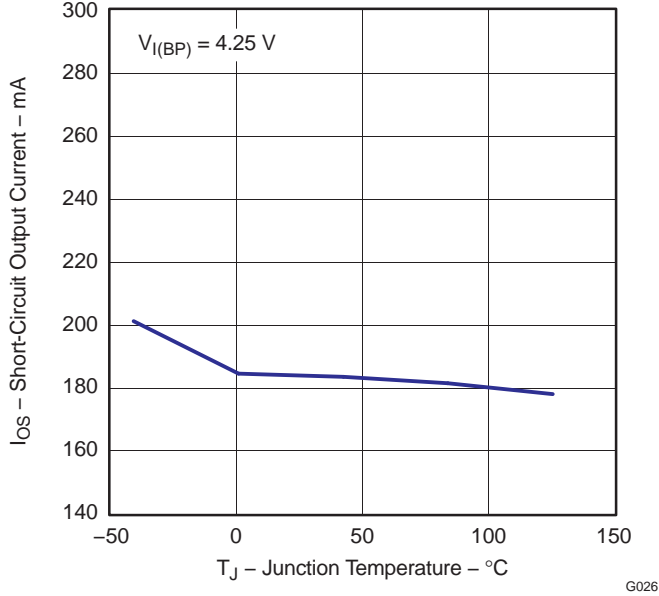


Figure 28.

SHORT-CIRCUIT OUTPUT CURRENT  
vs  
JUNCTION TEMPERATURE  
(BUS-POWER SWITCHES)

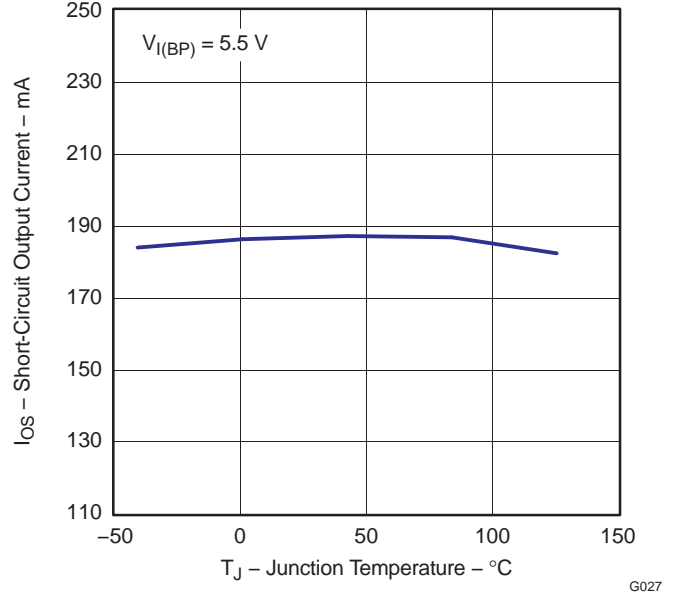


Figure 29.

SHORT-CIRCUIT OUTPUT CURRENT  
vs  
JUNCTION TEMPERATURE  
(SELF-POWER SWITCHES)

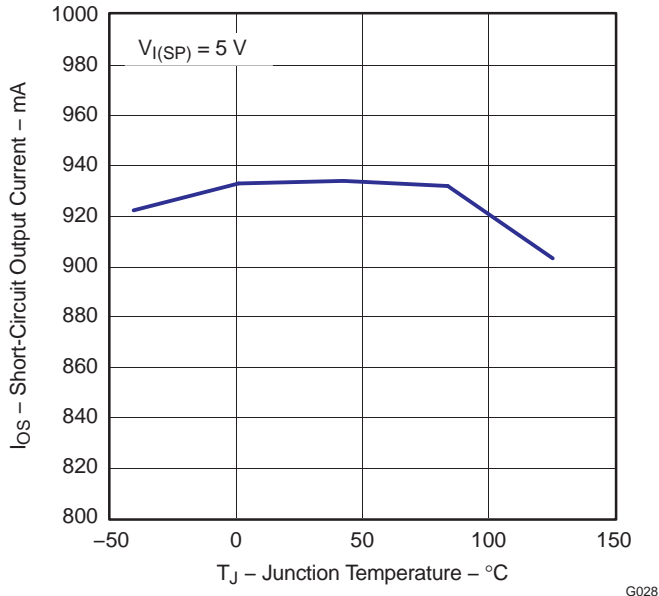


Figure 30.

INPUT VOLTAGE (BP UNDERVOLTAGE LOCKOUT)  
vs  
JUNCTION TEMPERATURE

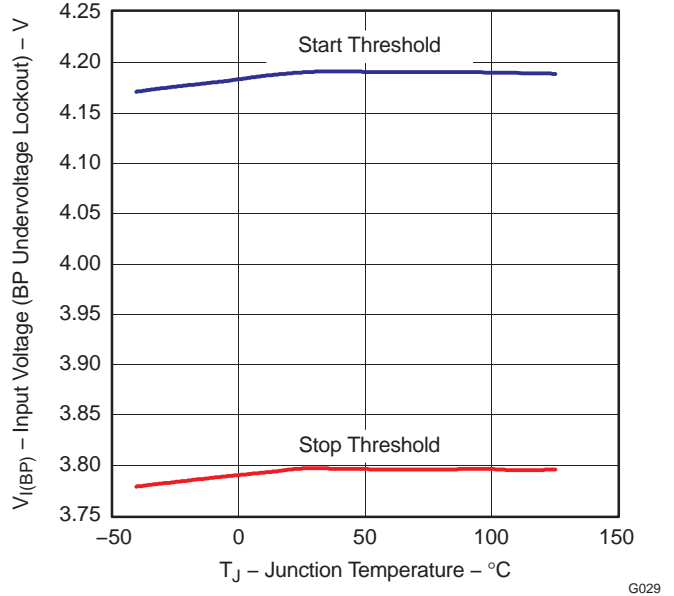


Figure 31.

TYPICAL CHARACTERISTICS (continued)

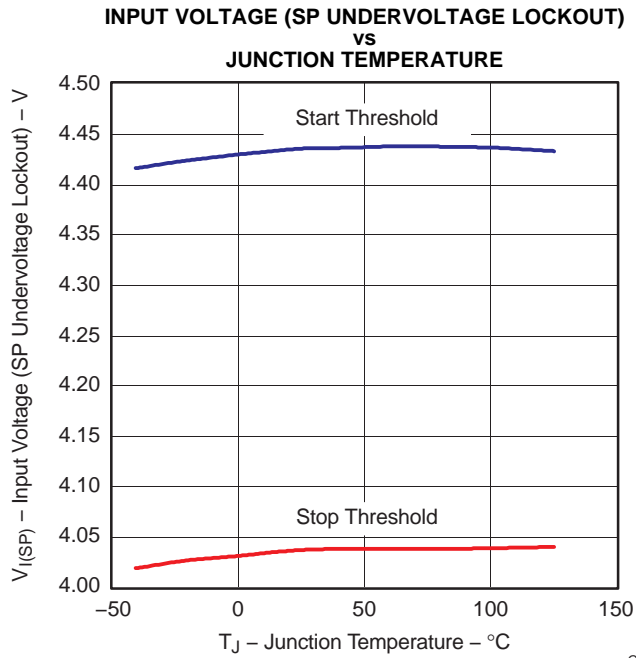


Figure 32.

G030

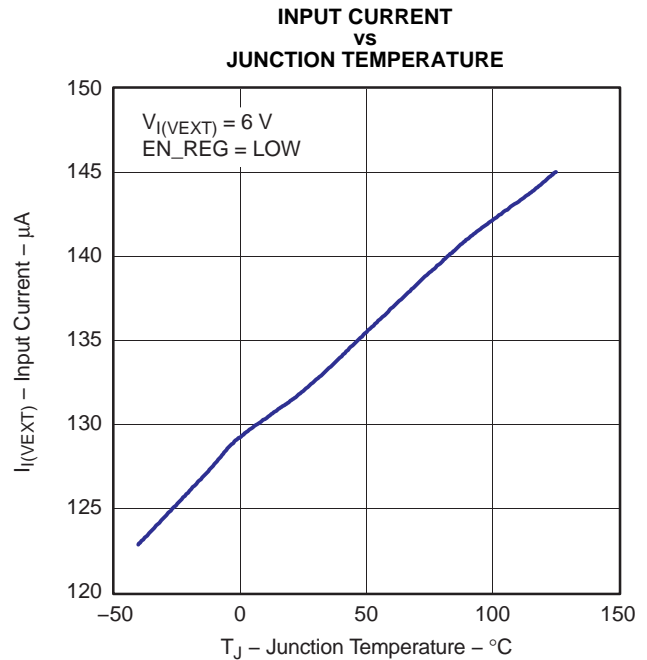


Figure 33.

G031

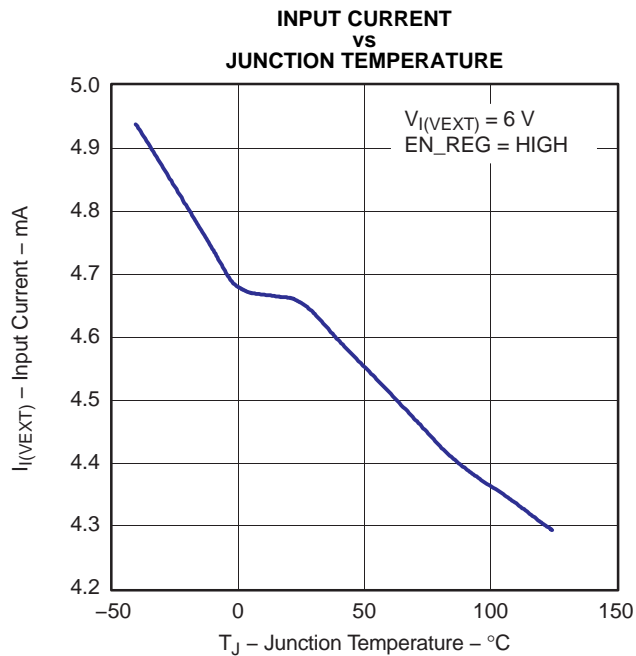


Figure 34.

G032

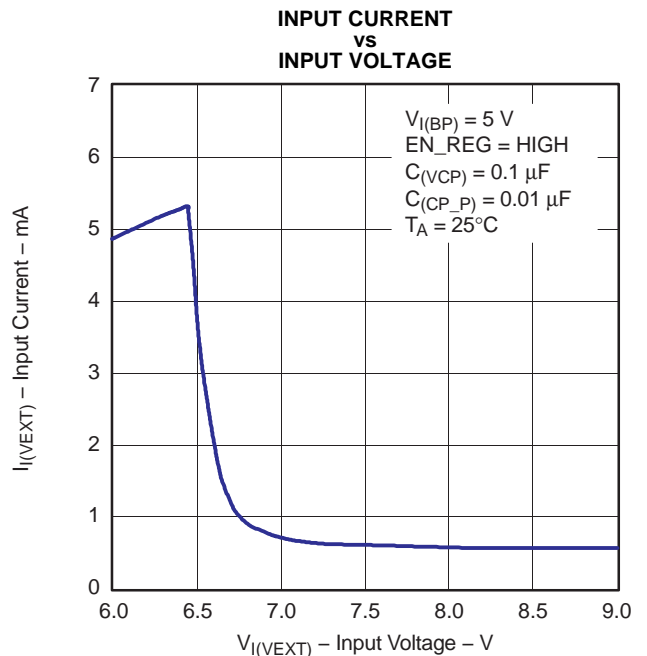
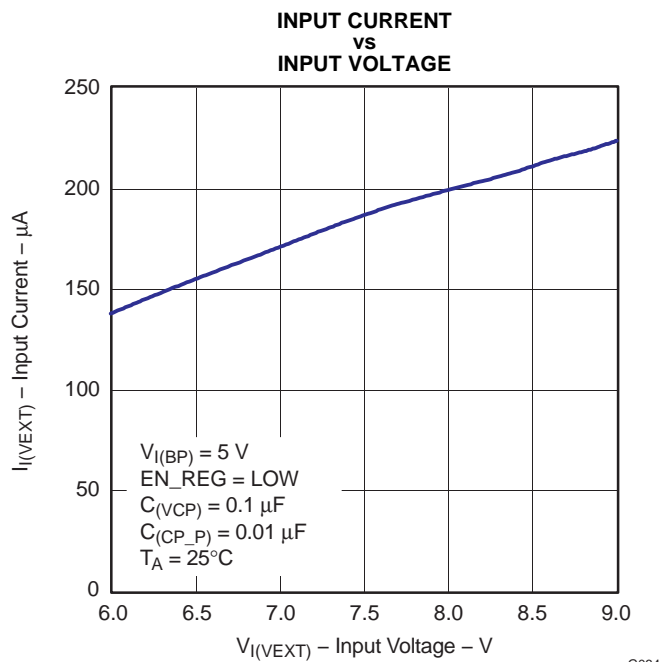


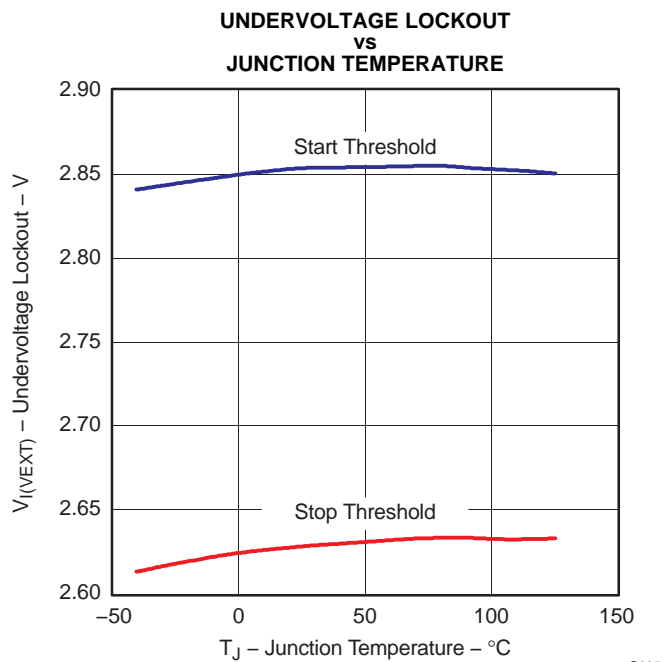
Figure 35.

G033

**TYPICAL CHARACTERISTICS (continued)**



**Figure 36.**



**Figure 37.**

## APPLICATION INFORMATION

### EXTERNAL CAPACITOR REQUIREMENTS

A 0.1- $\mu\text{F}$  ceramic bypass capacitor and a 10- $\mu\text{F}$  bulk capacitor between BP and AGND, close to the device, are recommended. Similarly, a 0.1- $\mu\text{F}$  ceramic and a 68- $\mu\text{F}$  bulk capacitor, from SP to AGND, and from VEXT to AGND if an external 5-V LDO is required, are recommended because of much higher current in the self-powered mode.

From each of the outputs (OUTx) to ground, a 33- $\mu\text{F}$  or higher-valued bulk capacitor is recommended when the output load is heavy. This precaution reduces power-supply transients. Additionally, bypassing the outputs with a 0.1- $\mu\text{F}$  ceramic capacitor improves the immunity of the device to short-circuit transients.

An output capacitor connected between 3.3V\_OUT and GND is required to stabilize the internal control loop. The internal LDO is designed for a capacitor range of 4.7  $\mu\text{F}$  to 33  $\mu\text{F}$  with an ESR of 0.2  $\Omega$  to 10  $\Omega$ . Solid tantalum-electrolytic, aluminum-electrolytic and multilayer ceramic capacitors are all suitable.

Ceramic capacitors have different types of dielectric material, each exhibiting different temperature and voltage variations. The most common types are X5R, X7R, Y5U, Z5U, and NPO. The NPO-type ceramic capacitors are generally the most stable over temperature. However, the X5R and X7R are also relatively stable over temperature (with the X7R being the more stable of the two) and are therefore acceptable for use. The Y5U and Z5U types provide high capacitance in a small geometry, but exhibit large variations over temperature. For this reason, the Y5U and Z5U are not generally recommended.

A transient condition occurs because of a sudden increase in output current. The output capacitor reduces the transient effect by providing the additional current needed by the load. Depending on the current demand at the output, a voltage drop occurs across the internal resistance, ESR, of the capacitor. Using a low-ESR capacitor helps minimize this voltage drop. A larger capacitor also reduces the voltage drop by supplying the current demand for a longer time, versus that provided by a smaller capacitor.

### OVERCURRENT

An internal sense FET checks for overcurrent conditions. Unlike current-sense resistors, sense FETs do not increase the series resistance of the current path. When an overcurrent condition is detected, the device maintains a constant output current and reduces the output voltage accordingly. Complete shutdown occurs only if the fault is present long enough to activate thermal limiting.

Three possible overload conditions can occur. In the first condition, the output has been shorted before the device is enabled or before BP and SP have been applied. The TPS2070 and TPS2071 sense the short and immediately switch into a constant-current output.

In the second condition, the short occurs while the device is enabled. At the instant the short occurs, very high currents may flow for a very short time before the current-limit circuit can react. After the current-limit circuit has tripped (reached the overcurrent trip threshold), the device switches into constant-current mode.

In the third condition, the load has been gradually increased beyond the recommended operating current. The current is permitted to rise until the current-limit threshold is reached or until the thermal limit of the device is exceeded. The TPS2070 and TPS2071 are capable of delivering current up to the current-limit threshold without damaging the device. Once the threshold has been reached, the device switches into its constant-current mode.

### $\overline{\text{OC}}$ RESPONSE

The  $\overline{\text{OCx}}$  output is asserted (active-low) when an overcurrent or overtemperature condition is encountered and remains asserted until the overcurrent or overtemperature condition is removed. Connecting a heavy capacitive load to an enabled device can cause momentary false overcurrent reporting from the inrush current flowing through the device and charging the downstream capacitor. The TPS2070 and TPS2071 are designed to reduce false overcurrent reporting by implementing an internal deglitch circuit. This circuit eliminates the need for an external filter, which requires extra components. Also, using low-ESR electrolytic capacitors on the outputs can reduce erroneous overcurrent reporting by providing a low-impedance energy source to lower the inrush current flow through the device during hot-plug events. The  $\overline{\text{OCx}}$  outputs are logic outputs, thereby requiring no pullup or pulldown resistors.

## POWER DISSIPATION AND JUNCTION TEMPERATURE

The major source of power dissipation for the TPS2070 and TPS2071 comes from the internal voltage regulator and the N-channel MOSFETs. Checking the power dissipation and junction temperature is always a good design practice. Begin by determining the  $r_{DS(on)}$  of the N-channel MOSFET according to the input voltage and operating temperature. As an initial estimate, use the highest operating ambient temperature of interest and read  $r_{DS(on)}$  from the graphs shown under the typical characteristics section of this data sheet. Using this value, the power dissipation per switch can be calculated by:

$$P_D = r_{DS(on)} \times I^2$$

Multiply this number by four to get the total power dissipation coming from the N-channel MOSFETs.

The power dissipation for the internal voltage regulator is calculated using:

$$P_D = (V_{I(BP)} - V_{O(min)}) \times I_{O(OUT)}$$

The total power dissipation for the device becomes:

$$P_{D(total)} = P_{D(voltage\ regulator)} + (4 \times P_{D( switch)})$$

Finally, calculate the junction temperature:

$$T_J = P_D \times R_{\theta JA} + T_A$$

where:

$T_A$  = ambient temperature in °C

$R_{\theta JA}$  = Thermal resistance in °C/W, equal to inverting of derating factor found on the power dissipation table in this data sheet

Compare the calculated junction temperature with the initial estimate. If they do not agree within a few degrees, repeat the calculation, using the calculated value as the new estimate. Two or three iterations are generally sufficient to get a reasonable answer.

## THERMAL PROTECTION

Thermal protection prevents damage to the IC when heavy-overload or short-circuit faults are present for extended periods. The faults force the TPS2070 and TPS2071 into constant-current mode at first, which causes the voltage across the high-side switch to increase; under short-circuit conditions, the voltage across the switch is equal to the input voltage. The increased dissipation causes the junction temperature to rise to high levels.

The protection circuit senses the junction temperature of the switch and shuts it off. Hysteresis is built into the thermal sense circuit, and after the device has cooled approximately 20 degrees, the switch turns back on. The switch continues to cycle in this manner until the load fault or input power is removed.

The TPS2070 and TPS2071 implement a dual thermal trip to allow fully independent operation of the power distribution switches. In an overcurrent or short-circuit condition, the junction temperature rises. Once the die temperature rises to approximately 140°C, the internal thermal-sense circuitry determines which power switch is in an overcurrent condition and turns only that power switch off, thus isolating the fault without interrupting operation of the adjacent power switch. If the die temperature exceeds the first thermal trip point of 140°C and reaches 150°C, the device turns off. The  $\overline{OC}$  output is asserted (active-low) when overtemperature or overcurrent occurs.

## UNDERVOLTAGE LOCKOUT (UVLO)

An undervoltage lockout ensures that the device (LDO and switches) is in the off state at power up. The UVLO also keeps the device from being turned on until the power supply has reached the start threshold (see undervoltage lockout table), even if the switches are enabled. The UVLO activates whenever the input voltage falls below the stop threshold as defined in the undervoltage lockout table. This facilitates the design of hot-insertion systems, where it is not possible to turn off the power switches before input power is removed. Upon reinsertion, the power switches are turned on with a controlled rise time to reduce EMI and voltage overshoots.

## SELF-POWER TO BUS-POWER OR BUS-POWER TO SELF-POWER TRANSITION

An autoswitching function between bus-powered mode and self-powered mode is a feature of the TPS2070 and TPS2071. When this feature is enabled (BP\_DIS is inactive) and SP is removed or applied, a transition is initiated. The transition sequence begins with the internal LDO being turned off and its external capacitance discharged. Any enabled switches are also turned off and the external capacitors discharged. Once the LDO and switch outputs are low, the internal logic turns the LDO back on. This entire sequence occurs whenever power to the SP input is removed or applied, regardless of the source of power, i.e., an external power supply or the use of the external regulator.

## UNIVERSAL SERIAL BUS (USB) APPLICATIONS

The universal serial bus interface is a 1.5/12-Mb/s (for USB), or 480 Mb/s (for Hi-Speed USB), multiplexed serial bus designed for low-to-medium bandwidth PC peripherals (e.g., keyboards, printers, scanners, and mice). The four-wire USB interface is conceived for dynamic attach-detach (hot plug-unplug) of peripherals. Two lines are provided for differential data, and two lines are provided for 5-V power distribution.

USB data is a 3.3-V-level signal, but power is distributed at 5 V to allow for voltage drops in cases where power is distributed through more than one hub or across long cables. Each function must provide its own regulated 3.3 V from the 5-V input or its own internal power supply.

The USB specification defines the following five classes of devices, each differentiated by power-consumption requirements:

- Hosts/self-powered hubs (SPH)
- Bus-powered hubs (BPH)
- Low-power, bus-powered functions
- High-power, bus-powered functions
- Self-powered functions

Self-powered and bus-powered hubs distribute data and power to downstream functions. The TPS2070 and TPS2071 can provide power-distribution solutions for hybrid hubs that need switching between BPH and SPH according to power availability and application requirements.

## USB POWER-DISTRIBUTION REQUIREMENTS

USB can be implemented in several ways, and, regardless of the type of USB device being developed, several power-distribution features must be implemented.

- Hosts/self-powered hubs must:
  - Current-limit downstream ports
  - Report overcurrent conditions on USB  $V_{BUS}$
  - Output 5.25 V to 4.75 V at 500 mA
- Bus-powered hubs must:
  - Enable/disable power to downstream ports
  - Power up at <100 mA
  - Limit inrush current (<44  $\Omega$  and 10  $\mu$ F)
  - Output 5.25 V to 4.4 V at 100 mA
  - Not send power back upstream
- Functions must:
  - Limit inrush currents
  - Power up at <100 mA
  - Not send power back upstream (SP functions)

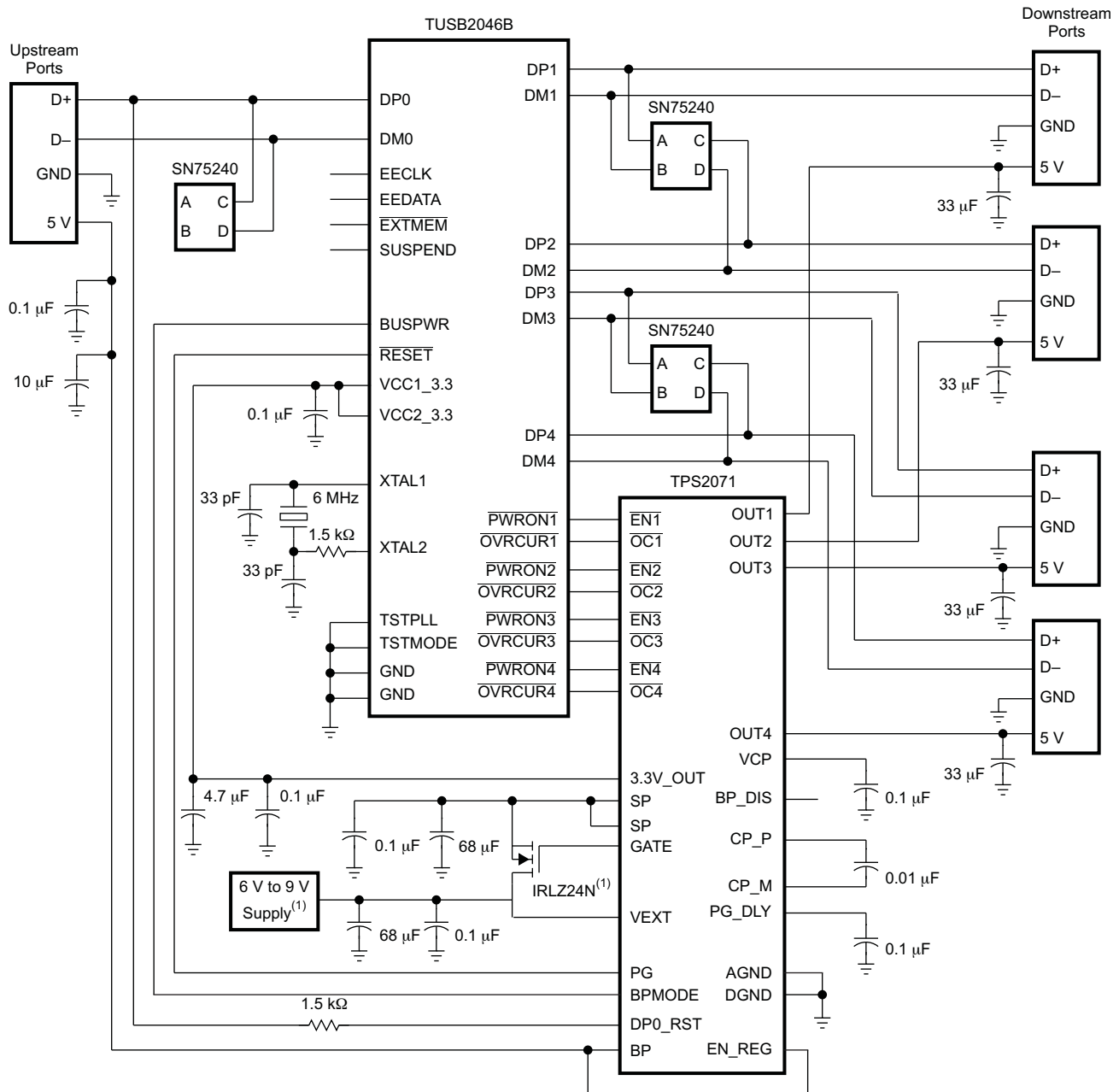
The feature set of the TPS2070 and TPS2071 allows them to meet each of these requirements. The integrated current-limiting and overcurrent reporting is required by hosts and self-powered hubs. The logic-level enable and controlled rise times meet the needs of both input and output ports on hubs, as well as the input ports for bus-powered functions.



## USB HYBRID HUB

A USB hybrid hub can be simply implemented using the TPS2071 USB power controller and a TUSB2046 USB hub controller as shown in [Figure 38](#). The TPS2071 USB power controller provides all the power needs to the four downstream ports and meets all the USB power specifications for both self-powered hubs and bus-powered hubs. The integrated 3.3-V LDO of the power controller is used to provide power for the hub controller and any other local functions (e.g., transient suppressor SN75240 ), which saves board space and cost. The TPS2071 also provides the hub controller with a power-good (PG) signal that connects to the  $\overline{\text{RESET}}$  input of the hub controller to reinitialize the hub automatically when switching between self-powered mode and bus-powered mode whenever the self-power supply is connected or disconnected. The amount of time in which the hub controller is kept in a reset state is controlled by a capacitor connected between the PG\_DLY pin of the power controller and ground.

By using an external N-channel MOSFET and the TPS2071 internal voltage-regulator controller, a regulated 5-V self-powered source can be generated from an input voltage range of 6 V to 9 V (see [Figure 38](#)). In this configuration, the internal voltage regulator controller is enabled by connecting the EN\_REG input to the BP input. Using the internal voltage regulator controller also requires connecting a 0.01- $\mu\text{F}$  capacitor between CP\_P and CP\_M of the TPS2071 power controller. Also, a 0.1- $\mu\text{F}$  capacitor is needed between VCP of the power controller and ground.



B0271-01

- (1) This hybrid hub can also be implemented by connecting a 5-V power supply to the SP input of the TPS2071 and eliminating the external FET. However, this type of implementation is best suited for the TPS2074/75 (see the *TPS2074, TPS2075 Four-Port USB Hub Power Controllers* data sheet, [SLVS288](#), for details).

**Figure 38. USB Hybrid Hub Using TPS2071 Power Controller and TUSB2046 Hub Controller**

**PACKAGING INFORMATION**

Orderable Device	Status <sup>(1)</sup>	Package Type	Package Drawing	Pins	Package Qty	Eco Plan <sup>(2)</sup>	Lead/ Ball Finish	MSL Peak Temp <sup>(3)</sup>	Samples (Requires Login)
TPS2070DAP	ACTIVE	HTSSOP	DAP	32	46	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	<a href="#">Request Free Samples</a>
TPS2070DAPG4	ACTIVE	HTSSOP	DAP	32	46	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	<a href="#">Request Free Samples</a>
TPS2071DAP	ACTIVE	HTSSOP	DAP	32	46	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	<a href="#">Request Free Samples</a>
TPS2071DAPG4	ACTIVE	HTSSOP	DAP	32	46	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	<a href="#">Request Free Samples</a>
TPS2071DAPR	OBSOLETE	HTSSOP	DAP	32		TBD	Call TI	Call TI	Samples Not Available
TPS2071DAPRG4	OBSOLETE	HTSSOP	DAP	32		TBD	Call TI	Call TI	Samples Not Available

<sup>(1)</sup> The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

<sup>(2)</sup> Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

<sup>(3)</sup> MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

**Important Information and Disclaimer:** The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.



## IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, modifications, enhancements, improvements, and other changes to its products and services at any time and to discontinue any product or service without notice. Customers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All products are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its hardware products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by government requirements, testing of all parameters of each product is not necessarily performed.

TI assumes no liability for applications assistance or customer product design. Customers are responsible for their products and applications using TI components. To minimize the risks associated with customer products and applications, customers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any TI patent right, copyright, mask work right, or other TI intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information published by TI regarding third-party products or services does not constitute a license from TI to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of TI information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. Reproduction of this information with alteration is an unfair and deceptive business practice. TI is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

Resale of TI products or services with statements different from or beyond the parameters stated by TI for that product or service voids all express and any implied warranties for the associated TI product or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

TI products are not authorized for use in safety-critical applications (such as life support) where a failure of the TI product would reasonably be expected to cause severe personal injury or death, unless officers of the parties have executed an agreement specifically governing such use. Buyers represent that they have all necessary expertise in the safety and regulatory ramifications of their applications, and acknowledge and agree that they are solely responsible for all legal, regulatory and safety-related requirements concerning their products and any use of TI products in such safety-critical applications, notwithstanding any applications-related information or support that may be provided by TI. Further, Buyers must fully indemnify TI and its representatives against any damages arising out of the use of TI products in such safety-critical applications.

TI products are neither designed nor intended for use in military/aerospace applications or environments unless the TI products are specifically designated by TI as military-grade or "enhanced plastic." Only products designated by TI as military-grade meet military specifications. Buyers acknowledge and agree that any such use of TI products which TI has not designated as military-grade is solely at the Buyer's risk, and that they are solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI products are neither designed nor intended for use in automotive applications or environments unless the specific TI products are designated by TI as compliant with ISO/TS 16949 requirements. Buyers acknowledge and agree that, if they use any non-designated products in automotive applications, TI will not be responsible for any failure to meet such requirements.

Following are URLs where you can obtain information on other Texas Instruments products and application solutions:

<b>Products</b>		<b>Applications</b>	
Amplifiers	<a href="http://amplifier.ti.com">amplifier.ti.com</a>	Audio	<a href="http://www.ti.com/audio">www.ti.com/audio</a>
Data Converters	<a href="http://dataconverter.ti.com">dataconverter.ti.com</a>	Automotive	<a href="http://www.ti.com/automotive">www.ti.com/automotive</a>
DLP® Products	<a href="http://www.dlp.com">www.dlp.com</a>	Communications and Telecom	<a href="http://www.ti.com/communications">www.ti.com/communications</a>
DSP	<a href="http://dsp.ti.com">dsp.ti.com</a>	Computers and Peripherals	<a href="http://www.ti.com/computers">www.ti.com/computers</a>
Clocks and Timers	<a href="http://www.ti.com/clocks">www.ti.com/clocks</a>	Consumer Electronics	<a href="http://www.ti.com/consumer-apps">www.ti.com/consumer-apps</a>
Interface	<a href="http://interface.ti.com">interface.ti.com</a>	Energy	<a href="http://www.ti.com/energy">www.ti.com/energy</a>
Logic	<a href="http://logic.ti.com">logic.ti.com</a>	Industrial	<a href="http://www.ti.com/industrial">www.ti.com/industrial</a>
Power Mgmt	<a href="http://power.ti.com">power.ti.com</a>	Medical	<a href="http://www.ti.com/medical">www.ti.com/medical</a>
Microcontrollers	<a href="http://microcontroller.ti.com">microcontroller.ti.com</a>	Security	<a href="http://www.ti.com/security">www.ti.com/security</a>
RFID	<a href="http://www.ti-rfid.com">www.ti-rfid.com</a>	Space, Avionics & Defense	<a href="http://www.ti.com/space-avionics-defense">www.ti.com/space-avionics-defense</a>
RF/IF and ZigBee® Solutions	<a href="http://www.ti.com/lprf">www.ti.com/lprf</a>	Video and Imaging	<a href="http://www.ti.com/video">www.ti.com/video</a>
		Wireless	<a href="http://www.ti.com/wireless-apps">www.ti.com/wireless-apps</a>

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265  
Copyright © 2010, Texas Instruments Incorporated

[www.BDTIC.com/TI](http://www.BDTIC.com/TI)