

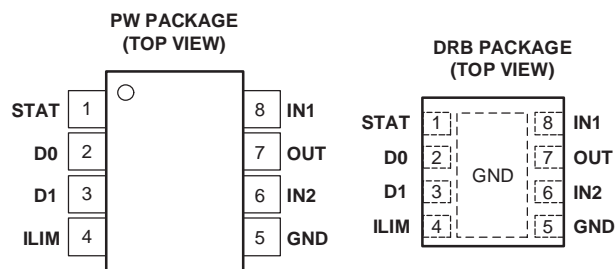
AUTOSWITCHING POWER MUX

FEATURES

- Two-Input, One-Output Power Multiplexer With Low $r_{DS(on)}$ Switches:
 - 84 mΩ Typ (TPS2115A)
 - 120 mΩ Typ (TPS2114A)
- Reverse and Cross-Conduction Blocking
- Wide Operating Voltage Range . . . 2.8 V to 5.5 V
- Low Standby Current 0.5-μA Typ
- Low Operating Current 55-μA Typ
- Adjustable Current Limit
- Controlled Output Voltage Transition Times, Limits Inrush Current and Minimizes Output Voltage Hold-Up Capacitance
- CMOS- and TTL-Compatible Control Inputs
- Manual and Auto-Switching Operating Modes
- Thermal Shutdown
- Available in TSSOP-8 and 3mm x 3mm SON-8 Packages

APPLICATIONS

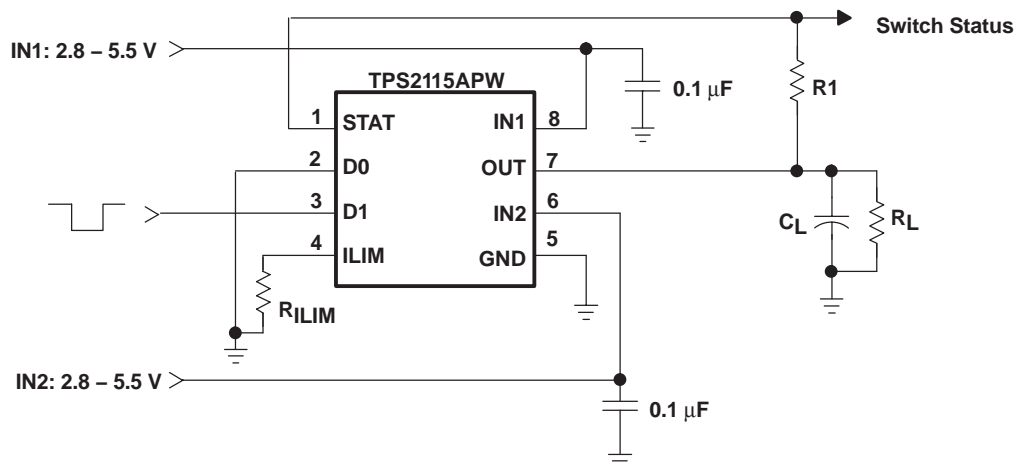
- PCs
- PDAs
- Digital Cameras
- Modems
- Cell Phones
- Digital Radios
- MP3 Players



DESCRIPTION

The TPS211xA family of power multiplexers enables seamless transition between two power supplies, such as a battery and a wall adapter, each operating at 2.8–5.5 V and delivering up to 1 A. The TPS211xA family includes extensive protection circuitry, including user-programmable current limiting, thermal protection, inrush current control, seamless supply transition, cross-conduction blocking, and reverse-conduction blocking. These features greatly simplify designing power multiplexer applications.

TYPICAL APPLICATION



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

All trademarks are the property of their respective owners.



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

AVAILABLE OPTIONS

FEATURE		TPS2114A	TPS2115A
Current Limit Adjustment Range		0.31–0.75A	0.63–1.25A
Switching Modes	Manual	Yes	Yes
	Automatic	Yes	Yes
Switch Status Output		Yes	Yes
Package	TSSOP-8		TSSOP-8
			SON-8

ORDERING INFORMATION

T _A	PACKAGE	ORDERING NUMBER ⁽¹⁾	MARKINGS
–40°C to 85°C	TSSOP-8 (PW)	TPS2114APW	2114A
		TPS2115APW	2115A
	SON-8 (DRB)	TPS2115ADRB	2115A

(1) The PW package is available taped and reeled. Add an R suffix to the device type (e.g., TPS2114APWR) to indicate tape and reel.

PACKAGE DISSIPATION RATINGS

PACKAGE	DERATING FACTOR ABOVE T _A = 25°C	T _A ≤ 25°C POWER RATING	T _A = 70°C POWER RATING	T _A = 85°C POWER RATING
TSSOP-8 (PW)	3.9 mW/°C	387 mW	213 mW	155 mW
SON-8 (DRB)	25.0 mW/°C	2.50 W	1.38 W	1.0 W

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range unless otherwise noted⁽¹⁾

		TPS2114A, TPS2115A
Input voltage range at pins IN1, IN2, D0, D1, ILIM ⁽²⁾		–0.3 V to 6 V
Output voltage range, V _{O(OUT)} , V _{O(STAT)} ⁽²⁾		–0.3 V to 6 V
Output sink current, I _{O(STAT)}		5 mA
Continuous output current, I _O	TPS2114A	0.9 A
	TPS2115A	1.5 A
Continuous total power dissipation		See Dissipation Rating Table
Operating virtual junction temperature range, T _J		–40°C to 125°C
Storage temperature range, T _{stg}		–65°C to 150°C
Lead temperature soldering 1.6 mm (1/16 inch) from case for 10 seconds		260°C

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) All voltages are with respect to GND.

RECOMMENDED OPERATING CONDITIONS

		MIN	MAX	UNIT
Input voltage at IN1, V _{I(IN1)}	V _{I(IN2)} ≥ 2.8 V	1.5	5.5	V
	V _{I(IN2)} < 2.8 V	2.8	5.5	
Input voltage at IN2, V _{I(IN2)}	V _{I(IN1)} ≥ 2.8 V	1.5	5.5	V
	V _{I(IN1)} < 2.8 V	2.8	5.5	
Input voltage, V _{I(D0)} , V _{I(D1)}		0	5.5	V
Current limit adjustment range, I _{O(OUT)}	TPS2114A	0.31	0.75	A
	TPS2115A	0.63	1.25	
Operating virtual junction temperature, T _J		–40	125	°C

ELECTROSTATIC DISCHARGE (ESD) PROTECTION

	MIN	MAX	UNIT
Human body model		2	kV
CDM		500	V

ELECTRICAL CHARACTERISTICS

over recommended operating junction temperature range, $V_{I(IN1)} = V_{I(IN2)} = 5.5\text{ V}$, $R_{LIM} = 400\ \Omega$ (unless otherwise noted)

PARAMETER	TEST CONDITIONS		TPS2114A			TPS2115A			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
POWER SWITCH									
$r_{DS(on)}^{(1)}$ Drain-source on-state resistance (INx–OUT)	$T_J = 25^{\circ}\text{C}$, $I_L = 500\text{ mA}$	$V_{I(IN1)} = V_{I(IN2)} = 5.0\text{ V}$	120	140		84	110	mΩ	
		$V_{I(IN1)} = V_{I(IN2)} = 3.3\text{ V}$	120	140		84	110		
		$V_{I(IN1)} = V_{I(IN2)} = 2.8\text{ V}$	120	140		84	110		
	$T_J = 125^{\circ}\text{C}$, $I_L = 500\text{ mA}$	$V_{I(IN1)} = V_{I(IN2)} = 5.0\text{ V}$		220		150		mΩ	
		$V_{I(IN1)} = V_{I(IN2)} = 3.3\text{ V}$		220		150			
		$V_{I(IN1)} = V_{I(IN2)} = 2.8\text{ V}$		220		150			

(1) The TPS211xA can switch a voltage as low as 1.5 V as long as there is a minimum of 2.8 V at one of the input power pins. In this specific case, the lower supply voltage has no effect on the IN1 and IN2 switch on-resistances.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
LOGIC INPUTS (D0 AND D1)					
V _{IH} High-level input voltage		2			V
V _{IL} Low-level input voltage				0.7	V
Input current at D0 or D1	D0 or D1 = High, sink current			1	μA
	D0 or D1 = Low, source current	0.5	1.4	5	
SUPPLY AND LEAKAGE CURRENTS					
Supply current from IN1 (operating)	D1 = High, D0 = Low (IN1 active), V _{I(IN1)} = 5.5 V, V _{I(IN2)} = 3.3 V, I _{O(OUT)} = 0 A		55	90	μA
	D1 = High, D0 = Low (IN1 active), V _{I(IN1)} = 3.3 V, V _{I(IN2)} = 5.5 V, I _{O(OUT)} = 0 A		1	12	
	D0 = D1 = Low (IN2 active), V _{I(IN1)} = 5.5 V, V _{I(IN2)} = 3.3 V, I _{O(OUT)} = 0 A			75	
	D0 = D1 = Low (IN2 active), V _{I(IN1)} = 3.3 V, V _{I(IN2)} = 5.5 V, I _{O(OUT)} = 0 A			1	
Supply current from IN2 (operating)	D1 = High, D0 = Low (IN1 active), V _{I(IN1)} = 5.5 V, V _{I(IN2)} = 3.3 V, I _{O(OUT)} = 0 A			1	μA
	D1 = High, D0 = Low (IN1 active), V _{I(IN1)} = 3.3 V, V _{I(IN2)} = 5.5 V, I _{O(OUT)} = 0 A			75	
	D0 = D1 = Low (IN2 active), V _{I(IN1)} = 5.5 V, V _{I(IN2)} = 3.3 V, I _{O(OUT)} = 0 A		1	12	
	D0 = D1 = Low (IN2 active), V _{I(IN1)} = 3.3 V, V _{I(IN2)} = 5.5 V, I _{O(OUT)} = 0 A		55	90	
Quiescent current from IN1 (STANDBY)	D0 = D1 = High (inactive), V _{I(IN1)} = 5.5 V, V _{I(IN2)} = 3.3 V, I _{O(OUT)} = 0 A		0.5	2	μA
	D0 = D1 = High (inactive), V _{I(IN1)} = 3.3 V, V _{I(IN2)} = 5.5 V, I _{O(OUT)} = 0 A			1	
Quiescent current from IN2 (STANDBY)	D0 = D1 = High (inactive), V _{I(IN1)} = 5.5 V, V _{I(IN2)} = 3.3 V, I _{O(OUT)} = 0 A			1	μA
	D0 = D1 = High (inactive), V _{I(IN1)} = 3.3 V, V _{I(IN2)} = 5.5 V, I _{O(OUT)} = 0 A		0.5	2	
Forward leakage current from IN1 (measured from OUT to GND)	D0 = D1 = High (inactive), V _{I(IN1)} = 5.5 V, IN2 open, V _{O(OUT)} = 0 V (shorted), T _J = 25°C		0.1	5	μA
Forward leakage current from IN2 (measured from OUT to GND)	D0 = D1 = High (inactive), V _{I(IN2)} = 5.5 V, IN1 open, V _{O(OUT)} = 0 V (shorted), T _J = 25°C		0.1	5	μA
Reverse leakage current to INx (measured from INx to GND)	D0 = D1 = High (inactive), V _{I(INx)} = 0 V, V _{O(OUT)} = 5.5 V, T _J = 25°C		0.3	5	μA

ELECTRICAL CHARACTERISTICS (Continued)

over recommended operating junction temperature range, $V_{I(IN1)} = V_{I(IN2)} = 5.5\text{ V}$, $R_{ILIM} = 400\ \Omega$ (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
CURRENT LIMIT CIRCUIT						
Current limit accuracy	TPS2114A	$R_{ILIM} = 400\ \Omega$	0.51	0.63	0.80	A
		$R_{ILIM} = 700\ \Omega$	0.30	0.36	0.50	
	TPS2115A	$R_{ILIM} = 400\ \Omega$	0.95	1.25	1.56	
		$R_{ILIM} = 700\ \Omega$	0.47	0.71	0.99	
t_d	Current limit settling time ⁽¹⁾		Time for short-circuit output current to settle within 10% of its steady state value.			ms
Input current at ILIM		$V_{I(ILIM)} = 0\text{ V}$, $I_{O(OUT)} = 0\text{ A}$	-15		0	μA

(1) Not tested in production.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
UVLO						
IN1 and IN2 UVLO	Falling edge		1.15	1.25		V
	Rising edge			1.30	1.35	
IN1 and IN2 UVLO hysteresis ⁽¹⁾			30	57	65	mV
Internal V_{DD} UVLO (the higher of IN1 and IN2)	Falling edge		2.4	2.53		V
	Rising edge			2.58	2.8	
Internal V_{DD} UVLO hysteresis ⁽¹⁾			30	50	75	mV
UVLO deglitch for IN1, IN2 ⁽¹⁾		Falling edge		110		μs

(1) Not tested in production.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
REVERSE CONDUCTION BLOCKING						
$\Delta V_{O(I_block)}$	Minimum input-to-output voltage difference to block switching	$D0 = D1 = \text{high}$, $V_{I(INx)} = 3.3\text{ V}$. Connect OUT to a 5 V supply through a series 1-k Ω resistor. Let D0 = low. Slowly decrease the supply voltage until OUT connects to IN1.	80	100	120	mV

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
THERMAL SHUTDOWN					
Thermal shutdown threshold ⁽¹⁾	TPS211xA is in current limit.	135			°C
Recovery from thermal shutdown ⁽¹⁾	TPS211xA is in current limit.	125			
Hysteresis ⁽¹⁾			10		
IN2-IN1 COMPARATORS					
Hysteresis of IN2-IN1 comparator		0.1		0.2	V
Deglitch of IN2-IN1 comparator (both ↑↓) ⁽¹⁾		10	20	50	μs

(1) Not tested in production.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
STAT OUTPUT						
Leakage current		$V_{O(STAT)} = 5.5\text{ V}$		0.01	1	μA
Saturation voltage		$I_{I(STAT)} = 2\text{ mA}$, IN1 switch is on		0.13	0.4	V
Deglitch time (falling edge only)				150		μs

SWITCHING CHARACTERISTICS

over recommended operating junction temperature range, $V_{I(IN1)} = V_{I(IN2)} = 5.5\text{ V}$, $R_{ILIM} = 400\ \Omega$ (unless otherwise noted)

PARAMETER		TEST CONDITIONS	TPS2114A			TPS2115A			UNIT				
			MIN	TYP	MAX	MIN	TYP	MAX					
POWER SWITCH													
t _r	Output rise time from an enable ⁽¹⁾	V _I (IN1) = V _I (IN2) = 5 V	T _J = 25°C, C _L = 1 μF, I _L = 500 mA, See Figure 1(a)		0.5	1.0	1.5	1	1.8	3	ms		
t _f	Output fall time from a disable ⁽¹⁾	V _I (IN1) = V _I (IN2) = 5 V	T _J = 25°C, C _L = 1 μF, I _L = 500 mA, See Figure 1(a)		0.35	0.5	0.7	0.5	1	2	ms		
t _t	Transition time ⁽¹⁾	IN1 to IN2 transition, V _I (IN1) = 3.3 V, V _I (IN2) = 5 V	T _J = 125°C, C _L = 10 μF, I _L = 500 mA [Measure transition time as 10–90% rise time or from 3.4 V to 4.8 V on V _O (OUT)], See Figure 1(b)		40		60	40		60	μs		
		40			60	40		60					
t _{PLH1}	Turn-on propagation delay from enable ⁽¹⁾	V _I (IN1) = V _I (IN2) = 5 V Measured from enable to 10% of V _O (OUT)	T _J = 25°C, C _L = 10 μF, I _L = 500 mA, See Figure 1(a)		0.5		1		ms				
t _{PHL1}	Turn-off propagation delay from a disable ⁽¹⁾	V _I (IN1) = V _I (IN2) = 5 V, Measured from disable to 90% of V _O (OUT)	T _J = 25°C, C _L = 10 μF, I _L = 500 mA, See Figure 1(a)		3		5		ms				
t _{PLH2}	Switch-over rising propagation delay ⁽¹⁾	Logic 1 to Logic 0 transition on D1, V _I (IN1) = 1.5 V, V _I (IN2) = 5 V, V _I (D0) = 0 V, Measured from D1 to 10% of V _O (OUT)	T _J = 25°C, C _L = 10 μF, I _L = 500 mA, See Figure 1(c)		40		100	40		100	μs		
t _{PHL2}	Switch-over falling propagation delay ⁽¹⁾	Logic 0 to Logic 1 transition on D1, V _I (IN1) = 1.5V, V _I (IN2) = 5V, V _I (D0) = 0 V, Measured from D1 to 90% of V _O (OUT)	T _J = 25°C, C _L = 10 μF, I _L = 500 mA, See Figure 1(c)		2		3	10	2		5	10	ms

⁽¹⁾ Not tested in production.

TRUTH TABLE

D1	D0	$V_I(IN2) > V_I(IN1)$	STAT	OUT ⁽¹⁾
0	0	X	Hi-Z	IN2
0	1	No	0	IN1
0	1	Yes	Hi-Z	IN2
1	0	X	0	IN1
1	1	X	0	Hi-Z

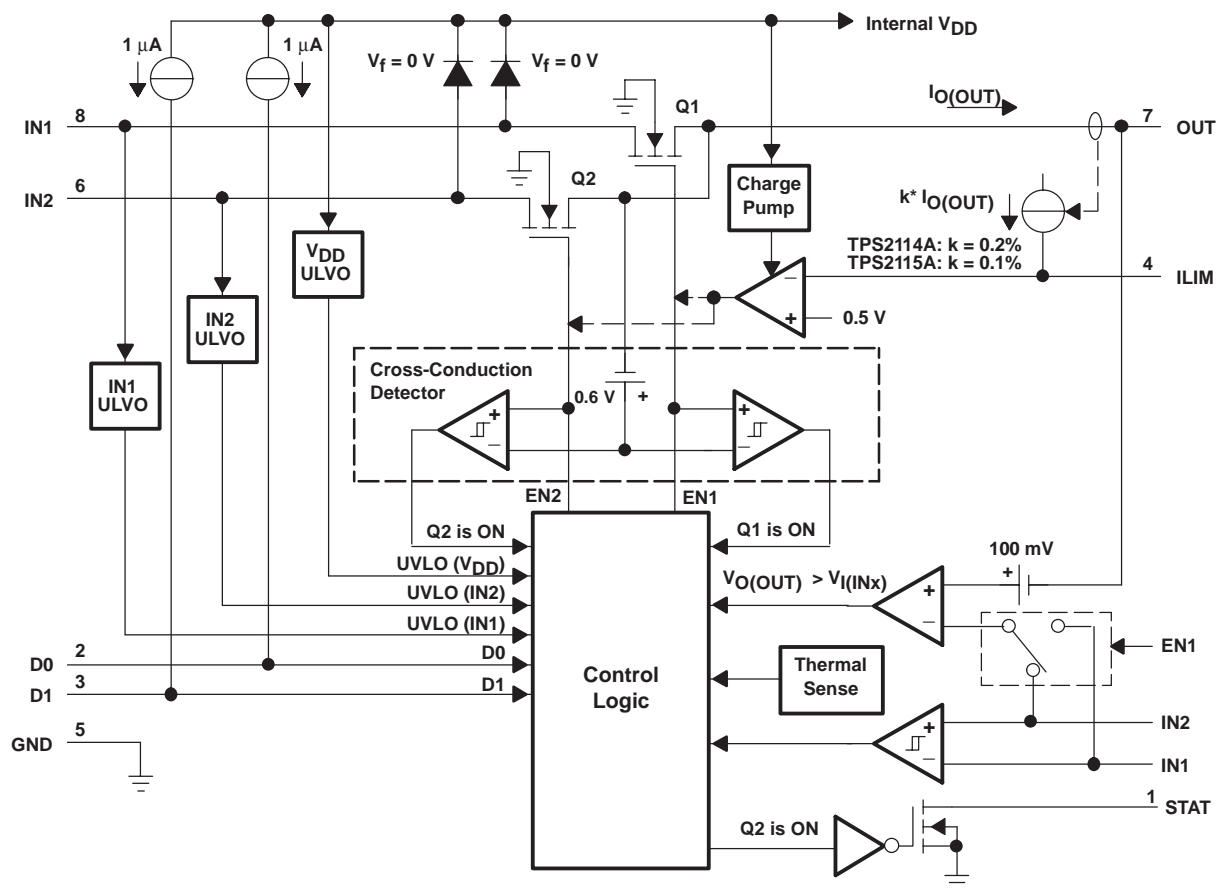
X = Don't care.

⁽¹⁾The under-voltage lockout circuit causes the output OUT to go Hi-Z if the selected power supply does not exceed the IN1/IN2 UVLO, or if neither of the supplies exceeds the internal V_{DD} UVLO

Terminal Functions

TERMINAL NAME	NO.	I/O	DESCRIPTION
D0	2	I	TTL- and CMOS-compatible input pins. Each pin has a 1- μ A pull-up. The truth table shown above illustrates the functionality of D0 and D1.
D1	3	I	
GND	5	I	Ground
IN1	8	I	Primary power switch input. The IN1 switch can be enabled only if the IN1 supply is above the UVLO threshold and at least one supply exceeds the internal V_{DD} UVLO.
IN2	6	I	Secondary power switch input. The IN2 switch can be enabled only if the IN2 supply is above the UVLO threshold and at least one supply exceeds the internal V_{DD} UVLO.
ILIM	4	I	A resistor R_{ILIM} from ILIM to GND sets the current limit I_L to $250/R_{ILIM}$ and $500/R_{ILIM}$ for the TPS2114A and TPS2115A, respectively.
OUT	7	O	Power switch output
STAT	1	O	STAT is an open-drain output that is Hi-Z if the IN2 switch is ON. STAT pulls low if the IN1 switch is ON or if OUT is Hi-Z (i.e., \overline{EN} is equal to logic 0).

FUNCTIONAL BLOCK DIAGRAM



PARAMETER MEASUREMENT INFORMATION

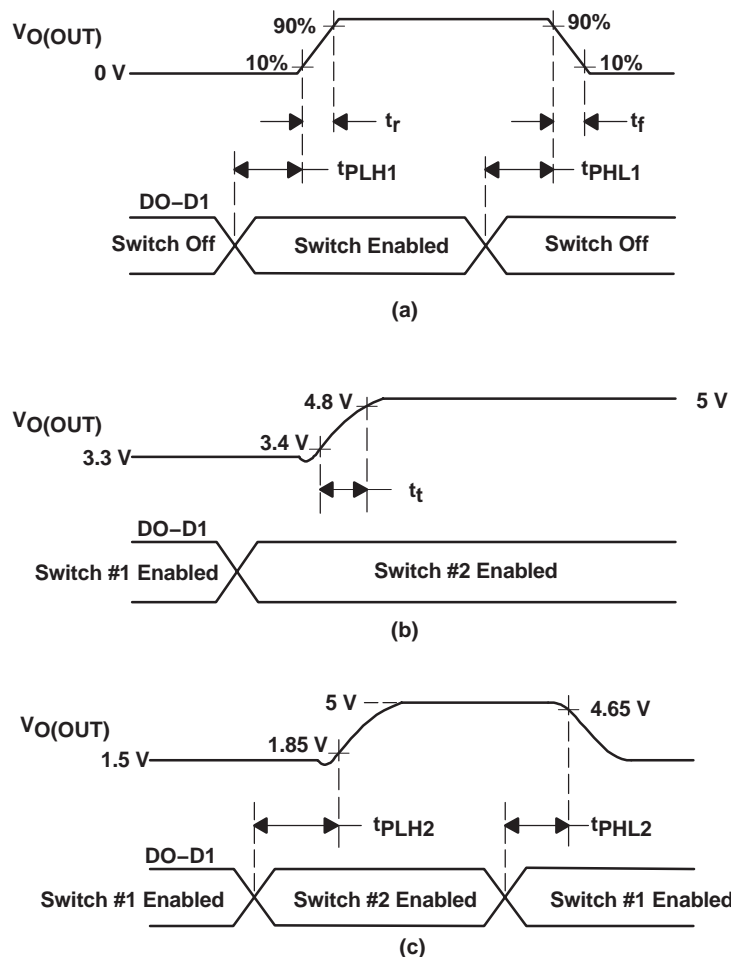
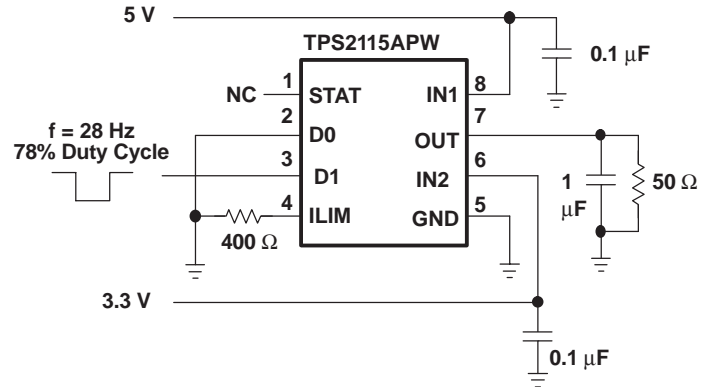
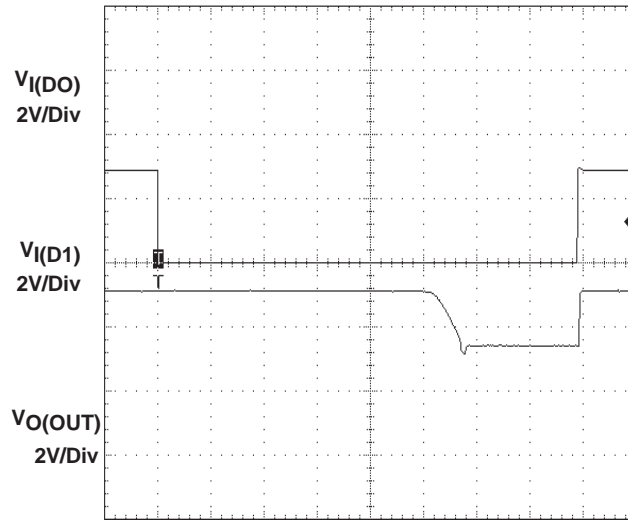


Figure 1. Propagation Delays and Transition Timing Waveforms

TYPICAL CHARACTERISTICS

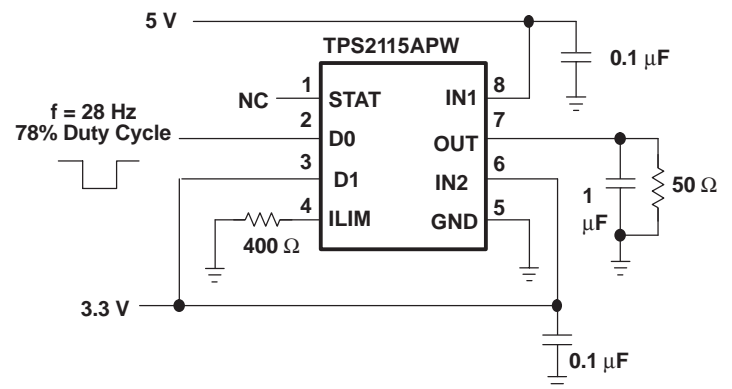
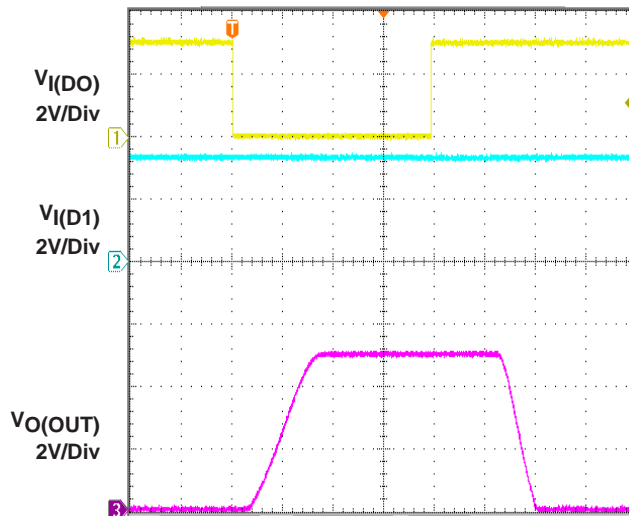
OUTPUT SWITCHOVER RESPONSE



Output Switchover Response Test Circuit

Figure 2

OUTPUT TURN-ON RESPONSE

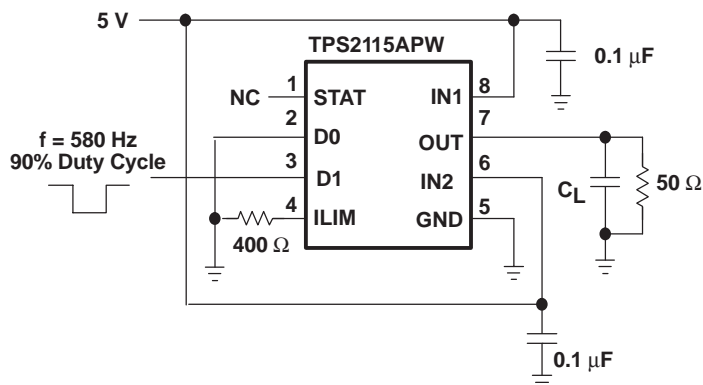
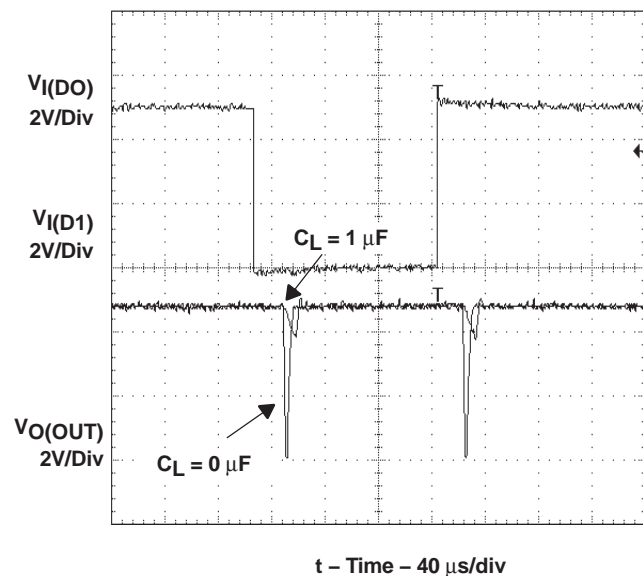


Output Turn-On Response Test Circuit

Figure 3

TYPICAL CHARACTERISTICS

OUTPUT SWITCHOVER VOLTAGE DROOP

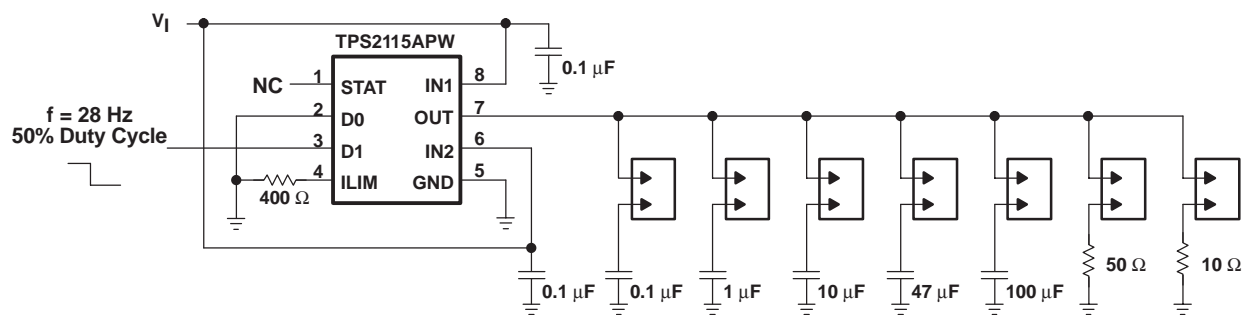
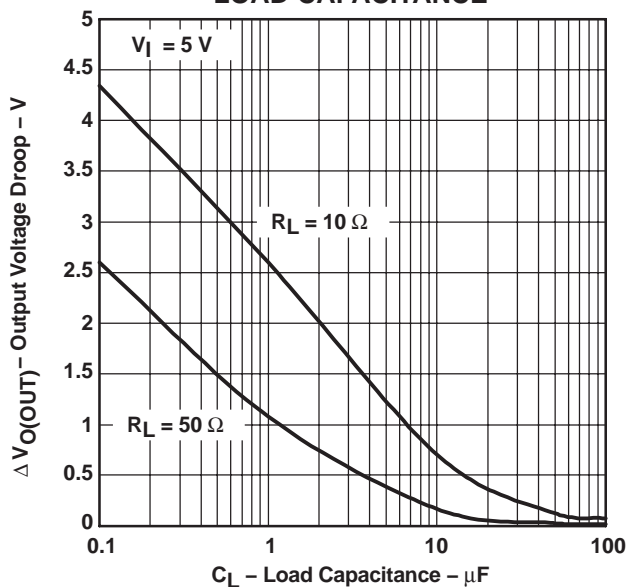


Output Switchover Voltage Droop Test Circuit

Figure 4

TYPICAL CHARACTERISTICS

OUTPUT SWITCHOVER VOLTAGE DROOP vs LOAD CAPACITANCE

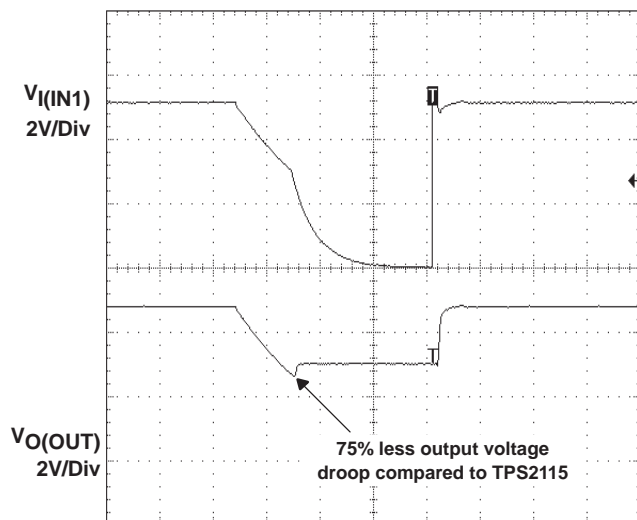


Output Switchover Voltage Droop Test Circuit

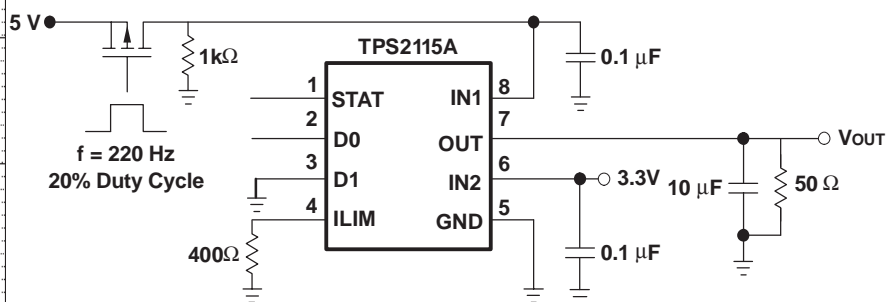
Figure 5

TYPICAL CHARACTERISTICS

AUTO SWITCHOVER VOLTAGE DROOP



t – Time – 250 μ s/div

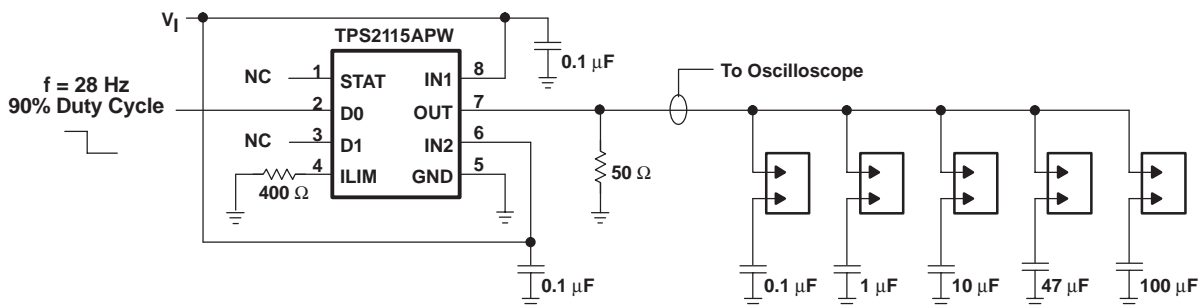
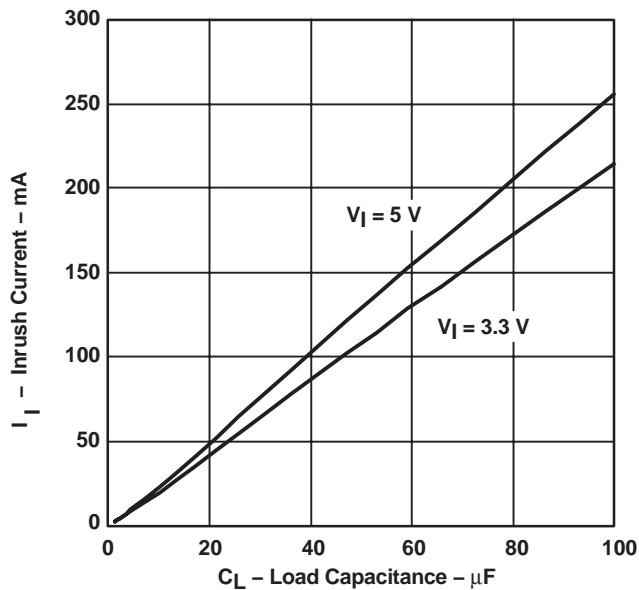


Auto Switchover Voltage Droop Test Circuit

Figure 6

TYPICAL CHARACTERISTICS

INRUSH CURRENT VS LOAD CAPACITANCE



Output Capacitor Inrush Current Test Circuit

Figure 7

TYPICAL CHARACTERISTICS

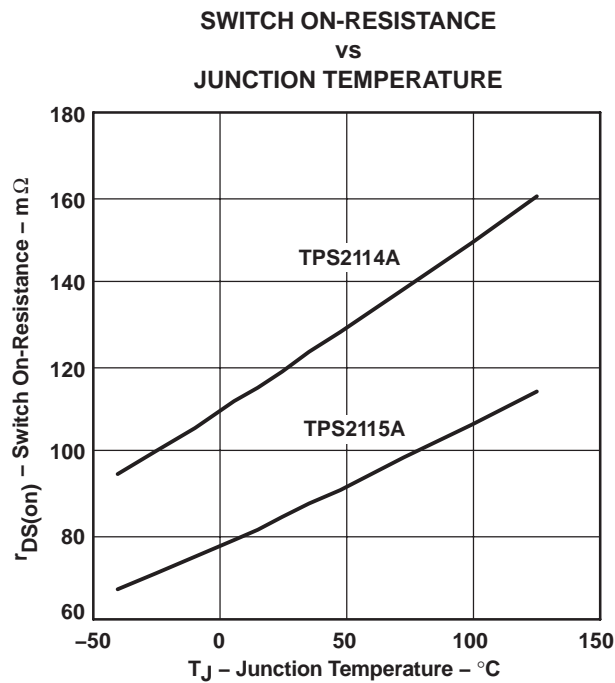


Figure 8

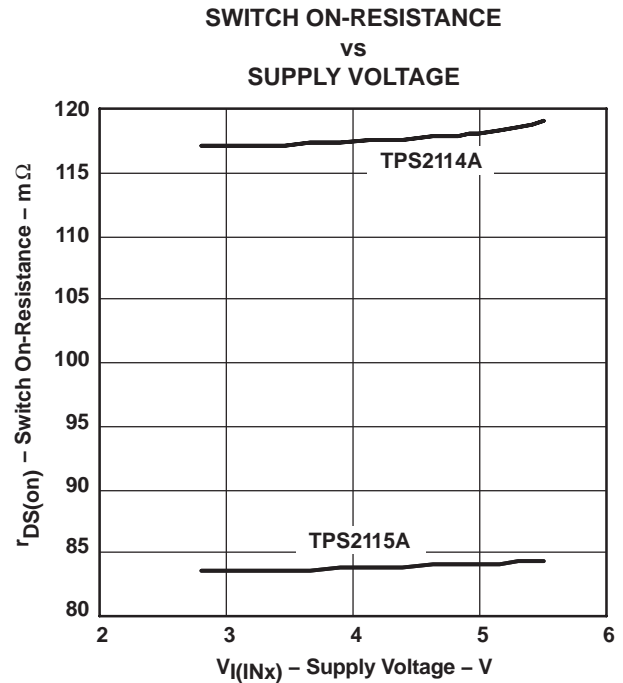


Figure 9

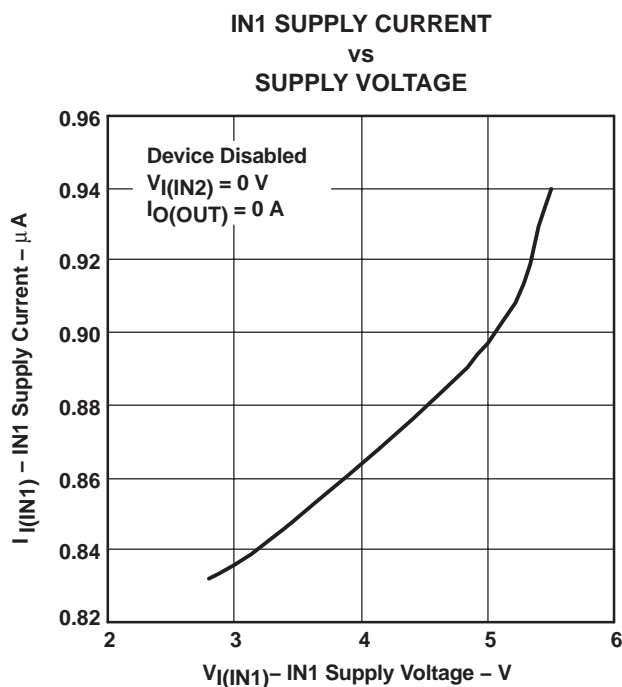


Figure 10

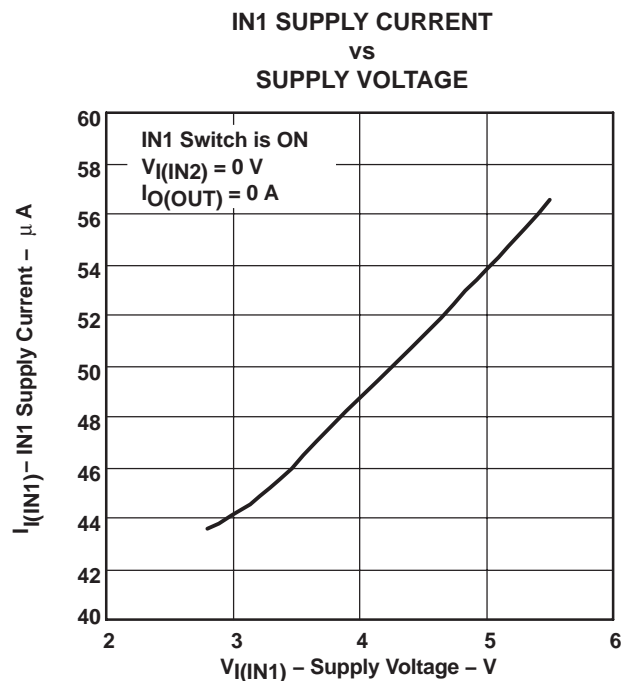
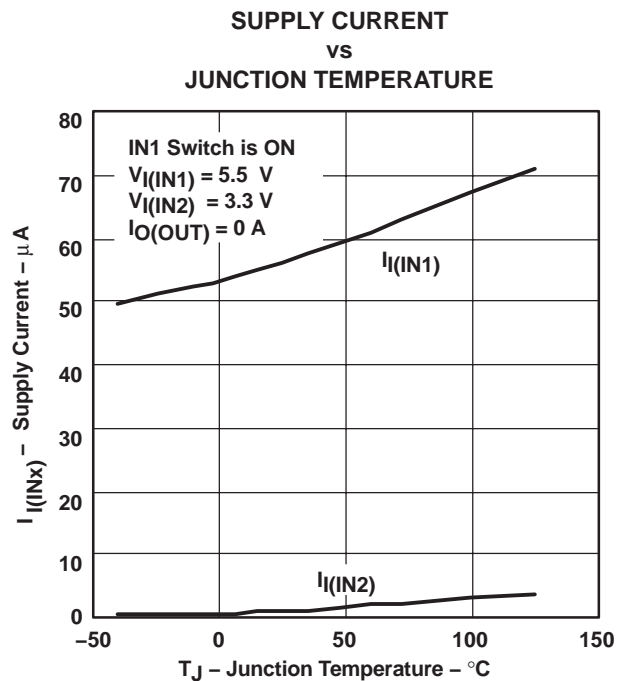
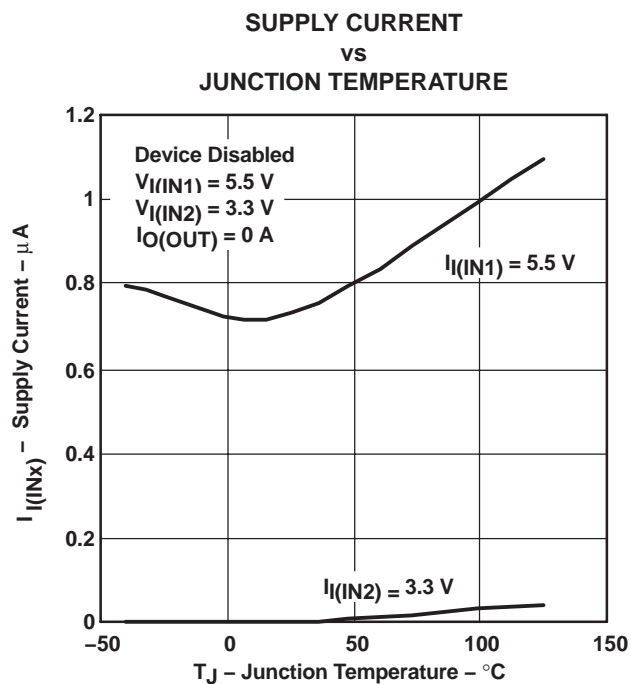


Figure 11

TYPICAL CHARACTERISTICS



APPLICATION INFORMATION

Some applications have two energy sources, one of which should be used in preference to another. Figure 14 shows a circuit that will connect IN1 to OUT until the voltage at IN1 falls below a user-specified value. Once the voltage on IN1 falls below this value, the TPS2114A/5A will select the higher of the two supplies. This usually means that the TPS2114A/5A will swap to IN2.

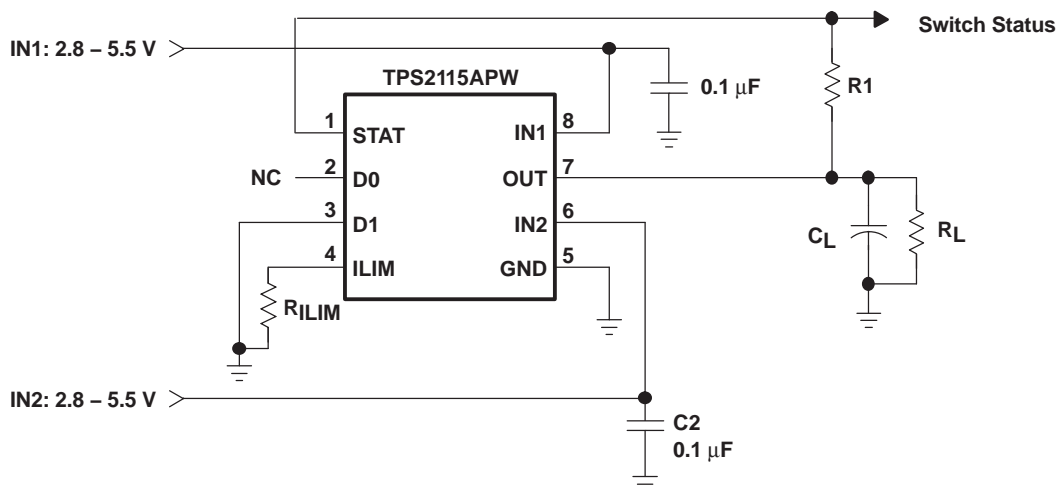


Figure 14. Auto-Selecting for a Dual Power Supply Application

In Figure 15, the multiplexer selects between two power supplies based upon the D1 logic signal. OUT connects to IN1 if D1 is logic 1; otherwise, OUT connects to IN2. The logic thresholds for the D1 terminal are compatible with both TTL and CMOS logic.

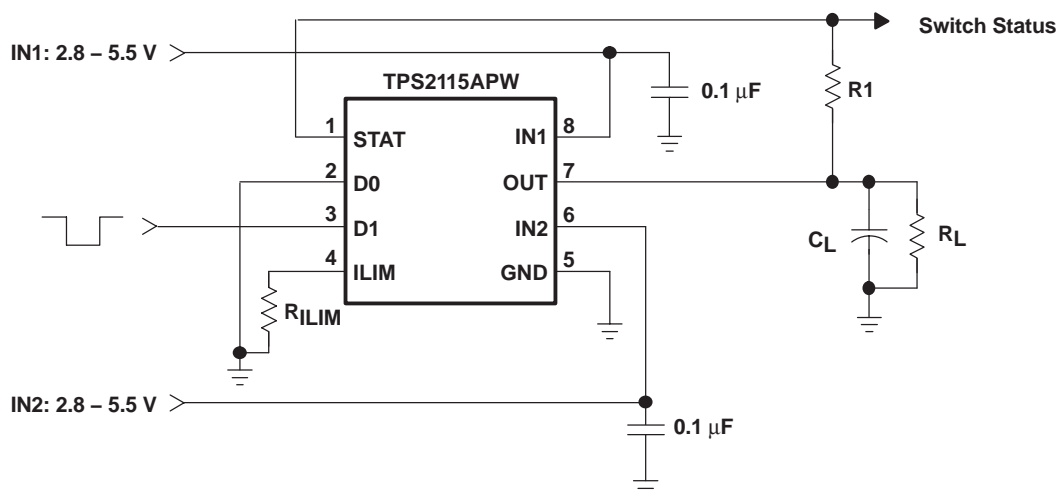


Figure 15. Manually Switching Power Sources

DETAILED DESCRIPTION

AUTO-SWITCHING MODE

D0 equal to logic 1 and D1 equal to logic 0 selects the auto-switching mode. In this mode, OUT connects to the higher of IN1 and IN2.

MANUAL SWITCHING MODE

D0 equal to logic 0 selects the manual-switching mode. In this mode, OUT connects to IN1 if D1 is equal to logic 1, otherwise OUT connects to IN2.

N-CHANNEL MOSFETs

Two internal high-side power MOSFETs implement a single-pole double-throw (SPDT) switch. Digital logic selects the IN1 switch, IN2 switch, or no switch (Hi-Z state). The MOSFETs have no parallel diodes so output-to-input current cannot flow when the FET is off. An integrated comparator prevents turn-on of a FET switch if the output voltage is greater than the input voltage.

CROSS-CONDUCTION BLOCKING

The switching circuitry ensures that both power switches will never conduct at the same time. A comparator monitors the gate-to-source voltage of each power FET and allows a FET to turn on only if the gate-to-source voltage of the other FET is below the turn-on threshold voltage.

REVERSE-CONDUCTION BLOCKING

When the TPS211xA switches from a higher-voltage supply to a lower-voltage supply, current can potentially flow back from the load capacitor into the lower-voltage supply. To minimize such reverse conduction, the TPS211xA will not connect a supply to the output until the output voltage has fallen to within 100 mV of the supply voltage. Once a supply has been connected to the output, it will remain connected regardless of output voltage.

CHARGE PUMP

The higher of supplies IN1 and IN2 powers the internal charge pump. The charge pump provides power to the current limit amplifier and allows the output FET gate voltage to be higher than the IN1 and IN2 supply voltages. A gate voltage that is higher than the source voltage is necessary to turn on the N-channel FET.

CURRENT LIMITING

A resistor R_{ILIM} from ILIM to GND sets the current limit to $250/R_{ILIM}$ and $500/R_{ILIM}$ for the TPS2114A and TPS2115A, respectively. Setting resistor R_{ILIM} equal to zero is not recommended as that disables current limiting.

OUTPUT VOLTAGE SLEW-RATE CONTROL

The TPS2114A/5A slews the output voltage at a slow rate when OUT switches to IN1 or IN2 from the Hi-Z state (see *Truth Table*). A slow slew rate limits the inrush current into the load capacitor. High inrush currents can glitch the voltage bus and cause a system to hang up or reset. It can also cause reliability issues—like pit the connector power contacts, when hot-plugging a load such as a PCI card. The TPS2114A/5A slews the output voltage at a much faster rate when OUT switches between IN1 and IN2. The fast rate minimizes the output voltage droop and reduces the output voltage hold-up capacitance requirement.

PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp ⁽³⁾
TPS2114APW	ACTIVE	TSSOP	PW	8	150	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS2114APWG4	ACTIVE	TSSOP	PW	8	150	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS2114APWR	ACTIVE	TSSOP	PW	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS2114APWRG4	ACTIVE	TSSOP	PW	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS2115ADRBR	ACTIVE	SON	DRB	8	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
TPS2115ADRBRG4	ACTIVE	SON	DRB	8	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
TPS2115ADRBT	ACTIVE	SON	DRB	8	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
TPS2115ADRBTG4	ACTIVE	SON	DRB	8	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
TPS2115APW	ACTIVE	TSSOP	PW	8	150	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS2115APWG4	ACTIVE	TSSOP	PW	8	150	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS2115APWR	ACTIVE	TSSOP	PW	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS2115APWRG4	ACTIVE	TSSOP	PW	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

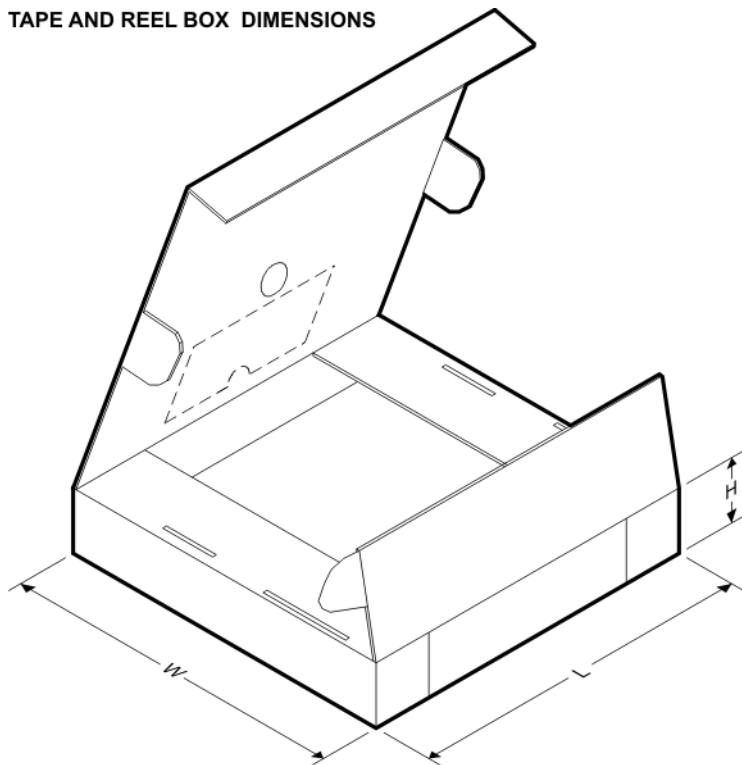
TAPE AND REEL INFORMATION



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS2114APWR	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1
TPS2115ADRBR	SON	DRB	8	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS2115ADRBT	SON	DRB	8	250	180.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS2115APWR	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS

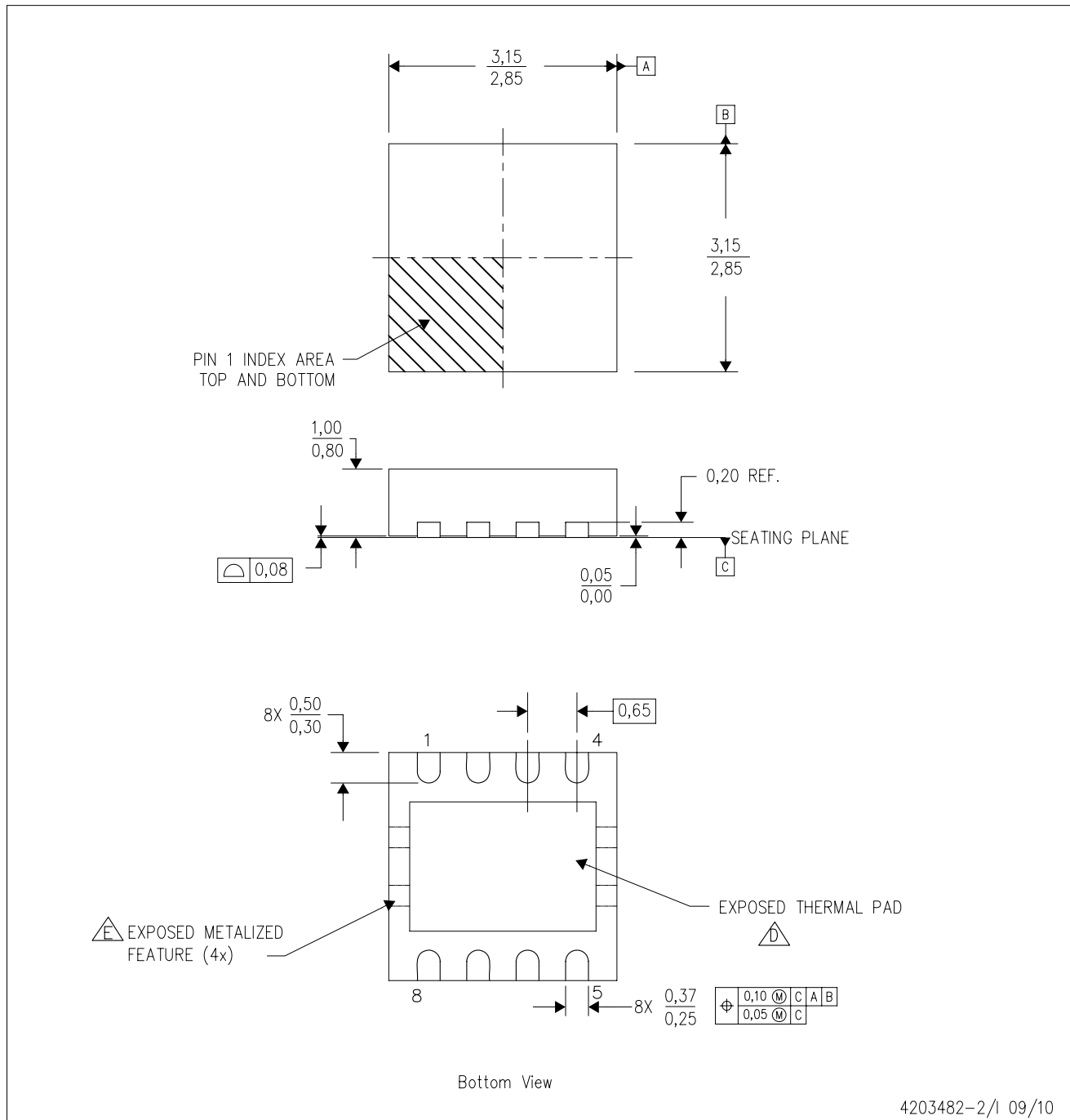


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS2114APWR	TSSOP	PW	8	2000	346.0	346.0	29.0
TPS2115ADRBR	SON	DRB	8	3000	346.0	346.0	29.0
TPS2115ADRBT	SON	DRB	8	250	190.5	212.7	31.8
TPS2115APWR	TSSOP	PW	8	2000	346.0	346.0	29.0

DRB (S-PVSON-N8)

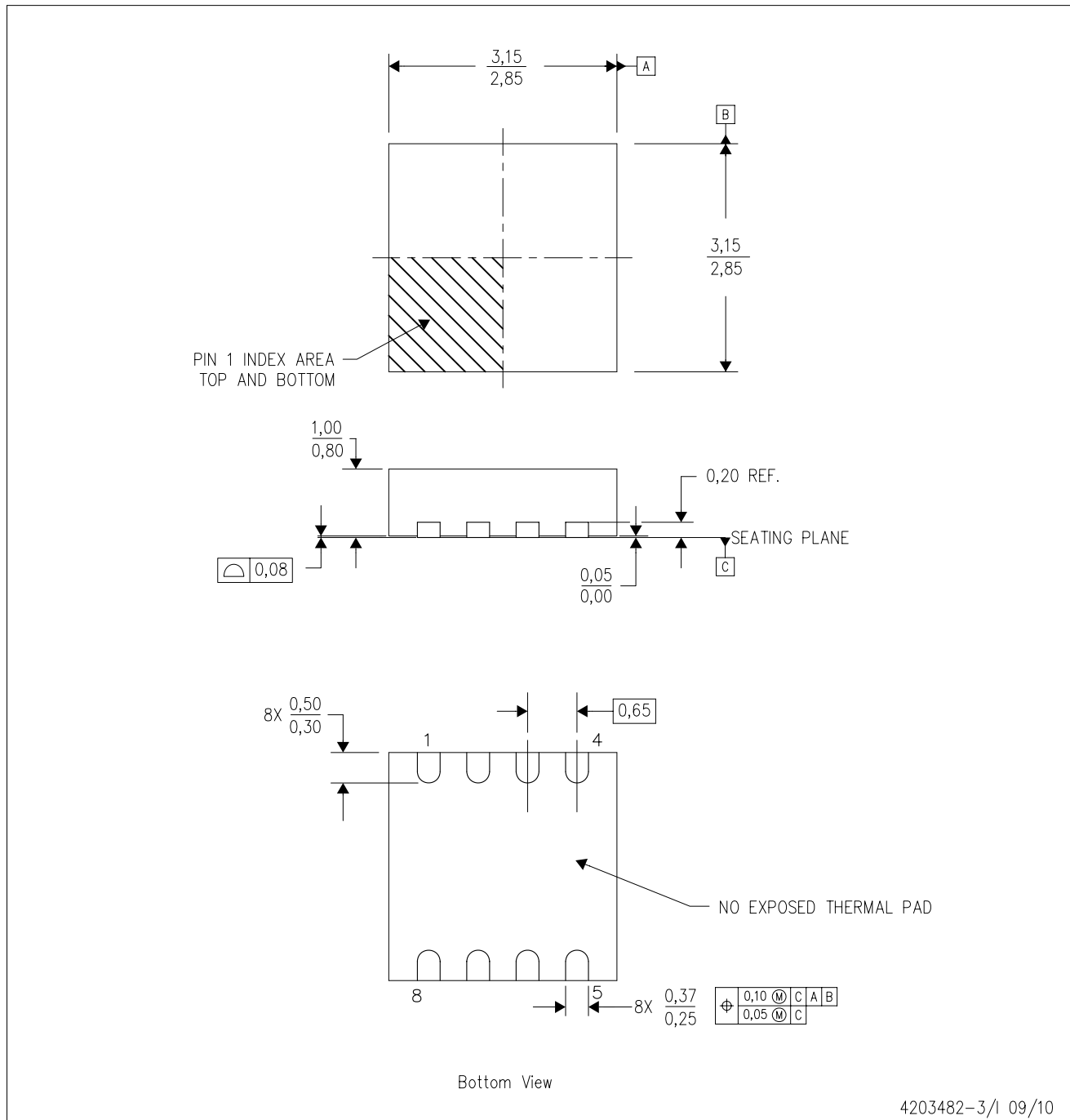
PLASTIC SMALL OUTLINE NO-LEAD



- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
 - B. This drawing is subject to change without notice.
 - C. Small Outline No-Lead (SON) package configuration.
 - The package thermal pad must be soldered to the board for thermal and mechanical performance.
 - See the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.

DRB (S-PVSON-N8)

PLASTIC SMALL OUTLINE NO-LEAD



- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
 - B. This drawing is subject to change without notice.
 - C. Small Outline No-Lead (SON) package configuration.

THERMAL PAD MECHANICAL DATA

DRB (S-PVSON-N8)

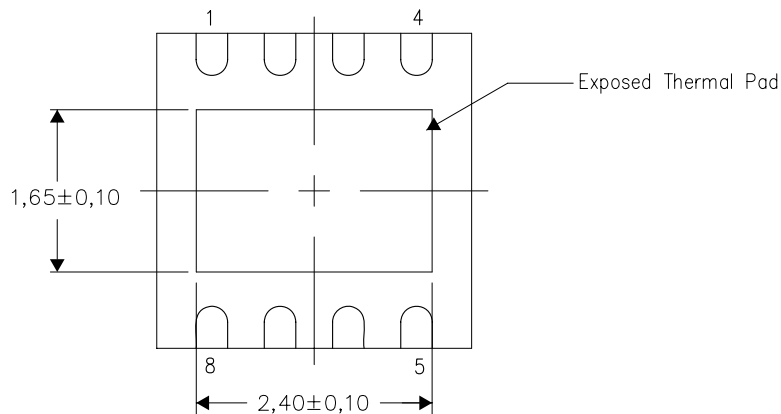
PLASTIC SMALL OUTLINE NO-LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No-Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Bottom View

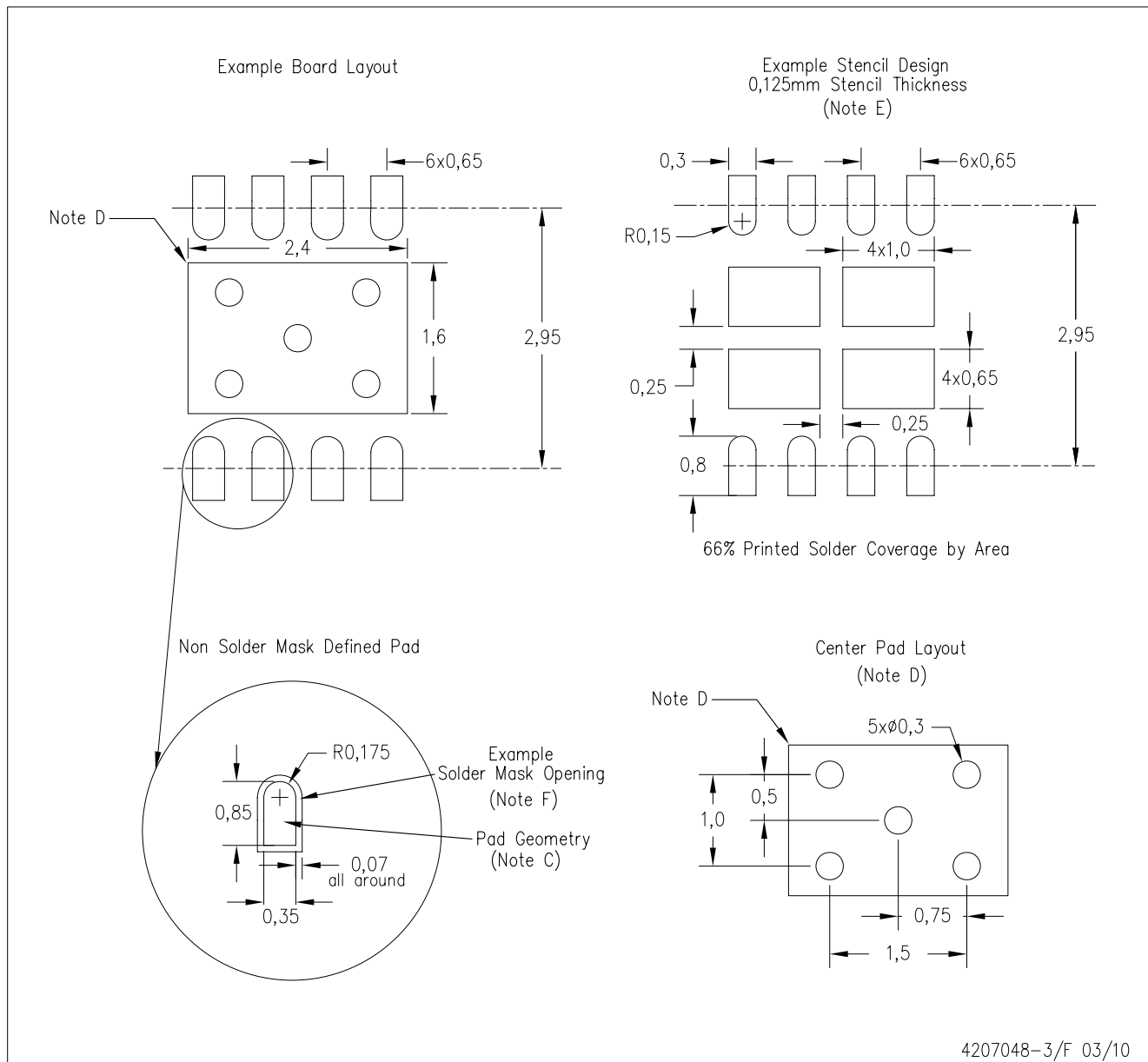
NOTE: All linear dimensions are in millimeters

Exposed Thermal Pad Dimensions

4206340-3/J 07/10

DRB (S-PVSON-N8)

PLASTIC SMALL OUTLINE

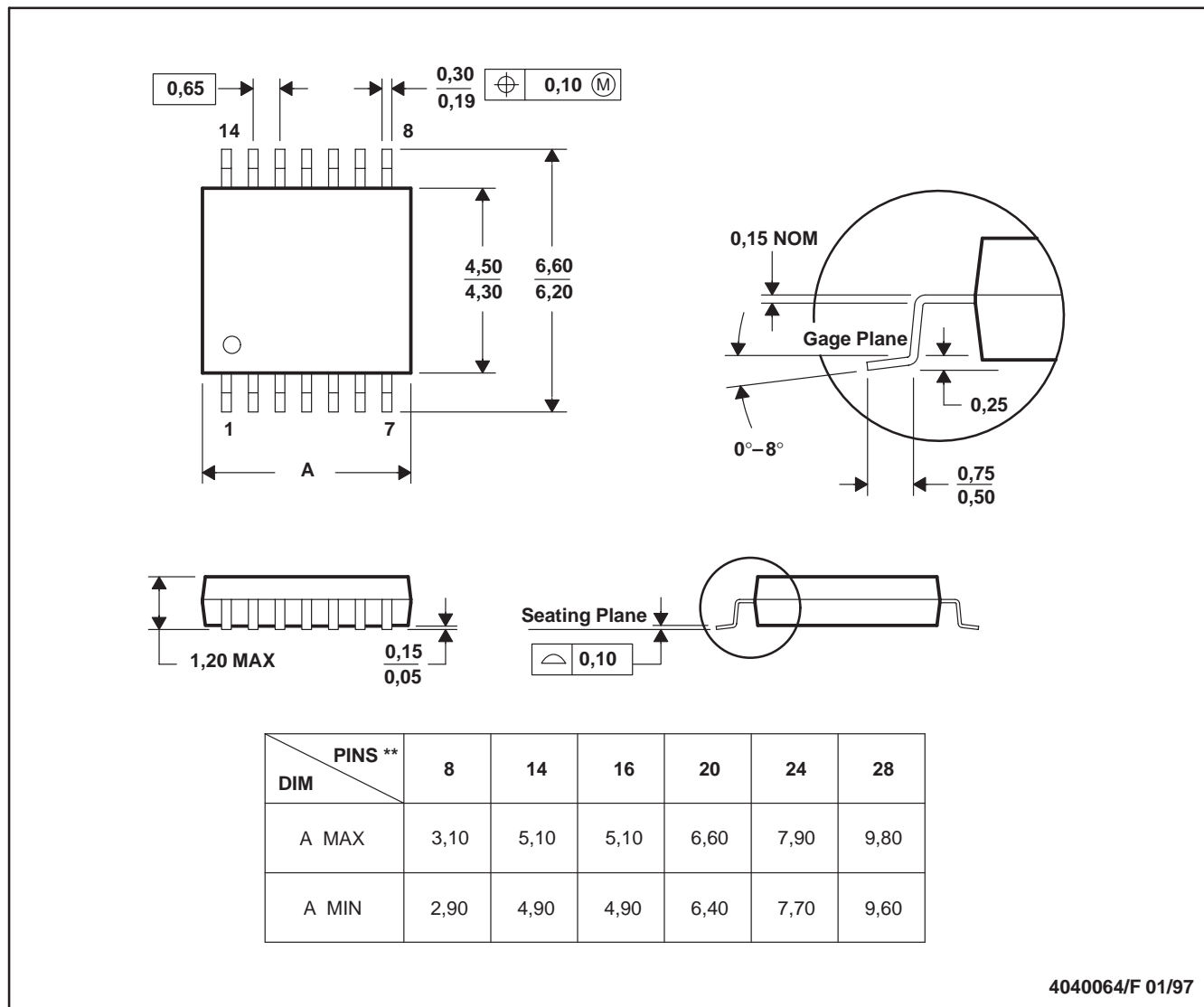


- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Publication IPC-7351 is recommended for alternate designs.
 - D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, QFN Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <<http://www.ti.com>>.
 - E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
 - F. Customers should contact their board fabrication site for solder mask tolerances.

PW (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

14 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
 D. Falls within JEDEC MO-153

IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, modifications, enhancements, improvements, and other changes to its products and services at any time and to discontinue any product or service without notice. Customers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All products are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its hardware products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by government requirements, testing of all parameters of each product is not necessarily performed.

TI assumes no liability for applications assistance or customer product design. Customers are responsible for their products and applications using TI components. To minimize the risks associated with customer products and applications, customers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any TI patent right, copyright, mask work right, or other TI intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information published by TI regarding third-party products or services does not constitute a license from TI to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of TI information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. Reproduction of this information with alteration is an unfair and deceptive business practice. TI is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

Resale of TI products or services with statements different from or beyond the parameters stated by TI for that product or service voids all express and any implied warranties for the associated TI product or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

TI products are not authorized for use in safety-critical applications (such as life support) where a failure of the TI product would reasonably be expected to cause severe personal injury or death, unless officers of the parties have executed an agreement specifically governing such use. Buyers represent that they have all necessary expertise in the safety and regulatory ramifications of their applications, and acknowledge and agree that they are solely responsible for all legal, regulatory and safety-related requirements concerning their products and any use of TI products in such safety-critical applications, notwithstanding any applications-related information or support that may be provided by TI. Further, Buyers must fully indemnify TI and its representatives against any damages arising out of the use of TI products in such safety-critical applications.

TI products are neither designed nor intended for use in military/aerospace applications or environments unless the TI products are specifically designated by TI as military-grade or "enhanced plastic." Only products designated by TI as military-grade meet military specifications. Buyers acknowledge and agree that any such use of TI products which TI has not designated as military-grade is solely at the Buyer's risk, and that they are solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI products are neither designed nor intended for use in automotive applications or environments unless the specific TI products are designated by TI as compliant with ISO/TS 16949 requirements. Buyers acknowledge and agree that, if they use any non-designated products in automotive applications, TI will not be responsible for any failure to meet such requirements.

Following are URLs where you can obtain information on other Texas Instruments products and application solutions:

Products		Applications	
Amplifiers	amplifier.ti.com	Audio	www.ti.com/audio
Data Converters	dataconverter.ti.com	Automotive	www.ti.com/automotive
DLP® Products	www.dlp.com	Communications and Telecom	www.ti.com/communications
DSP	dsp.ti.com	Computers and Peripherals	www.ti.com/computers
Clocks and Timers	www.ti.com/clocks	Consumer Electronics	www.ti.com/consumer-apps
Interface	interface.ti.com	Energy	www.ti.com/energy
Logic	logic.ti.com	Industrial	www.ti.com/industrial
Power Mgmt	power.ti.com	Medical	www.ti.com/medical
Microcontrollers	microcontroller.ti.com	Security	www.ti.com/security
RFID	www.ti-rfid.com	Space, Avionics & Defense	www.ti.com/space-avionics-defense
RF/IF and ZigBee® Solutions	www.ti.com/lprf	Video and Imaging	www.ti.com/video
		Wireless	www.ti.com/wireless-apps

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
Copyright © 2010, Texas Instruments Incorporated

www.BDTIC.com/TI