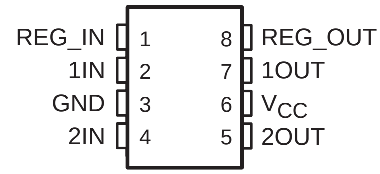
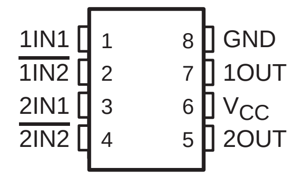
- **Industry-Standard Driver Replacement**
- **25-ns Max Rise/Fall Times and 40-ns Max Propagation Delay − 1-nF Load, V_{CC} = 14 V**
- **2-A Peak Output Current, V_{CC} = 14 V**
- **5-µA Supply Current — Input High or Low**
- **4-V to 14-V Supply-Voltage Range; Internal Regulator Extends Range to 40 V (TPS2811, TPS2812, TPS2813)**
- **−40°C to 125°C Ambient-Temperature Operating Range**

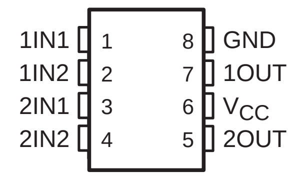
TPS2811, TPS2812, TPS2813 . . . D, P, AND PW PACKAGES
(TOP VIEW)



TPS2814 . . . D, P, AND PW PACKAGES
(TOP VIEW)



TPS2815 . . . D, P, AND PW PACKAGES
(TOP VIEW)



description

The TPS28xx series of dual high-speed MOSFET drivers are capable of delivering peak currents of 2 A into highly capacitive loads. This performance is achieved with a design that inherently minimizes shoot-through current and consumes an order of magnitude less supply current than competitive products.

The TPS2811, TPS2812, and TPS2813 drivers include a regulator to allow operation with supply inputs between 14 V and 40 V. The regulator output can power other circuitry, provided power dissipation does not exceed package limitations. When the regulator is not required, REG_IN and REG_OUT can be left disconnected or both can be connected to V_{CC} or GND.

The TPS2814 and the TPS2815 have 2-input gates that give the user greater flexibility in controlling the MOSFET. The TPS2814 has AND input gates with one inverting input. The TPS2815 has dual-input NAND gates.

TPS281x series drivers, available in 8-pin PDIP, SOIC, and TSSOP packages operate over a ambient temperature range of −40°C to 125°C.

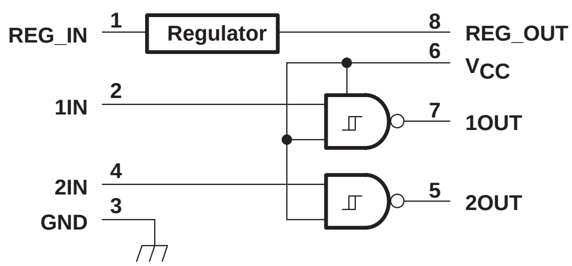
AVAILABLE OPTIONS

T_A	INTERNAL REGULATOR	LOGIC FUNCTION	PACKAGED DEVICES		
			SMALL OUTLINE (D)	PLASTIC DIP (P)	TSSOP (PW)
−40°C to 125°C	Yes	Dual inverting drivers Dual noninverting drivers One inverting and one noninverting driver	TPS2811D TPS2812D TPS2813D	TPS2811P TPS2812P TPS2813P	TPS2811PW TPS2812PW TPS2813PW
	No	Dual 2-input AND drivers, one inverting input on each driver Dual 2-input NAND drivers	TPS2814D TPS2815D	TPS2814P TPS2815P	TPS2814PW TPS2815PW

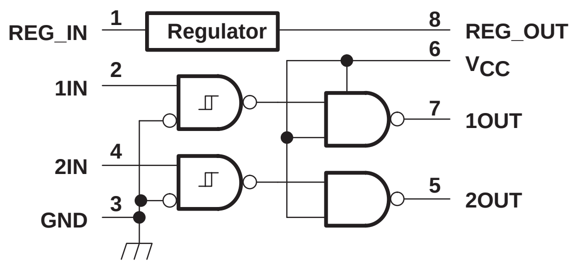
The D package is available taped and reeled. Add R suffix to device type (e.g., TPS2811DR). The PW package is only available left-end taped and reeled and is indicated by the R suffix on the device type (e.g., TPS2811PWR).

functional block diagram

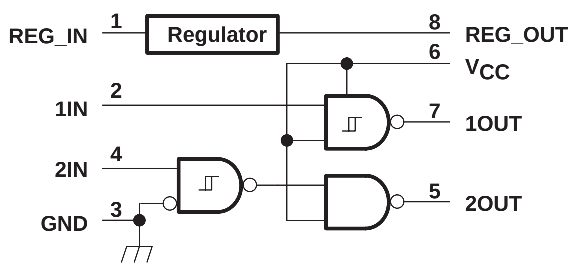
TPS2811



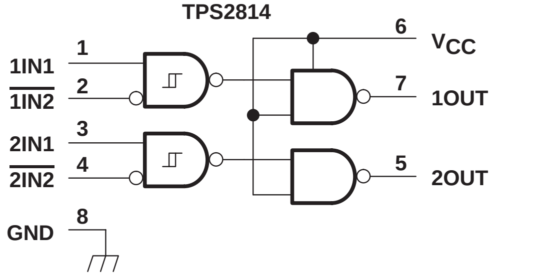
TPS2812



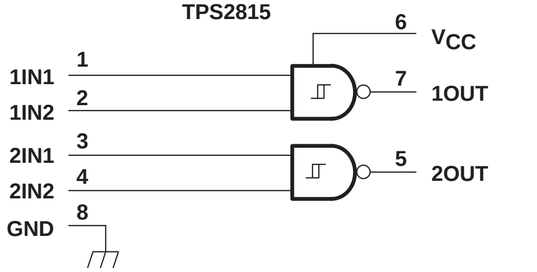
TPS2813



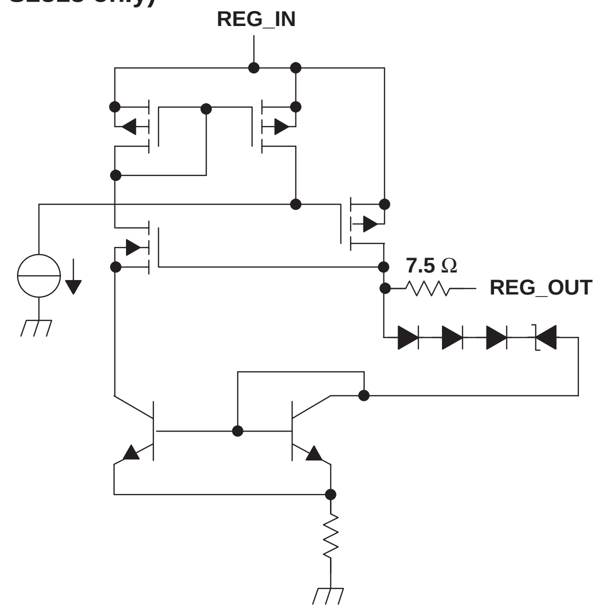
TPS2814



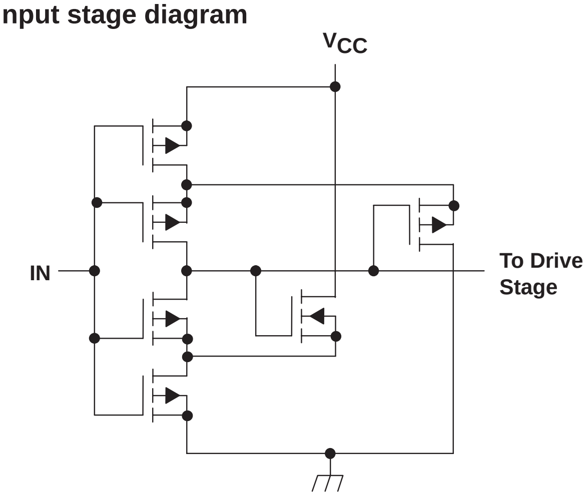
TPS2815



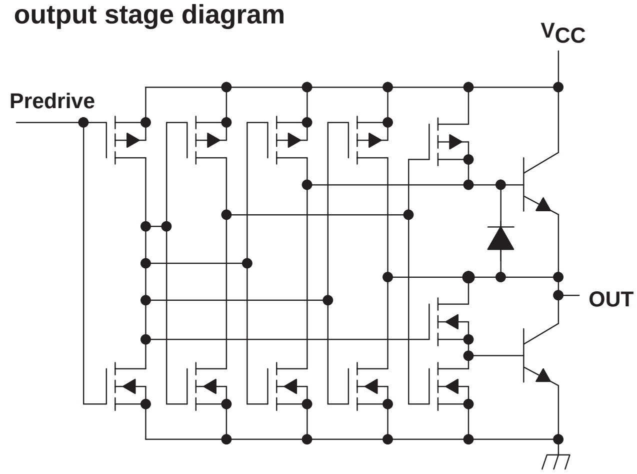
regulator diagram (TPS2811, TPS2812, TPS2813 only)



input stage diagram



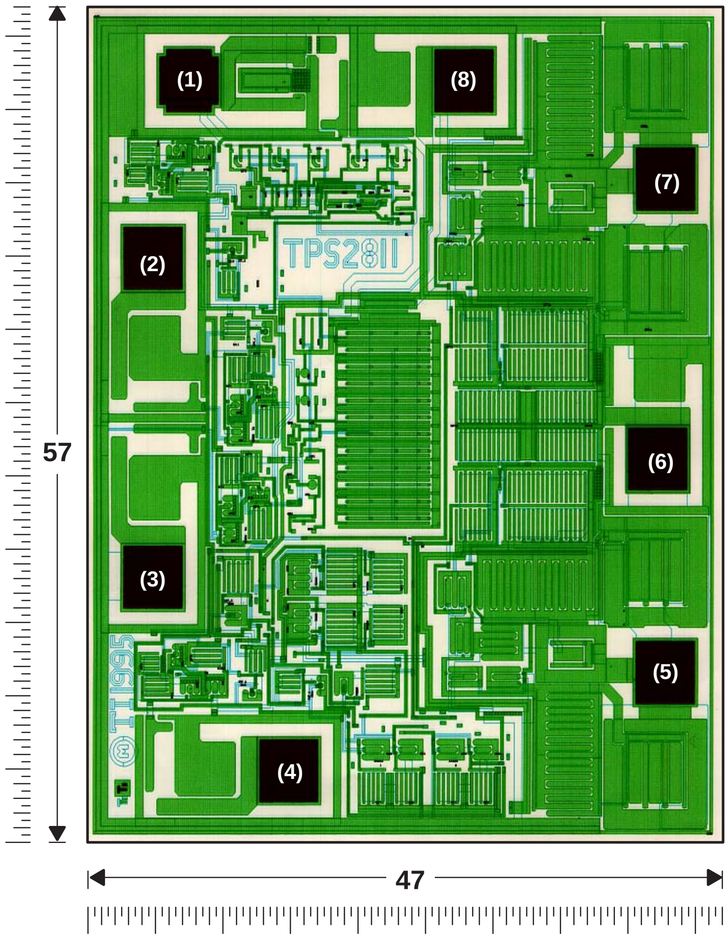
output stage diagram

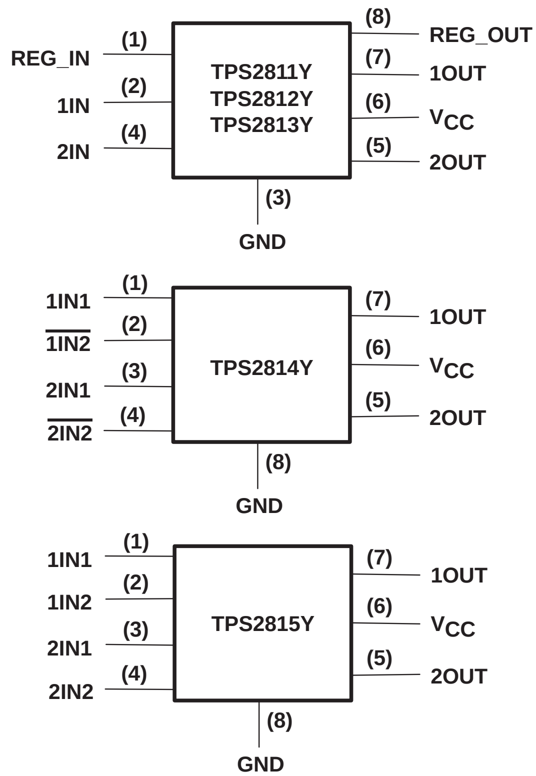


TPS28xxY chip information

This chip, when properly assembled, displays characteristics similar to those of the TPS28xx. Thermal compression or ultrasonic bonding may be used on the doped aluminum bonding pads. The chip may be mounted with conductive epoxy or a gold-silicon preform.

BONDING PAD ASSIGNMENTS





CHIP THICKNESS: 15 MILS TYPICAL

BONDING PADS: 4 × 4 MILS MINIMUM

$T_J$max OPERATING TEMPERATURE = 150°C

TOLERANCES ARE ±10%.

ALL DIMENSIONS ARE IN MILS.

Terminal Functions

TPS2811, TPS2812, TPS2813

TERMINAL NAME	TERMINAL NUMBERS			DESCRIPTION
	TPS2811 Dual Inverting Drivers	TPS2812 Dual Noninverting Drivers	TPS2813 Complimentary Drivers	
REG_IN	1	1	1	Regulator input
1IN	2	2	2	Input 1
GND	3	3	3	Ground
2IN	4	4	4	Input 2
2OUT	5 = $\overline{2IN}$	5 = 2IN	5 = 2IN	Output 2
V_{CC}	6	6	6	Supply voltage
1OUT	7 = $\overline{1IN}$	7 = 1IN	7 = $\overline{1IN}$	Output 1
REG_OUT	8	8	8	Regulator output

TPS2814, TPS2815

TERMINAL NAME	TERMINAL NUMBERS		DESCRIPTION
	TPS2814 Dual AND Drivers with Single Inverting Input	TPS2815 Dual NAND Drivers	
1IN1	1	1	Noninverting input 1 of driver 1
$\overline{1IN2}$	2	-	Inverting input 2 of driver 1
1IN2	-	2	Noninverting input 2 of driver 1
2IN1	3	3	Noninverting input 1 of driver 2
$\overline{2IN2}$	4	-	Inverting input 2 of driver 2
2IN2	-	4	Noninverting input 2 of driver 2
2OUT	5 = 2IN1 • $\overline{2IN2}$	5 = $\overline{2IN1 \bullet 2IN2}$	Output 2
V_{CC}	6	6	Supply voltage
1OUT	7 = 1IN1 • $\overline{1IN2}$	7 = $\overline{1IN1 \bullet 1IN2}$	Output 1
GND	8	8	Ground

DISSIPATION RATING TABLE

PACKAGE	$T_A \leq 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING
P	1090 mW	8.74 mW/°C	697 mW	566 mW
D	730 mW	5.84 mW/°C	467 mW	380 mW
PW	520 mW	4.17 mW/°C	332 mW	270 mW

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{CC} . . . . −0.3 V to 15 V
Regulator input voltage range, REG_IN . . . . V_{CC} −0.3 V to 42 V
Input voltage range, 1IN, 2IN, 1IN1, 1IN2, $\overline{1IN2}$, 2IN1, 2IN2, $\overline{2IN2}$ . . . . −0.3 V to V_{CC} +0.5 V
Output voltage range, 1OUT, 2OUT . . . . −0.5 < V < V_{CC} +0.5 V
Continuous regulator output current, REG_OUT . . . . 25 mA
Continuous output current, 1OUT, 2OUT . . . . ±100 mA
Continuous total power dissipation . . . . See Dissipation Rating Table
Operating ambient temperature range, T_A . . . . −40°C to 125°C
Storage temperature range, T_{stg} . . . . −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds . . . . 260°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
NOTE 1: All voltages are with respect to device GND pin.

recommended operating conditions

	MIN	MAX	UNIT
Regulator input voltage range	8	40	V
Supply voltage, V_{CC}	4	14	V
Input voltage, 1IN1, 1IN2, $\overline{1IN2}$, 2IN1, 2IN2, $\overline{2IN2}$, 1IN, 2IN	−0.3	V_{CC}	V
Continuous regulator output current, REG_OUT	0	20	mA
Ambient temperature operating range	−40	125	°C

TPS28xx electrical characteristics over recommended operating ambient temperature range, V_{CC} = 10 V, REG_IN open for TPS2811/12/13, C_L = 1 nF (unless otherwise noted)

inputs

PARAMETER	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
Positive-going input threshold voltage	V_{CC} = 5 V		3.3	4	V
	V_{CC} = 10 V		5.8	9	V
	V_{CC} = 14 V		8.3	13	V
Negative-going input threshold voltage	V_{CC} = 5 V	1	1.6		V
	V_{CC} = 10 V	1	4.2		V
	V_{CC} = 14 V	1	6.2		V
Input hysteresis	V_{CC} = 5 V		1.6		V
Input current	Inputs = 0 V or V_{CC}	−1	0.2	1	µA
Input capacitance			5	10	pF

† Typicals are for T_A = 25°C unless otherwise noted.

outputs

PARAMETER	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
High-level output voltage	I_O = −1 mA	9.75	9.9		V
	I_O = −100 mA	8	9.1		
Low-level output voltage	I_O = 1 mA		0.18	0.25	V
	I_O = 100 mA		1	2	
Peak output current	V_{CC} = 10 V		2		A

† Typicals are for T_A = 25°C unless otherwise noted.

regulator (TPS2811/2812/2813 only)

PARAMETER	TEST CONDITIONS		MIN	TYP†	MAX	UNIT
Output voltage	14 ≤ REG_IN ≤ 40 V,	0 ≤ I_O ≤ 20 mA	10	11.5	13	V
Output voltage in dropout	I_O = 10 mA,	REG_IN = 10 V	9	9.6		V

† Typicals are for T_A = 25°C unless otherwise noted.

supply current

PARAMETER	TEST CONDITIONS		MIN	TYP†	MAX	UNIT
Supply current into V_{CC}	Inputs high or low			0.2	5	µA
Supply current into REG_IN	REG_IN = 20 V,	REG_OUT open		40	100	µA

† Typicals are for T_A = 25°C unless otherwise noted.

TPS28xxY electrical characteristics at T_A = 25°C, V_{CC} = 10 V, REG_IN open for TPS2811/12/13, C_L = 1 nF (unless otherwise noted)

inputs

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Positive-going input threshold voltage	V_{CC} = 5 V		3.3		V
	V_{CC} = 10 V		5.8		V
	V_{CC} = 14 V		8.2		V
Negative-going input threshold voltage	V_{CC} = 5 V		1.6		V
	V_{CC} = 10 V		3.3		V
	V_{CC} = 14 V		4.2		V
Input hysteresis	V_{CC} = 5 V		1.2		V
Input current	Inputs = 0 V or V_{CC}		0.2		µA
Input capacitance			5		pF

outputs

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
High-level output voltage	I_O = −1 mA		9.9		V
	I_O = −100 mA		9.1		
Low-level output voltage	I_O = 1 mA		0.18		V
	I_O = 100 mA		1		
Peak output current	V_{CC} = 10.5 V		2		A

regulator (TPS2811, 2812, 2813)

PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
Output voltage	14 ≤ REG_IN ≤ 40 V,	0 ≤ I_O ≤ 20 mA		11.5		V
Output voltage in dropout	I_O = 10 mA,	REG_IN = 10 V		9.6		V

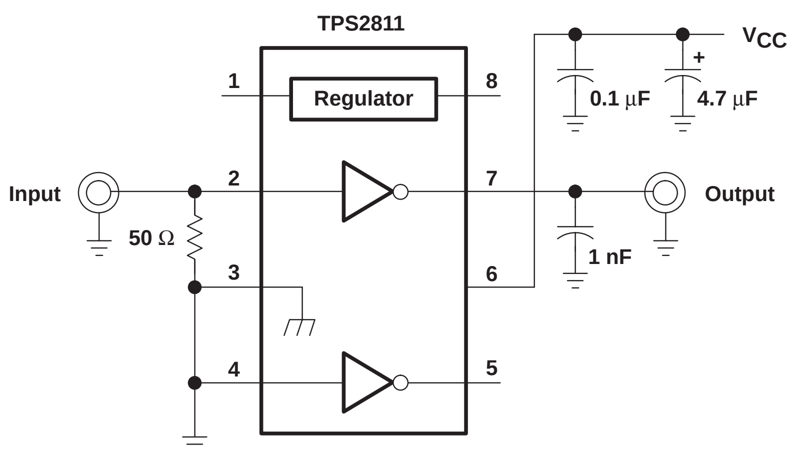
power supply current

PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
Supply current into V_{CC}	Inputs high or low			0.2		µA
Supply current into REG_IN	REG_IN = 20 V,	REG_OUT open		40		µA

switching characteristics for all devices over recommended operating ambient temperature range, REG_IN open for TPS2811/12/13, C_L = 1 nF (unless otherwise specified)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_r	Rise time	V_{CC} = 14 V		14	25	ns
		V_{CC} = 10 V		15	30	
		V_{CC} = 5 V		20	35	
t_f	Fall time	V_{CC} = 14 V		15	25	ns
		V_{CC} = 10 V		15	30	
		V_{CC} = 5 V		18	35	
t_{PHL}	Prop delay time high-to-low-level output	V_{CC} = 14 V		25	40	ns
		V_{CC} = 10 V		25	45	
		V_{CC} = 5 V		34	50	
t_{PLH}	Prop delay time low-to-high-level output	V_{CC} = 14 V		24	40	ns
		V_{CC} = 10 V		26	45	
		V_{CC} = 5 V		36	50	

PARAMETER MEASUREMENT INFORMATION



NOTE A: Input rise and fall times should be ≤10 ns for accurate measurement of ac parameters.

Figure 1. Test Circuit For Measurement of Switching Characteristics

PARAMETER MEASUREMENT INFORMATION

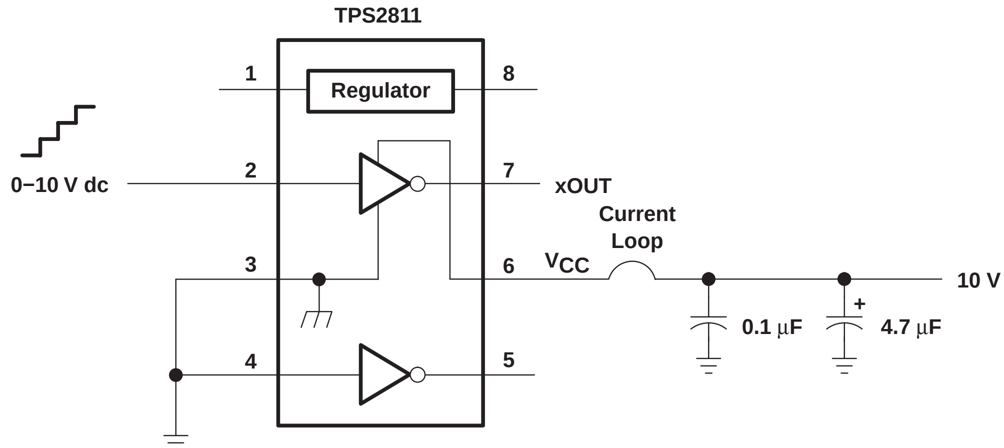


Figure 2. Shoot-through Current Test Setup

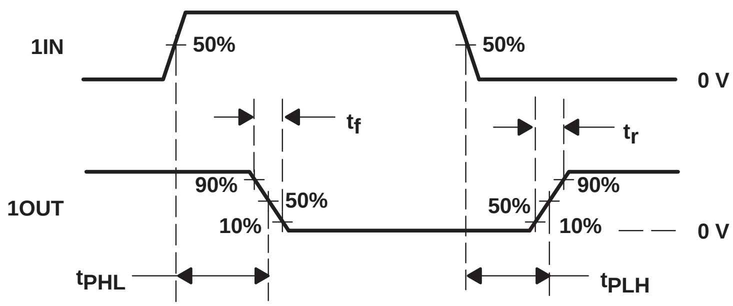


Figure 3. Typical Timing Diagram (TPS2811)

TYPICAL CHARACTERISTICS

Tables of Characteristics Graphs and Application Information

typical characteristics

PARAMETER	vs PARAMETER 2	FIGURE	PAGE
Rise time	Supply voltage	4	10
Fall time	Supply voltage	5	10
Propagation delay time	Supply voltage	6, 7	10
Supply current	Supply voltage	8	11
	Load capacitance	9	11
	Ambient temperature	10	11
Input threshold voltage	Supply voltage	11	11
Regulator output voltage	Regulator input voltage	12, 13	12
Regulator quiescent current	Regulator input voltage	14	12
Peak source current	Supply voltage	15	12
Peak sink current	Supply voltage	16	13
Shoot-through current	Input voltage, high-to-low	17	13
	Input voltage, low-to-high	18	13

TYPICAL CHARACTERISTICS

Tables of Characteristics Graphs and Application Information (Continued)

general applications

PARAMETER	vs PARAMETER 2		FIGURE	PAGE
Switching test circuits and application information			19, 20	15
Voltage of 1OUT vs 2OUT	Time	Low-to-high	21, 23, 25	16, 17
		High-to-low	22, 24, 26	16, 17

circuit for measuring paralleled switching characteristics

PARAMETER	vs PARAMETER 2		FIGURE	PAGE
Switching test circuits and application information			27	17
Input voltage vs output voltage	Time	Low-to-high	28, 30	18
		High-to-low	29, 31	18

Hex-1 to Hex-4 application information

PARAMETER	vs PARAMETER 2		FIGURE	PAGE
Driving test circuit and application information			32	19
Drain-source voltage vs drain current	Time	Hex-1 size	33	20
		Hex-2 size	36	20
		Hex-3 size	39	21
		Hex-4 size	41	22
		Hex-4 size parallel drive	45	23
Drain-source voltage vs gate-source voltage at turn-on	Time	Hex-1 size	34	20
		Hex-2 size	37	21
		Hex-3 size	40	21
		Hex-4 size	43	22
		Hex-4 size parallel drive	46	23
Drain-source voltage vs gate-source voltage at turn-off	Time	Hex-1 size	35	20
		Hex-2 size	38	21
		Hex-3 size	42	22
		Hex-4 size	44	22
		Hex-4 size parallel drive	47	23

synchronous buck regulator application

PARAMETER	vs PARAMETER 2		FIGURE	PAGE
3.3-V 3-A Synchronous-Rectified Buck Regulator Circuit			48	24
Q1 drain voltage vs gate voltage at turn-on	Time		49	26
Q1 drain voltage vs gate voltage at turn-off			50	26
Q1 drain voltage vs Q2 gate-source voltage			51, 52, 53	26, 27
Output ripple voltage vs inductor current		3 A	54	27
		5 A	55	27

TYPICAL CHARACTERISTICS

RISE TIME vs SUPPLY VOLTAGE

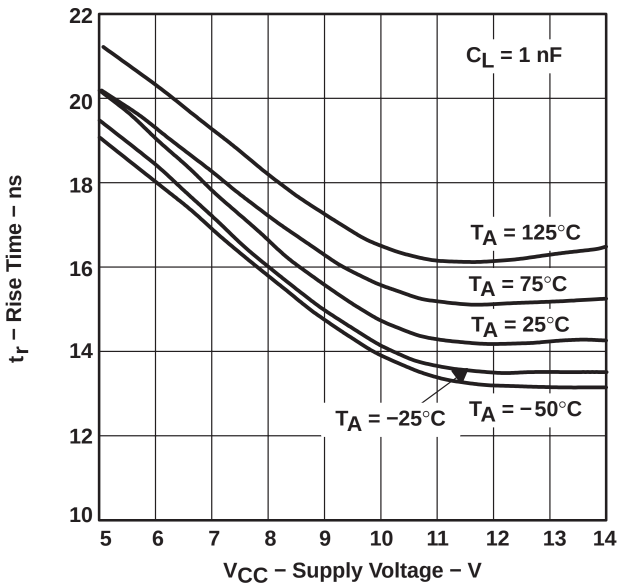


Figure 4

FALL TIME vs SUPPLY VOLTAGE

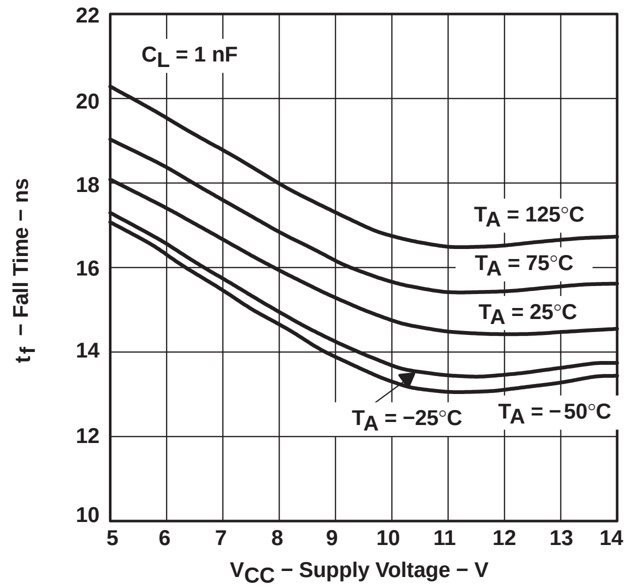


Figure 5

PROPAGATION DELAY TIME, HIGH-TO-LOW-LEVEL OUTPUT vs SUPPLY VOLTAGE

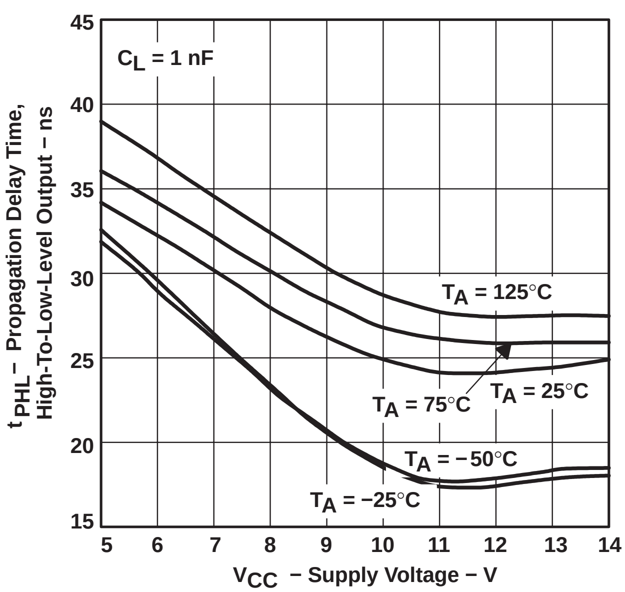


Figure 6

PROPAGATION DELAY TIME, LOW-TO-HIGH-LEVEL OUTPUT vs SUPPLY VOLTAGE

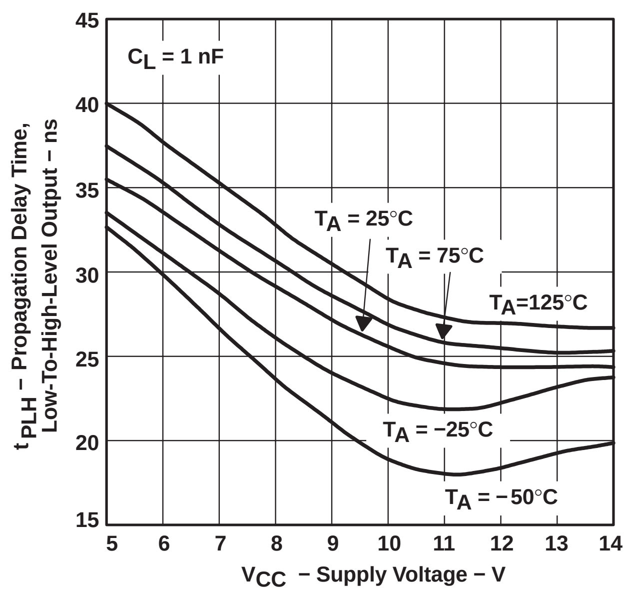


Figure 7

TYPICAL CHARACTERISTICS

SUPPLY CURRENT
vs
SUPPLY VOLTAGE

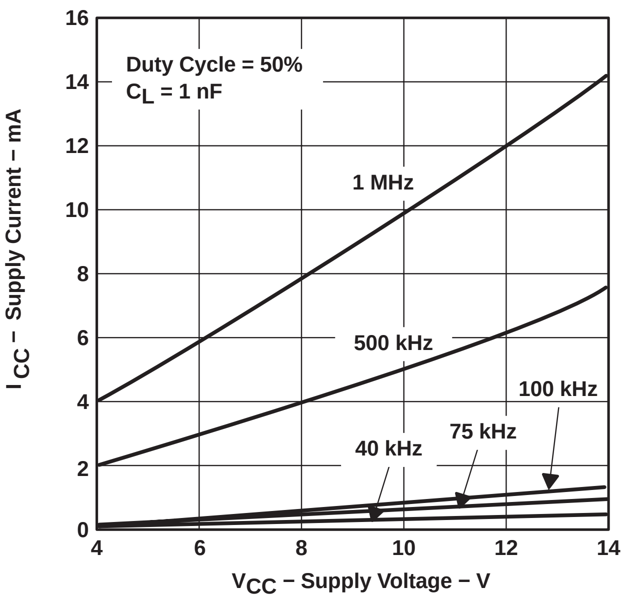


Figure 8

SUPPLY CURRENT
vs
LOAD CAPACITANCE

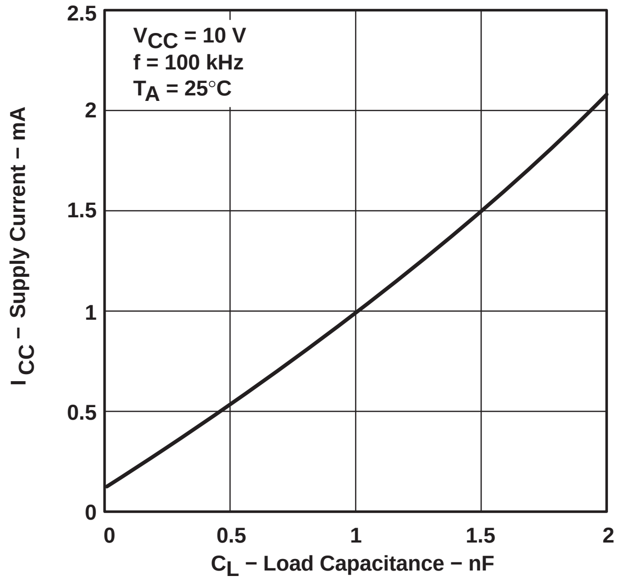


Figure 9

SUPPLY CURRENT
vs
AMBIENT TEMPERATURE

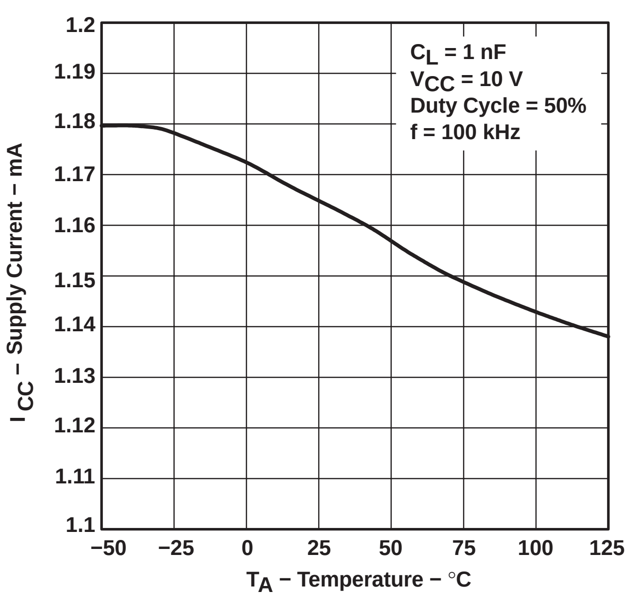


Figure 10

INPUT THRESHOLD VOLTAGE
vs
SUPPLY VOLTAGE

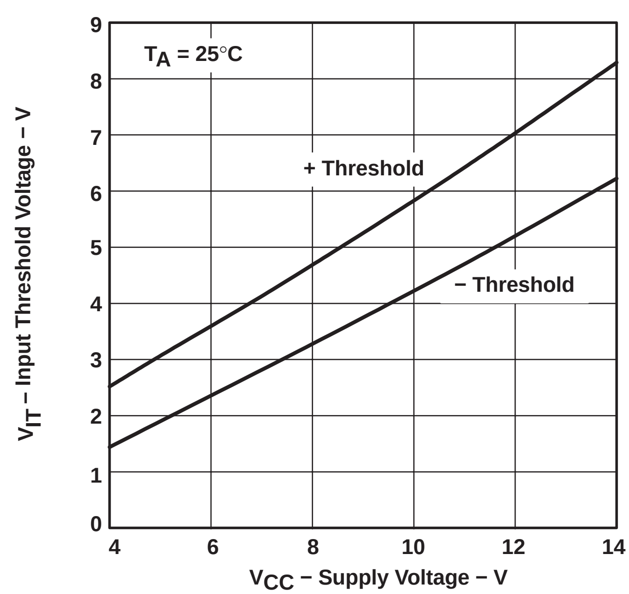


Figure 11

TYPICAL CHARACTERISTICS

REGULATOR OUTPUT VOLTAGE
vs
REGULATOR INPUT VOLTAGE

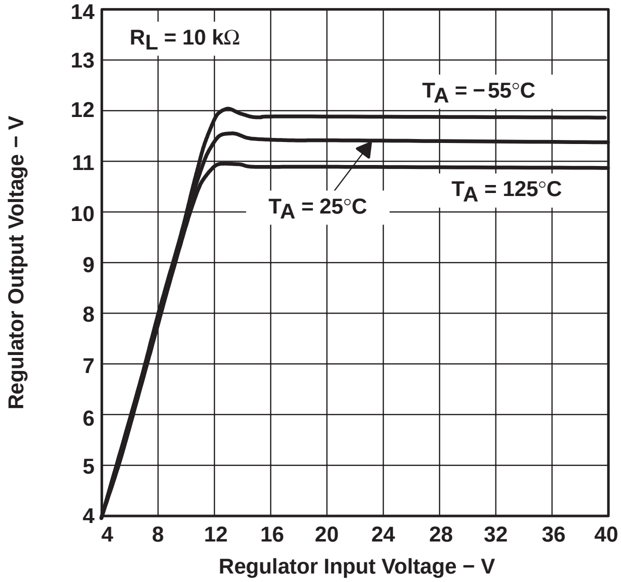


Figure 12

REGULATOR OUTPUT VOLTAGE
vs
REGULATOR INPUT VOLTAGE

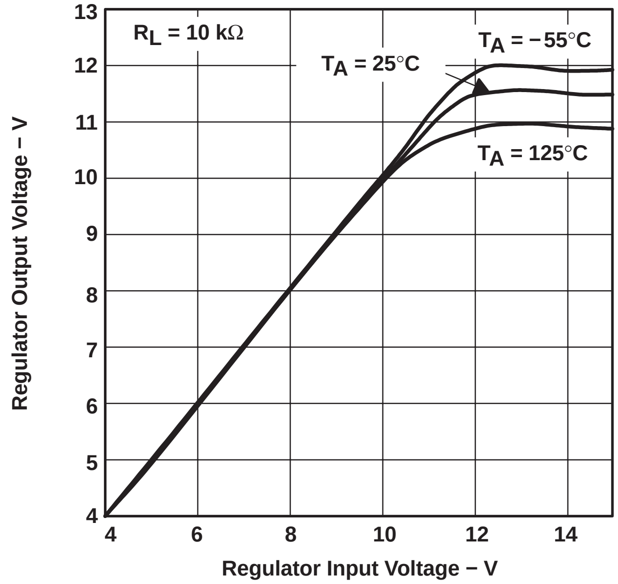


Figure 13

REGULATOR QUIESCENT CURRENT
vs
REGULATOR INPUT VOLTAGE

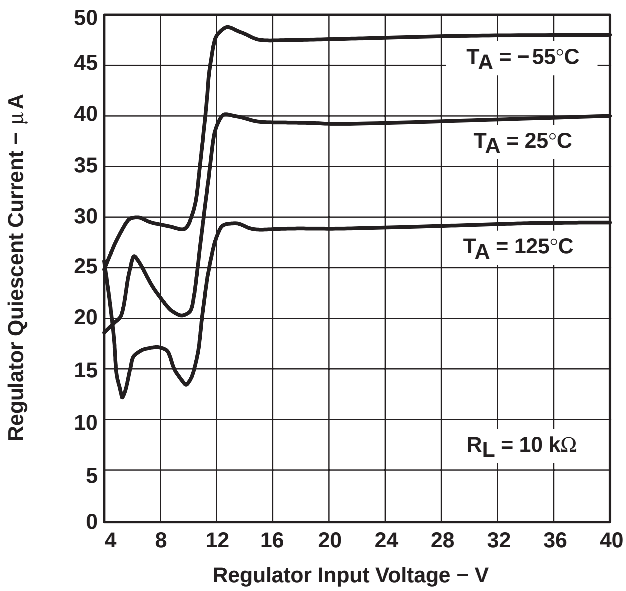


Figure 14

PEAK SOURCE CURRENT
vs
SUPPLY VOLTAGE

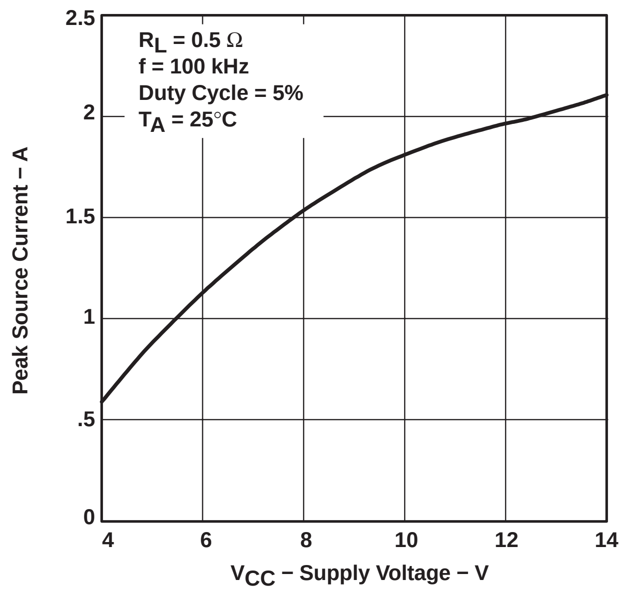


Figure 15

TYPICAL CHARACTERISTICS

PEAK SINK CURRENT
vs
SUPPLY VOLTAGE

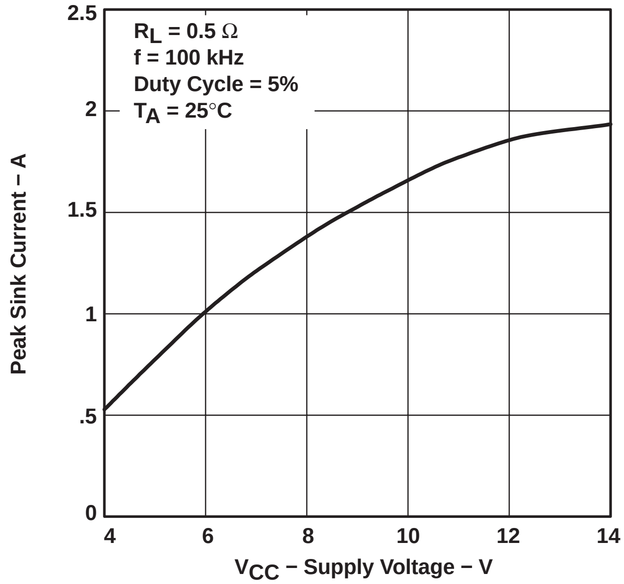


Figure 16

SHOOT-THROUGH CURRENT
vs
INPUT VOLTAGE, HIGH-TO-LOW

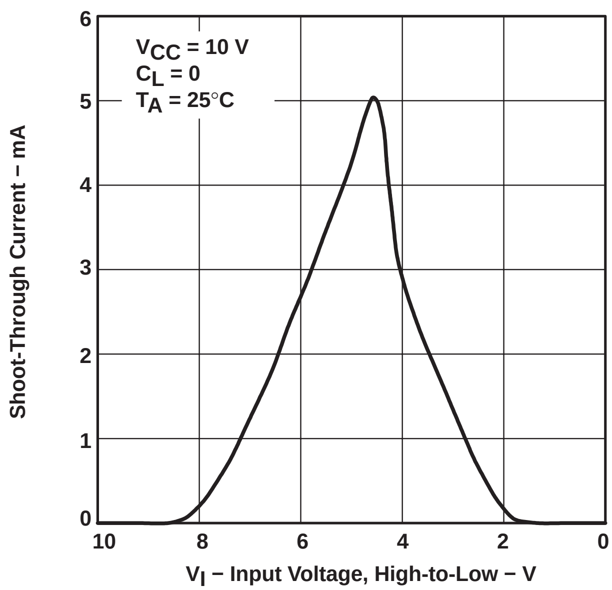


Figure 17

SHOOT-THROUGH CURRENT
vs
INPUT VOLTAGE, LOW-TO-HIGH

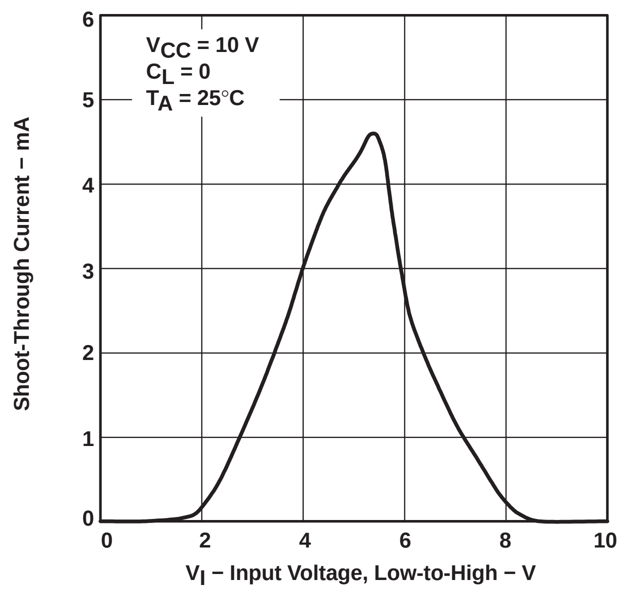


Figure 18

APPLICATION INFORMATION

The TPS2811, TPS2812 and TPS2813 circuits each contain one regulator and two MOSFET drivers. The regulator can be used to limit V_{CC} to between 10 V and 13 V for a range of input voltages from 14 V to 40 V, while providing up to 20 mA of dc drive. The TPS2814 and TPS2815 both contain two drivers, each of which has two inputs. The TPS2811 has inverting drivers, the TPS2812 has noninverting drivers, and the TPS2813 has one inverting and one noninverting driver. The TPS2814 is a dual 2-input AND driver with one inverting input on each driver, and the TPS2815 is a dual 2-input NAND driver. These MOSFET drivers are capable of supplying up to 2.1 A or sinking up to 1.9 A (see Figures 15 and 16) of instantaneous current to n-channel or p-channel MOSFETs. The TPS2811 family of MOSFET drivers have very fast switching times combined with very short propagation delays. These features enhance the operation of today's high-frequency circuits.

The CMOS input circuit has a positive threshold of approximately 2/3 of V_{CC}, with a negative threshold of 1/3 of V_{CC}, and a very high input impedance in the range of $10^9\ \Omega$. Noise immunity is also very high because of the Schmidt trigger switching. In addition, the design is such that the normal shoot-through current in CMOS (when the input is biased halfway between V_{CC} and ground) is limited to less than 6 mA. The limited shoot-through is evident in the graphs in Figures 17 and 18. The input stage shown in the functional block diagram better illustrates the way the front end works. The circuitry of the device is such that regardless of the rise and/or fall time of the input signal, the output signal will always have a fast transition speed; this basically isolates the waveforms at the input from the output. Therefore, the specified switching times are not affected by the slopes of the input waveforms.

The basic driver portion of the circuits operate over a supply voltage range of 4 V to 14 V with a maximum bias current of 5 µA. Each driver consists of a CMOS input and a buffered output with a 2-A instantaneous drive capability. They have propagation delays of less than 30 ns and rise and fall times of less than 20 ns each. Placing a 0.1-µF ceramic capacitor between V_{CC} and ground is recommended; this will supply the instantaneous current needed by the fast switching and high current surges of the driver when it is driving a MOSFET.

The output circuit is also shown in the functional block diagram. This driver uses a unique combination of a bipolar transistor in parallel with a MOSFET for the ability to swing from V_{CC} to ground while providing 2 A of instantaneous driver current. This unique parallel combination of bipolar and MOSFET output transistors provides the drive required at V_{CC} and ground to guarantee turn-off of even low-threshold MOSFETs. Typical bipolar-only output devices don't easily approach V_{CC} or ground.

The regulator, included in the TPS2811, TPS2812 and TPS2813, has an input voltage range of 14 V to 40 V. It produces an output voltage of 10 V to 13 V and is capable of supplying from 0 to 20 mA of output current. In grounded source applications, this extends the overall circuit operation to 40 V by clamping the driver supply voltage (V_{CC}) to a safe level for both the driver and the MOSFET gate. The bias current for full operation is a maximum of 150 µA. A 0.1-µF capacitor connected between the regulator output and ground is required to ensure stability. For transient response, an additional 4.7-µF electrolytic capacitor on the output and a 0.1-µF ceramic capacitor on the input will optimize the performance of this circuit. When the regulator is not in use, it can be left open at both the input and the output, or the input can be shorted to the output and tied to either the V_{CC} or the ground pin of the chip.

APPLICATION INFORMATION

matching and paralleling connections

Figures 21 and 22 show the delays for the rise and fall time of each channel. As can be seen on a 5-ns scale, there is very little difference between the two channels at no load. Figures 23 and 24 show the difference between the two channels for a 1-nF load on each output. There is a slight delay on the rising edge, but little or no delay on the falling edge. As an example of extreme overload, Figures 25 and 26 show the difference between the two channels, or two drivers in the package, each driving a 10-nF load. As would be expected, the rise and fall times are significantly slowed down. Figures 28 and 29 show the effect of paralleling the two channels and driving a 1-nF load. A noticeable improvement is evident in the rise and fall times of the output waveforms. Finally, Figures 30 and 31 show the two drivers being paralleled to drive the 10-nF load and as could be expected the waveforms are improved. In summary, the paralleling of the two drivers in a package enhances the capability of the drivers to handle a larger load. Because of manufacturing tolerances, it is not recommended to parallel drivers that are not in the same package.

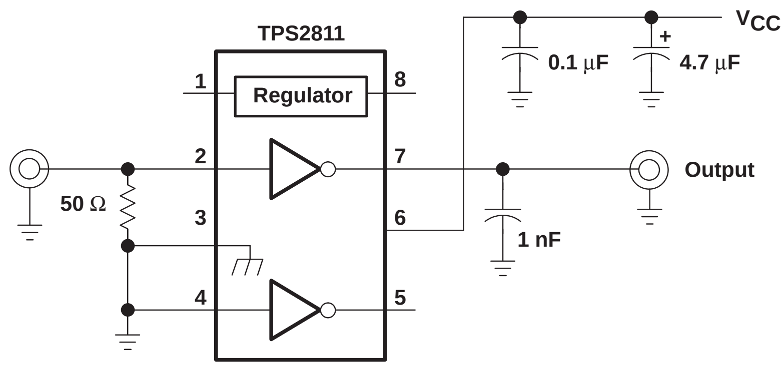
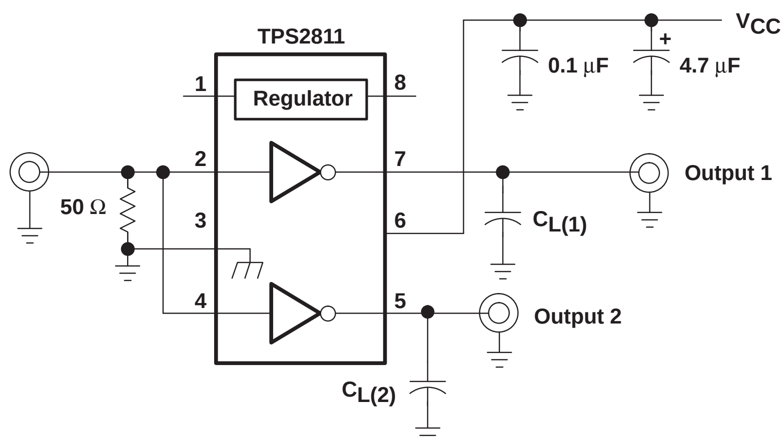


Figure 19. Test Circuit for Measuring Switching Characteristics



NOTE A: Input rise and fall times should be ≤10 ns for accurate measurement of ac parameters.

Figure 20. Test Circuit for Measuring Switching Characteristics with the Inputs Connected in Parallel

APPLICATION INFORMATION

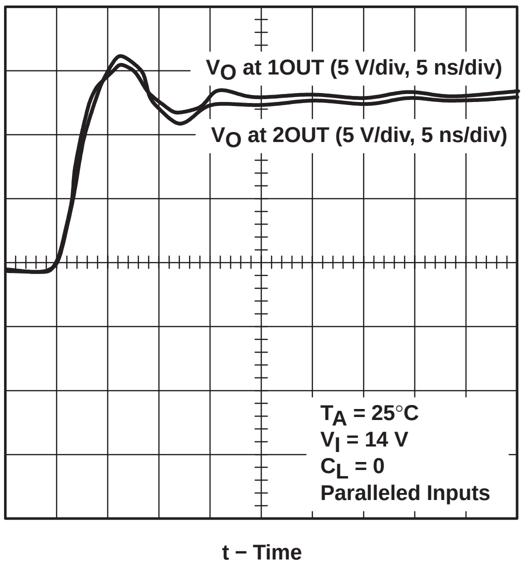


Figure 21. Voltage of 1OUT vs Voltage at 2OUT, Low-to-High Output Delay

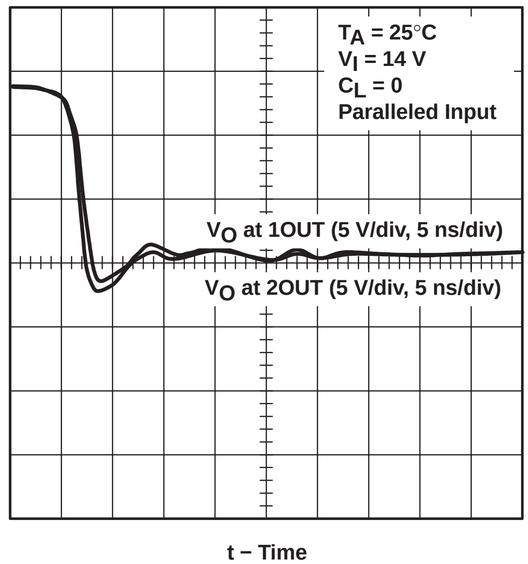


Figure 22. Voltage at 1OUT vs Voltage at 2OUT, High-to-Low Output Delay

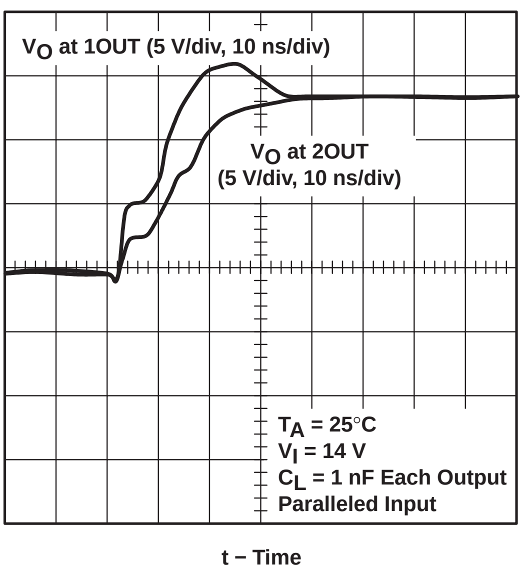


Figure 23. Voltage at 1OUT vs Voltage at 2OUT, Low-to-High Output Delay

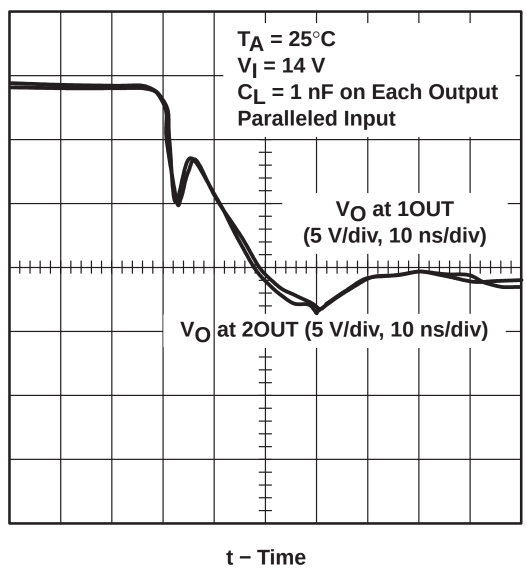


Figure 24. Voltage at 1OUT vs Voltage at 2OUT, High-to-Low Output Delay

APPLICATION INFORMATION

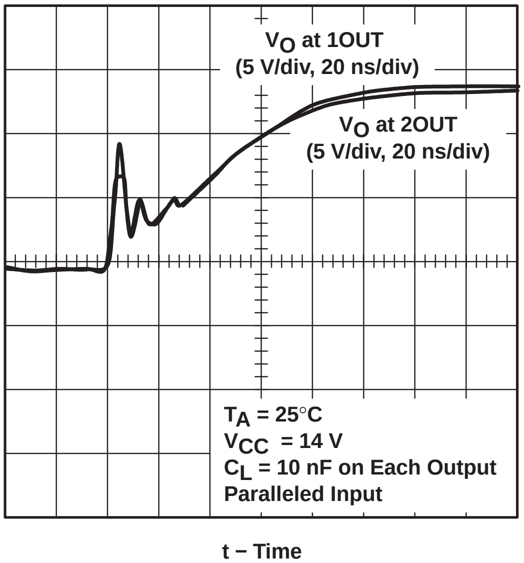


Figure 25. Voltage at 1OUT vs Voltage at 2OUT, Low-to-High Output Delay

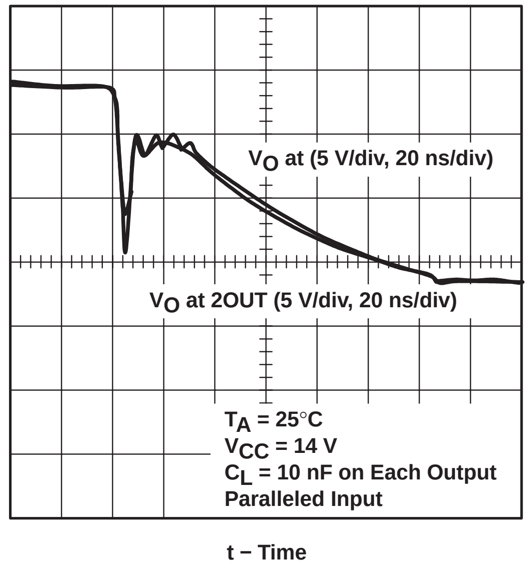
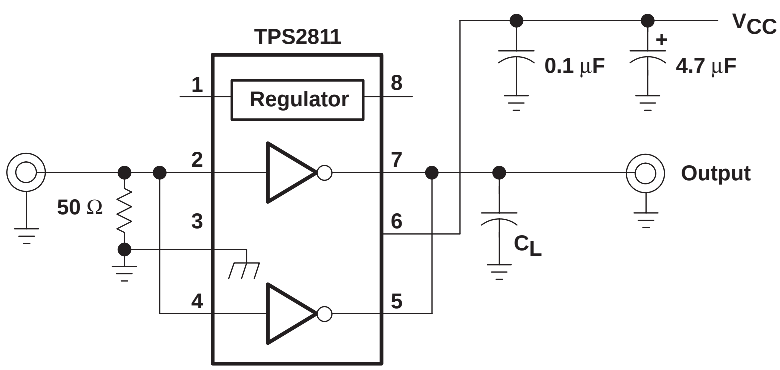


Figure 26. Voltage at 1OUT vs Voltage at 2OUT, High-to-Low Output Delay



NOTE A: Input rise and fall times should be ≤10 ns for accurate measurement of ac parameters.

Figure 27. Test Circuit for Measuring Paralleled Switching Characteristics

APPLICATION INFORMATION

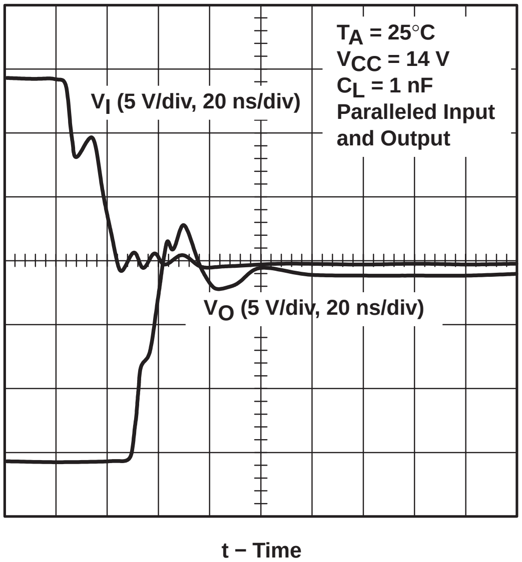


Figure 28. Input Voltage vs Output Voltage, Low-to-High Propagation Delay of Paralleled Drivers

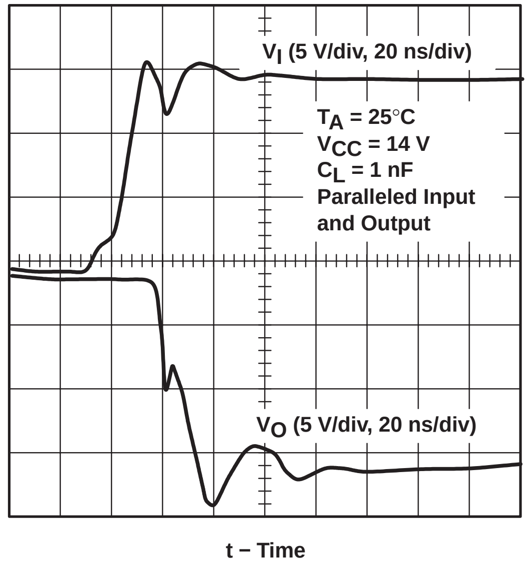


Figure 29. Input Voltage vs Output Voltage, High-to-Low Propagation Delay of Paralleled Drivers

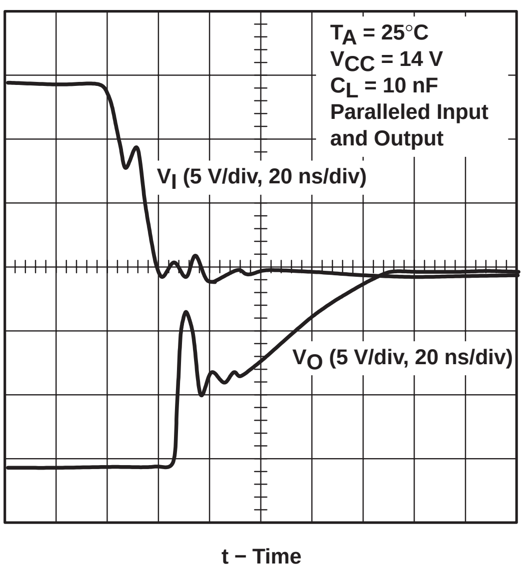


Figure 30. Input Voltage vs Output Voltage, Low-to-High Propagation Delay of Paralleled Drivers

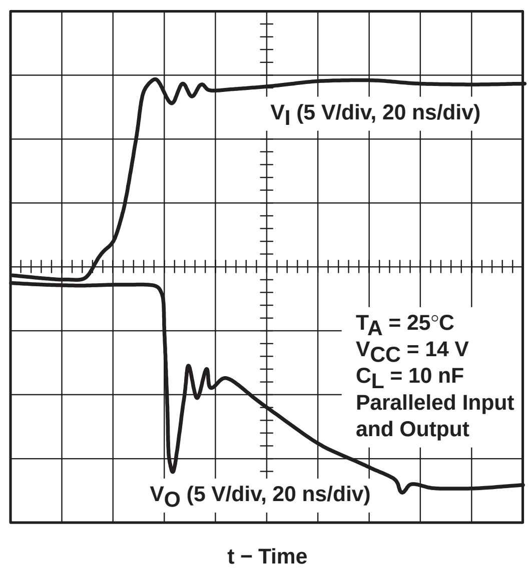


Figure 31. Input Voltage vs Output Voltage, High-to-Low Propagation Delay of Paralleled Drivers

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Figures 33 through 47 illustrate the performance of the TPS2811 driving MOSFETs with clamped inductive loads, similar to what is encountered in discontinuous-mode flyback converters. The MOSFETs that were tested range in size from Hex-1 to Hex-4, although the TPS28xx family is only recommended for Hex-3 or below.

The test circuit is shown in Figure 32. The layout rules observed in building the test circuit also apply to real applications. Decoupling capacitor C1 is a 0.1-µF ceramic device, connected between V_{CC} and GND of the TPS2811, with short lead lengths. The connection between the driver output and the MOSFET gate, and between GND and the MOSFET source, are as short as possible to minimize inductance. Ideally, GND of the driver is connected directly to the MOSFET source. The tests were conducted with the pulse generator frequency set very low to eliminate the need for heat sinking, and the duty cycle was set to turn off the MOSFET when the drain current reached 50% of its rated value. The input voltage was adjusted to clamp the drain voltage at 80% of its rating.

As shown, the driver is capable of driving each of the Hex-1 through Hex-3 MOSFETs to switch in 20 ns or less. Even the Hex-4 is turned on in less than 20 ns. Figures 45, 46 and 47 show that paralleling the two drivers in a package enhances the gate waveforms and improves the switching speed of the MOSFET. Generally, one driver is capable of driving up to a Hex-4 size. The TPS2811 family is even capable of driving large MOSFETs that have a low gate charge.

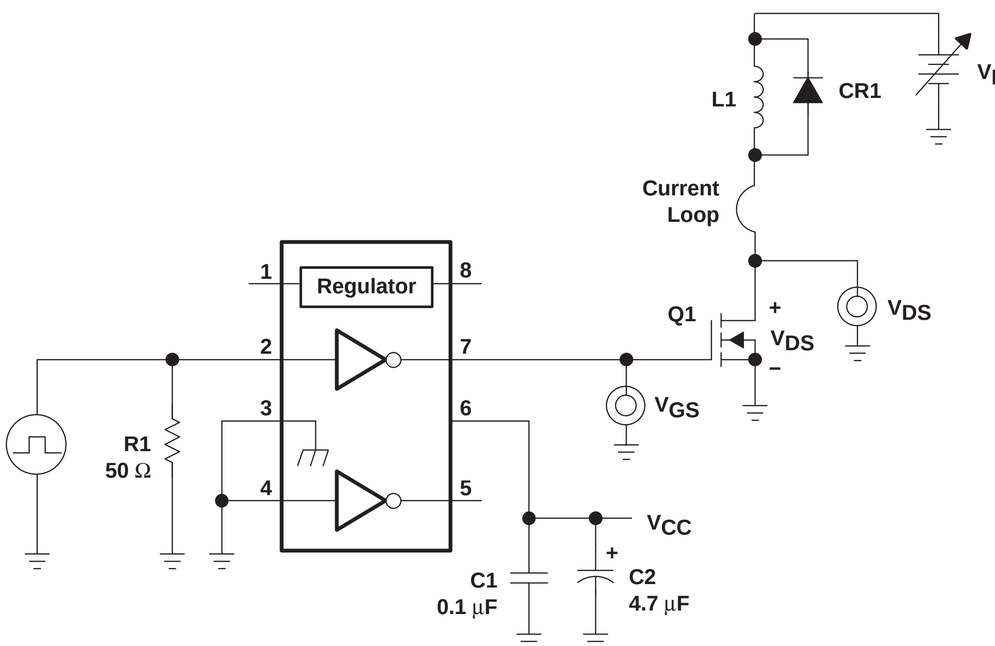

Figure 32. TPS2811 Driving Hex-1 through Hex-4 Devices

APPLICATION INFORMATION

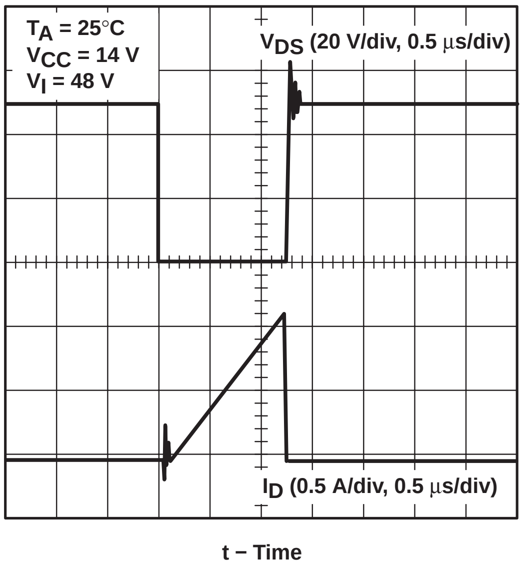

Figure 33. Drain-Source Voltage vs Drain Current, TPS2811 Driving an IRFD014 (Hex-1 Size)

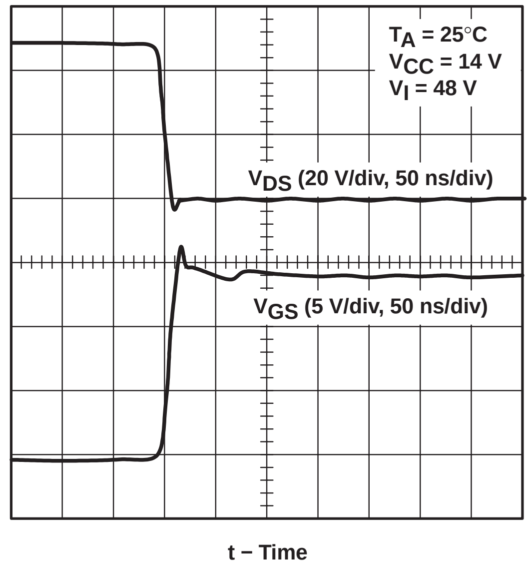

Figure 34. Drain-Source Voltage vs Gate-Source Voltage, at Turn-on, TPS2811 Driving an IRFD014 (Hex-1 Size)

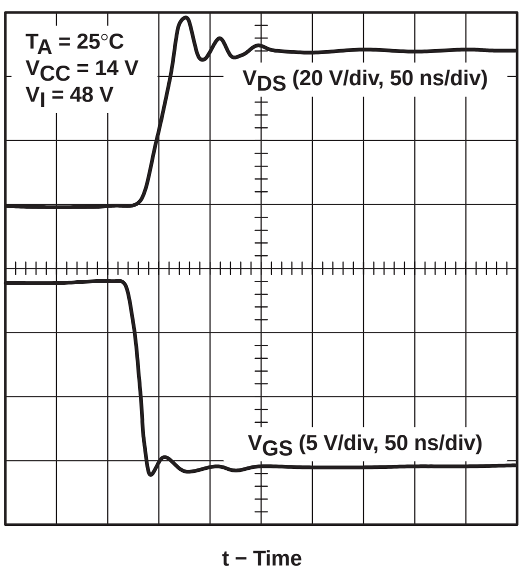

Figure 35. Drain-Source Voltage vs Gate-Source Voltage, at Turn-off, TPS2811 Driving an IRFD014 (Hex-1 Size)

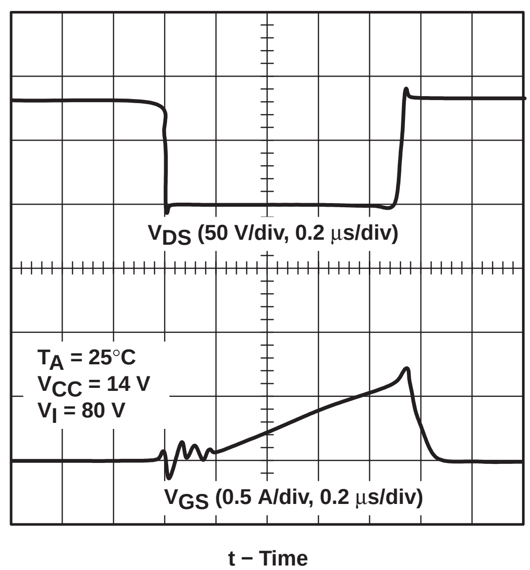

Figure 36. Drain-Source Voltage vs Drain Current, TPS2811 Driving an IRFD120 (Hex-2 Size)

APPLICATION INFORMATION

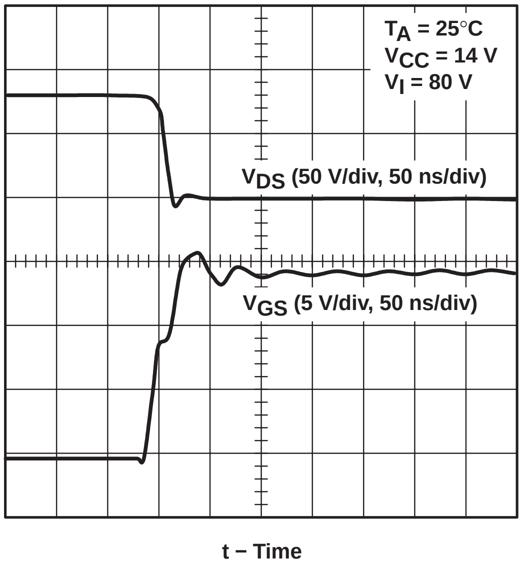

Figure 37. Drain-Source Voltage vs Gate-Source Voltage, at Turn-on, TPS2811 Driving an IRFD120 (Hex-2 Size)

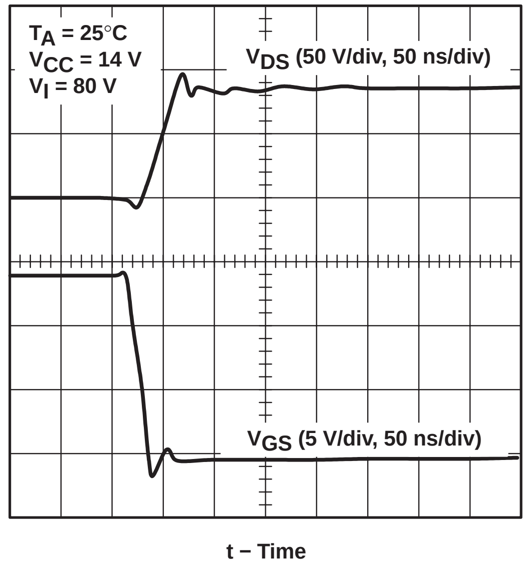

Figure 38. Drain-Source Voltage vs Gate-Source Voltage, at Turn-off, TPS2811 Driving an IRFD120 (Hex-2 Size)

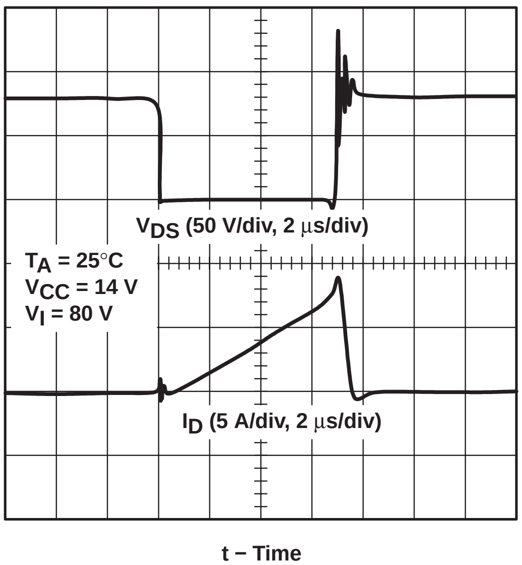

Figure 39. Drain-Source Voltage vs Drain Current, TPS2811 Driving an IRF530 (Hex-3 Size)

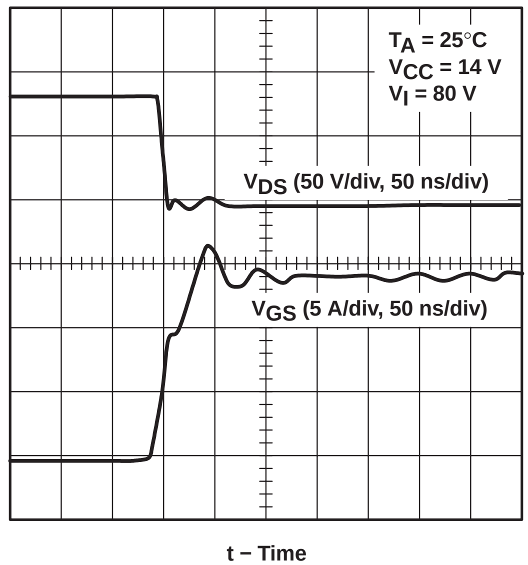

Figure 40. Drain-Source Voltage vs Gate-Source Voltage, at Turn-on, TPS2811 Driving an IRF530 (Hex-3 Size)

APPLICATION INFORMATION

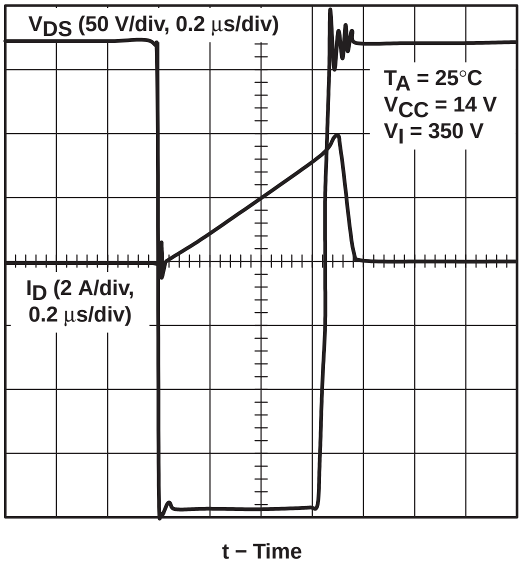

Figure 41. Drain-Source Voltage vs Drain Current, One Driver, TPS2811 Driving an IRF840 (Hex-4 Size)

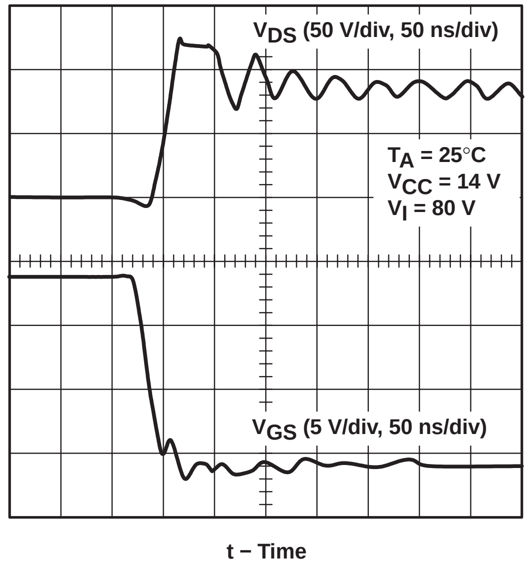

Figure 42. Drain-Source Voltage vs Gate-Source Voltage, at Turn-off, TPS2811 Driving an IRF530 (Hex-3 Size)

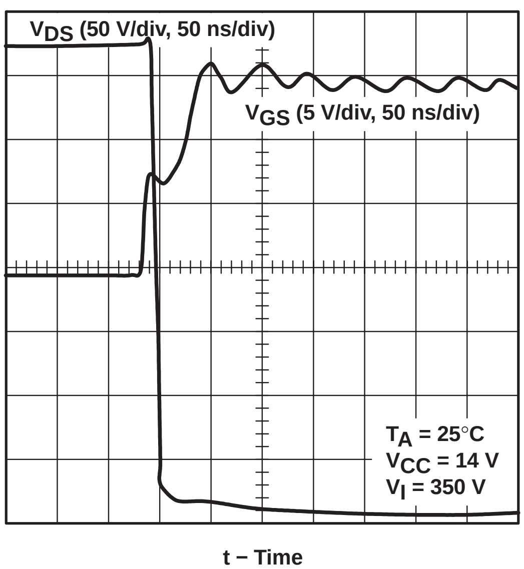

Figure 43. Drain-Source Voltage vs Gate-Source Voltage, at Turn-on, One Driver, TPS2811 Driving an IRF840 (Hex-4 Size)

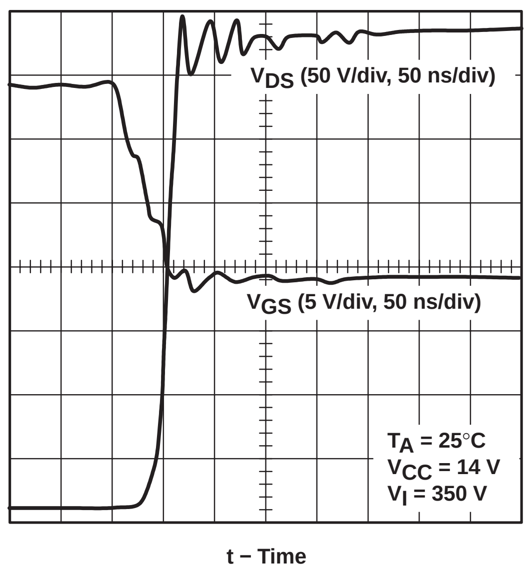

Figure 44. Drain-Source Voltage vs Gate-Source Voltage, at Turn-off, One Driver, TPS2811 Driving an IRF840 (Hex-4 Size)

APPLICATION INFORMATION

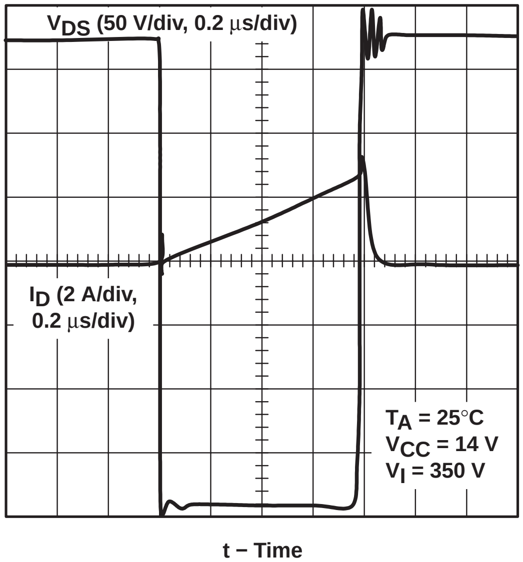

Figure 45. Drain-Source Voltage vs Drain Current, Parallel Drivers, TPS2811 Driving an IRF840 (Hex-4 Size)

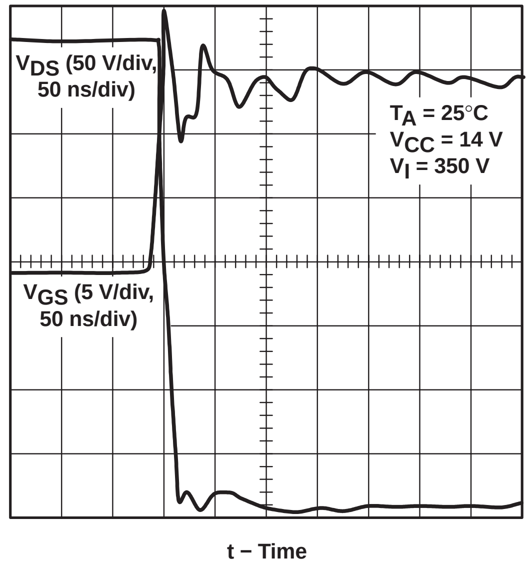

Figure 46. Drain-Source Voltage vs Gate-Source Voltage, at Turn-on, Parallel Drivers, TPS2811 Driving an IRF840 (Hex-4 Size)

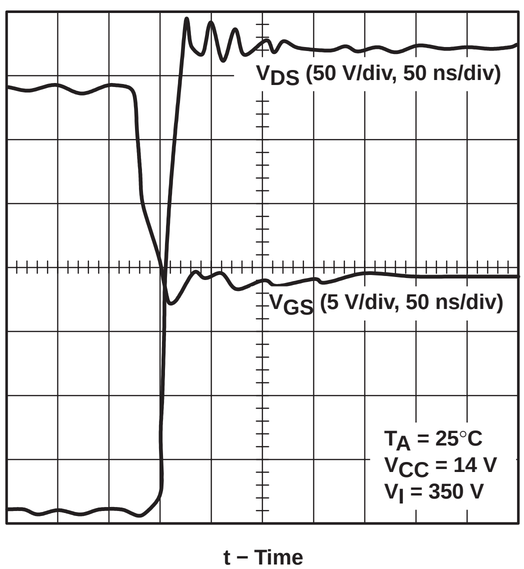

Figure 47. Drain-Source Voltage vs Gate-Source Voltage, at Turn-off, Parallel Drivers, TPS2811 Driving an IRF840 (Hex-4 Size)

APPLICATION INFORMATION

synchronous buck regulator

Figure 48 is the schematic for a 100-kHz synchronous-rectified buck converter implemented with a TL5001 pulse-width-modulation (PWM) controller and a TPS2812 driver. The bill of materials is provided in Table 1. The converter operates over an input range from 5.5 V to 12 V and has a 3.3-V output capable of supplying 3 A continuously and 5 A during load surges. The converter achieves an efficiency of 90.6% at 3 A and 87.6% at 5 A. Figures 49 and 50 show the power switch switching performance. The output ripple voltage waveforms are documented in Figures 54 and 55.

The TPS2812 drives both the power switch, Q2, and the synchronous rectifier, Q1. Large shoot-through currents, caused by power switch and synchronous rectifier remaining on simultaneously during the transitions, are prevented by small delays built into the drive signals, using CR2, CR3, R11, R12, and the input capacitance of the TPS2812. These delays allow the power switch to turn off before the synchronous rectifier turns on and vice versa. Figure 51 shows the delay between the drain of Q2 and the gate of Q1; expanded views are provided in Figures 52 and 53.

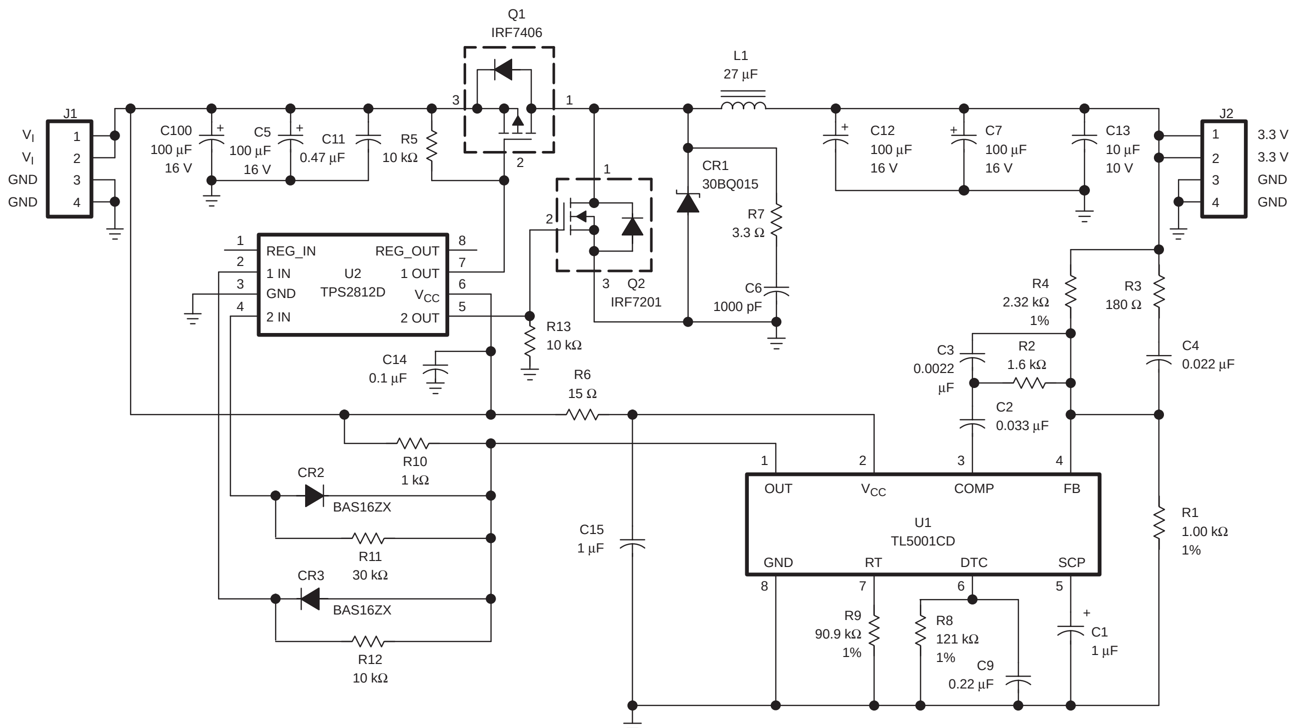

Figure 48. 3.3-V 3-A Synchronous-Rectified Buck Regulator Circuit

NOTE: If the parasitics of the external circuit cause the voltage to violate the Absolute Maximum Rating for the Output pins, Schottky diodes should be added from ground to output and from output to Vcc.

APPLICATION INFORMATION

Table 1. Bill of Materials, 3.3-V, 3-A Synchronous-Rectified Buck Converter

REFERENCE	DESCRIPTION	VENDOR	
U1	TL5001CD, PWM	Texas Instruments,	972-644-5580
U2	TPS2812D, N.I. MOSFET Driver	Texas Instruments,	972-644-5580
CR1	3 A, 15 V, Schottky, 30BQ015	International Rectifier,	310-322-3331
CR2,CR3	Signal Diode, BAS16ZX	Zetex,	516-543-7100
C1	1 µF, 16 V, Tantalum		
C2	0.033 µF, 50 V		
C3	0.0022 µF, 50 V		
C4	0.022 µF, 50 V		
C5,C7,C10,C12	100 µF, 16 V, Tantalum, TPSE107M016R0100	AVX,	800-448-9411
C6	1000 pF, 50 V		
C9	0.22 µF, 50 V		
C11	0.47 µF, 50 V, Z5U		
C13	10 µF, 10 V, Ceramic, CC1210CY5V106Z	TDK,	708-803-6100
C14	0.1 µF, 50 V		
C15	1.0 µF, 50 V		
J1,J2	4-Pin Header		
L1	27 µH, 3 A/5 A, SML5040	Nova Magnetics, Inc.,	972-272-8287
Q1	IRF7406, P-FET	International Rectifier,	310-322-3331
Q2	IRF7201, N-FET	International Rectifier,	310-322-3331
R1	1.00 kΩ, 1%		
R2	1.6 kΩ		
R3	180 Ω		
R4	2.32 kΩ, 1 %		
R5,R12,R13	10 kΩ		
R6	15 Ω		
R7	3.3 Ω		
R8	121 kΩ, 1%		
R9	90.9 kΩ, 1%		
R10	1 kΩ		
R11	30 kΩ		

NOTES: 2. Unless otherwise specified, capacitors are X7R ceramics.
3. Unless otherwise specified, resistors are 5%, 1/10 W.

APPLICATION INFORMATION

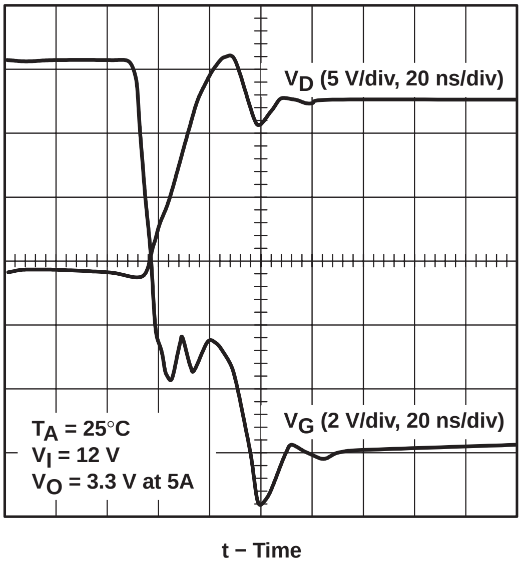

Figure 49. Q1 Drain Voltage vs Gate Voltage, at Switch Turn-on

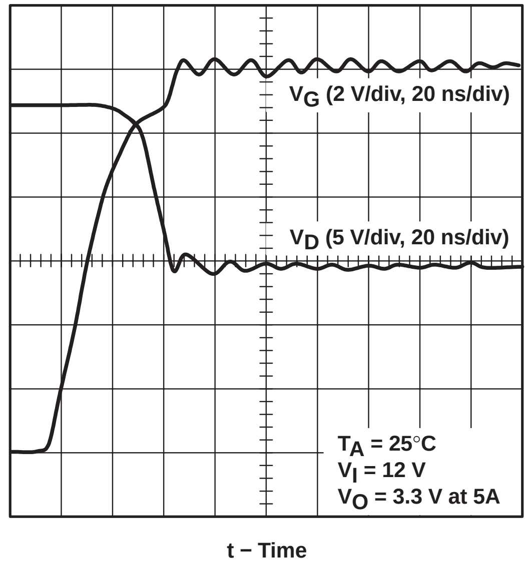

Figure 50. Q1 Drain Voltage vs Gate Voltage, at Switch Turn-off

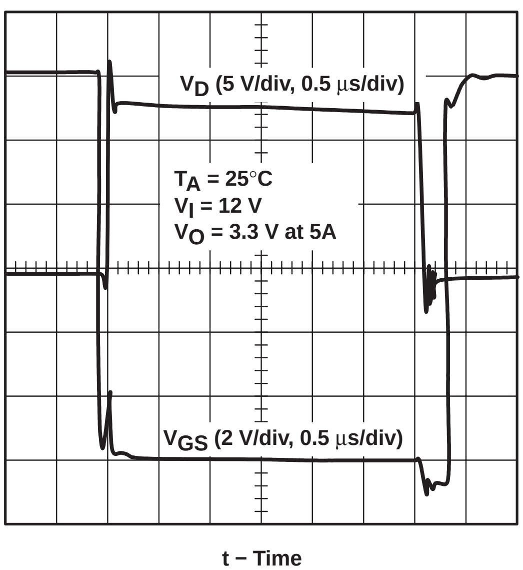

Figure 51. Q1 Drain Voltage vs Q2 Gate-Source Voltage

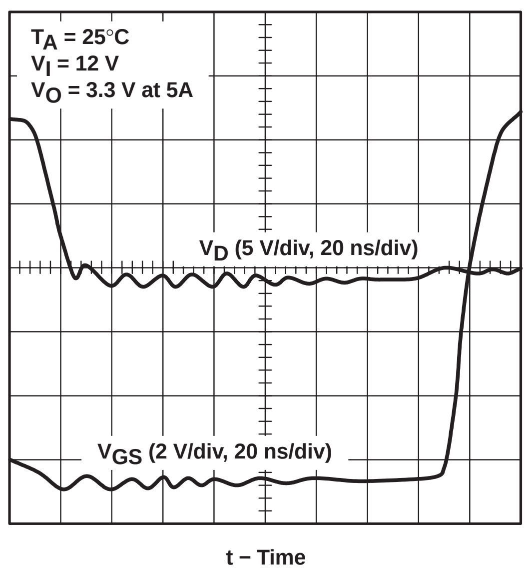

Figure 52. Q1 Drain Voltage vs Q2 Gate-Source Voltage

APPLICATION INFORMATION

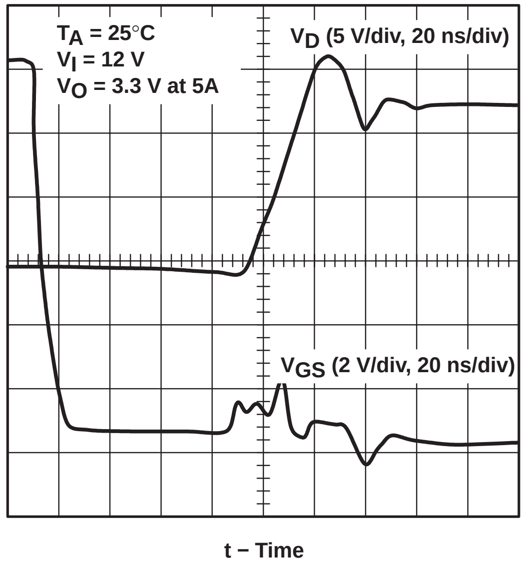

Figure 53. Q1 Drain Voltage vs Q2 Gate-Source Voltage

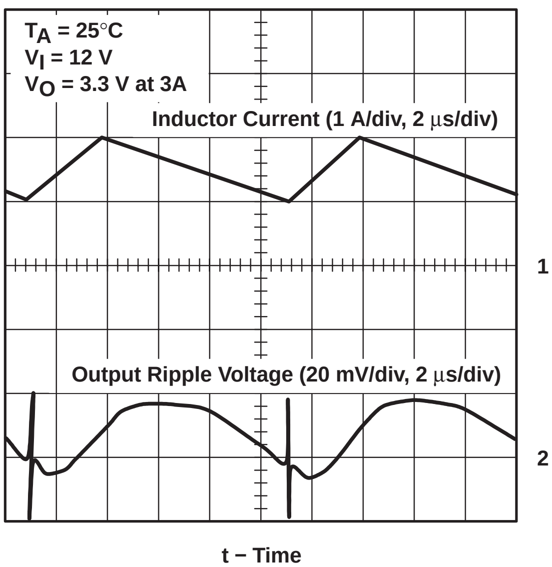

Figure 54. Output Ripple Voltage vs Inductor Current, at 3 A

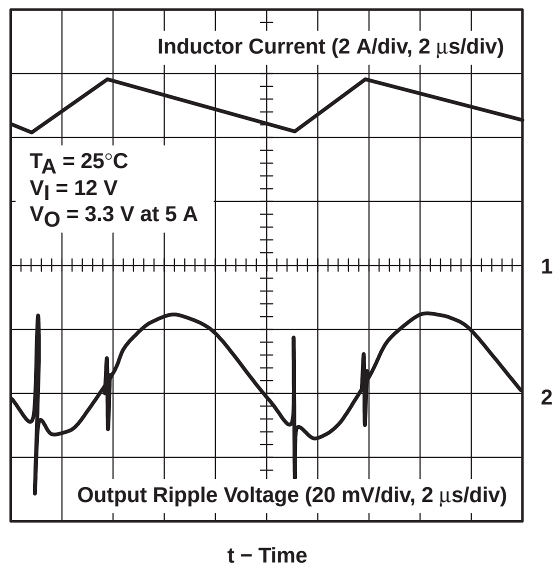

Figure 55. Output Ripple Voltage vs Inductor Current, at 5 A

PACKAGING INFORMATION

Orderable Device	Status [(1)]	Package Type	Package Drawing	Pins	Package Qty	Eco Plan [(2)]	Lead/Ball Finish	MSL Peak Temp [(3)]
TPS2811D	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS2811DG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS2811DR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS2811DRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS2811P	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
TPS2811PE4	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
TPS2811PW	ACTIVE	TSSOP	PW	8	150	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS2811PWG4	ACTIVE	TSSOP	PW	8	150	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS2811PWLE	OBSOLETE	TSSOP	PW	8		TBD	Call TI	Call TI
TPS2811PWR	ACTIVE	TSSOP	PW	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS2811PWRG4	ACTIVE	TSSOP	PW	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS2812D	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS2812DG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS2812DR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS2812DRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS2812P	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
TPS2812PE4	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
TPS2812PWLE	OBSOLETE	TSSOP	PW	8		TBD	Call TI	Call TI
TPS2812PWR	ACTIVE	TSSOP	PW	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS2812PWRG4	ACTIVE	TSSOP	PW	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS2813D	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS2813DG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS2813DR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS2813DRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS2813P	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
TPS2813PE4	ACTIVE	PDIP	P	8	50	Pb-Free	CU NIPDAU	N / A for Pkg Type

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)
						(RoHS)		
TPS2813PW	ACTIVE	TSSOP	PW	8	150	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS2813PWG4	ACTIVE	TSSOP	PW	8	150	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS2813PWLE	OBSOLETE	TSSOP	PW	8		TBD	Call TI	Call TI
TPS2813PWR	ACTIVE	TSSOP	PW	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS2813PWRG4	ACTIVE	TSSOP	PW	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS2814D	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS2814DG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS2814DR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS2814DRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS2814P	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
TPS2814PE4	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
TPS2814PW	ACTIVE	TSSOP	PW	8	150	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS2814PWG4	ACTIVE	TSSOP	PW	8	150	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS2814PWLE	OBSOLETE	TSSOP	PW	8		TBD	Call TI	Call TI
TPS2814PWR	ACTIVE	TSSOP	PW	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS2814PWRG4	ACTIVE	TSSOP	PW	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS2815D	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS2815DG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS2815DR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS2815DRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS2815P	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
TPS2815PE4	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
TPS2815PWLE	OBSOLETE	TSSOP	PW	8		TBD	Call TI	Call TI
TPS2815PWR	ACTIVE	TSSOP	PW	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS2815PWRG4	ACTIVE	TSSOP	PW	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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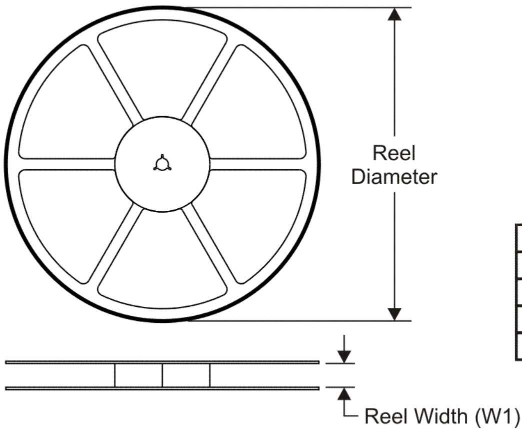
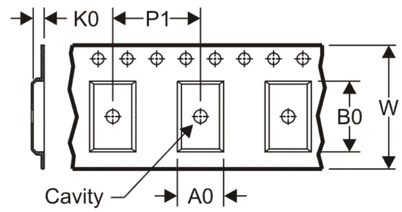
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

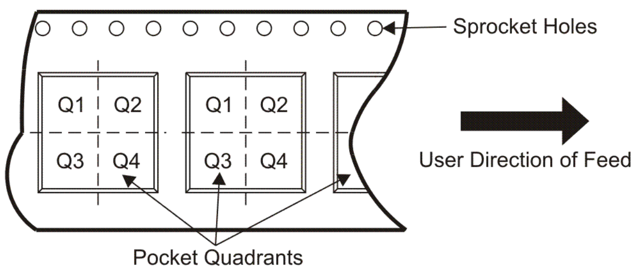


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

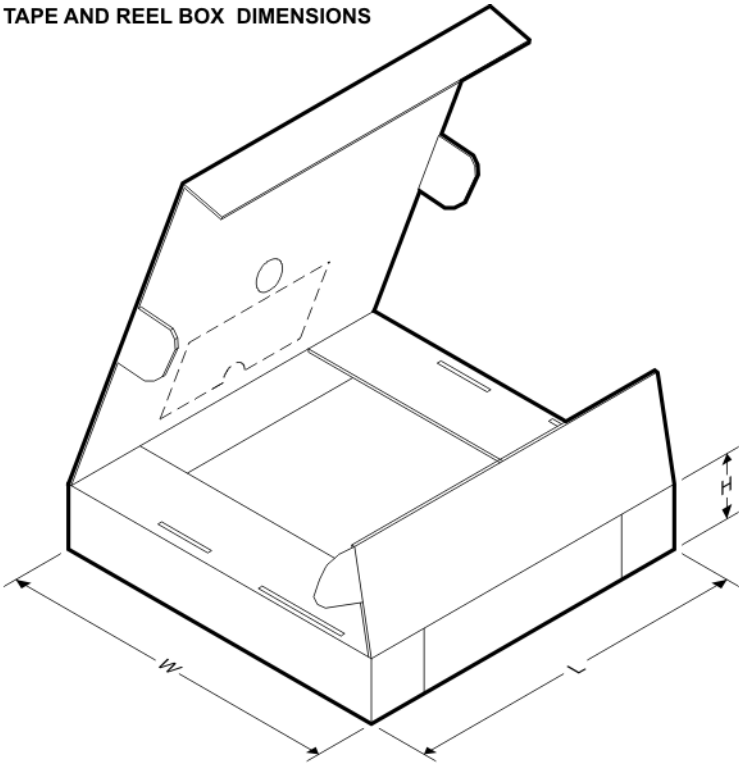
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS2811DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TPS2811PWR	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1
TPS2812DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TPS2812PWR	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1
TPS2813DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TPS2813PWR	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1
TPS2814DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TPS2814PWR	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1
TPS2815DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TPS2815PWR	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1

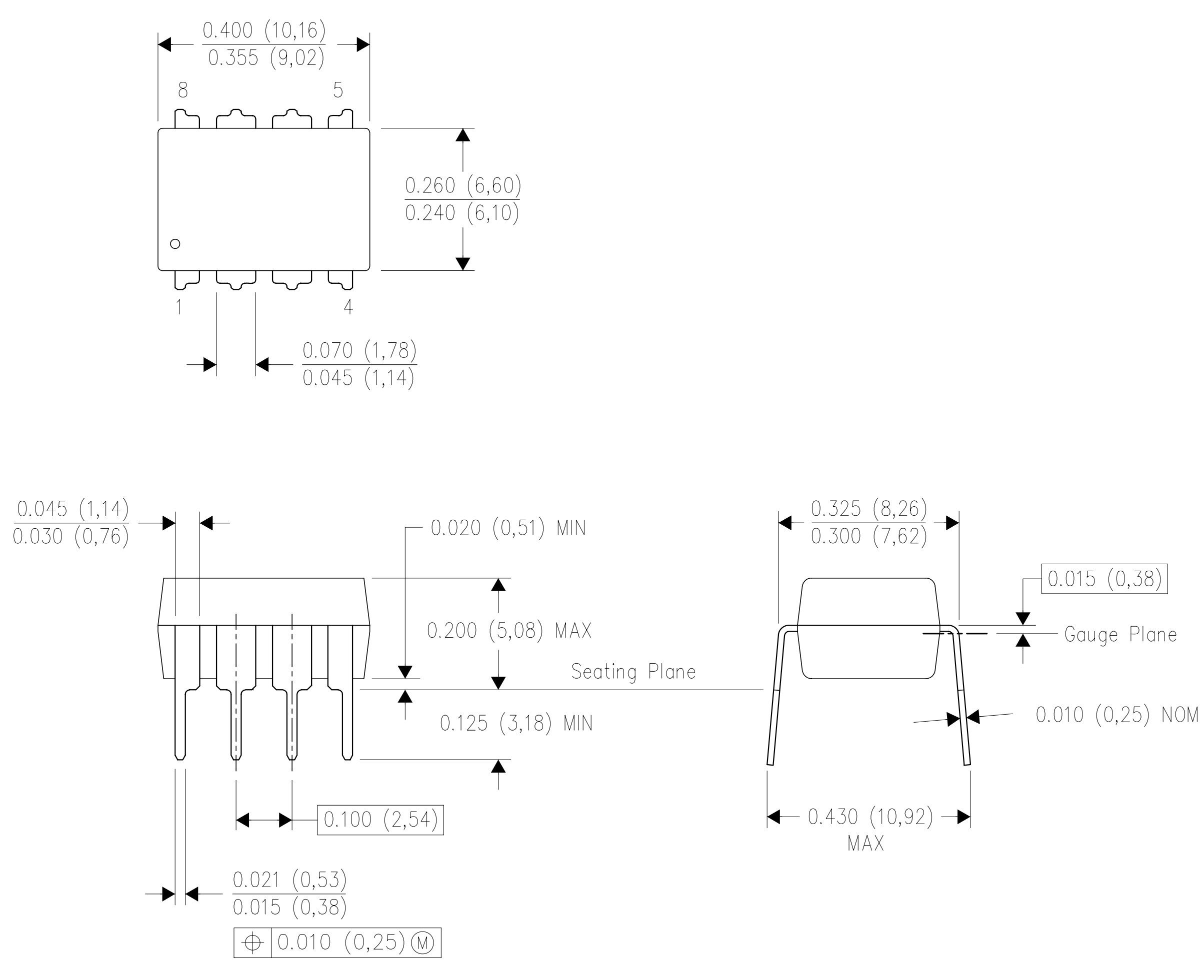
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS2811DR	SOIC	D	8	2500	346.0	346.0	29.0
TPS2811PWR	TSSOP	PW	8	2000	346.0	346.0	29.0
TPS2812DR	SOIC	D	8	2500	346.0	346.0	29.0
TPS2812PWR	TSSOP	PW	8	2000	346.0	346.0	29.0
TPS2813DR	SOIC	D	8	2500	346.0	346.0	29.0
TPS2813PWR	TSSOP	PW	8	2000	346.0	346.0	29.0
TPS2814DR	SOIC	D	8	2500	346.0	346.0	29.0
TPS2814PWR	TSSOP	PW	8	2000	346.0	346.0	29.0
TPS2815DR	SOIC	D	8	2500	346.0	346.0	29.0
TPS2815PWR	TSSOP	PW	8	2000	346.0	346.0	29.0

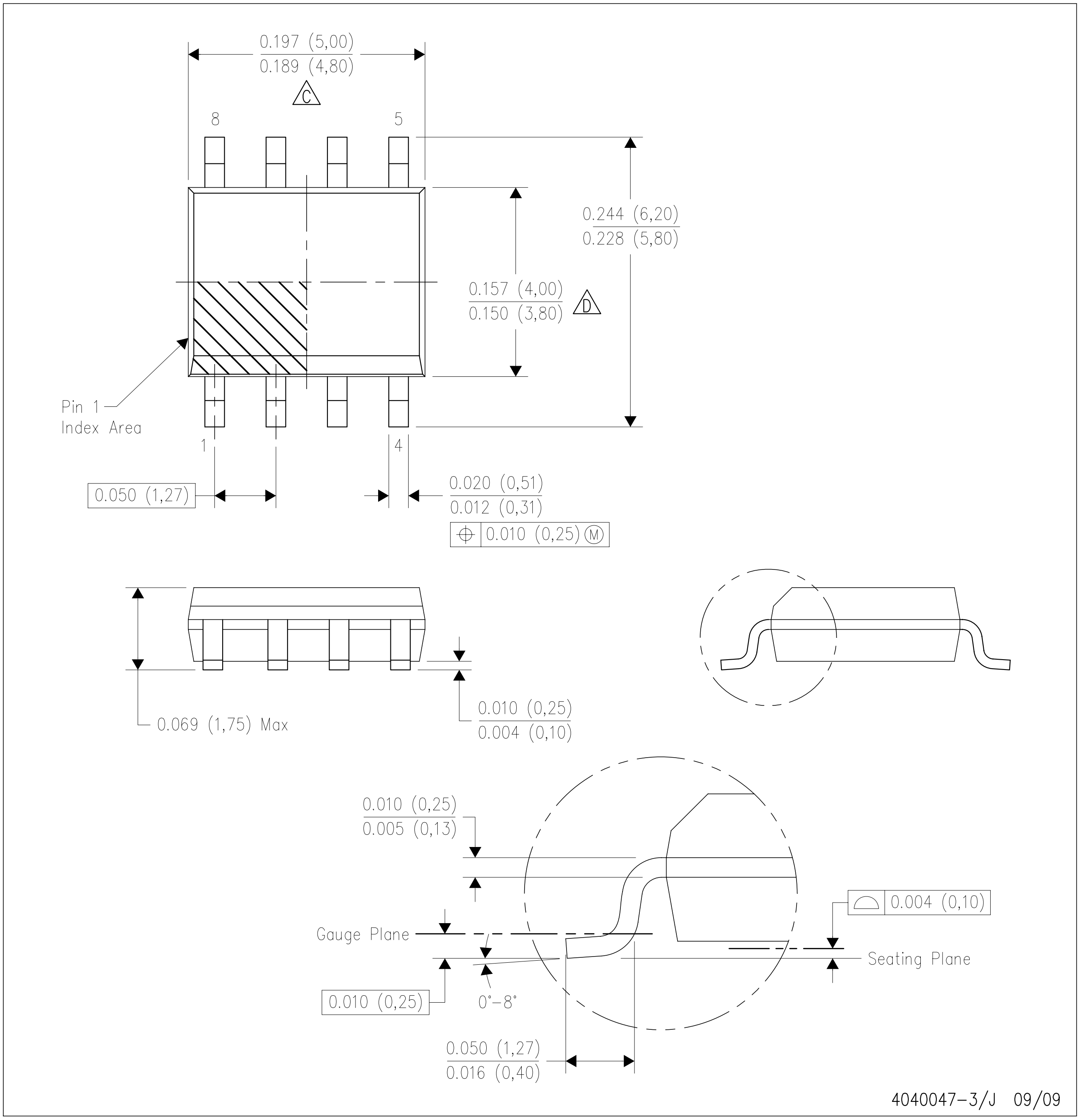
P (R–PDIP–T8) PLASTIC DUAL–IN–LINE PACKAGE



4040082/E 04/2010

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001 variation BA.

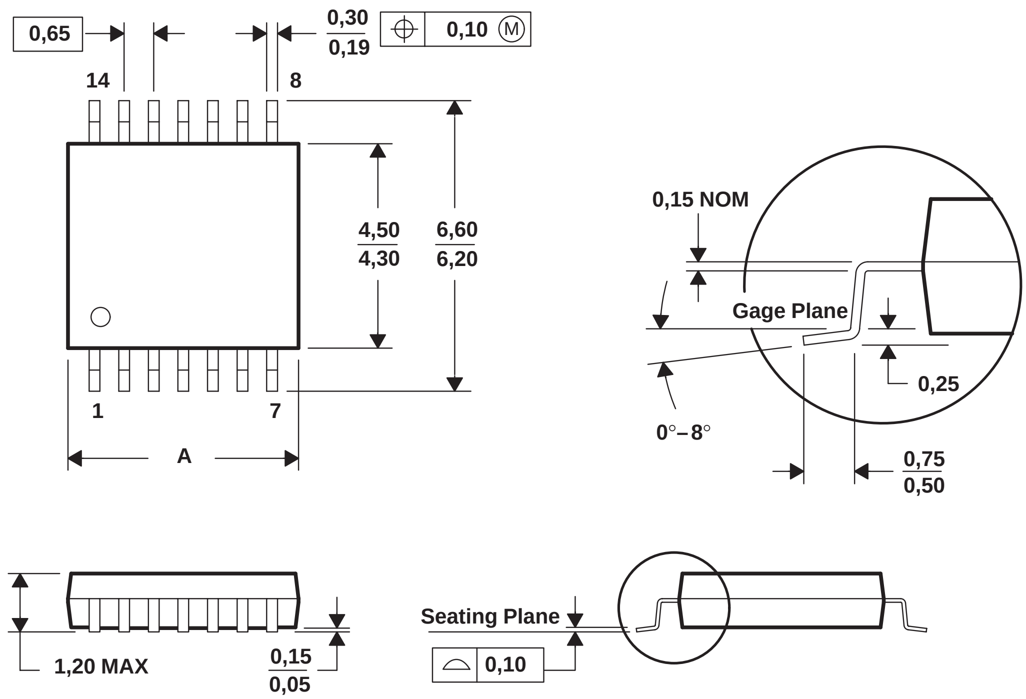
D (R-PDSO-G8) PLASTIC SMALL-OUTLINE PACKAGE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 (0,15) per end.
D. Body width does not include interlead flash. Interlead flash shall not exceed .017 (0,43) per side.
E. Reference JEDEC MS-012 variation AA.

PW (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

14 PINS SHOWN



DIM \ PINS **	8	14	16	20	24	28
A MAX	3,10	5,10	5,10	6,60	7,90	9,80
A MIN	2,90	4,90	4,90	6,40	7,70	9,60

4040064/F 01/97

NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
- D. Falls within JEDEC MO-153