500-mA, 6-MHz HIGH-EFFICIENCY STEP-DOWN CONVERTER IN LOW PROFILE CHIP SCALE PACKAGING (HEIGHT < 0.4mm)

Check for Samples: TPS6267x

FEATURES

- **92% Efficiency at 6MHz Operation**
- **17µA Quiescent Current**
- **Wide V_{IN} Range From 2.3V to 4.8V**
- **6MHz Regulated Frequency Operation**
- **Spread Spectrum, PWM Frequency Dithering**
- ***Best in Class* Load and Line Transient**
- **±2% Total DC Voltage Accuracy**
- **Low Ripple Light-Load PFM Mode**
- **>50dB V_{IN} PSRR (1kHz to 10kHz)**
- **Simple Logic Enable Inputs**
- **Supports External Clock Presence Detect Enable Input**
- **Three Surface-Mount External Components Required (One 0603 MLCC Inductor, Two 0402 Ceramic Capacitors)**
- **Complete Sub 0.33-mm Component Profile Solution**
- **Total Solution Size <10 mm^2**
- **Available in a 6-Pin NanoFree™ (CSP) Ultra-Thin Packaging, 0,4mm Max. Height**

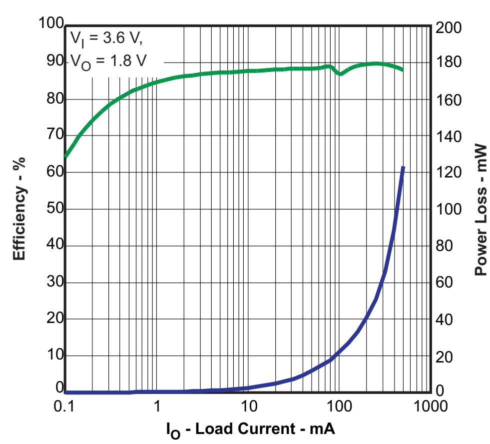


Figure 1. Efficiency vs. Load Current

APPLICATIONS

- **Cell Phones, Smart-Phones**
- **Camera Module Embedded Power**
- **Digital TV, WLAN, GPS and Bluetooth™ Applications**
- **DC/DC Micro Modules**

DESCRIPTION

The TPS6267x device is a high-frequency synchronous step-down dc-dc converter optimized for battery-powered portable applications. Intended for low-power applications, the TPS6267x supports up to 500-mA load current, and allows the use of low cost chip inductor and capacitors.

With a wide input voltage range of 2.3V to 4.8V, the device supports applications powered by Li-Ion batteries with extended voltage range. Different fixed voltage output versions are available from 1.0V to 2.3V.

The TPS6267x operates at a regulated 6-MHz switching frequency and enters the power-save mode operation at light load currents to maintain high efficiency over the entire load current range.

The PFM mode extends the battery life by reducing the quiescent current to 17µA (typ) during light load operation. For noise-sensitive applications, the device has PWM spread spectrum capability providing a lower noise regulated output, as well as low noise at the input. These features, combined with high PSRR and AC load regulation performance, make this device suitable to replace a linear regulator to obtain better power conversion efficiency.

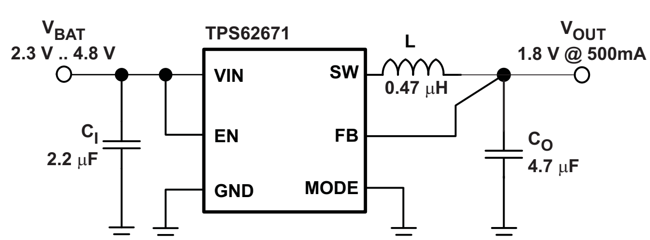


Figure 2. Smallest Solution Size Application

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

ORDERING INFORMATION(1)

T_A	PART NUMBER	OUTPUT VOLTAGE(2)	DEVICE SPECIFIC FEATURE	ORDERING(3)	PACKAGE MARKING CHIP CODE
-40°C to 85°C	TPS62671(4)	1.8V	PWM Spread Spectrum Modulation	TPS62671YFD	NZ
	TPS62672(4)	1.5V	PWM Spread Spectrum Modulation	TPS62672YFD	OA
	TPS62674	1.26V	PWM Spread Spectrum Modulation PWM Operation Only Output Capacitor Discharge	TPS62674YFD	PN
	TPS62676(4)	2.1V	PWM Spread Spectrum Modulation	TPS62676YFD	PM
	TPS62677(4)	1.2V	PWM Spread Spectrum Modulation	TPS62677YFD	

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.
(2) Internal tap points are available to facilitate output voltages in 25mV increments.
(3) The YFD package is available in tape and reel. Add a R suffix (e.g. TPS62670YFDR) to order quantities of 3000 parts. Add a T suffix (e.g. TPS62670YFDT) to order quantities of 250 parts.
(4) Product preview.

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted)(1)

		UNIT
V_I	Voltage at VIN(2), SW(3)	–0.3 V to 6 V
	Voltage at FB(3)	–0.3 V to 3.6 V
	Voltage at EN, MODE (3)	–0.3 V to V_I + 0.3 V
	Power dissipation	Internally limited
T_A	Operating temperature range(4)	–40°C to 85°C
T_J (max)	Maximum operating junction temperature	150°C
T_{stg}	Storage temperature range	–65°C to 150°C
ESD rating (5)	Human body model	2 kV
	Charge device model	1 kV
	Machine model	200 V

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) Operation above 4.8V input voltage for extended periods may affect device reliability.
(3) All voltage values are with respect to network ground terminal.
(4) In applications where high power dissipation and/or poor package thermal resistance is present, the maximum ambient temperature may have to be derated. Maximum ambient temperature ($T_{A(max)}$) is dependent on the maximum operating junction temperature ($T_{J(max)}$), the maximum power dissipation of the device in the application ($P_{D(max)}$), and the junction-to-ambient thermal resistance of the part/package in the application (θ_{JA}), as given by the following equation: $T_{A(max)} = T_{J(max)} – (\theta_{JA} \times P_{D(max)})$. To achieve optimum performance, it is recommended to operate the device with a maximum junction temperature of 105°C.
(5) The human body model is a 100-pF capacitor discharged through a 1.5-kΩ resistor into each pin. The machine model is a 200-pF capacitor discharged directly into each pin.

RECOMMENDED OPERATING CONDITIONS

		MIN	NOM	MAX	UNIT
V_I	Input voltage range	2.3		4.8 (1)	V
I_O	Output current range	0		500	mA
L	Inductance	0.3		1.8	µH
C_O	Output capacitance	1.4	2.5	12	µF
T_A	Ambient temperature	–40		+85	°C
T_J	Operating junction temperature	–40		+125	°C

(1) Operation above 4.8V input voltage for extended periods may affect device reliability.

DISSIPATION RATINGS (1)

PACKAGE	$R_{\theta JA}$ (2)	$R_{\theta JB}$ (2)	POWER RATING $T_A \leq 25°C$	DERATING FACTOR ABOVE T_A = 25°C
YFD-6	125°C/W	53°C/W	800mW	8mW/°C

(1) Maximum power dissipation is a function of T_J(max), θ_{JA} and T_A. The maximum allowable power dissipation at any allowable ambient temperature is $P_D = [T_J(max)–T_A] / \theta_{JA}$.
(2) This thermal data is measured with high-K board (4 layers board according to JESD51-7 JEDEC standard).

ELECTRICAL CHARACTERISTICS

Minimum and maximum values are at V_I = 2.3V to 5.5V, V_O = 1.8V, EN = 1.8V, AUTO mode and T_A = –40°C to 85°C; Circuit of Parameter Measurement Information section (unless otherwise noted). Typical values are at V_I = 3.6V, V_O = 1.8V, EN = 1.8V, AUTO mode and T_A = 25°C (unless otherwise noted).

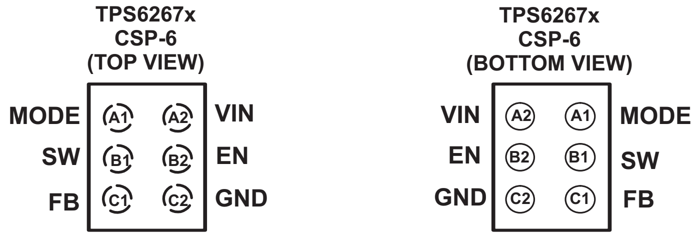
PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY CURRENT							
I_Q	Operating quiescent current	TPS62671 TPS62672 TPS62676 TPS62677	I_O = 0mA. Device not switching		17	40	µA
		TPS62671	I_O = 0mA, PWM mode		5.5		mA
		TPS62674	I_O = 0mA, PWM mode		5.0		mA
$I_{(SD)}$	Shutdown current		EN = GND		0.2	1	µA
UVLO	Undervoltage lockout threshold				2.05	2.1	V
ENABLE, MODE							
V_{IH}	High-level input voltage	TPS62671 TPS62672 TPS62676 TPS62677		1.0			V
V_{IL}	Low-level input voltage					0.4	V
I_{lkg}	Input leakage current		Input connected to GND or VIN		0.01	1.5	µA
V_{IH}	High-level input voltage (ENABLE)	TPS62674		1.26			V
	High-level input voltage (MODE)			1.0			V
V_{IL}	Low-level input voltage (ENABLE)					0.54	V
I_{lkg}	Input leakage current		Input connected to GND or VIN		0.01	1.5	µA
C_{IN}	Input capacitance (ENABLE)				5		pF
EXTCLK	Clock presence detect frequency			4		27	MHz
	Clock presence detect duty cycle			40		60	%

ELECTRICAL CHARACTERISTICS (continued)

Minimum and maximum values are at V_I = 2.3V to 5.5V, V_O = 1.8V, EN = 1.8V, AUTO mode and T_A = –40°C to 85°C; Circuit of Parameter Measurement Information section (unless otherwise noted). Typical values are at V_I = 3.6V, V_O = 1.8V, EN = 1.8V, AUTO mode and T_A = 25°C (unless otherwise noted).

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
POWER SWITCH							
$r_{DS(on)}$	P-channel MOSFET on resistance		$V_I = V_{(GS)}$ = 3.6V. PWM mode		170		mΩ
			$V_I = V_{(GS)}$ = 2.5V. PWM mode		230		mΩ
I_{lkg}	P-channel leakage current, PMOS		$V_{(DS)}$ = 5.5V, -40°C ≤ T_J ≤ 85°C			1	µA
$r_{DS(on)}$	N-channel MOSFET on resistance		$V_I = V_{(GS)}$ = 3.6V. PWM mode		120		mΩ
			$V_I = V_{(GS)}$ = 2.5V. PWM mode		180		mΩ
I_{lkg}	N-channel leakage current, NMOS		$V_{(DS)}$ = 5.5V, -40°C ≤ T_J ≤ 85°C			2	µA
r_{DIS}	Discharge resistor for power-down sequence				70	150	Ω
	P-MOS current limit		2.3V ≤ V_I ≤ 4.8V. Open loop	900	1000	1150	mA
	Input current limit under short-circuit conditions		V_O shorted to ground		12		mA
	Thermal shutdown				140		°C
	Thermal shutdown hysteresis				10		°C
OSCILLATOR							
f_{SW}	Oscillator center frequency	TPS62671 TPS62672 TPS62676 TPS62677	I_O = 0mA. PWM operation	5.4	6	6.6	MHz
	Oscillator center frequency	TPS62674	I_O = 0mA. PWM operation	4.9	5.45	6.0	MHz
OUTPUT							
$V_{(OUT)}$	Regulated DC output voltage	TPS62671 TPS62672 TPS62676 TPS62677	2.3V ≤ V_I ≤ 4.8V, 0mA ≤ I_O ≤ 500 mA PFM/PWM operation	0.98×V_{NOM}	V_{NOM}	1.03×V_{NOM}	V
			2.3V ≤ V_I ≤ 5.5V, 0mA ≤ I_O ≤ 500 mA PFM/PWM operation	0.98×V_{NOM}	V_{NOM}	1.04×V_{NOM}	V
			2.3V ≤ V_I ≤ 5.5V, 0mA ≤ I_O ≤ 500 mA PWM operation	0.98×V_{NOM}	V_{NOM}	1.02×V_{NOM}	V
		TPS62674	2.3V ≤ V_I ≤ 5.5V, 0mA ≤ I_O ≤ 500 mA PWM operation	0.98×V_{NOM}	V_{NOM}	1.02×V_{NOM}	V
	Line regulation	TPS6267X	$V_I = V_O$ + 0.5V (min 2.3V) to 5.5V, I_O = 200 mA		0.23		%/V
	Load regulation		I_O = 0mA to 500 mA. PWM operation		–0.00045		%/mA
	Feedback input resistance				480		kΩ
ΔV_O	Power-save mode ripple voltage	TPS62671	I_O = 1mA, V_O = 1.8 V		20		mV_{PP}
		TPS62677	I_O = 1mA, V_O = 1.2 V		24		mV_{PP}
PSRR	Power Supply Rejection Ratio	TPS62671	f = 10kHz, I_O = 150mA. PWM mode		TBD		dB
	Start-up time	TPS62671	I_O = 0mA, Time from active EN to V_O		130		µs
		TPS62674	I_O = 0mA, Time from EXTCLK clock active to V_O		125		µs
	Shutdown time	TPS62674	I_O = 0mA, Time from EXTCLK clock inactive to V_O down		1.2		ms

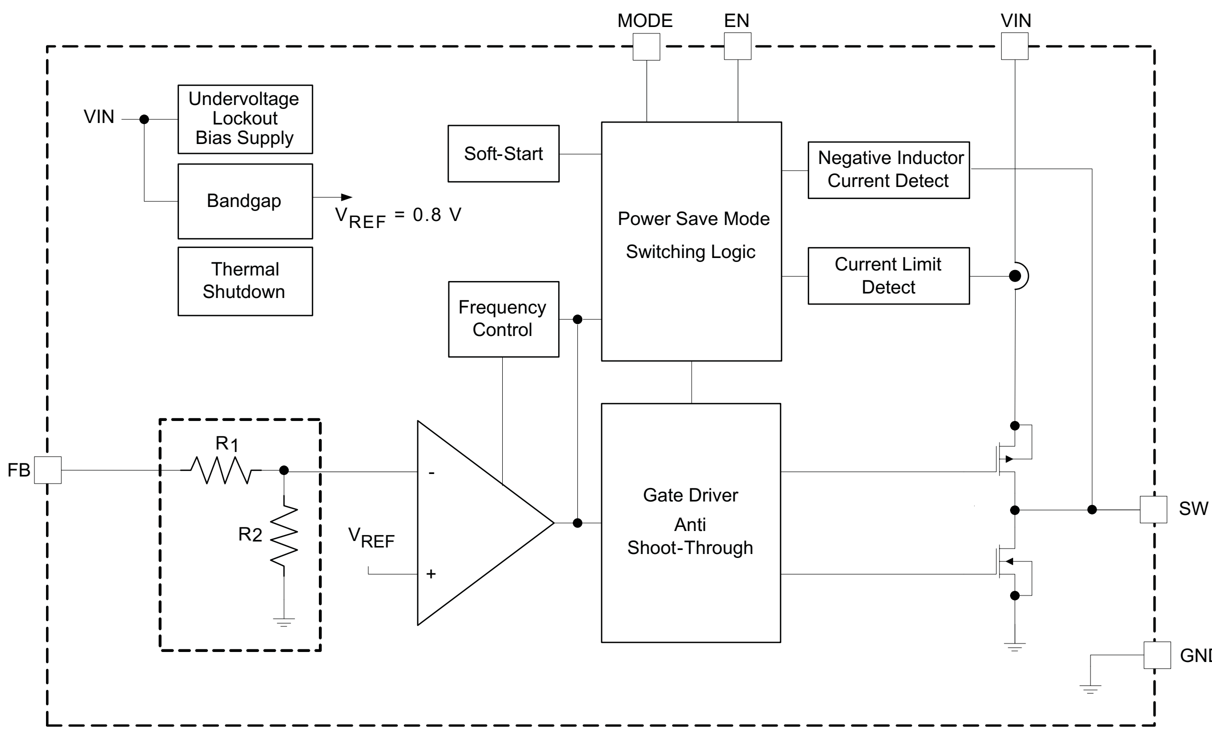
PIN ASSIGNMENTS



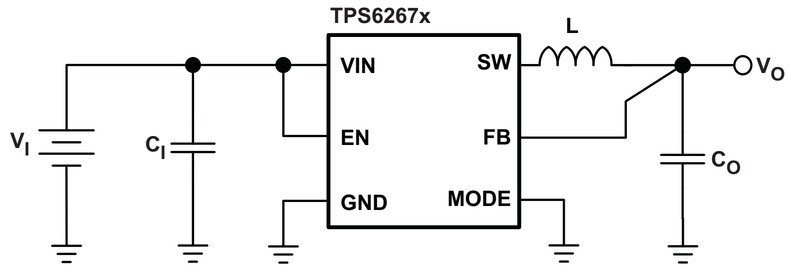
TERMINAL FUNCTIONS

TERMINAL		I/O	DESCRIPTION
NAME	NO.		
FB	C1	I	Output feedback sense input. Connect FB to the converter's output.
VIN	A2	I	Power supply input.
SW	B1	I/O	This is the switch pin of the converter and is connected to the drain of the internal Power MOSFETs.
EN	B2	I	This is the enable pin of the device. Connecting this pin to ground forces the device into shutdown mode. Pulling this pin to V_I enables the device. If an external clock (4MHz to 27MHz) is detected the device will automatically power up. This pin must not be left floating and must be terminated.
MODE	A1	I	This is the mode selection pin of the device. This pin must not be left floating and must be terminated.
			MODE = LOW: The device is operating in regulated frequency pulse width modulation mode (PWM) at high-load currents and in pulse frequency modulation mode (PFM) at light load currents. MODE = HIGH: Low-noise mode enabled, regulated frequency PWM operation forced.
GND	C2	–	Ground pin.

FUNCTIONAL BLOCK DIAGRAM



PARAMETER MEASUREMENT INFORMATION



List of components:

- L = MURATA LQM21PN1R0NGR
- C_I = MURATA GRM155R60J225ME15 (2.2µF, 6.3V, 0402, X5R)
- C_O = MURATA GRM155R60J475M (4.7µF, 6.3V, 0402, X5R)

TYPICAL CHARACTERISTICS

Table of Graphs

			FIGURE
η	Efficiency	vs Load current	3, 4, 5, 6
		vs Input voltage	7
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	Load transient response		12, 13, 14, 15, 16, 17, 18
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I_Q	Quiescent current	vs Input voltage	24
f_s	PWM switching frequency	vs Input voltage	25, 26
	PFM switching frequency	vs Input voltage	27
PSRR	Power supply rejection ratio	vs. Frequency	28
	PWM operation		29, 30
	Power-save mode operation		31
	Start-up		32, 33
	Shutdown		34
	Spurious output noise (PWM mode)	vs. Frequency	35, 36, 38
	Spurious output noise (PFM mode)	vs. Frequency	37

EFFICIENCY
vs
LOAD CURRENT

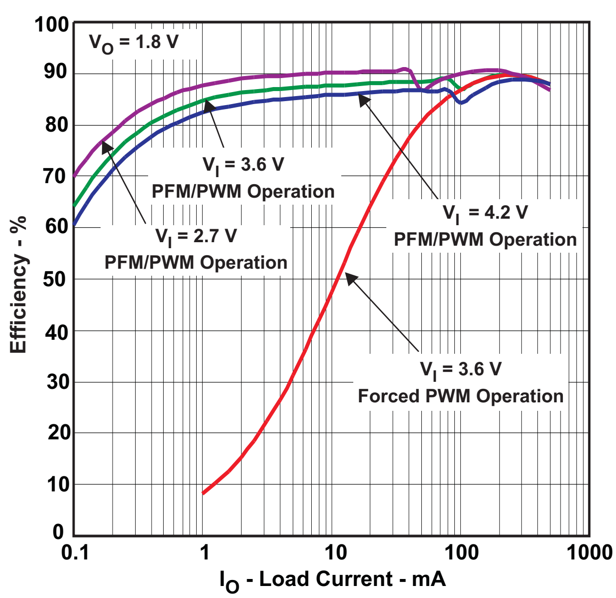


Figure 3.

EFFICIENCY
vs
LOAD CURRENT

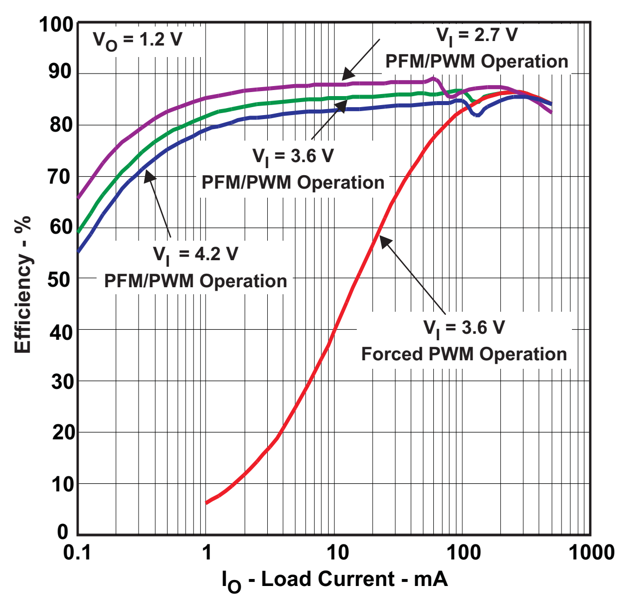


Figure 4.

TYPICAL CHARACTERISTICS (continued)

EFFICIENCY
vs
LOAD CURRENT

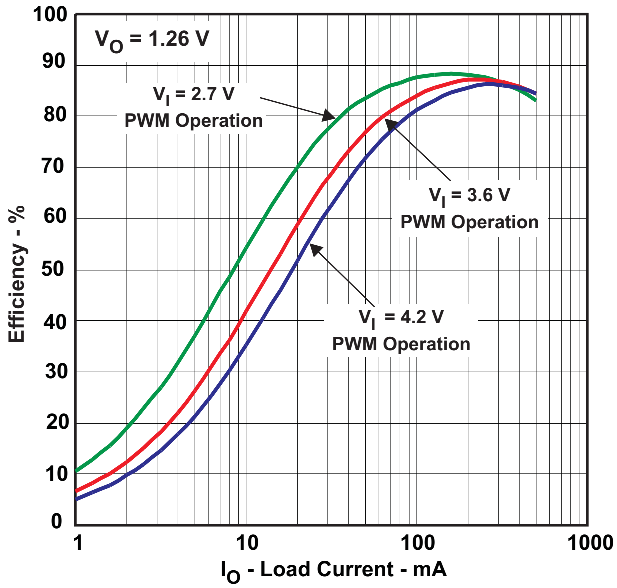


Figure 5.

EFFICIENCY
vs
LOAD CURRENT

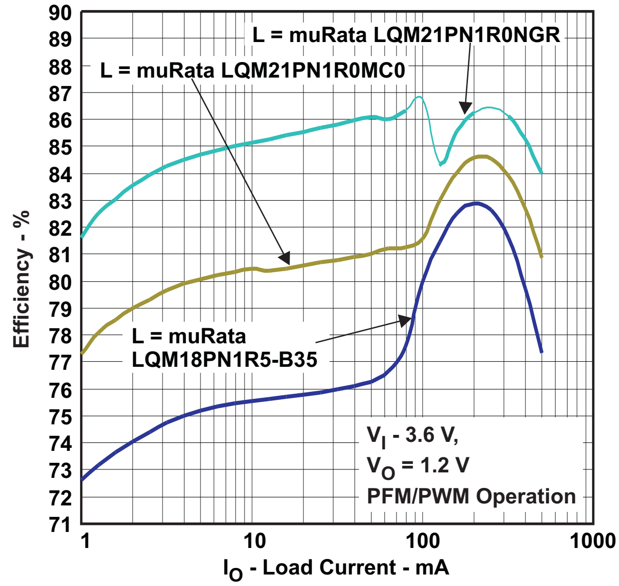


Figure 6.

EFFICIENCY
vs
INPUT VOLTAGE

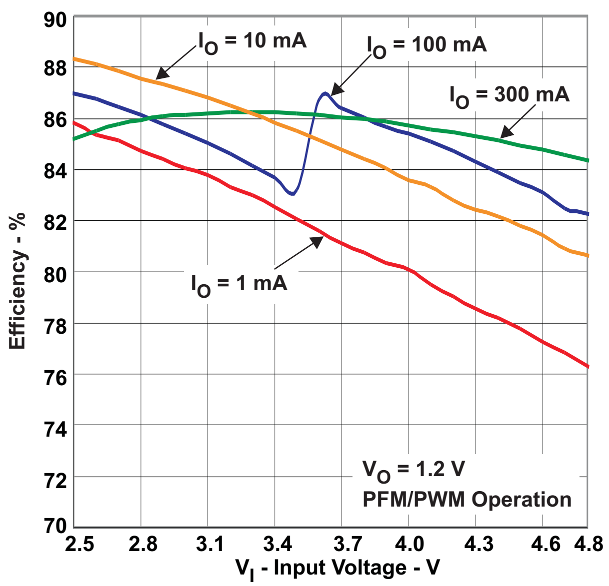


Figure 7.

PEAK-TO-PEAK OUTPUT RIPPLE VOLTAGE
vs
LOAD CURRENT

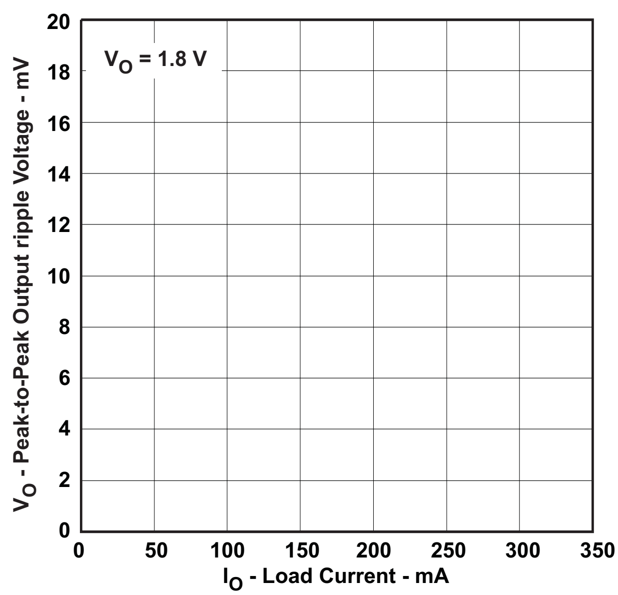


Figure 8.

TYPICAL CHARACTERISTICS (continued)

PEAK-TO-PEAK OUTPUT RIPPLE VOLTAGE
vs
LOAD CURRENT

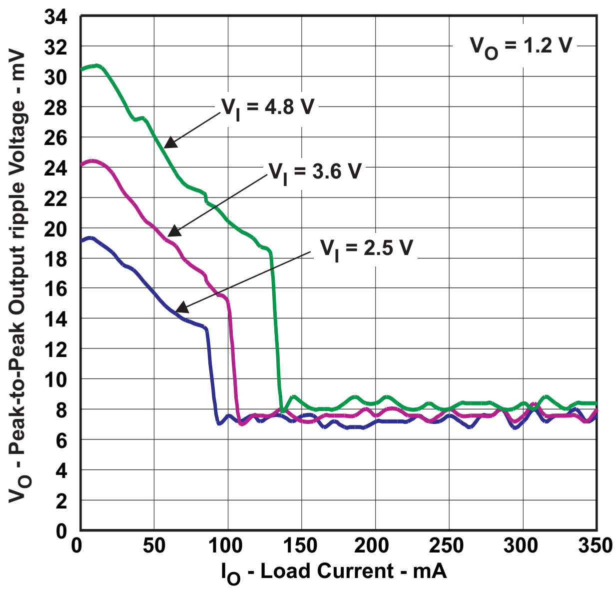


Figure 9.

COMBINED LINE/LOAD TRANSIENT RESPONSE

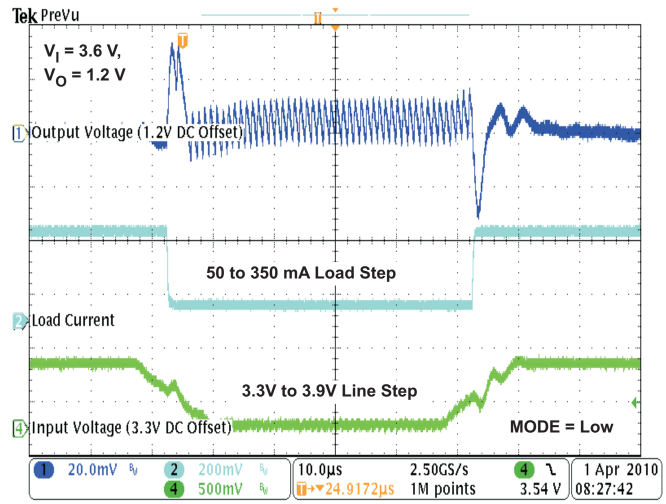


Figure 10.

COMBINED LINE/LOAD TRANSIENT RESPONSE

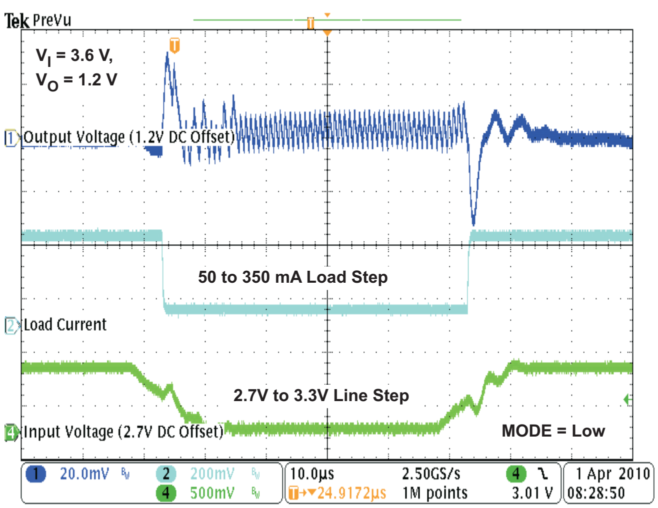


Figure 11.

LOAD TRANSIENT RESPONSE IN
PFM/PWM OPERATION

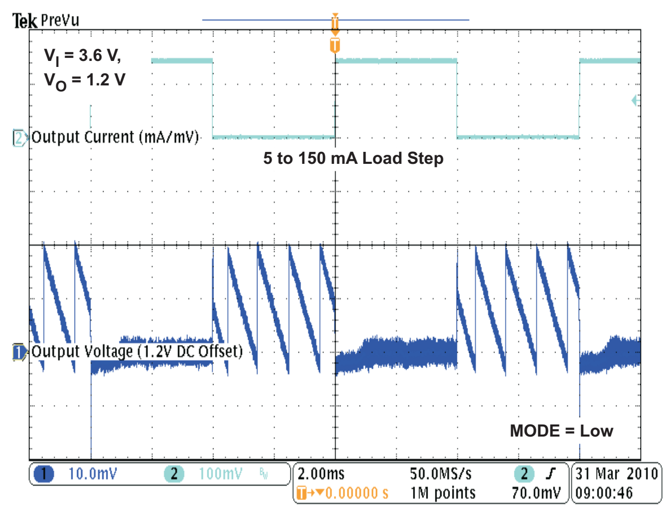


Figure 12.

TYPICAL CHARACTERISTICS (continued)

LOAD TRANSIENT RESPONSE IN PFM/PWM OPERATION

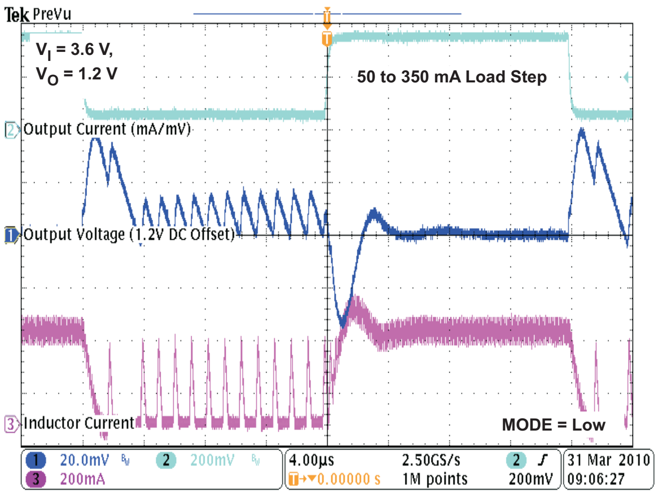


Figure 13.

LOAD TRANSIENT RESPONSE IN PFM/PWM OPERATION

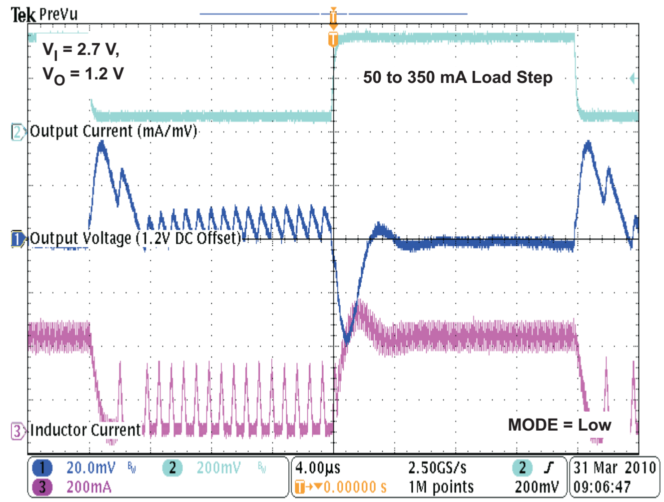


Figure 14.

LOAD TRANSIENT RESPONSE IN PFM/PWM OPERATION

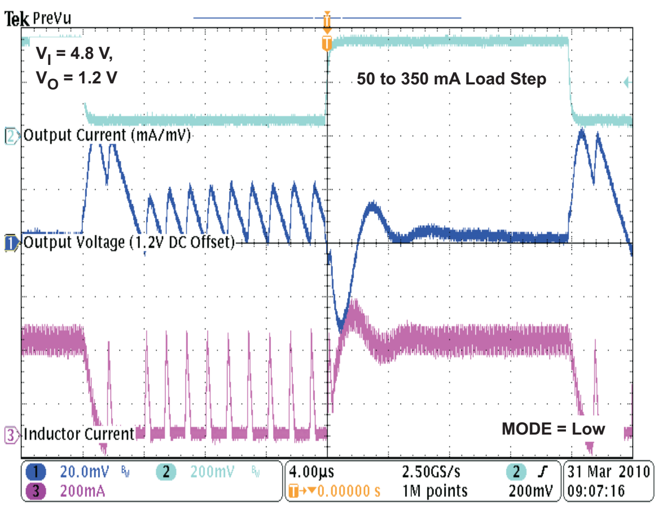


Figure 15.

LOAD TRANSIENT RESPONSE IN PFM/PWM OPERATION

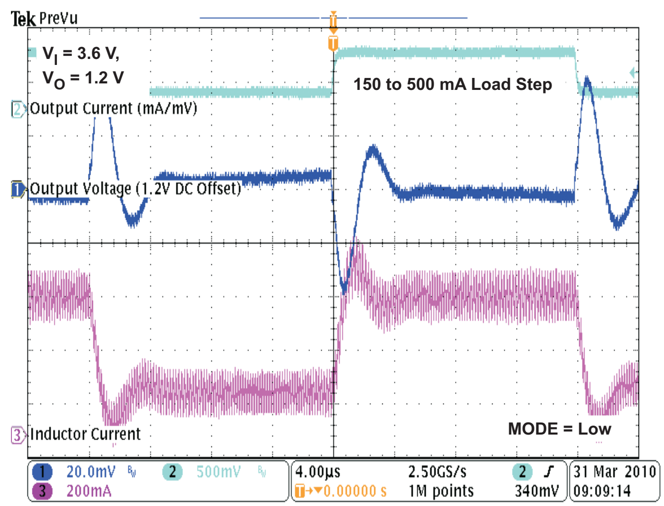


Figure 16.

TYPICAL CHARACTERISTICS (continued)

LOAD TRANSIENT RESPONSE IN PFM/PWM OPERATION

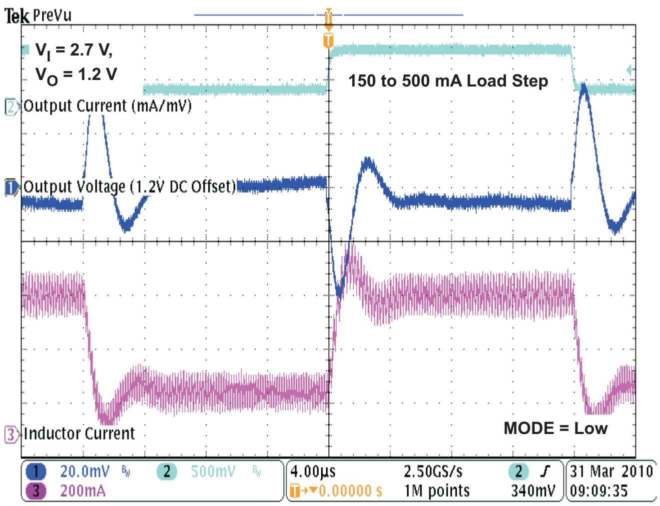


Figure 17.

LOAD TRANSIENT RESPONSE IN PFM/PWM OPERATION

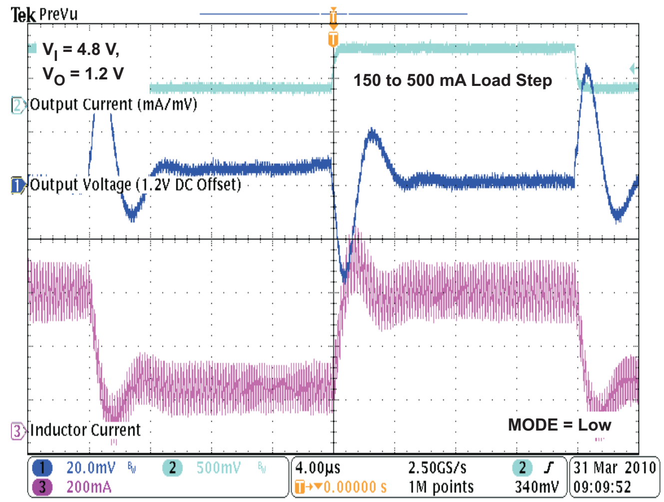


Figure 18.

AC LOAD TRANSIENT RESPONSE

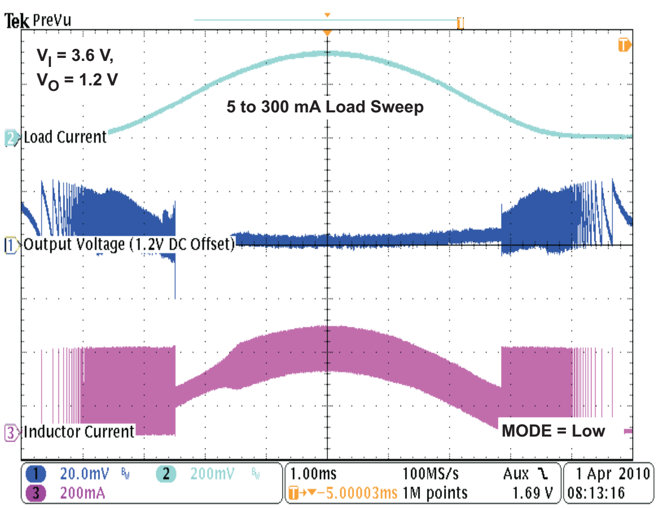


Figure 19.

DC OUTPUT VOLTAGE vs LOAD CURRENT

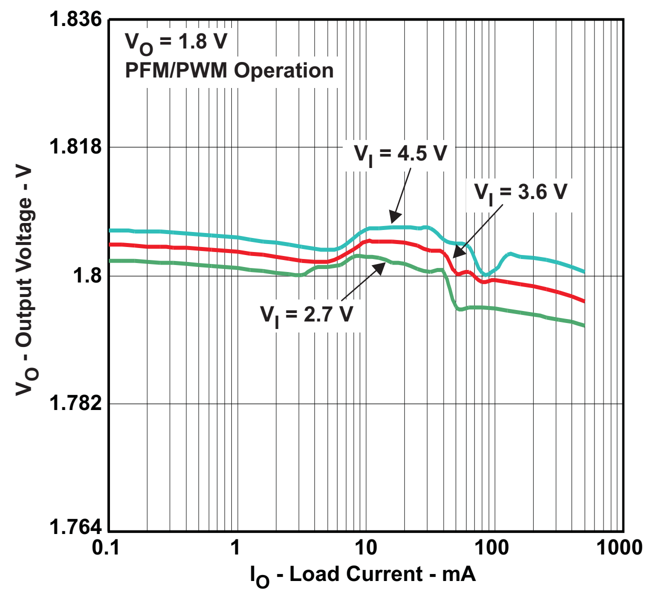


Figure 20.

TYPICAL CHARACTERISTICS (continued)

DC OUTPUT VOLTAGE
vs
LOAD CURRENT

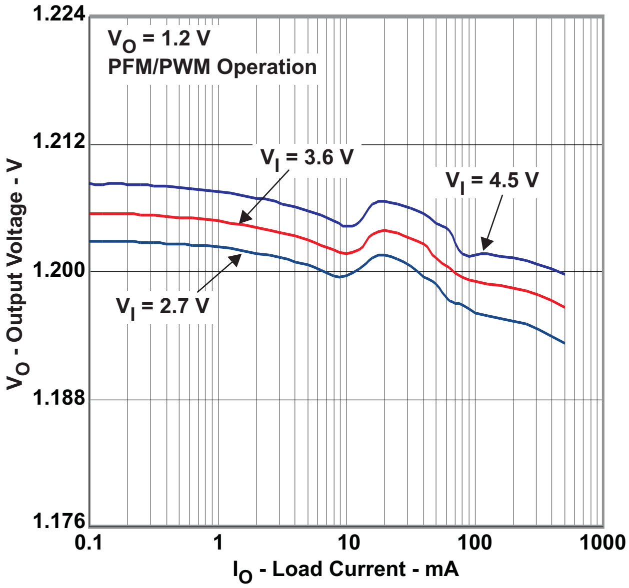


Figure 21.

OUTPUT VOLTAGE
vs
LOAD CURRENT

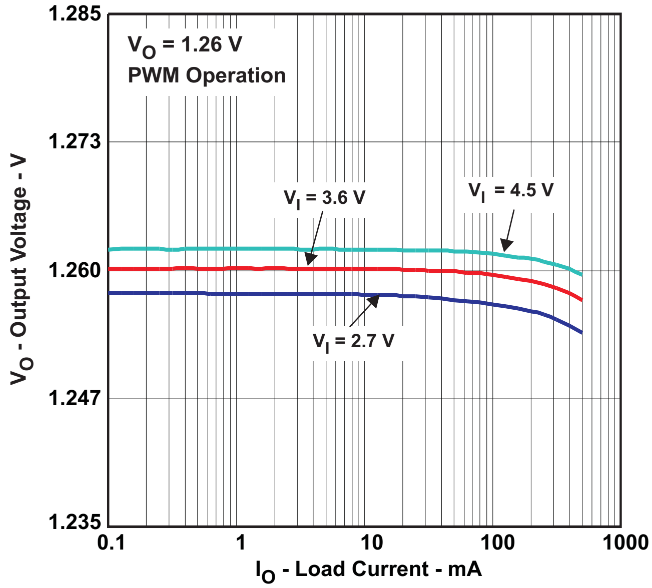


Figure 22.

PFM/PWM BOUNDARIES

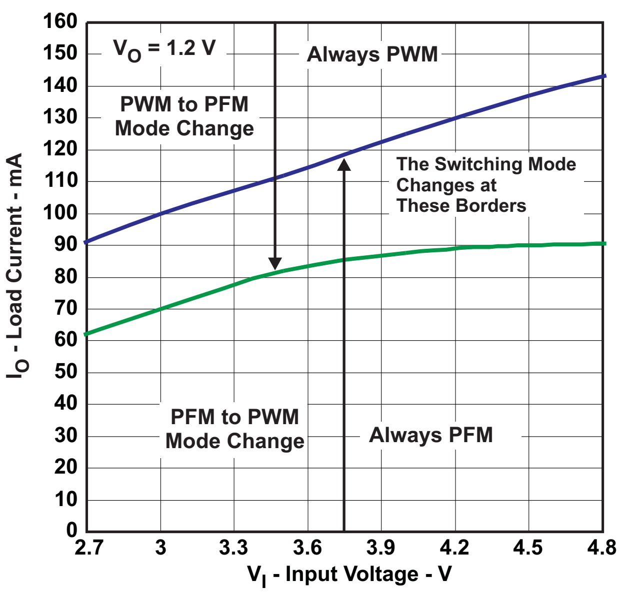


Figure 23.

QUIESCENT CURRENT
vs
INPUT VOLTAGE

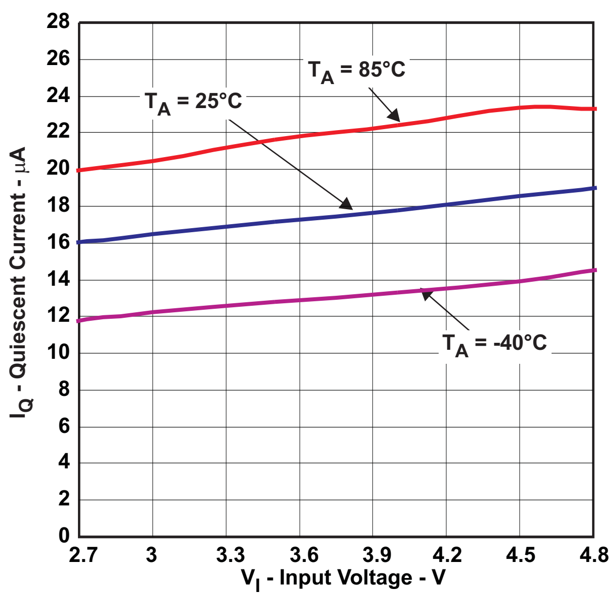


Figure 24.

TYPICAL CHARACTERISTICS (continued)

PWM SWITCHING FREQUENCY
vs
INPUT VOLTAGE

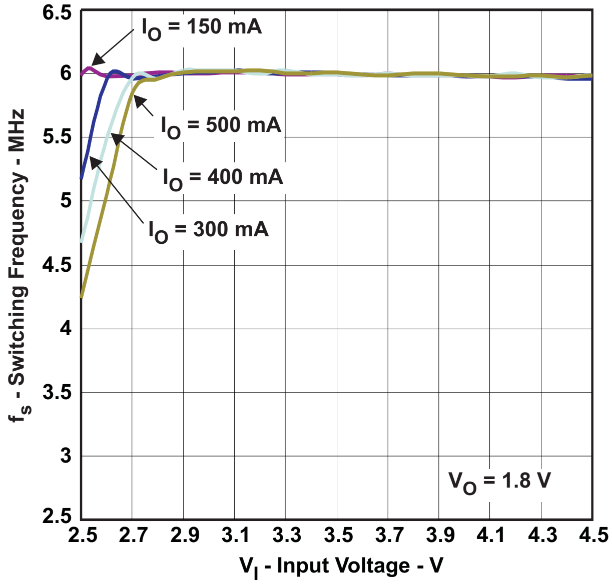


Figure 25.

PWM SWITCHING FREQUENCY
vs
INPUT VOLTAGE

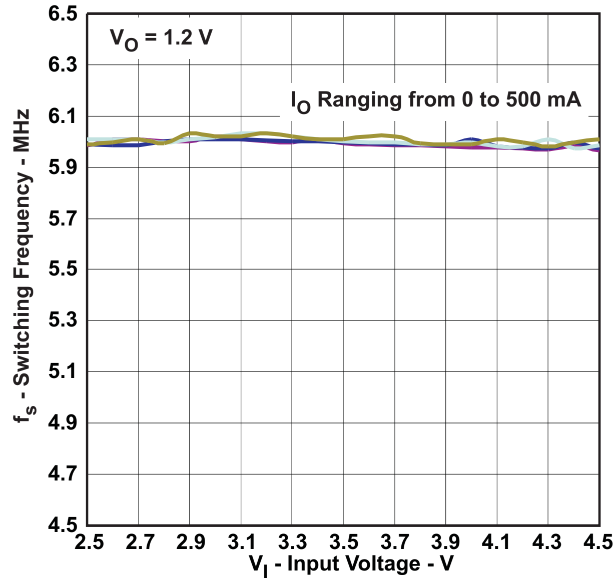


Figure 26.

PFM SWITCHING FREQUENCY
vs
INPUT VOLTAGE

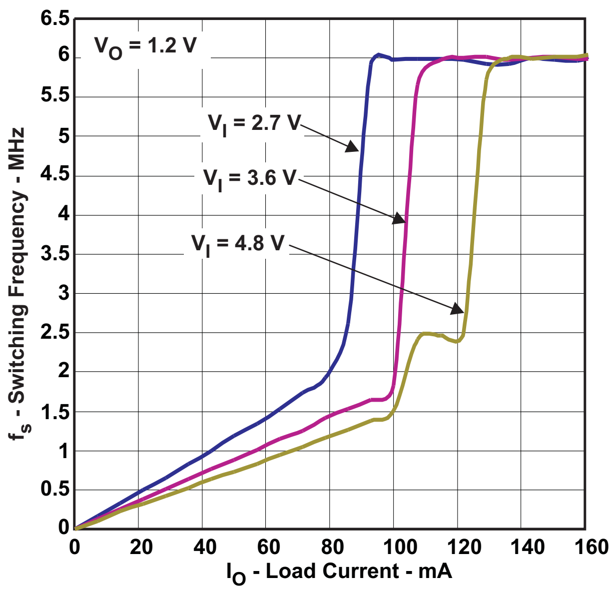


Figure 27.

POWER SUPPLY REJECTION RATIO
vs
FREQUENCY

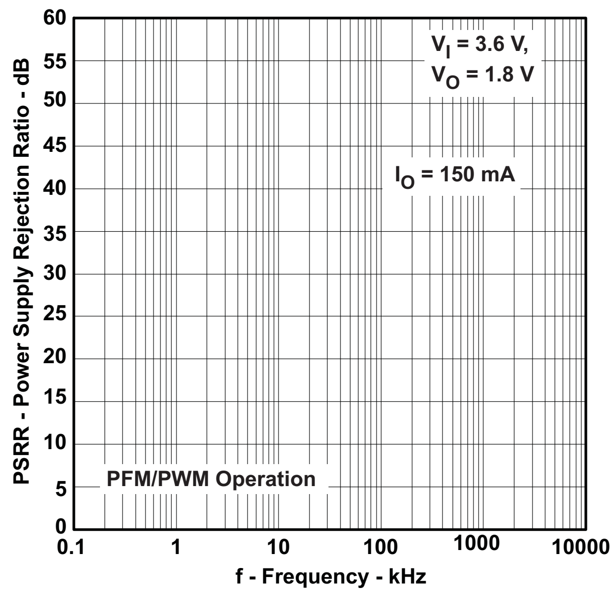


Figure 28.

TYPICAL CHARACTERISTICS (continued)

PWM OPERATION

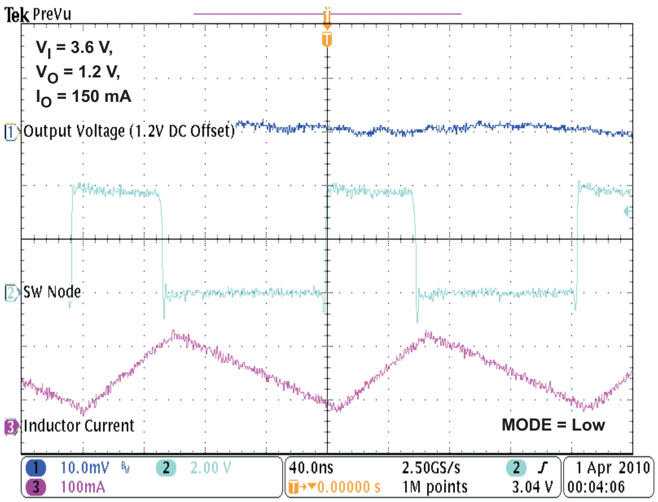


Figure 29.

PWM OPERATION SSFM MODULATION

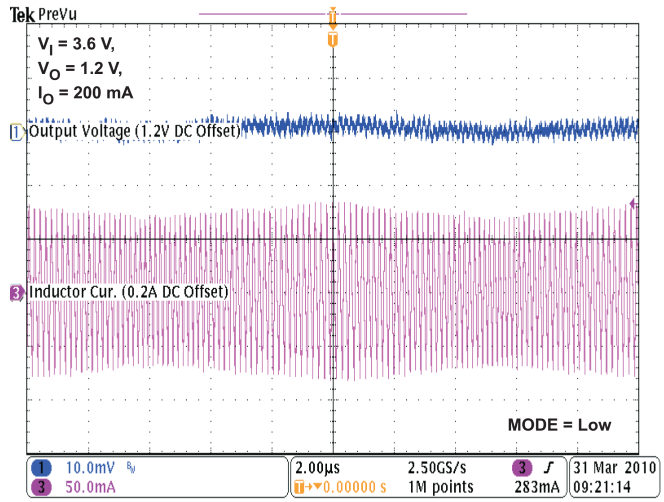


Figure 30.

POWER-SAVE MODE OPERATION

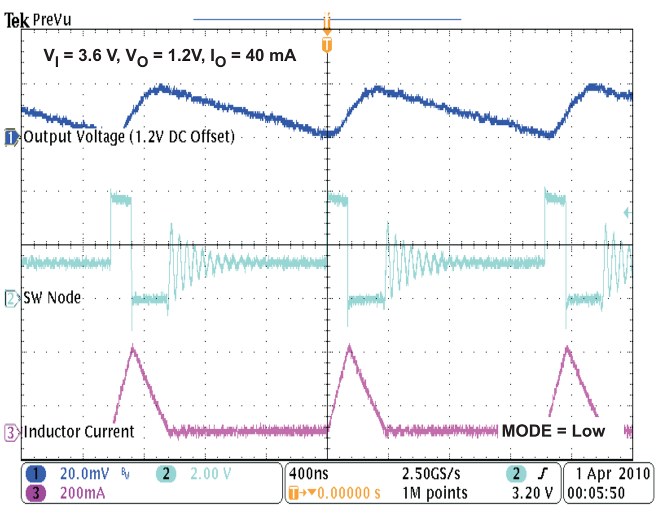


Figure 31.

START-UP

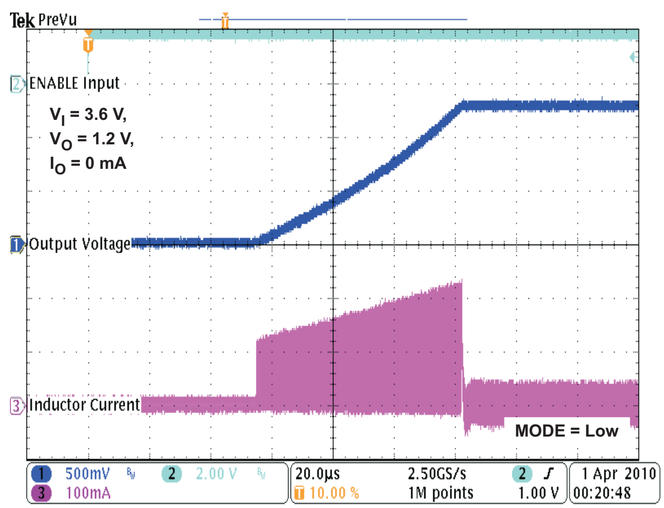


Figure 32.

TYPICAL CHARACTERISTICS (continued)

START-UP (RF CLOCK)

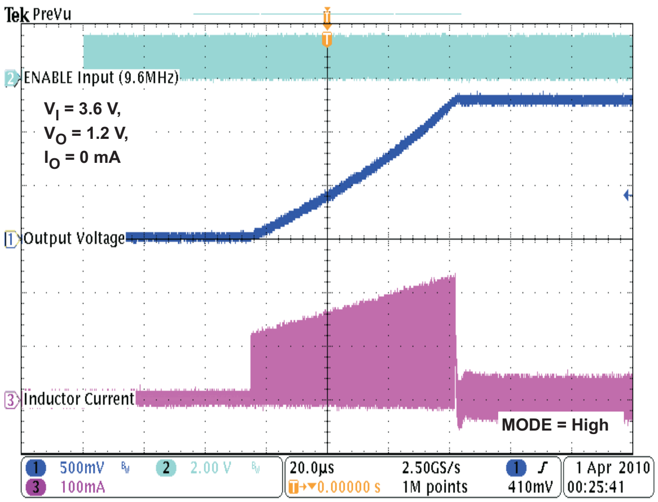


Figure 33.

SHUT-DOWN (RF CLOCK)
vs

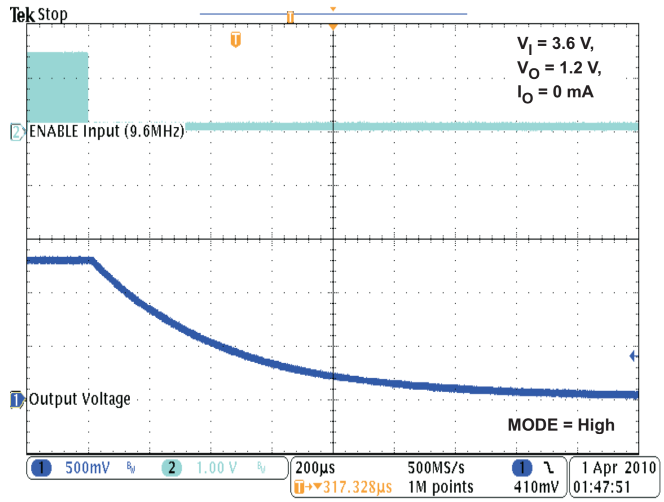


Figure 34.

SPURIOUS OUTPUT NOISE (PWM MODE)
vs
FREQUENCY

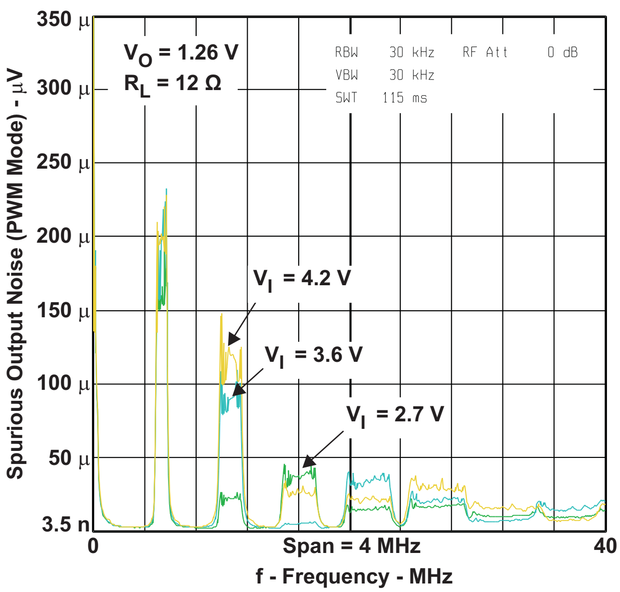


Figure 35.

SPURIOUS OUTPUT NOISE (PWM MODE)
vs
FREQUENCY

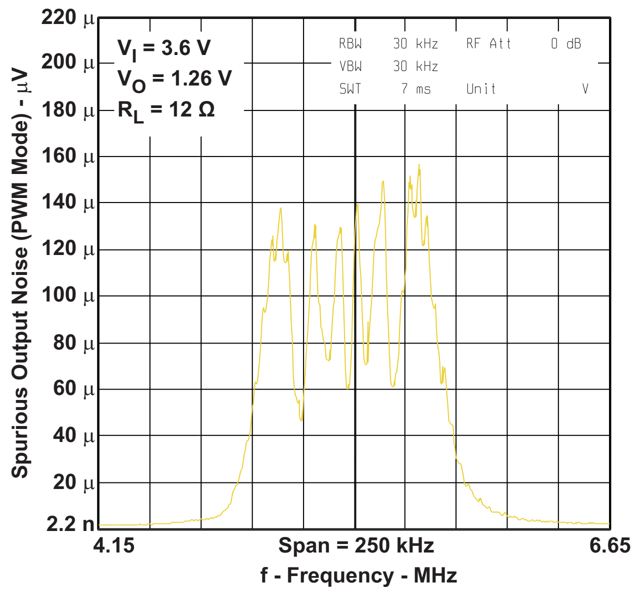


Figure 36.

TYPICAL CHARACTERISTICS (continued)

SPURIOUS OUTPUT NOISE (PFM MODE)
vs
FREQUENCY

Figure 37.

SPURIOUS OUTPUT NOISE (PWM MODE)
vs
FREQUENCY

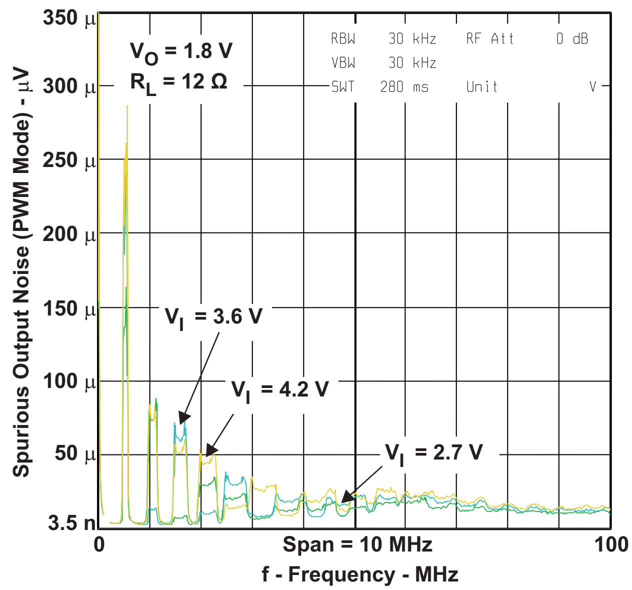


Figure 38.

DETAILED DESCRIPTION

OPERATION

The TPS6267x is a synchronous step-down converter typically operates at a regulated 6-MHz frequency pulse width modulation (PWM) at moderate to heavy load currents. At light load currents, the TPS6267x converter operates in power-save mode with pulse frequency modulation (PFM).

The converter uses a unique frequency locked ring oscillating modulator to achieve *best-in-class* load and line response and allows the use of tiny inductors and small ceramic input and output capacitors. At the beginning of each switching cycle, the P-channel MOSFET switch is turned on and the inductor current ramps up rising the output voltage until the main comparator trips, then the control logic turns off the switch.

One key advantage of the non-linear architecture is that there is no traditional feed-back loop. The loop response to change in V_O is essentially instantaneous, which explains the transient response. The absence of a traditional, high-gain compensated linear loop means that the TPS6267x is inherently stable over a range of L and C_O.

Although this type of operation normally results in a switching frequency that varies with input voltage and load current, an internal frequency lock loop (FLL) holds the switching frequency constant over a large range of operating conditions.

Combined with *best in class* load and line transient response characteristics, the low quiescent current of the device (ca. 17μA) allows to maintain high efficiency at light load, while preserving fast transient response for applications requiring tight output regulation.

Using the YFD package allows for a low profile solution size (0.4mm max height, including external components). The recommended external components are stated within the application information. The maximum output current is 500mA when these specific low profile external components are used.

SWITCHING FREQUENCY

The magnitude of the internal ramp, which is generated from the duty cycle, reduces for duty cycles either set of 50%. Thus, there is less overdrive on the main comparator inputs which tends to slow the conversion down. The intrinsic maximum operating frequency of the converter is about 10MHz to 12MHz, which is controlled to circa. 6MHz by a frequency locked loop.

When high or low duty cycles are encountered, the loop runs out of range and the conversion frequency falls below 6MHz. The tendency is for the converter to operate more towards a "constant inductor peak current" rather than a "constant frequency". In addition to this behavior which is observed at high duty cycles, it is also noted at low duty cycles.

When the converter is required to operate towards the 6MHz nominal at extreme duty cycles, the application can be assisted by decreasing the ratio of inductance (L) to the output capacitor's equivalent serial inductance (ESL). This increases the *ESL step* seen at the main comparator's feed-back input thus decreasing its propagation delay, hence increasing the switching frequency.

POWER-SAVE MODE

If the load current decreases, the converter will enter Power Save Mode operation automatically (does not apply for TPS62674). During power-save mode the converter operates in discontinuous current (DCM) single-pulse PFM mode, which produces low output ripple compared with other PFM architectures.

When in power-save mode, the converter resumes its operation when the output voltage trips below the nominal voltage. It ramps up the output voltage with a minimum of one pulse and goes into power-save mode when the inductor current has returned to a zero steady state. The PFM on-time varies inversely proportional to the input voltage and proportional to the output voltage giving the regulated switching frequency when in steady-state.

PFM mode is left and PWM operation is entered as the output current can no longer be supported in PFM mode. As a consequence, the DC output voltage is typically positioned ca. 0.5% above the nominal output voltage and the transition between PFM and PWM is seamless.

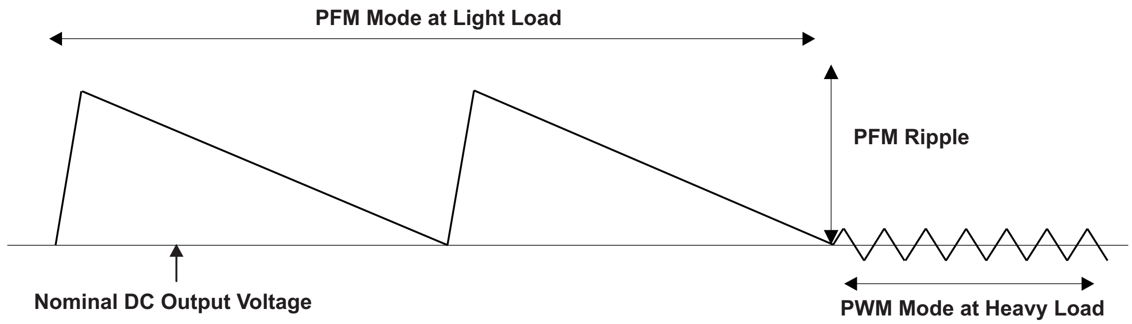


Figure 39. Operation in PFM Mode and Transfer to PWM Mode

MODE SELECTION

The MODE pin allows to select the operating mode of the device. Connecting this pin to GND enables the automatic PWM and power-save mode operation. The converter operates in regulated frequency PWM mode at moderate to heavy loads and in the PFM mode during light loads, which maintains high efficiency over a wide load current range.

Pulling the MODE pin high forces the converter to operate in the PWM mode even at light load currents. The advantage is that the converter modulates its switching frequency according to a spread spectrum PWM modulation technique allowing simple filtering of the switching harmonics in noise-sensitive applications. In this mode, the efficiency is lower compared to the power-save mode during light loads. Notice that the TPS62674 device only permits PWM operation and required the MODE input to be tied high.

For additional flexibility, it is possible to switch from power-save mode to PWM mode during operation. This allows efficient power management by adjusting the operation of the converter to the specific system requirements.

SPREAD SPECTRUM, PWM FREQUENCY DITHERING

The goal is to spread out the emitted RF energy over a larger frequency range so that the resulting EMI is similar to white noise. The end result is a spectrum that is continuous and lower in peak amplitude, making it easier to comply with electromagnetic interference (EMI) standards and with the power supply ripple requirements in cellular and non-cellular wireless applications. Radio receivers are typically susceptible to narrowband noise that is focused on specific frequencies.

Switching regulators can be particularly troublesome in applications where electromagnetic interference (EMI) is a concern. Switching regulators operate on a cycle-by-cycle basis to transfer power to an output. In most cases, the frequency of operation is either fixed or regulated, based on the output load. This method of conversion creates large components of noise at the frequency of operation (fundamental) and multiples of the operating frequency (harmonics).

The spread spectrum architecture varies the switching frequency by ca. ±10% of the nominal switching frequency thereby significantly reducing the peak radiated and conducting noise on both the input and output supplies. The frequency dithering scheme is modulated with a triangle profile and a modulation frequency f_m.

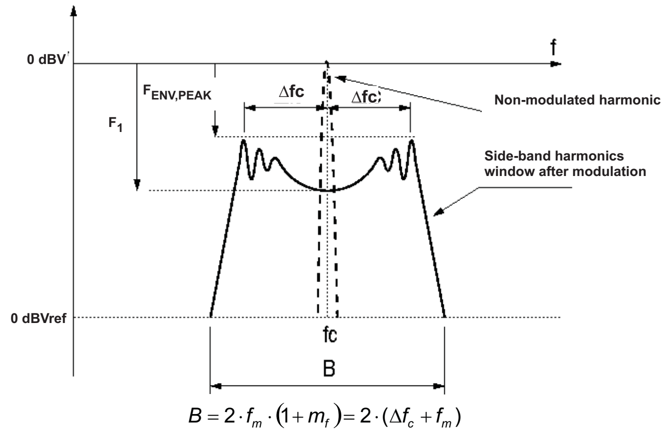


Figure 40. Spectrum of a Frequency Modulated Sin. Wave with Sinusoidal Variation in Time

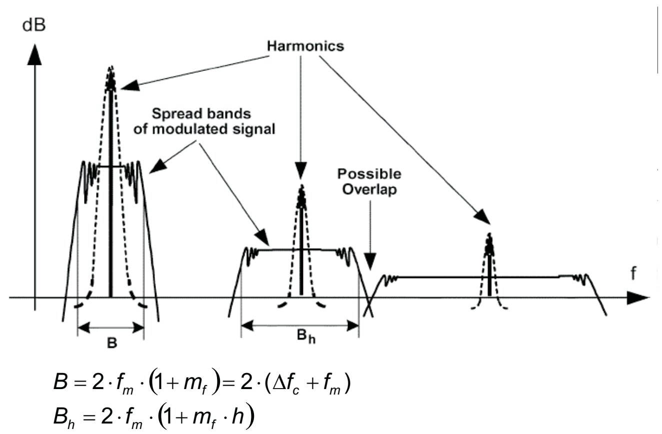


Figure 41. Spread Bands of Harmonics in Modulated Square Signals

The above figures show that after modulation the sideband harmonic is attenuated compared to the non-modulated harmonic, and the harmonic energy is spread into a certain frequency band. The higher the modulation index (*mf*) the larger the attenuation.

$$m_f = \frac{\delta \times f_c}{f_m} \tag{1}$$

With:

f_c is the carrier frequency

f_m is the modulating frequency (approx. 0.008*f_c)

δ is the modulation ratio (approx 0.1)

$$\delta = \frac{\Delta f_c}{f_c} \tag{2}$$

The maximum switching frequency f_c is limited by the process and finally the parameter modulation ratio (δ), together with f_m , which is the side-band harmonics bandwidth around the carrier frequency f_c . The bandwidth of a frequency modulated waveform is approximately given by the Carson's rule and can be summarized as:

$$B = 2 \times f_m \times \left(1 + m_f\right) = 2 \times \left(\Delta f_c + f_m\right) \tag{3}$$

f_m < RBW: The receiver is not able to distinguish individual side-band harmonics, so, several harmonics are added in the input filter and the measured value is higher than expected in theoretical calculations.

f_m > RBW: The receiver is able to properly measure each individual side-band harmonic separately, so the measurements match with the theoretical calculations.

ENABLE

The TPS6267x device starts operation when EN is set high and starts up with the soft start as previously described. For proper operation, the EN pin must be terminated and must not be left floating.

Pulling the EN pin low forces the device into shutdown, with a shutdown quiescent current of typically 0.1µA. In this mode, the P and N-channel MOSFETs are turned off, the internal resistor feedback divider is disconnected, and the entire internal-control circuitry is switched off. The TPS6267x device can actively discharge the output capacitor when it turns off. The integrated discharge resistor has a typical resistance of 100 Ω. The required time to discharge the output capacitor at the output node depends on load current and the output capacitance value.

When an external clock signal (EXTCLK), 4MHz to 27MHz is applied to the TPS62674, the DC/DC converter powers-up automatically within approx. 120µs. When the external clock signal is stopped, the DC/DC converter is powered down and the output capacitor is discharged actively.

SOFT START

The TPS6267x has an internal soft-start circuit that limits the inrush current during start-up. This limits input voltage drops when a battery or a high-impedance power source is connected to the input of the converter.

The soft-start system progressively increases the on-time from a minimum pulse-width of 35ns as a function of the output voltage. This mode of operation continues for c.a. 100μs after enable. Should the output voltage not have reached its target value by this time, such as in the case of heavy load, the soft-start transitions to a second mode of operation.

The converter then operates in a current limit mode, specifically the P-MOS current limit is set to half the nominal limit, and the N-channel MOSFET remains on until the inductor current has reset. After a further 100 μs, the device ramps up to the full current limit operation if the output voltage has risen above 0.5V (approximately). Therefore, the start-up time mainly depends on the output capacitor and load current.

UNDERVOLTAGE LOCKOUT

The undervoltage lockout circuit prevents the device from misoperation at low input voltages. It prevents the converter from turning on the switch or rectifier MOSFET under undefined conditions. The TPS6267x device have a UVLO threshold set to 2.05V (typical). Fully functional operation is permitted down to 2.1V input voltage.

SHORT-CIRCUIT PROTECTION

The TPS6267x integrates a P-channel MOSFET current limit to protect the device against heavy load or short circuits. When the current in the P-channel MOSFET reaches its current limit, the P-channel MOSFET is turned off and the N-channel MOSFET is turned on. The regulator continues to limit the current on a cycle-by-cycle basis.

As soon as the output voltage falls below ca. 0.4V, the converter current limit is reduced to half of the nominal value. Because the short-circuit protection is enabled during start-up, the device does not deliver more than half of its nominal current limit until the output voltage exceeds approximately 0.5V. This needs to be considered when a load acting as a current sink is connected to the output of the converter.

THERMAL SHUTDOWN

As soon as the junction temperature, T_J, exceeds typically 140°C, the device goes into thermal shutdown. In this mode, the P- and N-channel MOSFETs are turned off. The device continues its operation when the junction temperature again falls below typically 130°C.

APPLICATION INFORMATION

INDUCTOR SELECTION

The TPS6267x series of step-down converters have been optimized to operate with an effective inductance value in the range of 0.3µH to 1.8µH and with output capacitors in the range of 2.2µF to 4.7µF. The internal compensation is optimized to operate with an output filter of L = 0.47µH and C_O = 2.2µF. Larger or smaller inductor values can be used to optimize the performance of the device for specific operation conditions. For more details, see the *CHECKING LOOP STABILITY* section.

The inductor value affects its peak-to-peak ripple current, the PWM-to-PFM transition point, the output voltage ripple and the efficiency. The selected inductor has to be rated for its dc resistance and saturation current. The inductor ripple current (ΔI_L) decreases with higher inductance and increases with higher V_I or V_O.

$$\Delta I_L = \frac{V_O}{V_I} \times \frac{V_I - V_O}{L \times f_{SW}} \qquad \Delta I_{L(MAX)} = I_{O(MAX)} + \frac{\Delta I_L}{2}$$

with: f_{SW} = switching frequency (6 MHz typical)

L = inductor value

ΔI_L = peak-to-peak inductor ripple current

$I_{L(MAX)}$ = maximum inductor current (4)

In high-frequency converter applications, the efficiency is essentially affected by the inductor AC resistance (i.e. quality factor) and to a smaller extent by the inductor DCR value. To achieve high efficiency operation, care should be taken in selecting inductors featuring a quality factor above 25 at the switching frequency. Increasing the inductor value produces lower RMS currents, but degrades transient response. For a given physical inductor size, increased inductance usually results in an inductor with lower saturation current.

The total losses of the coil consist of both the losses in the DC resistance $_{(DC)}$) and the following frequency-dependent components:

- The losses in the core material (magnetic hysteresis loss, especially at high switching frequencies)
- Additional losses in the conductor from the skin effect (current displacement at high frequencies)
- Magnetic field losses of the neighboring windings (proximity effect)
- Radiation losses

The following inductor series from different suppliers have been used with the TPS6267x converters.

Table 1. List of Inductors

MANUFACTURER	SERIES	DIMENSIONS (in mm)
MURATA	LQM21PN1R0NGR	2.0 x 1.2 x 1.0 max. height
	LQM21PNR47MC0	2.0 x 1.2 x 0.55 max. height
	LQM21PN1R0MC0	2.0 x 1.2 x 0.55 max. height
	LQM18PN1R5-B35	1.6 x 0.8 x 0.4 max. height
	LQM18PN1R5-A62	1.6 x 0.8 x 0.33 max. height
PANASONIC	ELGTEAR82NA	2.0 x 1.2 x 1.0 max. height
SEMCO	CIG21L1R0MNE	2.0 x 1.2 x 1.0 max. height
TAIYO YUDEN	BRC1608T1R0	1.6 x 0.8 x 0.9 max. height
	BRC1608T1R5	1.6 x 0.8 x 0.9 max. height
	CKP1608L1R5M	1.6 x 0.8 x 0.55 max. height
	CKP1608U1R5M	1.6 x 0.8 x 0.4 max. height
TDK	MLP2012SR82T	2.0 x 1.2 x 0.6 max. height
TOKO	MDT2012-CR1R0A	2.0 x 1.2 x 1.0 max. height

OUTPUT CAPACITOR SELECTION

The advanced fast-response voltage mode control scheme of the TPS6267x allows the use of tiny ceramic capacitors. Ceramic capacitors with low ESR values have the lowest output voltage ripple and are recommended. For best performance, the device should be operated with a minimum effective output capacitance of 0.8μF. The output capacitor requires either an X7R or X5R dielectric. Y5V and Z5U dielectric capacitors, aside from their wide variation in capacitance over temperature, become resistive at high frequencies.

At nominal load current, the device operates in PWM mode and the overall output voltage ripple is the sum of the voltage step caused by the output capacitor ESL and the ripple current flowing through the output capacitor impedance.

At light loads, the output capacitor limits the output ripple voltage and provides holdup during large load transitions. A 2.2μF capacitor typically provides sufficient bulk capacitance to stabilize the output during large load transitions. The typical output voltage ripple is 1% of the nominal output voltage V_O.

The output voltage ripple during PFM mode operation can be kept very small. The PFM pulse is time controlled, which allows to modify the charge transferred to the output capacitor by the value of the inductor. The resulting PFM output voltage ripple and PFM frequency depend in first order on the size of the output capacitor and the inductor value. The PFM frequency decreases with smaller inductor values and increases with larger once. Increasing the output capacitor value and the effective inductance will minimize the output ripple voltage.

INPUT CAPACITOR SELECTION

Because of the nature of the buck converter having a pulsating input current, a low ESR input capacitor is required to prevent large voltage transients that can cause misbehavior of the device or interferences with other circuits in the system. For most applications, a 1 or 2.2-μF capacitor is sufficient. If the application exhibits a noisy or erratic switching frequency, the remedy will probably be found by experimenting with the value of the input capacitor.

Take care when using only ceramic input capacitors. When a ceramic capacitor is used at the input and the power is being supplied through long wires, such as from a wall adapter, a load step at the output can induce ringing at the VIN pin. This ringing can couple to the output and be mistaken as loop instability or could even damage the part. Additional "bulk" capacitance (electrolytic or tantalum) should in this circumstance be placed between C_I and the power source lead to reduce ringing than can occur between the inductance of the power source leads and C_I.

CHECKING LOOP STABILITY

The first step of circuit and stability evaluation is to look from a steady-state perspective at the following signals:

- Switching node, SW
- Inductor current, I_L
- Output ripple voltage, $V_{O(AC)}$

These are the basic signals that need to be measured when evaluating a switching converter. When the switching waveform shows large duty cycle jitter or the output voltage or inductor current shows oscillations, the regulation loop may be unstable. This is often a result of board layout and/or L-C combination.

As a next step in the evaluation of the regulation loop, the load transient response is tested. The time between the application of the load transient and the turn on of the P-channel MOSFET, the output capacitor must supply all of the current required by the load. V_O immediately shifts by an amount equal to $\Delta I_{(LOAD)}$ x ESR, where ESR is the effective series resistance of C_O. $\Delta I_{(LOAD)}$ begins to charge or discharge C_O generating a feedback error signal used by the regulator to return V_O to its steady-state value. The results are most easily interpreted when the device operates in PWM mode.

During this recovery time, V_O can be monitored for settling time, overshoot or ringing that helps judge the converter's stability. Without any ringing, the loop has usually more than 45° of phase margin.

Because the damping factor of the circuitry is directly related to several resistive parameters (e.g., MOSFET $r_{DS(on)}$) that are temperature dependant, the loop stability analysis has to be done over the input voltage range, load current range, and temperature range.

LAYOUT CONSIDERATIONS

As for all switching power supplies, the layout is an important step in the design. High-speed operation of the TPS6267x devices demand careful attention to PCB layout. Care must be taken in board layout to get the specified performance. If the layout is not carefully done, the regulator could show poor line and/or load regulation, stability and switching frequency issues as well as EMI problems. It is critical to provide a low inductance, impedance ground path. Therefore, use wide and short traces for the main current paths.

The input capacitor should be placed as close as possible to the IC pins as well as the inductor and output capacitor. In order to get an optimum *ESL step*, the output voltage feedback point (FB) should be taken in the output capacitor path, approximately 1mm away for it. The feed-back line should be routed away from noisy components and traces (e.g. SW line).

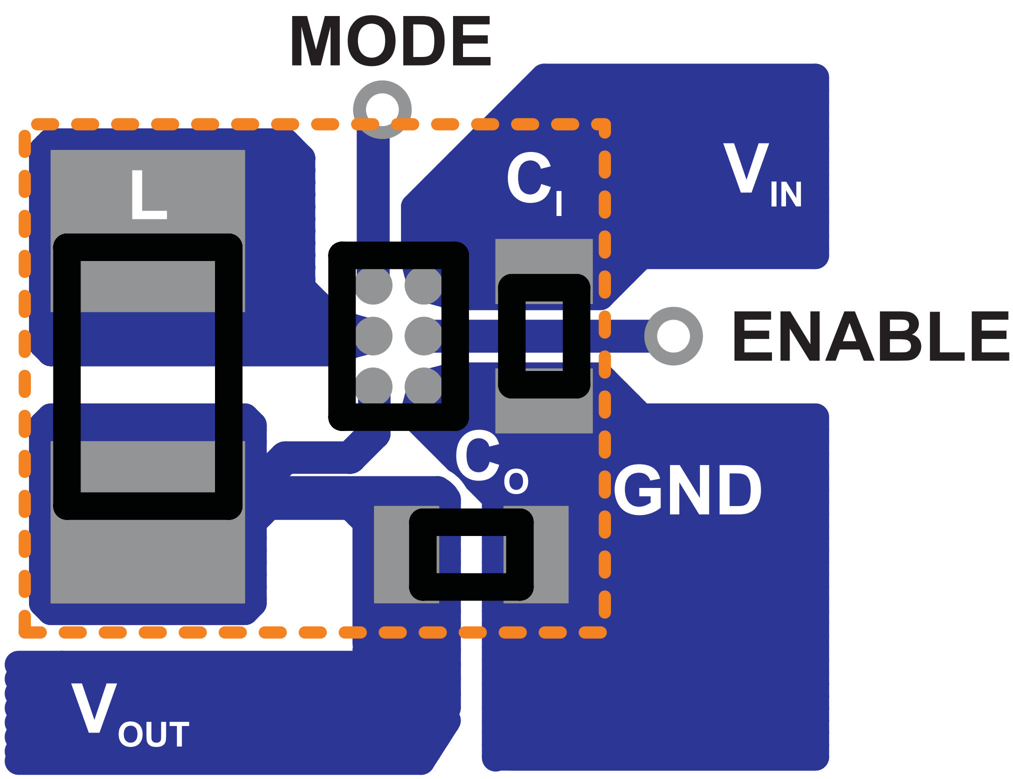


Figure 42. Suggested Layout (Top)

THERMAL INFORMATION

Implementation of integrated circuits in low-profile and fine-pitch surface-mount packages typically requires special attention to power dissipation. Many system-dependant issues such as thermal coupling, airflow, added heat sinks, and convection surfaces, and the presence of other heat-generating components, affect the power-dissipation limits of a given component.

Three basic approaches for enhancing thermal performance are listed below:

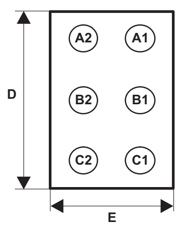
- Improving the power dissipation capability of the PCB design
- Improving the thermal coupling of the component to the PCB
- Introducing airflow into the system

The maximum recommended junction temperature (T_J) of the TPS6267x devices is 105°C. The thermal resistance of the 6-pin CSP package (YFD-6) is $R_{\theta JA}$ = 125°C/W. Regulator operation is specified to a maximum steady-state ambient temperature T_A of 85°C. Therefore, the maximum power dissipation is about 160 mW.

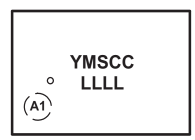
$$P_{D(MAX)} = \frac{T_{J(MAX)} - T_A}{R_{\theta JA}} = \frac{105°C - 85°C}{125°C/W} = 160mW \tag{5}$$

PACKAGE SUMMARY

CHIP SCALE PACKAGE
(BOTTOM VIEW)



CHIP SCALE PACKAGE
(TOP VIEW)



Code:

- YM — Year Month date Code
- S — Assembly site code
- CC— Chip code
- LLLL — Lot trace code

CHIP SCALE PACKAGE DIMENSIONS

The TPS6267x device is available in an 6-bump chip scale package (YFD, NanoFree™). The package dimensions are given as:

- D = 1.30 ±0.03 mm
- E = 0.926 ±0.03 mm

APPLICATION INFORMATION

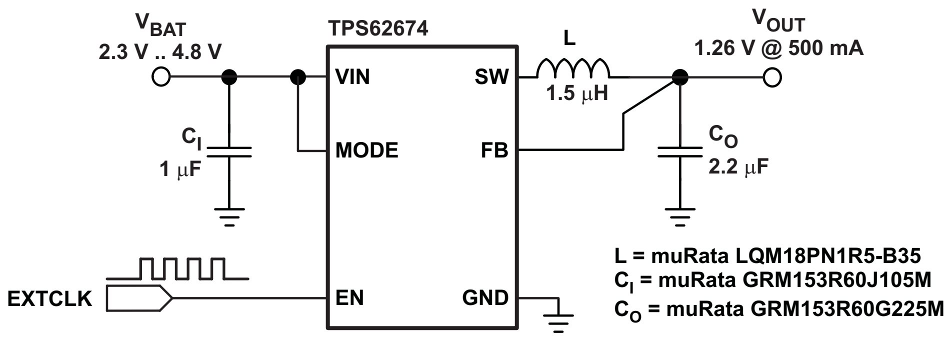


Figure 43. 1.26V CMOS Sensor Embedded Power Solution — Featuring Sub 0.4mm Profile

PACKAGING INFORMATION

Orderable Device	Status [1]	Package Type	Package Drawing	Pins	Package Qty	Eco Plan [2]	Lead/Ball Finish	MSL Peak Temp [3]
TPS62674YFDR	ACTIVE	DSBGA	YFD	6	3000	TBD	Call TI	Call TI
TPS62674YFDT	ACTIVE	DSBGA	YFD	6	250	TBD	Call TI	Call TI

[1] The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

[2] Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

[3] MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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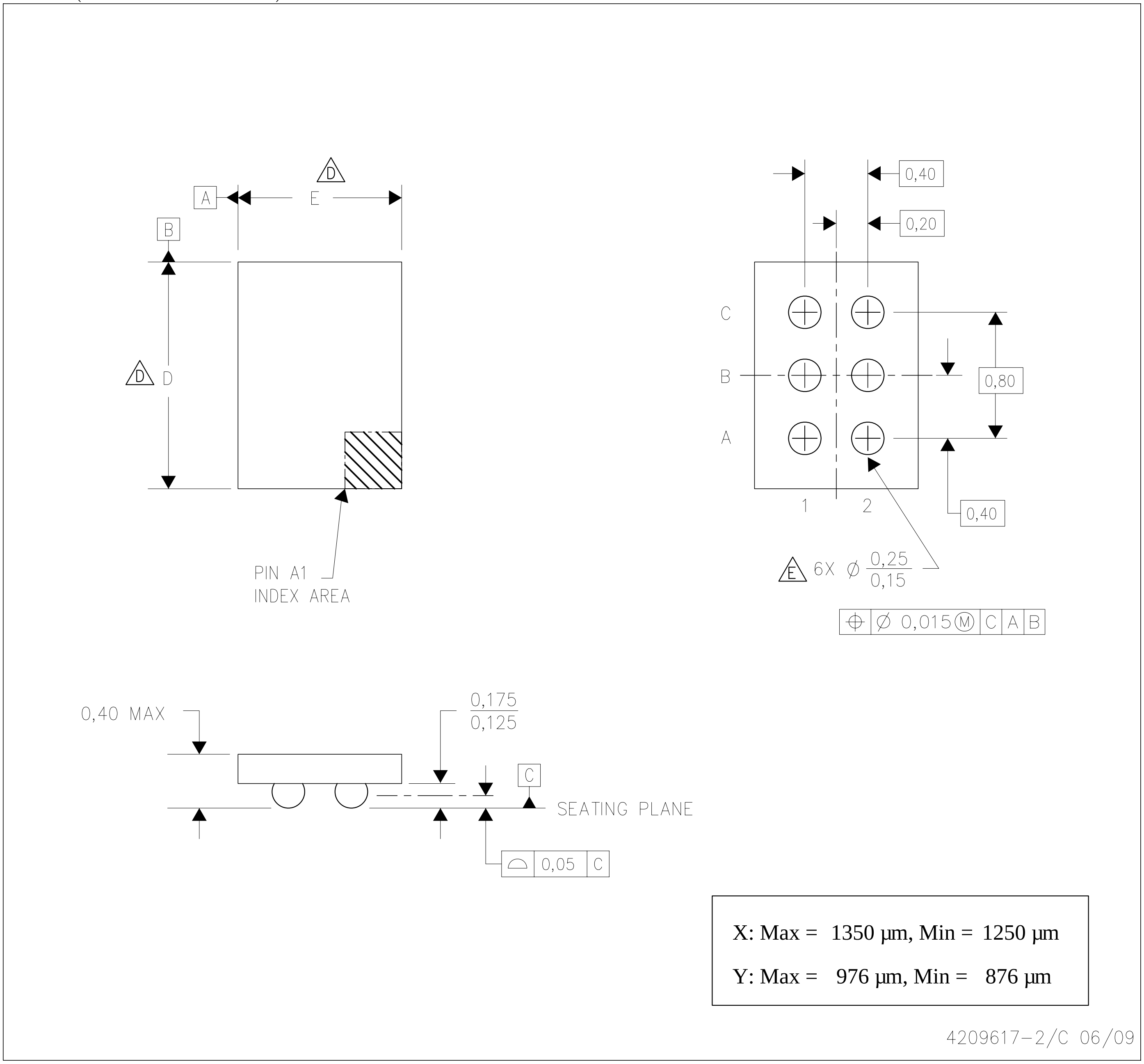
YFD (R-XBGA-N6) DIE-SIZE BALL GRID ARRAY



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. NanoFree™ package configuration.
D. Devices in YFD package can have dimensions D ranging from 1.16 to 1.85 mm and dimension E ranging from 0.76 to 1.45 mm. To determine the exact package size of a particular device, refer to the device datasheet or contact a local TI representative.
E. Reference Product Data Sheet for array population.
2 x 3 matrix pattern is shown for illustration only.
F. This package contains Pb–free balls.

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