POWER MANAGEMENT IC FOR LI-ION POWERED SYSTEMS

Check for Samples: TPS650231

FEATURES

- **1.7 A, 90% Efficient Step-Down Converter for Processor Core (VDCDC1)**
- **1.2 A, Up to 95% Efficient Step-Down Converter for System Voltage (VDCDC2)**
- **0.8 A, 92% Efficient Step-Down Converter for Memory Voltage (VDCDC3)**
- **30 mA LDO/Switch for Real Time Clock (VRTC)**
- **2 × 200 mA General-Purpose LDO**
- **Dynamic Voltage Management for Processor Core**
- **Preselectable LDO Voltage Using Two Digital Input Pins**
- **Externally Adjustable Reset Delay Time**
- **Battery Backup Functionality**
- **Separate Enable Pins for Inductive Converters**
- **I^2C™ Compatible Serial Interface**
- **85-µA Quiescent Current**
- **Low Ripple PFM Mode**
- **Thermal Shutdown Protection**
- **40 Pin, 5 mm × 5 mm QFN /RSB) Package or**
- **49 Ball 3 mm x 3 mm WCSP (YFF) package**

APPLICATIONS

- **Smart phones**
- **Netbooks / MIDs**
- **Portable Media Players**

DESCRIPTION

The TPS650231 is an integrated Power Management IC for applications powered by one Li-Ion or Li-Polymer cell, and which require multiple power rails. The TPS650231 provides three highly efficient, step-down converters targeted at providing the core voltage, peripheral, I/O and memory rails in a processor based system. The core converter allows for on-the-fly voltage changes via serial interface, allowing the system to implement dynamic power savings. All three step-down converters enter a low-power mode at light load for maximum efficiency across the widest possible range of load currents. The TPS650231 also integrates two general-purpose 200 mA LDO voltage regulators, which are enabled with an external input pin. Each LDO operates with an input voltage range between 1.5 V and 6.5 V, allowing them to be supplied from one of the step-down converters or directly from the battery. The default output voltage of the LDOs can be digitally set to 4 different voltage combinations using the DEFLDO1 and DEFLDO2 pins. The serial interface can be used for dynamic voltage scaling, masking interrupts, or for dis/enabling and setting the LDO output voltages. The interface is compatible with the Fast/Standard mode I^2C specification, allowing transfers at up to 400 kHz. The TPS650231 is available in a 40-pin (RSB) QFN package or in a 49 ball 3mm x 3mm WCSP (YFF) package, and operates over a free-air temperature of –40°C to 85°C.

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

ORDERING INFORMATION[1]

T_A	PACKAGE	PACKAGE SIZE	PART NUMBER[2]
–40°C to 85°C	40 pin QFN (RSB)	see package drawings	TPS650231RSB
–40°C to 85°C	49 ball WCSP (YFF)	see package drawings E = 3.082mm ± 30µm D = 3.066mm ± 30µm	TPS650231YFF

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI Web site at www.ti.com.

(2) The RSB and YFF packages are available in tape and reel. Add the R suffix (TPS650231RSBR, TPS650231YFFR) to order quantities of 3000 parts per reel. Add the T suffix (TPS650231RSBT, TPS650231YFFT) to order quantities of 250 parts per reel.

ABSOLUTE MAXIMUM RATINGS[1]

over operating free-air temperature range (unless otherwise noted)

		VALUE		UNIT
		MIN	MAX	
V_I	Input voltage range on all pins except AGND and PGND pins with respect to AGND	–0.3	7	V
	Current at VINDCDC1, L1, PGND1, VINDCDC2, L2, PGND2, VINDCDC3, L3, PGND3		2500	mA
	Peak current at all other pins		1000	mA
T_A	Operating free-air temperature	–40	85	°C
T_J	Junction temperature		125	°C
T_{stg}	Storage temperature	–65	150	°C

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability

THERMAL INFORMATION

THERMAL METRIC[1]		TPS650231		UNITS
		RSB	YFF	
		40 PINS	49 BALLS	
θ_{JA}	Junction-to-ambient thermal resistance	32.7	40	°C/W
θ_{JCtop}	Junction-to-case (top) thermal resistance	15.3	10	
θ_{JB}	Junction-to-board thermal resistance	13.6	15	
ψ_{JT}	Junction-to-top characterization parameter	0.1	0.1	
ψ_{JB}	Junction-to-board characterization parameter	5.4	14	
θ_{JCbot}	Junction-to-case (bottom) thermal resistance	1.1	n/a	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

RECOMMENDED OPERATING CONDITIONS

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{CC}	Input voltage range step-down converters (VINDCDC1, VINDCDC2, VINDCDC3)	2.5		6	V
V_O	Output voltage range for VDCDC1 step-down converter (1)	0.6		VINDCDC1	V
	Output voltage range for VDCDC2 step-down converter (1)	0.6		VINDCDC2	
	Output voltage range for VDCDC3 step-down converter (1)	0.6		VINDCDC3	
V_I	Input voltage range for LDOs (VINLDO)	1.5		6.5	V
V_O	Output voltage range for LDOs (VLDO1, VLDO2)	1		VINLDO1-2	V
$I_{O(DCDC1)}$	Output current at L1			1700	mA
	Inductor at L1 (2)	1.5	2.2		μH
$C_{I(DCDC1)}$	Input capacitor at VINDCDC1 (2)	10			μF
$C_{O(DCDC1)}$	Output capacitor at VDCDC1 (2)	10	22		μF
$I_{O(DCDC2)}$	Output current at L2			1200	mA
	Inductor at L2 (2)	1.5	2.2		μH
$C_{I(DCDC2)}$	Input capacitor at VINDCDC2 (2)	10			μF
$C_{O(DCDC2)}$	Output capacitor at VDCDC2 (2)	10	22		μF
$I_{O(DCDC3)}$	Output current at L3			800	mA
	Inductor at L3 (2)	1.5	2.2		μH
$C_{I(DCDC3)}$	Input capacitor at VINDCDC3 (2)	10			μF
$C_{O(DCDC3)}$	Output capacitor at VDCDC3 (2)	10	22		μF
$C_{I(VCC)}$	Input capacitor at VCC (2)	1			μF
$C_{I(VINLDO)}$	Input capacitor at VINLDO (2)	1			μF
$C_{O(VLDO1-2)}$	Output capacitor at VLDO1, VLDO2 (2)	2.2			μF
$I_{O(VLDO1-2)}$	Output current at VLDO1, VLDO2			200	mA
$C_{O(VRTC)}$	Output capacitor at VRTC (2)	4.7			μF
T_A	Operating ambient temperature	–40		85	°C
T_J	Operating junction temperature	–40		125	°C
	Resistor from VINDCDC3, VINDCDC2, VINDCDC1 to VCC used for filtering (3)		1	10	Ω

(1) When using an external resistor divider at DEFDCDC3, DEFDCDC2, DEFDCDC1
(2) See *Applications Information* section for more information.
(3) Up to 3 mA can flow into V_{CC} when all 3 converters are running in PWM. This resistor causes the UVLO threshold to be shifted accordingly.

ELECTRICAL CHARACTERISTICS

VINDCDC1 = VINDCDC2 = VINDCDC3 = VCC = VINLDO = 3.6 V, VBACKUP = 3 V, T_A = –40°C to 85°C, typical values are at T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
CONTROL SIGNALS : SCLK, SDAT (input)						
V_{IH}	High level input voltage for the SCLK pin	Rpullup at SCLK = 4.7 kΩ, pulled to VRTC; For V_{CC} = 2.5V to 5.25V	1.4		V_{CC}	V
V_{IH}	High level input voltage for the SDAT pin	Rpullup at SDAT = 4.7 kΩ, pulled to VRTC; For V_{CC} = 2.5V to 5.25V	1.69		V_{CC}	V
V_{IH}	High level input voltage for the SDAT pin	Rpullup at SDAT = 4.7 kΩ, pulled to VRTC; For V_{CC} = 2.5V to 4.5V	1.55		V_{CC}	V
V_{IL}	Low level input voltage	Rpullup at SCLK and SDAT = 4.7 kΩ, pulled to VRTC	0		0.35	V
I_H	Input bias current			0.01	0.1	µA
CONTROL SIGNALS : HOT_RESET , DCDC1_EN, DCDC2_EN, DCDC3_EN, LDO_EN, DEFLDO1, DEFLDO2						
V_{IH}	High-level input voltage		1.3		V_{CC}	V
V_{IL}	Low-level input voltage		0		0.4	V
I_{IB}	Input bias current			0.01	0.1	µA
t_{glitch}	Deglitch time at HOT_RESET		25	30	35	ms
CONTROL SIGNALS : LOWBAT, PWRFAIL, RESPWRON, INT, SDAT (output)						
V_{OH}	High-level output voltage				6	V
V_{OL}	Low-level output voltage	I_{IL} = 5 mA	0		0.3	V
	Duration of low pulse at RESPWRON	External capacitor 1 nF		100		ms
	Resetpwron threshold	VRTC falling	–3%	2.4	3%	V
	Resetpwron threshold	VRTC rising	–3%	2.52	3%	V
I_{LK}	leakage current	output inactive high		0.001	0.1	µA

ELECTRICAL CHARACTERISTICS

VINDCDC1 = VINDCDC2 = VINDCDC3 = VCC = VINLDO = 3.6 V, VBACKUP = 3 V, T_A = –40°C to 85°C, typical values are at T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
SUPPLY PINS: VCC, VINDCDC1, VINDCDC2, VINDCDC3, VINDCDC13 (for TPS650231YFF)							
$I_{(q)}$	Operating quiescent current, PFM	All 3 DCDC converters enabled, zero load, and no switching, LDOs enabled	VCC = 3.6 V, VBACKUP = 3 V; $V_{(VSYSIN)}$ = 0 V		85	100	μA
		All 3 DCDC converters enabled, zero load, and no switching, LDOs off	VCC = 3.6 V, VBACKUP = 3 V; $V_{(VSYSIN)}$ = 0 V		78	90	
		DCDC1 and DCDC2 converters enabled, zero load, and no switching, LDOs off	VCC = 3.6 V, VBACKUP = 3 V; $V_{(VSYSIN)}$ = 0 V		57	70	
		DCDC1 converter enabled, zero load, and no switching, LDOs off	VCC = 3.6 V, VBACKUP = 3 V; $V_{(VSYSIN)}$ = 0 V		43	55	
I_I	Current into VCC; PWM	All 3 DCDC converters enabled and running in PWM, LDOs off	VCC = 3.6 V, VBACKUP = 3 V; $V_{(VSYSIN)}$ = 0 V		2	3	mA
		DCDC1 and DCDC2 converters enabled and running in PWM, LDOs off	VCC = 3.6 V, VBACKUP = 3 V; $V_{(VSYSIN)}$ = 0 V		1.5	2.5	
		DCDC1 converter enabled and running in PWM, LDOs off	VCC = 3.6 V, VBACKUP = 3 V; $V_{(VSYSIN)}$ = 0 V		0.85	2	
$I_{(q)}$	Quiescent current	All converters disabled, LDOs off	VCC = 3.6 V, VBACKUP = 3 V; $V_{(VSYSIN)}$ = 0 V		23	33	μA
			VCC = 2.6 V, VBACKUP = 3 V; $V_{(VSYSIN)}$ = 0 V		3.5	5	μA
			VCC = 3.6 V, VBACKUP = 0 V; $V_{(VSYSIN)}$ = 0 V			43	μA
$I_{(SD)}$	Shutdown supply current into VINDCDC1; for TPS650231RSB		DCDC1_EN = GND		0.1	1	μA
	Shutdown supply current into VINDCDC2; for TPS650231RSB		DCDC2_EN = GND		0.1	1	μA
	Shutdown supply current into VINDCDC3; for TPS650231RSB		DCDC3_EN = GND		0.1	1	μA
	Shutdown supply current into VINDCDC13; for TPS650231YFF		DCDC1_EN = DCDC3_EN = GND		0.2	2	μA

ELECTRICAL CHARACTERISTICS

VINDCDC1 = VINDCDC2 = VINDCDC3 (VINDCDC13) = VCC = VINLDO = 3.6 V, VBACKUP = 3 V, T_A = –40°C to 85°C, typical values are at T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY PINS: VBACKUP, VSYSIN, VRTC						
$I_{(q)}$	Operating quiescent current	VBACKUP = 3 V, VSYSIN = 0 V; VCC = 2.6 V, current into VBACKUP		20	33	µA
$I_{(SD)}$	Operating quiescent current	VBACKUP < V_VBACKUP, current into VBACKUP		2	3	µA
	VRTC LDO output voltage	VSYSIN = VBACKUP = 0 V, I_O = 0 mA		3		V
I_O	Output current for VRTC	VSYSIN < 2.57 V and VBACKUP < 2.57 V			30	mA
	VRTC short-circuit current limit	VRTC = GND; VSYSIN = VBACKUP = 0 V			100	mA
	Maximum output current at VRTC for $\overline{\text{RESPWRON}}$ = 1	VRTC > 2.6 V, V_{CC} = 3 V; VSYSIN = VBACKUP = 0 V	30			mA
V_O	Output voltage accuracy for VRTC	VSYSIN = VBACKUP = 0 V; I_O = 0 mA	–1%		1%	
	Line regulation for VRTC	VCC = VRTC + 0.5 V to 6.5 V, I_O = 5 mA	–1%		1%	
	Load regulation VRTC	I_O = 1 mA to 30 mA; VSYSIN = VBACKUP = 0 V	–3%		1%	
	Regulation time for VRTC	Load change from 10% to 90%		10		µs
I_{lkg}	Input leakage current at VSYSIN	VSYSIN < V_VSYSIN			2	µA
	$r_{DS(on)}$ of VSYSIN switch				12.5	Ω
	$r_{DS(on)}$ of VBACKUP switch				12.5	Ω
	Input voltage range at VBACKUP		2.73		3.75	V
	Input voltage range at VSYSIN		2.73		3.75	V
	VSYSIN threshold	VSYSIN falling	–3%	2.55	3%	V
	VSYSIN threshold	VSYSIN rising	–3%	2.65	3%	V
	VBACKUP threshold	VBACKUP falling	–3%	2.55	3%	V
	VBACKUP threshold	VBACKUP falling	–3%	2.65	3%	V
SUPPLY PIN: VINLDO						
$I_{(q)}$	Operating quiescent current	Current per LDO into VINLDO		20	33	µA
$I_{(SD)}$	Shutdown current	Total current for both LDOs into VINLDO, VLDO = 0 V		0.1	1	µA

ELECTRICAL CHARACTERISTICS

VINDCDC1 = VINDCDC2 = VINDCDC3 = VCC = VINLDO = 3.6 V, VBACKUP = 3 V, T_A = –40°C to 85°C, typical values are at T_A = 25°C (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
VDCDC1 STEP-DOWN CONVERTER							
V_I	Input voltage range, VINDCDC1			2.5		6	V
I_O	Maximum output current			1700			mA
$r_{DS(on)}$	P-channel MOSFET on-resistance		VINDCDC1 (VINDCDC13) = $V_{(GS)}$ = 3.6 V		125	261	mΩ
I_{lkg}	P-channel leakage current		VINDCDC1 (VINDCDC13) = 6 V			2	μA
$r_{DS(on)}$	N-channel MOSFET on-resistance		VINDCDC1 (VINDCDC13) = $V_{(GS)}$ = 3.6 V		130	260	mΩ
I_{lkg}	N-channel leakage current		$V_{(DS)}$ = 6 V		7	10	μA
	Forward current limit (P-channel and N-channel)		2.5 V < $V_{(VINDCDC1)}$ < 6 V	1.94	2.19	2.44	A
f_S	Oscillator frequency			1.95	2.25	2.55	MHz
	Fixed output voltage FPWMDCDC1=0	All VDCDC1	VINDCDC1 (VINDCDC13) = 2.5 V to 6 V; 0 mA ≤ I_O ≤ 1.7 A	–2%		2%	
	Fixed output voltage FPWMDCDC1=1		VINDCDC1 (VINDCDC13) = 2.5 V to 6 V; 0 mA ≤ I_O ≤ 1.7 A	–1%		1%	
	Adjustable output voltage with resistor divider at DEFDCDC1; FPWMDCDC1=0		VINDCDC1 (VINDCDC13) = VDCDC1 + 0.5 V (min 2.5 V) to 6 V; 0 mA ≤ I_O ≤ 1.7 A	–2%		2%	
	Adjustable output voltage with resistor divider at DEFDCDC1; FPWMDCDC1=1		VINDCDC1 (VINDCDC13) = VDCDC1 + 0.5 V (min 2.5 V) to 6 V; 0 mA ≤ I_O ≤ 1.7 A	–1%		1%	
	Line Regulation		VINDCDC1 (VINDCDC13) = VDCDC1 + 0.3 V (min. 2.5 V) to 6 V; I_O = 10 mA		0		%/V
	Load Regulation		I_O = 10 mA to 1700 mA		0.25		%/A
t_{Start}	Start-up time		Time from active EN to start switching	145	175	200	µs
t_{Ramp}	V_{OUT} ramp-up time		Time to ramp from 5% to 95% of V_{OUT}	400	750	1000	µs
	Internal resistance from L1 to GND				1		MΩ
	VDCDC1 discharge resistance		DCDC1 discharge = 1		300		Ω

ELECTRICAL CHARACTERISTICS

VINDCDC1 = VINDCDC2 = VINDCDC3 (VINDCDC13) = VCC = VINLDO = 3.6 V, VBACKUP = 3 V, T_A = –40°C to 85°C, typical values are at T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
VDCDC2 STEP-DOWN CONVERTER						
V_I	Input voltage range, VINDCDC2		2.5		6	V
I_O	Maximum output current	VDCDC2 = 1.2V	1200			mA
		VINDCDC2 = 3.7 V; 3.3 V - 1% ≤ VDCDC2 ≤ 3.3V + 1%	1000			
$r_{DS(on)}$	P-channel MOSFET on-resistance	VINDCDC2 = $V_{(GS)}$ = 3.6 V		140	300	mΩ
I_{lkg}	P-channel leakage current	VINDCDC2 = 6 V			2	µA
$r_{DS(on)}$	N-channel MOSFET on-resistance	VINDCDC2 = $V_{(GS)}$ = 3.6 V		150	297	mΩ
I_{lkg}	N-channel leakage current	$V_{(DS)}$ = 6 V		7	10	µA
I_{LIMF}	Forward current limit (P-channel and N-channel)	2.5 V < VINDCDC2 < 6 V	1.74	1.94	2.12	A
f_S	Oscillator frequency		1.95	2.25	2.55	MHz
VDCDC2	Adjustable output voltage with resistor divider at DEFDCDC2; FPWMDCDC2=0	VINDCDC2 = VDCDC2 + 0.4 V (min 2.5 V) to 6 V; 0 mA ≤ I_O ≤ 1.2 A	–2%		2%	
VDCDC2	Adjustable output voltage with resistor divider at DEFDCDC2; FPWMDCDC2=1	VINDCDC2 = VDCDC2 + 0.4 V (min 2.5 V) to 6 V; 0 mA ≤ I_O ≤ 1.2 A	–1%		1%	
	Line Regulation	VINDCDC2 = VDCDC2 + 0.3 V (min. 2.5 V) to 6 V; I_O = 10 mA		0		%/V
	Load Regulation	I_O = 10 mA to 1.2 A		0.25		%/A
t_{Start}	Start-up time	Time from active EN to start switching	145	175	200	µs
t_{Ramp}	V_{OUT} ramp-up time	Time to ramp from 5% to 95% of V_{OUT}	400	750	1000	µs
	Internal resistance from L2 to GND			1		MΩ
	VDCDC2 discharge resistance	DCDC2 discharge =1		300		Ω

ELECTRICAL CHARACTERISTICS

VINDCDC1 = VINDCDC2 = VINDCDC3 (VINDCDC13) = VCC = VINLDO = 3.6 V, VBACKUP = 3 V, T_A = –40°C to 85°C, typical values are at T_A = 25°C (unless otherwise noted)

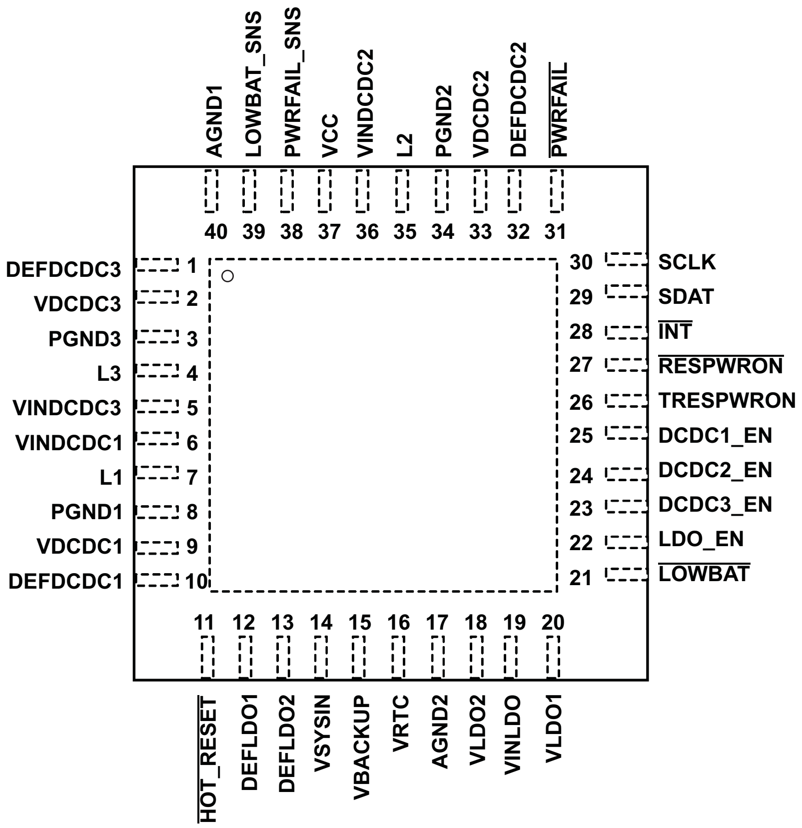
PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
VDCDC3 STEP-DOWN CONVERTER							
V_I	Input voltage range, VINDCDC3			2.5		6	V
I_O	Maximum output current		DEFDCDC3 = GND	800			mA
			VINDCDC3 (VINDCDC13) = 3.6 V; 3.3V - 1% ≤ VDCDC3 ≤ 3.3V + 1%	525			
$r_{DS(on)}$	P-channel MOSFET on-resistance		VINDCDC3 (VINDCDC13) = $V_{(GS)}$ = 3.6 V		310	698	mΩ
I_{lkg}	P-channel leakage current		VINDCDC3 (VINDCDC13) = 6 V		0.1	2	µA
$r_{DS(on)}$	N-channel MOSFET on-resistance		VINDCDC3 (VINDCDC13) = $V_{(GS)}$ = 3.6 V		220	503	mΩ
I_{lkg}	N-channel leakage current		$V_{(DS)}$ = 6 V		7	10	µA
	Forward current limit (P-channel and N-channel)		2.5 V < VINDCDC3 (VINDCDC13) < 6 V	1.28	1.49	1.69	A
f_S	Oscillator frequency			1.95	2.25	2.55	MHz
	Fixed output voltage FPWMDCDC3=0	VDCDC3 = 1.8V	VINDCDC3 (VINDCDC13) = 2.5 V to 6 V; 0 mA ≤ I_O ≤ 0.8 A	–2%		2%	
		VDCDC3 = 3.3V	VINDCDC3 (VINDCDC13) = 3.6 V to 6 V; 0 mA ≤ I_O ≤ 0.8 A	–1%		1%	
	Fixed output voltage FPWMDCDC3=1	VDCDC3 = 1.8V	VINDCDC3 (VINDCDC13) = 2.5 V to 6 V; 0 mA ≤ I_O ≤ 0.8 A	–2%		2%	
		VDCDC3 = 3.3V	VINDCDC3 (VINDCDC13) = 3.6 V to 6 V; 0 mA ≤ I_O ≤ 0.8 A	–1%		1%	
	Adjustable output voltage with resistor divider at DEFDCDC3 FPWMDCDC3=0		VINDCDC3 (VINDCDC13) = VDCDC3 + 0.5 V (min 2.5 V) to 6 V; 0 mA ≤ I_O ≤ 800 mA	–2%		2%	
	Adjustable output voltage with resistor divider at DEFDCDC3; FPWMDCDC3=1		VINDCDC3 (VINDCDC13) = VDCDC3 + 0.5 V (min 2.5 V) to 6 V; 0 mA ≤ I_O ≤ 800 mA	–1%		1%	
	Line Regulation		VINDCDC3 (VINDCDC13) = VDCDC3 + 0.3 V (min. 2.5 V) to 6 V; I_O = 10 mA		0		%/V
	Load Regulation		I_O = 10 mA to 800 mA		0.25		%/A
t_{Start}	Start-up time		Time from active EN to start switching	145	175	200	µs
t_{Ramp}	V_{OUT} ramp-up time		Time to ramp from 5% to 95% of V_{OUT}	400	750	1000	µs
	Internal resistance from L3 to GND				1		MΩ
	VDCDC3 discharge resistance		DCDC3 discharge =1		300		Ω

ELECTRICAL CHARACTERISTICS

VINDCDC1 = VINDCDC2 = VINDCDC3 (VINDCDC13) = VCC = VINLDO = 3.6 V, VBACKUP = 3 V, T_A = –40°C to 85°C, typical values are at T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
VLDO1 and VLDO2 LOW DROPOUT REGULATORS						
V_I	Input voltage range for LDO1, 2		1.5		6.5	V
$V_{O(LDO1)}$	LDO1 output voltage range		1		3.15	V
$V_{O(LDO2)}$	LDO2 output voltage range		1.05		3.3	V
I_O	Maximum output current for LDO1, LDO2	V_I = 1.8 V, V_O = 1.3 V	200			mA
		V_I = 1.5 V, V_O = 1.3 V		120		
$I_{(SC)}$	LDO1 and LDO2 short circuit current limit	$V_{(LDO1)}$ = GND, $V_{(LDO2)}$ = GND			400	mA
	Minimum voltage drop at LDO1, LDO2	I_O = 50 mA, VINLDO = 1.8 V			120	mV
		I_O = 50 mA, VINLDO = 1.5 V		65	150	
		I_O = 200 mA, VINLDO = 1.8 V			300	
	Output voltage accuracy for LDO1, LDO2	I_O = 10 mA	–2%		1%	
	Line regulation for LDO1, LDO2	VINLDO1, 2 = VLDO1,2 + 0.5 V (min. 2.5 V) to 6.5 V, I_O = 10 mA	–1%		1%	
	Load regulation for LDO1, LDO2	I_O = 0 mA to 50 mA	–1%		1%	
	Regulation time for LDO1, LDO2	Load change from 10% to 90%		10		µs
ANALOGIC SIGNALS DEFDCDC1, DEFDCDC2, DEFDCDC3						
V_{IH}	High-level input voltage		1.3		VCC	V
V_{IL}	Low-level input voltage		0		0.1	V
	Input bias current			0.001	0.05	µA
THERMAL SHUTDOWN						
$T_{(SD)}$	Thermal shutdown	Increasing junction temperature		160		°C
	Thermal shutdown hysteresis	Decreasing junction temperature		20		°C
INTERNAL UNDERVOLTAGE LOCK OUT						
UVLO	Internal UVLO	VCC falling	–2%	2.35	2%	V
$V_{(UVLO\_HYST)}$	Internal UVLO comparator hysteresis			120		mV
VOLTAGE DETECTOR COMPARATOR INPUTS PWRFAIL_SNS, LOWBAT_SNS						
	Comparator threshold (PWRFAIL_SNS, LOWBAT_SNS) LOWBAT_SNS for TPS650231RSB only	Falling threshold	–1%	1	1%	V
	Hysteresis		40	50	60	mV
	Propagation delay	25-mV overdrive			10	µs
I_{LK}	Input leakage current			0.001	0.1	µA
POWER GOOD						
$V_{(PGOODF)}$		VDCDC1, VDCDC2, VDCDC3, VLDO1, VLDO2, decreasing	–12%	–10%	–8%	
$V_{(PGOODR)}$		VDCDC1, VDCDC2, VDCDC3, VLDO1, VLDO2, increasing	–7%	–5%	–3%	

PIN ASSIGNMENT FOR TPS650231RSB
(TOP VIEW)



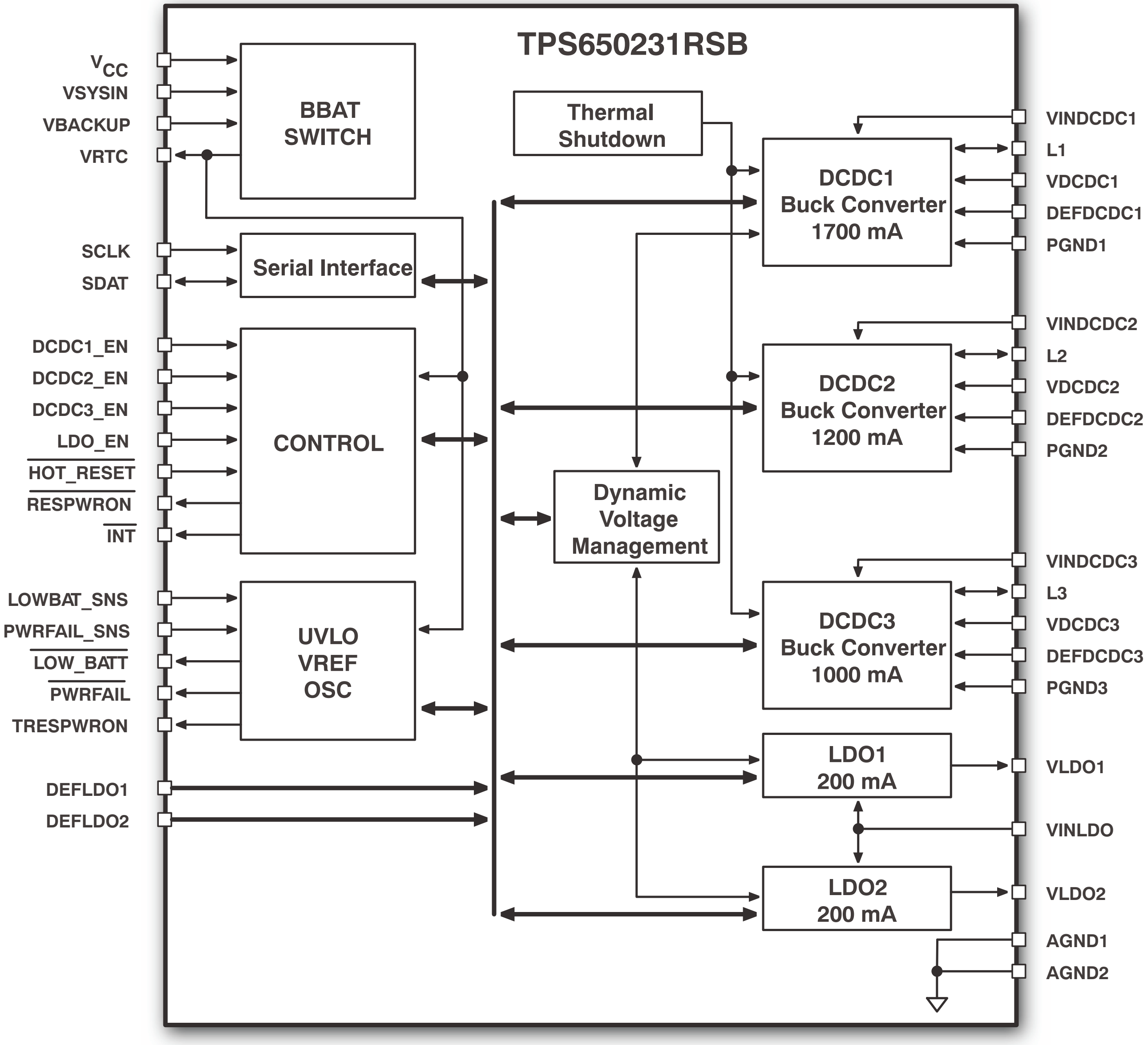
PIN FUNCTIONS FOR TPS650231RSB

PIN		I/O	DESCRIPTION
NAME	NO.		
SWITCHING REGULATOR SECTION			
AGND1	40		Analog ground. All analog ground pins are connected internally on the chip.
AGND2	17		Analog ground. All analog ground pins are connected internally on the chip.
PowerPAD™	–		Connect the power pad to analog ground.
VINDCDC1	6	I	Input voltage for VDCDC1 step-down converter. VINDCDC1 must be connected to the same voltage supply as VINDCDC2, VINDCDC3, and VCC.
L1	7		Switch pin of VDCDC1 converter. The VDCDC1 inductor is connected here.
VDCDC1	9	I	VDCDC1 feedback voltage sense input. Connect directly to VDCDC1
PGND1	8		Power ground for VDCDC1 converter.
VINDCDC2	36	I	Input voltage for VDCDC2 step-down converter. VINDCDC2 must be connected to the same voltage supply as VINDCDC1, VINDCDC3, and VCC.
L2	35		Switch pin of VDCDC2 converter. The VDCDC2 inductor is connected here.
VDCDC2	33	I	VDCDC2 feedback voltage sense input. Connect directly to VDCDC2
PGND2	34		Power ground for VDCDC2 converter
VINDCDC3	5	I	Input voltage for VDCDC3 step-down converter. VINDCDC3 must be connected to the same voltage supply as VINDCDC1, VINDCDC2, and VCC.
L3	4		Switch pin of VDCDC3 converter. The VDCDC3 inductor is connected here.
VDCDC3	2	I	VDCDC3 feedback voltage sense input. Connect directly to VDCDC3
PGND3	3		Power ground for VDCDC3 converter.
VCC	37	I	Power supply for digital and analog circuitry of VDCDC1, VDCDC2, and VDCDC3 dc-dc converters. VCC must be connected to the same voltage supply as VINDCDC3, VINDCDC1, and VINDCDC2. VCC also supplies serial interface block.

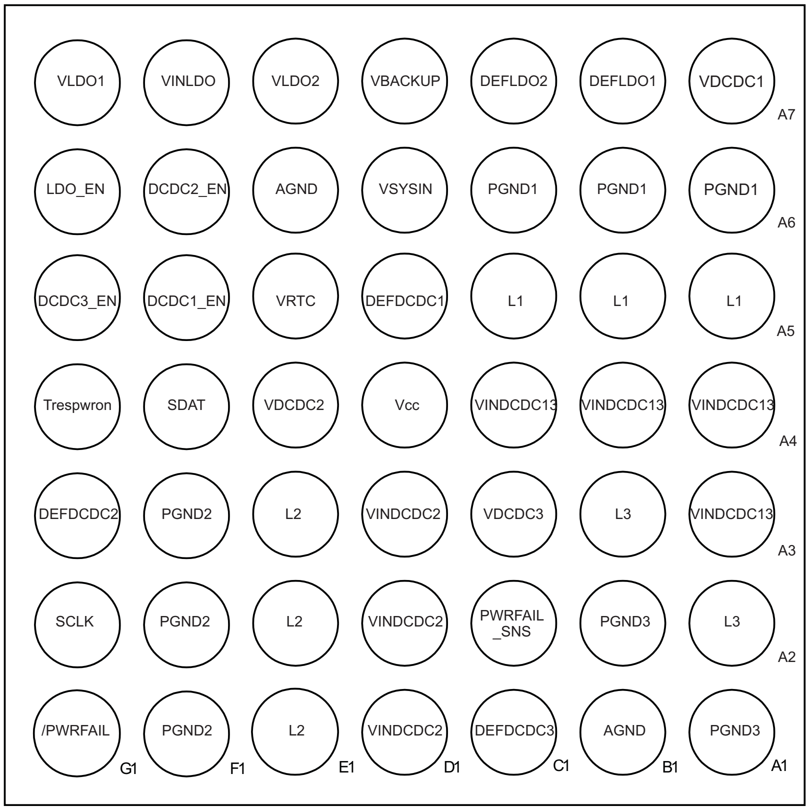
PIN FUNCTIONS FOR TPS650231RSB (continued)

PIN		I/O	DESCRIPTION
NAME	NO.		
DEFDCDC1	10	I	Input signal indicating default VDCDC1 voltage, **0** = 1.2 V, **1** = 1.6 V; DEFDCDC1 can also be connected to a resistor divider between VDCDC1 and GND, if the output voltage of the DCDC1 converter is set in a range from 0.6 V to VINDCDC1 V.
DEFDCDC2	32	I	Input signal indicating default VDCDC2 voltage, **0** = 1.8 V, **1** = 3.3 V; DEFDCDC2 can also be connected to a resistor divider between VDCDC2 and GND, if the output voltage of the DCDC2 converter is set in a range from 0.6 V to VINDCDC2 V.
DEFDCDC3	1	I	Input signal indicating default VDCDC3 voltage, **0** = 1.8 V, **1** = 3.3 V; DEFDCDC3 can also be connected to a resistor divider between VDCDC3 and GND, if the output voltage of the DCDC3 converter is set in a range from 0.6 V to VINDCDC3 V.
DCDC1_EN	25	I	VDCDC1 enable pin. A logic high enables the regulator, a logic low disables the regulator.
DCDC2_EN	24	I	VDCDC2 enable pin. A logic high enables the regulator, a logic low disables the regulator.
DCDC3_EN	23	I	VDCDC3 enable pin. A logic high enables the regulator, a logic low disables the regulator.
LDO REGULATOR SECTION			
VINLDO	19	I	Input voltage for LDO1 and LDO2
VLDO1	20	O	Output voltage of LDO1
VLDO2	18	O	Output voltage of LDO2
LDO_EN	22	I	Enable input for LDO1 and LDO2. A Logic high enables the LDOs, a logic low disables the LDOs.
VBACKUP	15	I	Connect the backup battery to this input pin.
VRTC	16	O	Output voltage of the LDO/switch for the real time clock.
VSYSIN	14	I	Input of system voltage for VRTC switch.
DEFLD01	12	I	Digital input. DEFLD01 sets the default output voltage of LDO1 and LDO2.
DEFLD02	13	I	Digital input. DEFLD02 sets the default output voltage of LDO1 and LDO2.
CONTROL AND I^2C SECTION			
$\overline{\text{HOT\_RESET}}$	11	I	Push button input that reboots or wakes up the processor via $\overline{\text{RESPWRON}}$ output pin.
TRESPWRON	26	I	Connect the timing capacitor to TRESPWRON to set the reset delay time: 1 nF → 100 ms.
$\overline{\text{RESPWRON}}$	27	O	Open drain system reset output.
$\overline{\text{PWRFAIL}}$	31	O	Open drain output. Active low when $\overline{\text{PWRFAIL}}$ comparator indicates low VBAT condition.
$\overline{\text{LOW\_BAT}}$	21	O	Open drain output of LOW_BAT comparator.
$\overline{\text{INT}}$	28	O	Open drain output
SCLK	30	I	Serial interface clock line
SDAT	29	I/O	Serial interface data/address
PWRFAIL_SNS	38	I	Input for the comparator driving the $\overline{\text{PWRFAIL}}$ output.
LOWBAT_SNS	39	I	Input for the comparator driving the $\overline{\text{LOW\_BAT}}$ output.

FUNCTIONAL BLOCK DIAGRAM



PIN ASSIGNMENT FOR TPS650231YFF (BOTTOM VIEW)



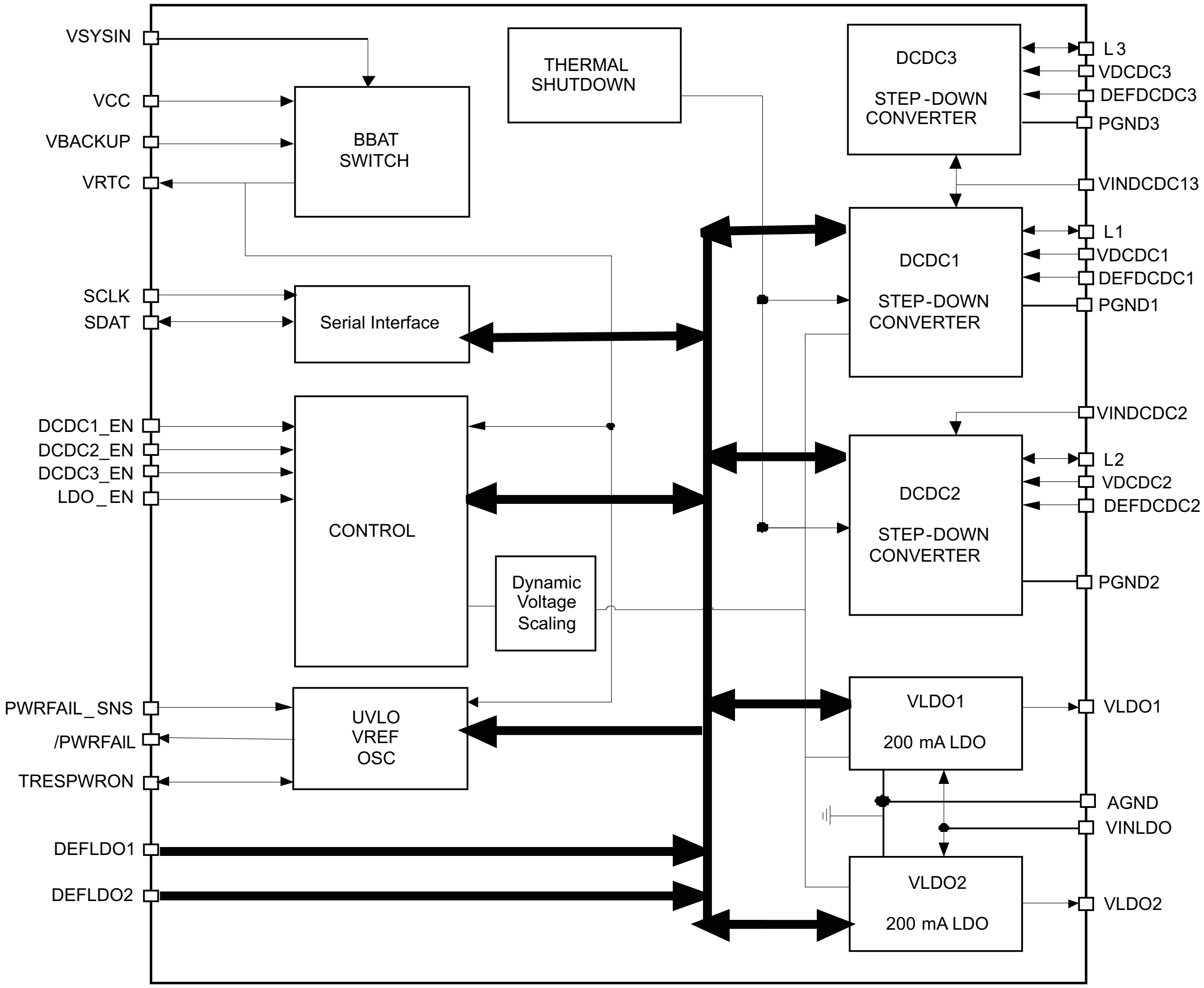
PIN FUNCTIONS FOR TPS650231YFF

PIN		I/O	DESCRIPTION
NAME	NO.		
SWITCHING REGULATOR SECTION			
AGND	B1, E6		Analog ground. All analog ground pins are connected internally on the chip.
VINDCDC13	A3, A4, B4, C4	I	Input voltage for VDCDC1 and VDCDC3 step-down converter. This must be connected to the same voltage supply as VINDCDC2 and VCC.
L1	A5, B5, C5	O	Switch pin of VDCDC1 converter. The VDCDC1 inductor is connected here.
VDCDC1	A7	I	VDCDC1 feedback voltage sense input. Connect directly to VDCDC1
PGND1	A6, B6, C6		Power ground for VDCDC1 converter.
VINDCDC2	D1, D2, D3	I	Input voltage for VDCDC2 step-down converter. VINDCDC2 must be connected to the same voltage supply as VINDCDC13 and VCC.
L2	E1, E2, E3	O	Switch pin of VDCDC2 converter. The VDCDC2 inductor is connected here.
VDCDC2	E4	I	VDCDC2 feedback voltage sense input. Connect directly to VDCDC2
PGND2	F1, F2, F3		Power ground for VDCDC2 converter
L3	A2, B3	O	Switch pin of VDCDC3 converter. The VDCDC3 inductor is connected here.
VDCDC3	C3	I	VDCDC3 feedback voltage sense input. Connect directly to VDCDC3
PGND3	A1, B2		Power ground for VDCDC3 converter.

PIN FUNCTIONS FOR TPS650231YFF (continued)

PIN		I/O	DESCRIPTION
NAME	**NO.**		
VCC	D4	I	Power supply for digital and analog circuitry of VDCDC1, VDCDC2, and VDCDC3 dc-dc converters. VCC must be connected to the same voltage supply as VINDCDC13 and VINDCDC2. VCC also supplies the serial interface block.
DEFDCDC1	D5	I	Input signal indicating default VDCDC1 voltage, **0** = 1.2 V, **1** = 1.6 V; DEFDCDC1 can also be connected to a resistor divider between VDCDC1 and GND, if the output voltage of the DCDC1 converter is set in a range from 0.6 V to VINDCDC1 V.
DEFDCDC2	G3	I	This pin needs to be connected to a resistor divider between VDCDC2 and GND. The output voltage of the DCDC2 converter is set in a range from 0.6 V to VINDCDC2 V.
DEFDCDC3	C1	I	Input signal indicating default VDCDC3 voltage, **0** = 1.8 V, **1** = 3.3 V; DEFDCDC3 can also be connected to a resistor divider between VDCDC3 and GND, if the output voltage of the DCDC3 converter is set in a range from 0.6 V to VINDCDC3 V.
DCDC1_EN	F5	I	VDCDC1 enable pin. A logic high enables the regulator, a logic low disables the regulator.
DCDC2_EN	F6	I	VDCDC2 enable pin. A logic high enables the regulator, a logic low disables the regulator.
DCDC3_EN	G5	I	VDCDC3 enable pin. A logic high enables the regulator, a logic low disables the regulator.
LDO REGULATOR SECTION			
VINLDO	F7	I	Input voltage for LDO1 and LDO2
VLDO1	G7	O	Output voltage of LDO1
VLDO2	E7	O	Output voltage of LDO2
LDO_EN	G6	I	Enable input for LDO1 and LDO2. A Logic high enables the LDOs, a logic low disables the LDOs.
VBACKUP	D7	I	Connect the backup battery to this input pin.
VRTC	E5	O	Output voltage of the LDO/switch for the real time clock.
VSYSIN	D6	I	Input of system voltage for VRTC switch.
DEFLD01	B7	I	Digital input. DEFLD01 sets the default output voltage of LDO1 and LDO2.
DEFLD02	C7	I	Digital input. DEFLD02 sets the default output voltage of LDO1 and LDO2.
CONTROL AND I^{2}C SECTION			
TRESPWRON	G4	I	Connect a 1nF capacitor from this pin to GND.
$\overline{\text{PWRFAIL}}$	G1	O	Open drain output. Active low when $\overline{\text{PWRFAIL}}$ comparator indicates low VBAT condition.
SCLK	G2	I	Serial interface clock line
SDAT	F4	I/O	Serial interface data/address
PWRFAIL_SNS	C2	I	Input for the comparator driving the $\overline{\text{PWRFAIL}}$ output.

FUNCTIONAL BLOCK DIAGRAM FOR TPS650231YFF



TYPICAL CHARACTERISTICS

Graphs were taken using the EVM with the following inductor/output capacitor combinations:

CONVERTER	INDUCTOR	OUTPUT CAPACITOR	OUTPUT CAPACITOR VALUE
VDCDC1	LQH32PN1R5	JMK107BJ106	2 × 10 μF
VDCDC2	LQH32PN2R2	JMK107BJ106	2 × 10 μF
VDCDC3	LQH32PN2R2	JMK107BJ106	2 × 10 μF

Table 1. Table of Graphs

			FIGURE
η	Efficiency	vs Output current	1, 2, 3, 4, 5, 6
	Output voltage	vs Output current at 85°C	7, 8
	Line transient response		9, 10, 11
	Load transient response		12, 13, 14
	VDCDC2 PFM operation		15
	VDCDC2 low ripple PFM operation		16
	VDCDC2 PWM operation		17
	Startup VDCDC1, VDCDC2 and VDCDC3		18
	Startup LDO1 and LDO2		19
	Line transient response		20, 21, 22
	Load transient response		23, 24, 25

DCDC1: EFFICIENCY
vs
OUTPUT CURRENT

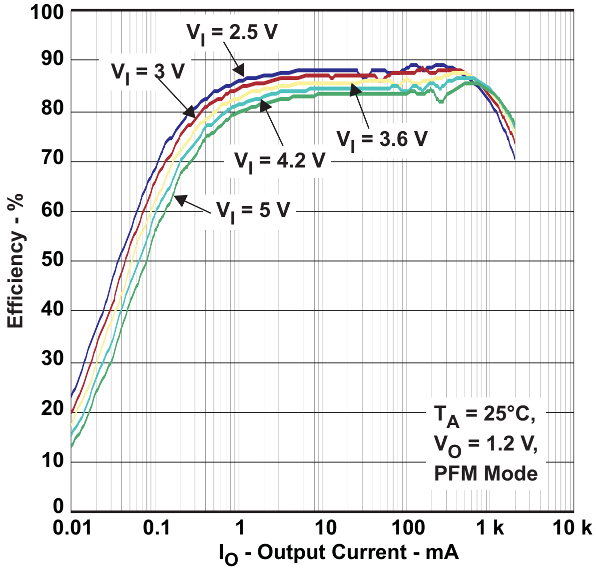


Figure 1.

DCDC1: EFFICIENCY
vs
OUTPUT CURRENT

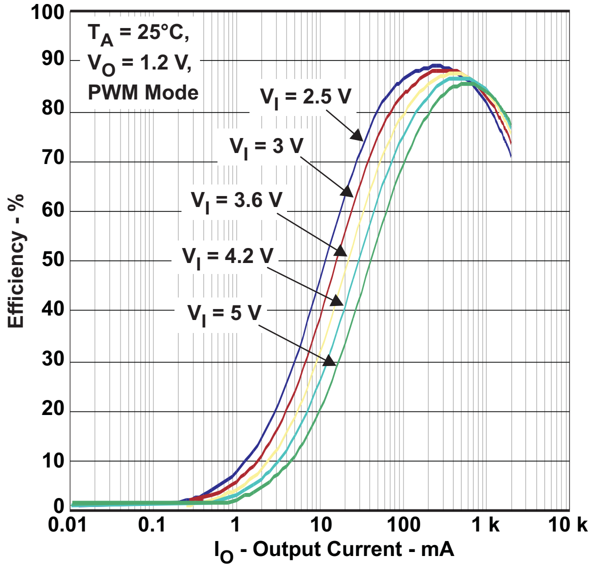


Figure 2.

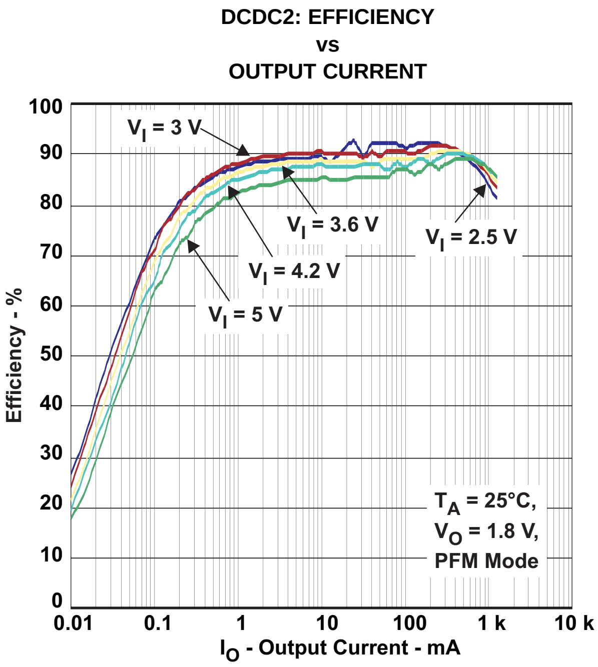

DCDC2: EFFICIENCY
vs
OUTPUT CURRENT

Figure 3.

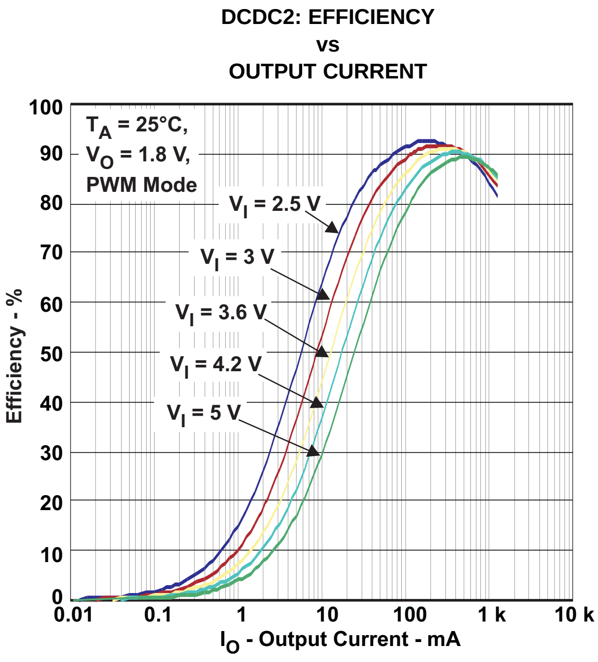

DCDC2: EFFICIENCY
vs
OUTPUT CURRENT

Figure 4.

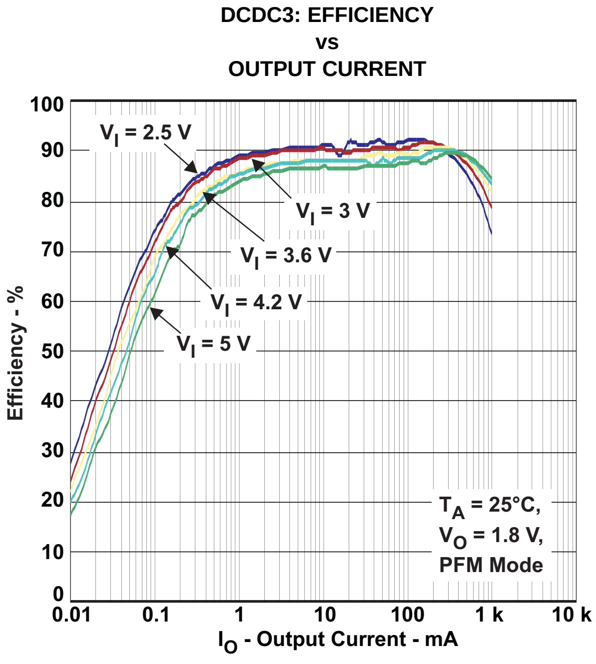

DCDC3: EFFICIENCY
vs
OUTPUT CURRENT

Figure 5.

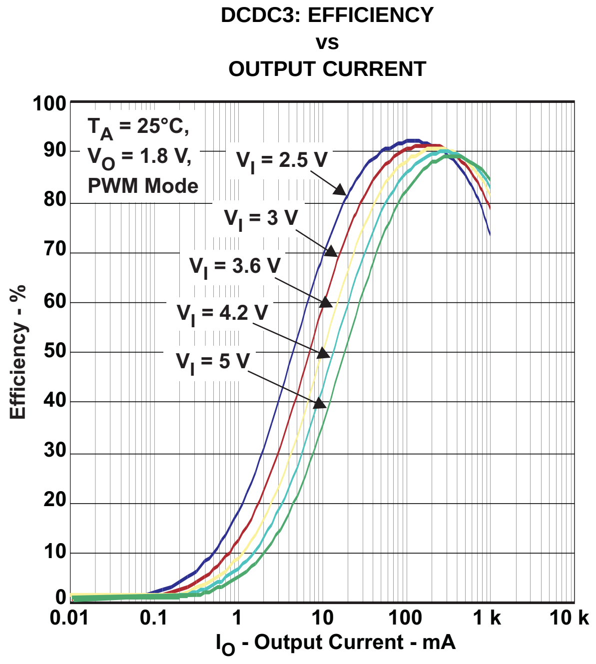

DCDC3: EFFICIENCY
vs
OUTPUT CURRENT

Figure 6.

DCDC2: OUTPUT VOLTAGE vs OUTPUT CURRENT at 85°C

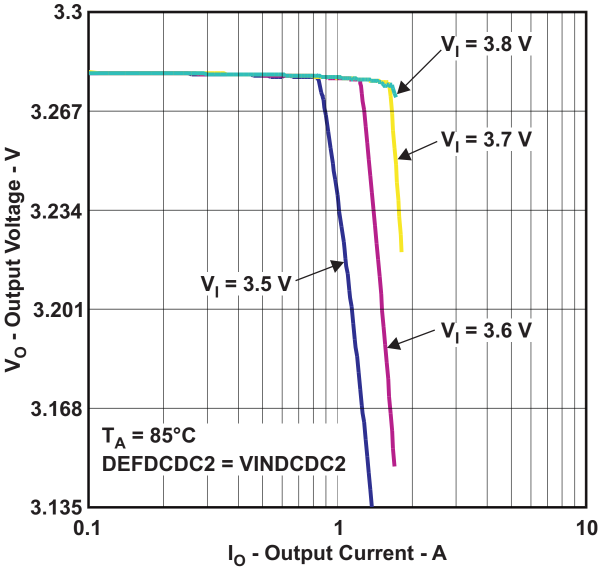


Figure 7.

DCDC3: OUTPUT VOLTAGE vs OUTPUT CURRENT at 85°C

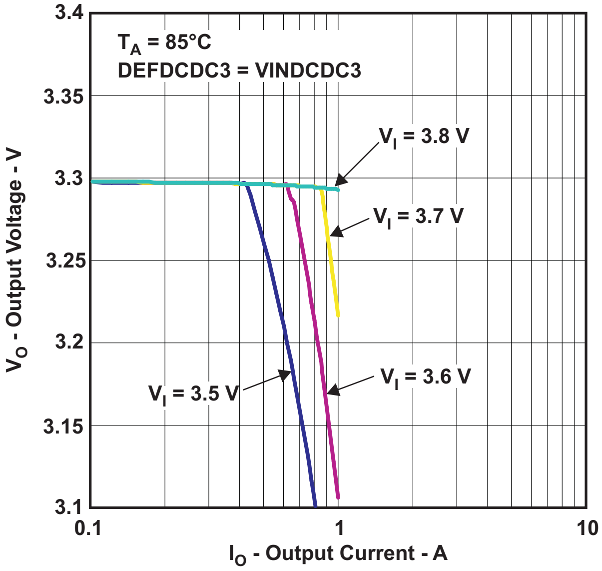


Figure 8.

VDCDC1 LINE TRANSIENT RESPONSE

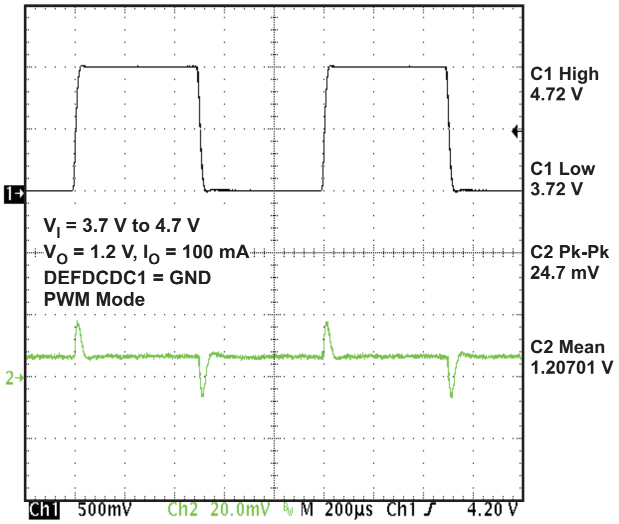


Figure 9.

VDCDC2 LINE TRANSIENT RESPONSE

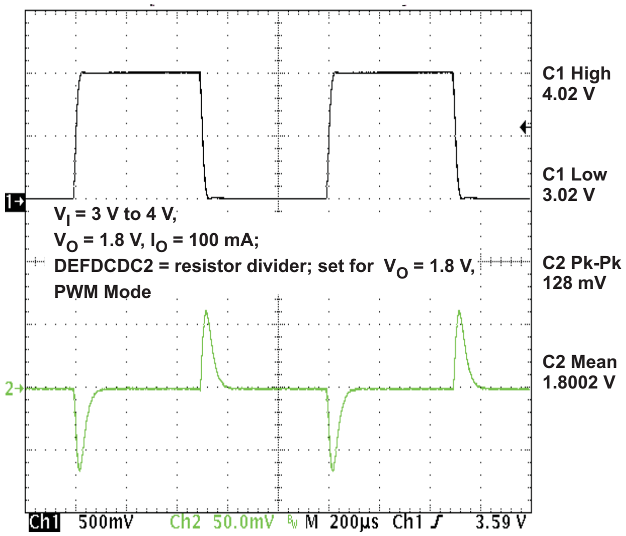


Figure 10.

VDCDC3 LINE TRANSIENT RESPONSE

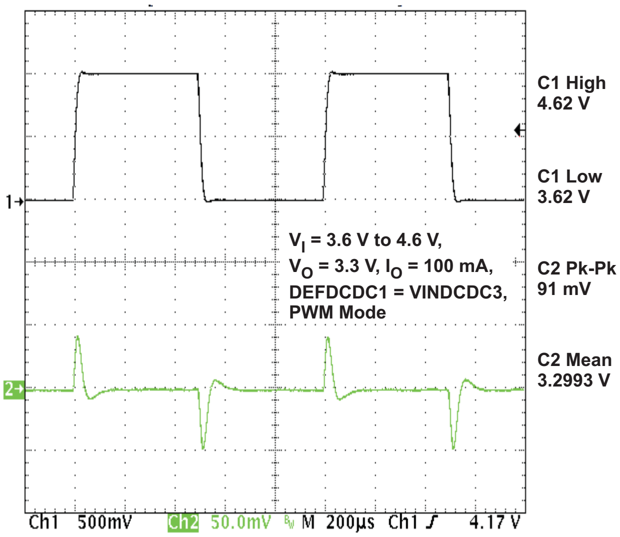


Figure 11.

VDCDC1 LOAD TRANSIENT RESPONSE

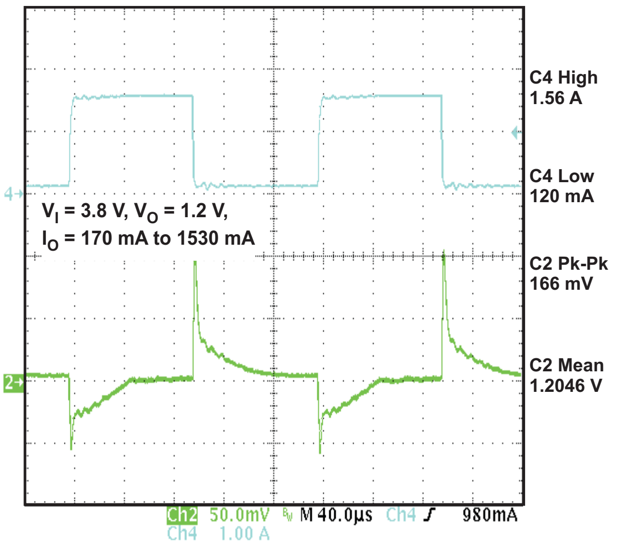


Figure 12.

VDCDC2 LOAD TRANSIENT RESPONSE

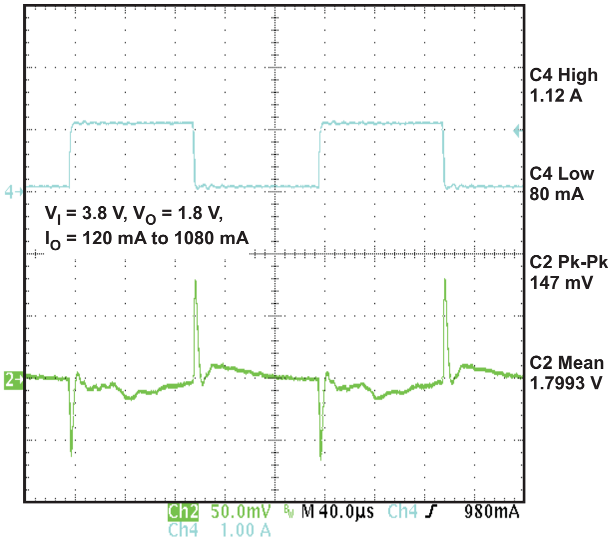


Figure 13.

VDCDC3 LOAD TRANSIENT RESPONSE

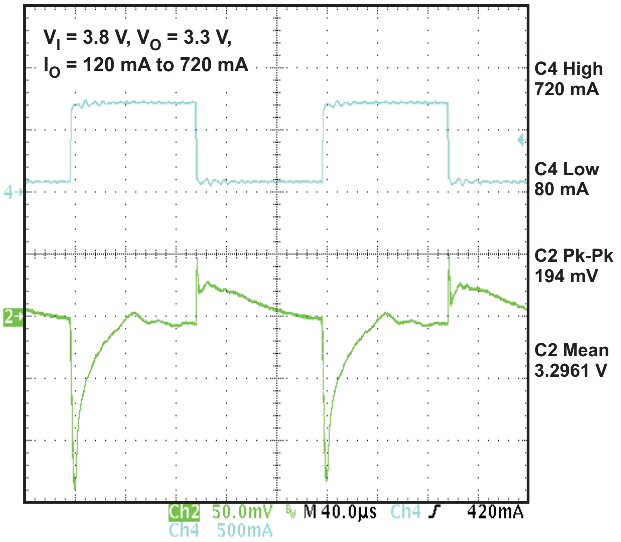


Figure 14.

VDCDC2 OUTPUT VOLTAGE RIPPLE

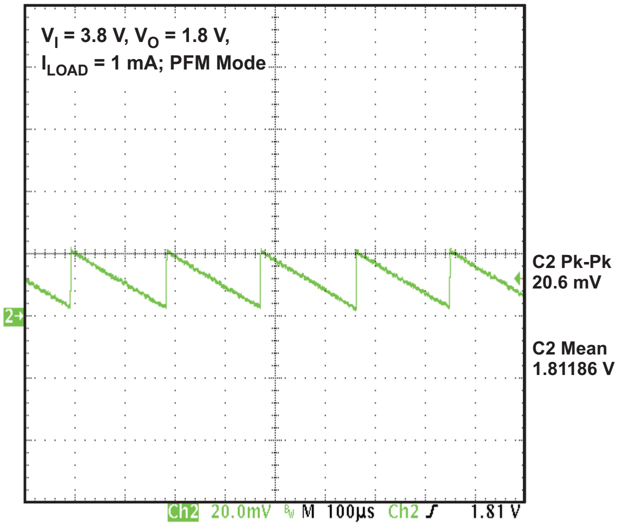


Figure 15.

VDCDC2 OUTPUT VOLTAGE RIPPLE

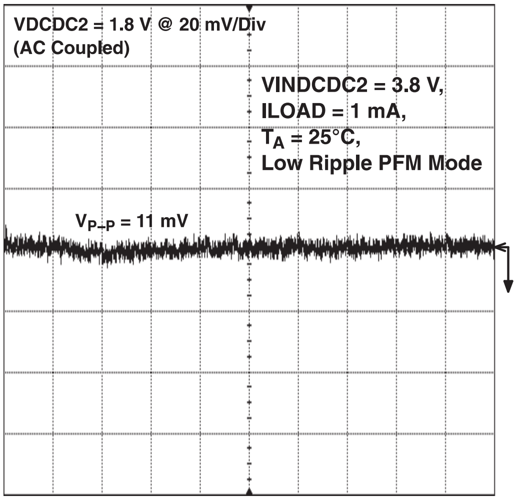


Figure 16.

VDCDC2 OUTPUT VOLTAGE RIPPLE

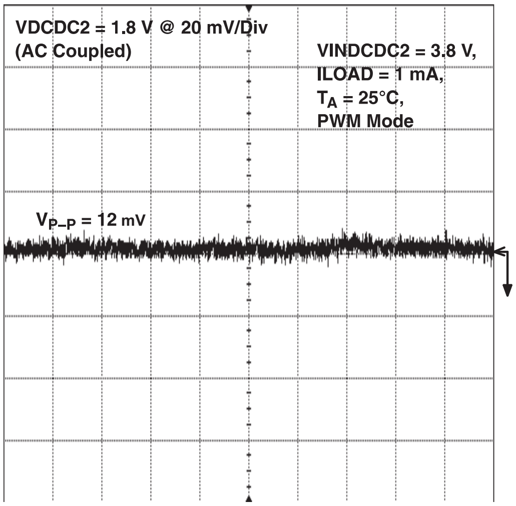


Figure 17.

STARTUP VDCDC1, VDCDC2, AND VDCDC3

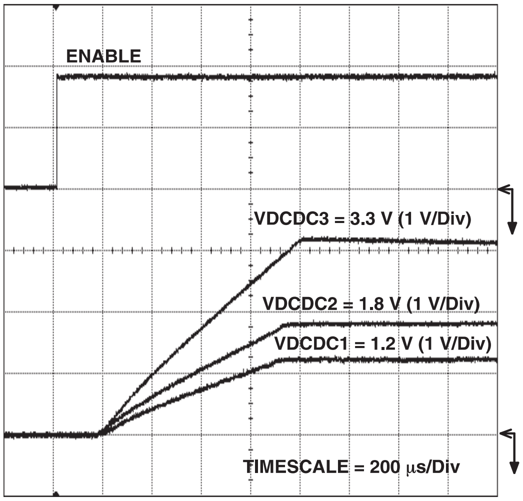


Figure 18.

STARTUP LDO1 AND LDO2

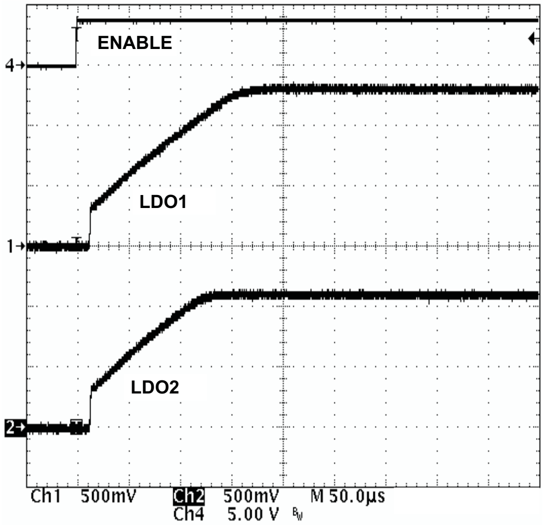


Figure 19.

LDO1 LINE TRANSIENT RESPONSE

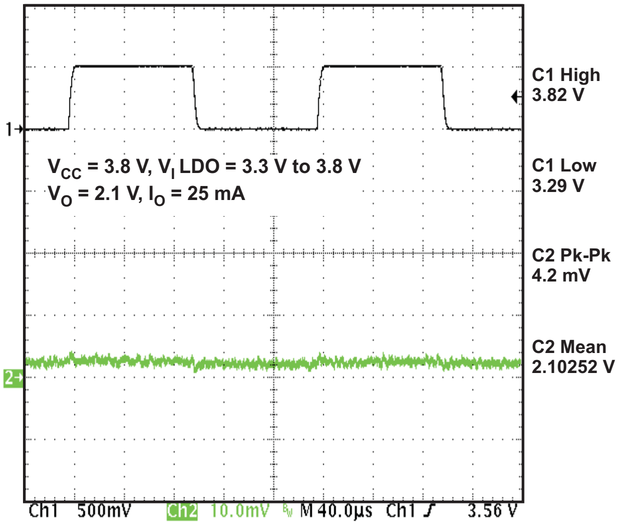


Figure 20.

LDO2 LINE TRANSIENT RESPONSE

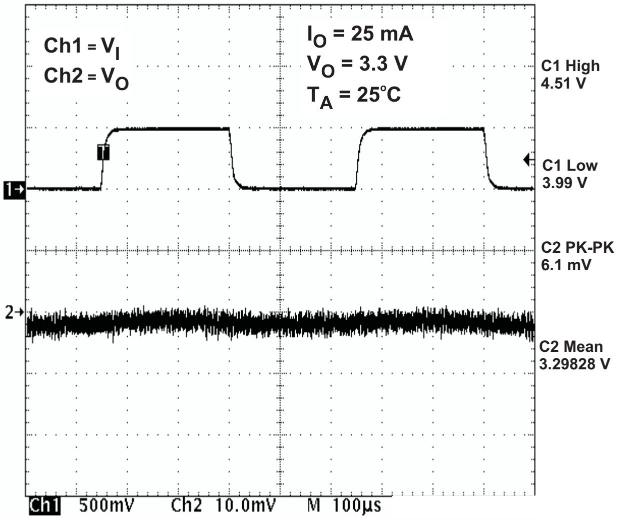


Figure 21.

VRTC LINE TRANSIENT RESPONSE

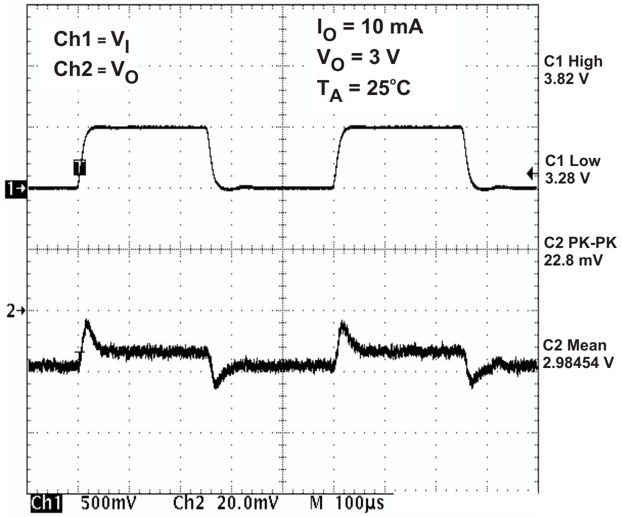


Figure 22.

LDO1 LOAD TRANSIENT RESPONSE

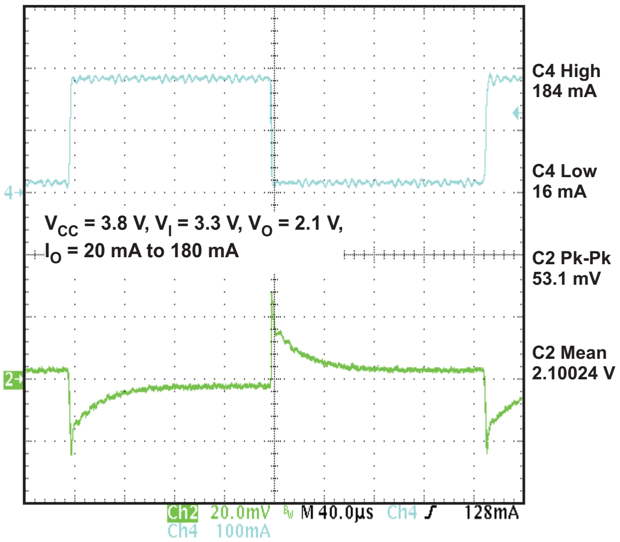


Figure 23.

LDO2 LOAD TRANSIENT RESPONSE

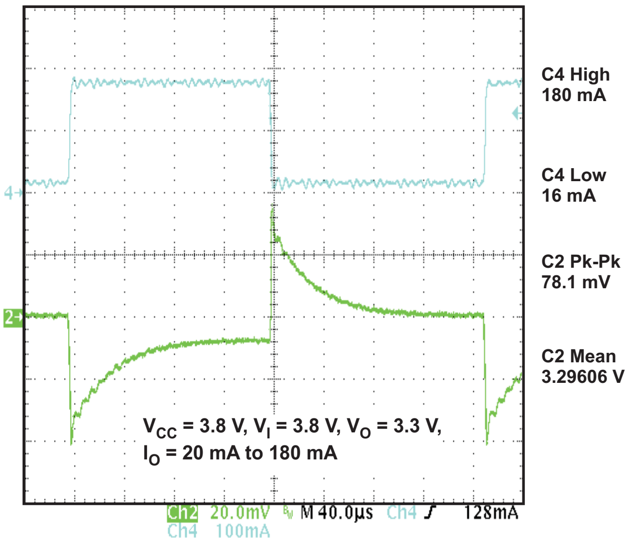


Figure 24.

VRTC LOAD TRANSIENT RESPONSE

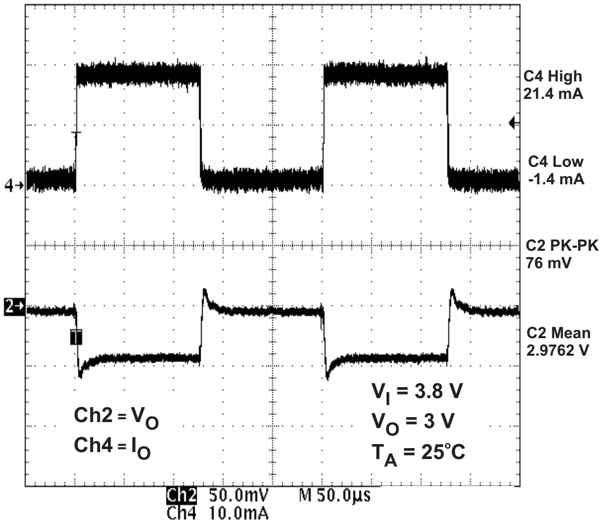


Figure 25.

DETAILED DESCRIPTION

VRTC OUTPUT AND OPERATION WITH OR WITHOUT BACKUP BATTERY

The VRTC pin is an always-on output, intended to supply up to 30 mA to a permanently required rail (i.e. for a Real Time Clock). The TPS650231 asserts the RESPWRON signal if VRTC drops below 2.4 V. VRTC is selected from a priority scheme based on the VSYSIN and VBACKUP inputs.

When the voltage at the VSYSIN pin exceeds 2.65 V, VRTC connects to the VSYSIN input via a PMOS switch and all other paths to VRTC are disabled. The PMOS switch drops a maximum of 375 mV at 30 mA, which should be considered when using VRTC. VSYSIN can be connected to any voltage source with the appropriate input voltage, including VCC or, if set to 3.3 V output, DCDC2 or DCDC3. When VSYSIN falls below 2.65 V or shorts to ground, the PMOS switch connecting VRTC and VSYSIN opens and VRTC then connects to either VBACKUP or the output of a dedicated 3V/30mA LDO. *Texas Instruments recommends connecting VSYSIN to VCC or ground - VCC if a non-replaceable primary cell is connected to VBACKUP and ground if the VRTC output will float.*

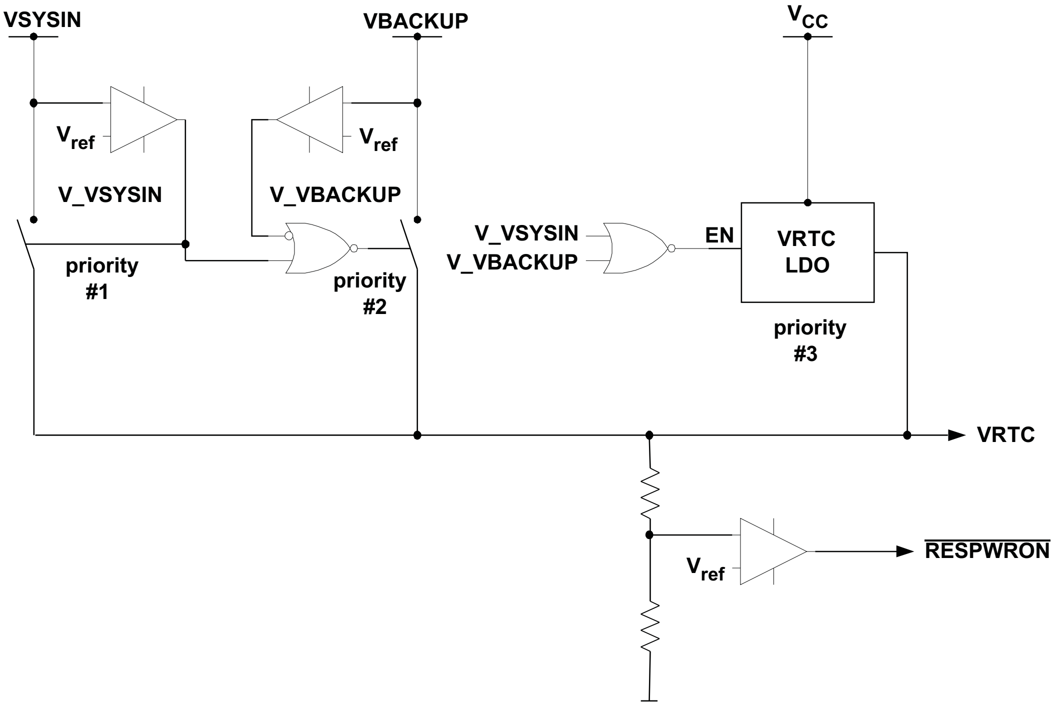
If the PMOS switch between VSYSIN and VRTC is open and VBACKUP exceeds 2.65 V, VRTC connects to VBACKUP via a PMOS switch. The PMOS switch drops a maximum of 375 mV at 30 mA, which should be considered if using VRTC. A typical application may connect VBACKUP to a primary Li button cell, but any battery that provides a voltage between 2.65 V and 6 V (i.e. a single Li-Ion cell or a single boosted NiMH battery) is acceptable, to supply the VRTC output. *In systems with no backup battery, the VBACKUP pin should be connected to GND.*

If the switches between VRTC and VSYSIN or VBACKUP are open, the dedicated 3-V/30-mA LDO, driven from VCC, connects to VRTC. This LDO is disabled if the voltage at the VSYSIN input exceeds 2.65 V.

Inside TPS650231 there is a switch (Vmax switch) which selects the higher voltage between VCC and VBACKUP. This is used as the supply voltage for some basic functions. The functions powered from the output of the Vmax switch are:

- INT output
- RESPWRON output
- HOT_RESET input
- LOW_BATT output
- PWRFAIL output
- Enable pins for dc-dc converters, LDO1 and LDO2
- Undervoltage lockout comparator (UVLO)
- Reference system with low frequency timing oscillators
- LOW_BATT and PWRFAIL comparators

The main 2.25-MHz oscillator, and the I^{2}C™ interface are only powered from V_{CC}.



A. V_VSYSIN, V_VBACKUP thresholds: falling = 2.55 V, rising = 2.65 V ±3%

B. $\overline{\text{RESPWRON}}$ thresholds: falling = 2.4 V, rising = 2.52 V ±3%

Figure 26.

STEP-DOWN CONVERTERS, VDCDC1, VDCDC2, and VDCDC3

The TPS650231 incorporates three synchronous step-down converters operating typically at 2.25MHz fixed frequency PWM (Pulse Width Modulation) at moderate to heavy load currents. At light load currents the converters automatically enter Power Save Mode and operate with PFM (Pulse Frequency Modulation). The VDCDC1 converter is capable of delivering 1.7A output current, the VDCDC2 converter is capable of delivering 1.2A and the VDCDC3 converter delivers up to 800mA.

The converter output voltages can be programmed via the DEFDCDC1, DEFDCDC2 and DEFDCDC3 pins. For DEFDCDC1 and DEFDCDC3, the pins can either be connected to GND, VCC or to a resistor divider between the output voltage and GND.

The VDCDC1 converter defaults to 1.2V or 1.6V depending on the DEFDCDC1 configuration pin, if DEFDCDC1 is tied to ground the default is 1.2V, if it is tied to VCC the default is 1.6V. When the DEFDCDC1 pin is connected to a resistor divider, the output voltage can be set in the range of 0.6V to VINDCDC1 V. See the application section for more details. The core voltage can be reprogrammed via the serial interface in the range of 0.8 V to 1.6 V with a programmable slew rate. The converter is forced into PWM operation whilst any programmed voltage change is underway, whether the voltage is being increased or decreased. The DEFCORE and DEFSLEW registers are used to program the output voltage and slew rate during voltage transitions.

The DEFDCDC2 pin does not have the logic function in parallel and always needs to be connected with a resistor divider, the output voltage can be set in the range of 0.6 V to VINDCDC2 V.

The VDCDC3 converter defaults to 1.8 V or 3.3 V depending on the DEFDCDC3 configuration pin. If DEFDCDC3 is tied to ground, the default is 1.8 V. If it is tied to VCC, the default is 3.3 V. When the DEFDCDC3 pin is connected to a resistor divider, the output voltage can be set in the range of 0.6 V to VINDCDC3 V. The step-down converter outputs (when enabled) are monitored by Power Good comparators, the outputs of which are available via the serial interface. The outputs of the DC-DC converters can be optionally discharged via on-chip 300Ω resistors when the DC-DC converters are disabled.

During PWM operation the converters use a unique fast response voltage mode controller scheme with input voltage feed-forward to achieve good line and load regulation allowing the use of small ceramic input and output capacitors. At the beginning of each clock cycle initiated by the clock signal, the P-channel MOSFET switch is turned on and the inductor current ramps up until the comparator trips and the control logic will turn off the switch. The current limit comparator will also turn off the switch in case the current limit of the P-channel switch is exceeded. After the adaptive dead time used to prevent shoot through current, the N-channel MOSFET rectifier is turned on and the inductor current will ramp down. The next cycle will be initiated by the clock signal again turning off the N-channel rectifier and turning on the P-channel switch.

The three DC-DC converters operate synchronized to each other, with the VDCDC1 converter as the master. A 180° phase shift between the VDCDC1 switch turn on and the VDCDC2 and a further 90° shift to the VDCDC3 switch turn on decreases the input RMS current and smaller input capacitors can be used. The phase of the three converters can be changed using the CON_CTRL register.

POWER SAVE MODE OPERATION

As the load current decreases, the converters enter the power save mode operation. During power save mode, the converters operate in a burst mode (PFM mode) with a frequency between 750 kHz and 2.25 MHz, nominal for one burst cycle. However, the frequency between different burst cycles depends on the actual load current and is typically far less than the switching frequency with a minimum quiescent current to maintain high efficiency.

In order to optimize the converter efficiency at light load, the average current is monitored and if in PWM mode the inductor current remains below a certain threshold, then PSM is entered. The typical threshold to enter PSM is calculated as follows:

$$I_{PFMDCDC1\ enter} = \frac{VINDCDC1}{24\ \Omega}$$

$$I_{PFMDCDC2\ enter} = \frac{VINDCDC2}{26\ \Omega}$$

$$I_{PFMDCDC3\ enter} = \frac{VINDCDC3}{39\ \Omega} \qquad (1)$$

During the power save mode the output voltage is monitored with a comparator, and by maximum skip burst width. As the output voltage falls below the threshold, set to the nominal V_O, the P-channel switch turns on and the converter effectively delivers a constant current defined as follows.

$$I_{PFMDCDC1\ leave} = \frac{VINDCDC1}{18\ \Omega}$$

$$I_{PFMDCDC2\ leave} = \frac{VINDCDC2}{20\ \Omega}$$

$$I_{PFMDCDC3\ leave} = \frac{VINDCDC3}{29\ \Omega} \qquad (2)$$

If the load is below the delivered current then the output voltage rises until the same threshold is crossed in the other direction. All switching activity ceases, reducing the quiescent current to a minimum until the output voltage has again dropped below the threshold. The power save mode is exited, and the converter returns to PWM mode if either of the following conditions are met:

1. the output voltage drops 2% below the nominal V_O due to increasing load current
2. the PFM burst time exceeds 16 × 1/fs (7.11 µs typical).

These control methods reduce the quiescent current to typically 14 μA per converter, and the switching activity to a minimum, thus achieving the highest converter efficiency. Setting the comparator thresholds at the nominal output voltage at light load current results in a low output voltage ripple. The ripple depends on the comparator delay and the size of the output capacitor. Increasing capacitor values makes the output ripple tend to zero. The PSM is disabled through the I^2C interface to force the individual converters to stay in fixed frequency PWM mode.

LOW RIPPLE MODE

Setting Bit 3 in register CON-CTRL to 1 enables the low ripple mode for all of the dc-dc converters if operated in PFM mode. For an output current less than approximately 10 mA, the output voltage ripple in PFM mode is reduced, depending on the actual load current. The lower the actual output current on the converter, the lower the output ripple voltage. For an output current above 10 mA, there is only minor difference in output voltage ripple between PFM mode and low ripple PFM mode. As this feature also increases switching frequency, it is used to keep the switching frequency above the audible range in PFM mode down to a low output current.

SOFT START

Each of the three converters has an internal soft start circuit that limits the inrush current during start-up. The soft start is realized by using a low current to initially charge the internal compensation capacitor. The soft start time is typically 750 μs if the output voltage ramps from 5% to 95% of the final target value. If the output is already precharged to some voltage when the converter is enabled, then this time is reduced proportionally. There is a short delay of typically 170 μs between the converter being enabled and switching activity actually starting. This allows the converter to bias itself properly, to recognize if the output is precharged, and if so to prevent discharging of the output while the internal soft start ramp catches up with the output voltage.

100% DUTY CYCLE LOW DROPOUT OPERATION

The TPS650231 converters offer a low input to output voltage difference while still maintaining operation with the use of the 100% duty cycle mode. In this mode the P-channel switch is constantly turned on. This is particularly useful in battery-powered applications to achieve longest operation time by taking full advantage of the whole battery voltage range. The minimum input voltage required to maintain dc regulation depends on the load current and output voltage. It is calculated as:

$$\mathrm{Vin}_{min} = \mathrm{Vout}_{min} + \mathrm{Iout}_{max} \times \left(r_{DS(on)}\,\mathrm{max} + R_L\right) \tag{3}$$

with:

$Iout_{max}$ = maximum load current (Note: ripple current in the inductor is zero under these conditions)
$r_{DS(on)}max$ = maximum P-channel switch $r_{DS(on)}$
R_L = DC resistance of the inductor
$Vout_{min}$ = nominal output voltage minus 2% tolerance limit

ACTIVE DISCHARGE WHEN DISABLED

When the VDCDC1, VDCDC2, and VDCDC3 converters are disabled, due to an UVLO, DCDC_EN or OVERTEMP condition, it is possible to actively pull down the outputs. This feature is disabled per default and is individually enabled via the CON_CTRL2 register in the serial interface. When this feature is enabled, the VDCDC1, VDCDC2, and VDCDC3 outputs are discharged by a 300 Ω (typical) load which is active as long as the converters are disabled.

POWER GOOD MONITORING

All three step-down converters and both the LDO1 and LDO2 linear regulators have power good comparators. Each comparator indicates when the relevant output voltage has dropped 10% below its target value with 5% hysteresis. The outputs of these comparators are available in the PGOODZ register via the serial interface. An interrupt is generated when any voltage rail drops below the 10% threshold. The comparators are disabled when the converters are disabled and the relevant PGOODZ register bits indicate that power is good.

LOW DROPOUT VOLTAGE REGULATORS

The low dropout voltage regulators are designed to operate well with low value ceramic input and output capacitors. They operate with input voltages down to 1.5 V. The LDOs offer a maximum dropout voltage of 300 mV at rated output current. Each LDO supports a current limit feature. Both LDOs are enabled by the LDO_EN pin, both LDOs can be disabled or programmed via the serial interface using the REG_CTRL and LDO_CTRL registers. The LDOs also have reverse conduction prevention. This allows the possibility to connect external regulators in parallel in systems with a backup battery. The TPS650231 step-down and LDO voltage regulators automatically power down when the V_{CC} voltage drops below the UVLO threshold or when the junction temperature rises above 160°C.

POWER GOOD MONITORING

Both the LDO1 and LDO2 linear regulators have power good comparators. Each comparator indicates when the relevant output voltage has dropped 10% below its target value, with 5% hysteresis. The outputs of these comparators are available in the PGOODZ register via the serial interface. An interrupt is generated when any voltage rail drops below the 10% threshold. The comparators are disabled when the LDOs are disabled and the relevant PGOODZ register bits indicate that power is good.

UNDERVOLTAGE LOCKOUT

The undervoltage lockout circuit for the five regulators on the TPS650231 prevents the device from malfunctioning at low-input voltages and from excessive discharge of the battery. It disables the converters and LDOs. The UVLO circuit monitors the VCC pin, the threshold is set internally to 2.35 V with 5% (120 mV) hysteresis. Note that when any of the dc-dc converters are running, there is an input current at the VCC pin, which is up to 3 mA when all three converters are running in PWM mode. This current needs to be taken into consideration if an external RC filter is used at the VCC pin to remove switching noise from the TPS650231 internal analog circuitry supply.

POWER-UP SEQUENCING

The TPS650231 power-up sequencing is designed to be entirely flexible and customer driven. This is achieved by providing separate enable pins for each switch-mode converter, and a common enable signal for the LDOs. The relevant control pins are described in Table 2.

Table 2. Control Pins and Status Outputs for DC-DC Converters

PIN NAME	I/O	FUNCTION
DEFDCDC3	I	Defines the default voltage of the VDCDC3 switching converter. DEFDCDC3 = 0 defaults VDCDC3 to 1.8 V, DEFDCDC3 = VCC defaults VDCDC3 to 3.3 V.
DEFDCDC2	I	Feedback pin of the VDCDC2 switching converter, connected to a resistive divider. The output voltage can be set between 0.6V and VINDCDC2 V.
DEFDCDC1	I	Defines the default voltage of the VDCDC1 switching converter. DEFDCDC1 = 0 defaults VDCDC1 to 1.2 V, DEFDCDC1 = VCC defaults VDCDC1 to 1.6 V.
DCDC3_EN	I	Set DCDC3_EN = 0 to disable and DCDC3_EN = 1 to enable the VDCDC3 converter
DCDC2_EN	I	Set DCDC2_EN = 0 to disable and DCDC2_EN = 1 to enable the VDCDC2 converter
DCDC1_EN	I	Set DCDC1_EN = 0 to disable and DCDC1_EN = 1 to enable the VDCDC1 converter
HOT_RESET	I	TPS650231RSB only: The HOT_RESET pin generates a reset (RESPWRON) for the processor.HOT_RESET does not alter any TPS650231 settings except the output voltage of VDCDC1. Activating HOT_RESET sets the voltage of VDCDC1 to its default value defined with the DEFDCDC1 pin. HOT_RESET is internally de-bounced by the TPS650231.
RESPWRON	O	TPS650231RSB only: RESPWRON is held low when power is initially applied to the TPS650231. The VRTC voltage is monitored: RESWPRON is low when VRTC < 2.4 V and remains low for a time defined by the external capacitor at the TRESPWRON pin. RESPWRON can also be forced low by activation of the HOT_RESET pin.
TRESPWRON	I	Connect a capacitor here to define the RESET time at the RESPWRON pin (1 nF typically gives 100 ms).

SYSTEM RESET + CONTROL SIGNALS

The $\overline{\text{RESPWRON}}$ signal can be used as a global reset for the application. It is an open drain output. The $\overline{\text{RESPWRON}}$ signal is generated according to the power good comparator of VRTC, and remains low for $t_{nrespwron}$ seconds after VRTC has risen above 2.52 V (falling threshold is 2.4 V, 5% hysteresis). $t_{nrespwron}$ is set by an external capacitor at the TRESPWRON pin. 1 nF gives typically 100 ms. $\overline{\text{RESPWRON}}$ is also triggered by the $\overline{\text{HOT\_RESET}}$ input. This input is internally debounced, with a filter time of typically 30 ms.

The $\overline{\text{PWRFAIL}}$ and $\overline{\text{LOW\_BAT}}$ signals are generated by two voltage detectors using the PWRFAIL_SNS and LOWBAT_SNS input signals. Each input signal is compared to a 1 V threshold (falling edge) with 5% (50 mV) hysteresis.

The DCDC1 converter is reset to its default output voltage defined by the DEFDCDC1 input, when $\overline{\text{HOT\_RESET}}$ is asserted. Other I^2C registers are not affected. Generally, the DCDC1 converter is set to its default voltage with one of these conditions: $\overline{\text{HOT\_RESET}}$ active, VRTC lower than its threshold voltage, undervoltage lockout (UVLO) condition, or $\overline{\text{RESPWRON}}$ active.

The $\overline{\text{RESPWRON}}$, $\overline{\text{HOT\_RESET}}$, $\overline{\text{LOW\_BAT}}$ and LOWBAT_SNS pins are not available in TPS650231YFF.

DEFLDO1 and DEFLDO2

These two pins are used to set the default output voltage of the two 200 mA LDOs. The digital value applied to the pins is latched during power up and determines the initial output voltage according to Table 3. The voltage of both LDOs can be changed during operation with the I^2C interface as described in the interface description.

Table 3.

DEFLDO2	DEFLDO1	VLDO1	VLDO2
0	0	1.3 V	3.3 V
0	1	2.8 V	3.3 V
1	0	1.3 V	1.8 V
1	1	2.1 V	3.3 V

Interrupt Management and the $\overline{\text{INT}}$ Pin

The $\overline{\text{INT}}$ pin combines the outputs of the PGOOD comparators from each dc-dc converter and the LDOs. The $\overline{\text{INT}}$ pin is used as a POWER_OK pin to indicate when all enabled supplies are in regulation. The $\overline{\text{INT}}$ pin remains active (low state) during power up as long as all enabled power rails are below their regulation limit. Once the last enabled power rail is within regulation, the $\overline{\text{INT}}$ pin transitions to a high state.

During operation, if one of the enabled supplies goes out of regulation, $\overline{\text{INT}}$ transitions to a low state, and the corresponding bit in the PGOODZ register goes high. If the supply goes back to its regulation limits, $\overline{\text{INT}}$ transitions back to a high state.

While $\overline{\text{INT}}$ is in an active low state, reading the PGOODZ register via the I^2C bus forces $\overline{\text{INT}}$ into a high-Z state. Since this pin requires an external pull-up resistor, the $\overline{\text{INT}}$ pin transitions to a logic high state even though the supply in question is still out of regulation. The corresponding bit in the PGOODZ register still indicates that the power rail is out of regulation.

Interrupts can be masked using the MASK register; default operation is not to mask any DCDC or LDO interrupts since this provides the POWER_OK function. If none of the DCDC converters or LDOs are enabled, /INT defaults to a low state independently of the settings of the MASK register.

TIMING DIAGRAMS

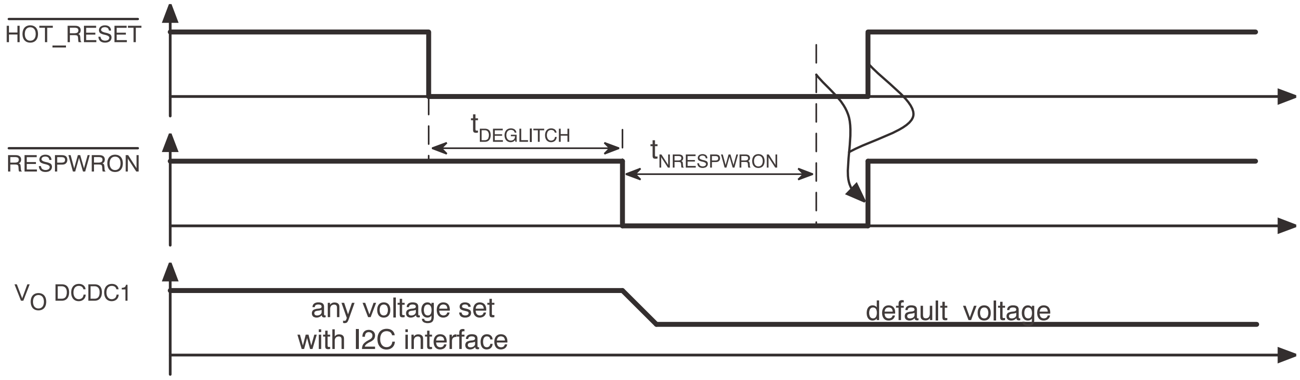
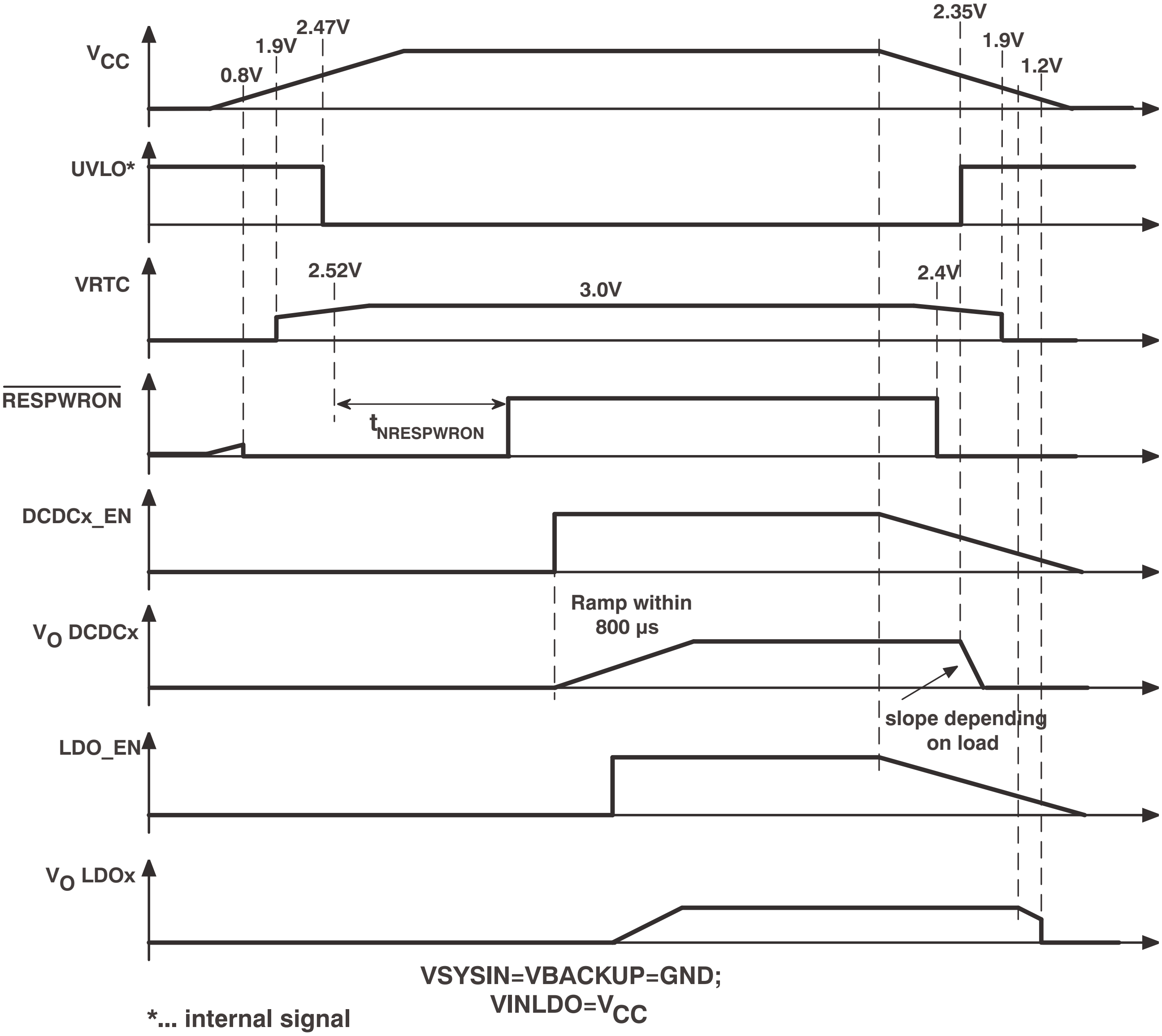


Figure 27. HOT_RESET Timing (TPS650231RSB only)



VSYSIN=VBACKUP=GND;
VINLDO=V_{CC}

*... internal signal

Figure 28. Power-Up and Power-Down Timing

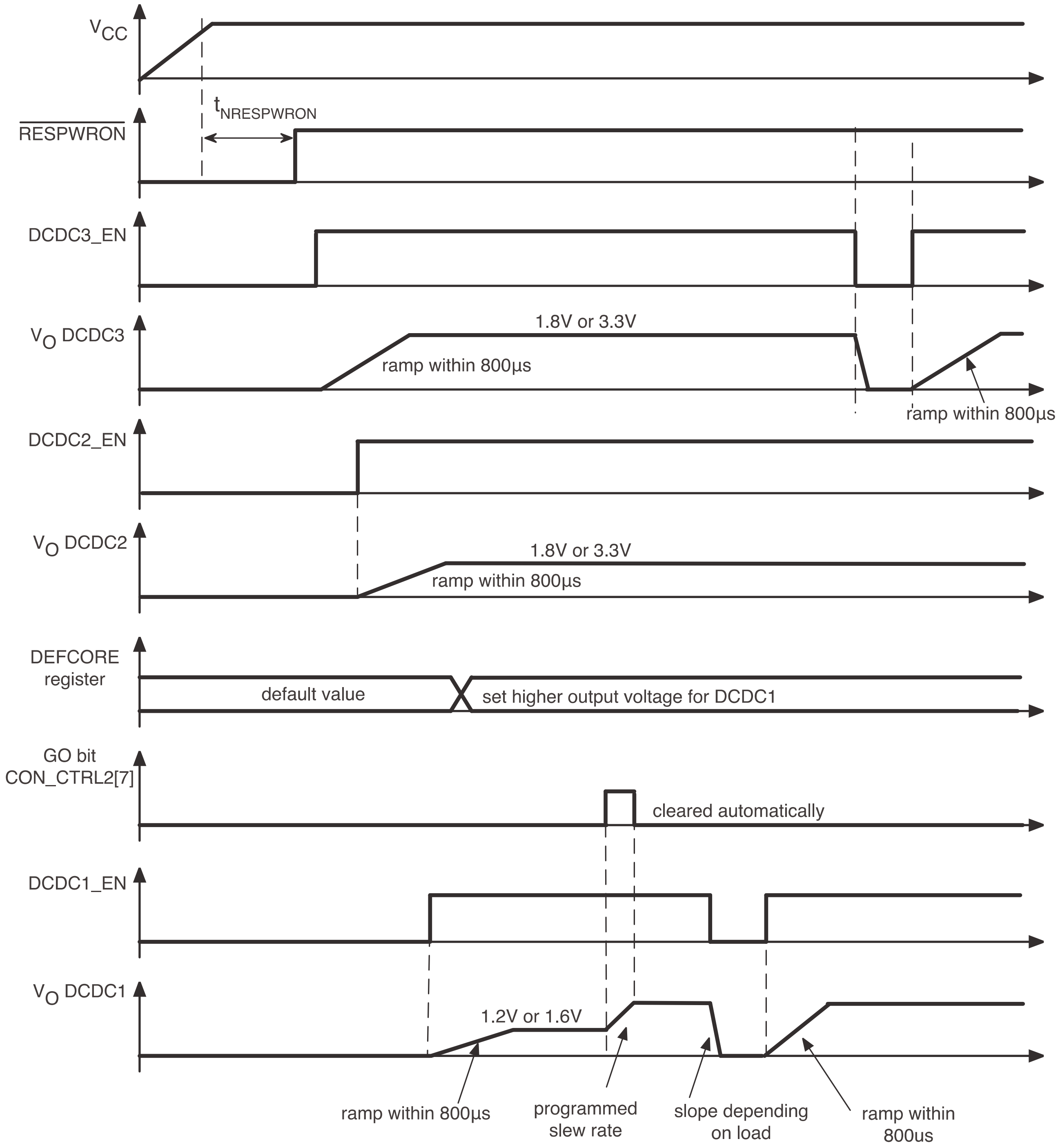


Figure 29. DVS Timing

SERIAL INTERFACE

The serial interface is compatible with the standard and fast mode I^2C specifications, allowing transfers at up to 400 kHz. The interface adds flexibility to the power supply solution, enabling most functions to be programmed to new values depending on the instantaneous application requirements and charger status to be monitored. Register contents remain intact as long as VCC remains above 2 V. The TPS650231 has a 7-bit address: 1001000, other addresses are available upon contact with the factory. Attempting to read data from the register addresses not listed in this section results in FFh being read out.

For normal data transfer, DATA is allowed to change only when CLK is low. Changes when CLK is high are reserved for indicating the start and stop conditions. During data transfer, the data line must remain stable whenever the clock line is high. There is one clock pulse per bit of data. Each data transfer is initiated with a start condition and terminated with a stop condition. When addressed, the TPS650231 device generates an acknowledge bit after the reception of each byte. The master device (microprocessor) must generate an extra clock pulse that is associated with the acknowledge bit. The TPS650231 device must pull down the DATA line during the acknowledge clock pulse so that the DATA line is a stable low during the high period of the acknowledge clock pulse. The DATA line is a stable low during the high period of the acknowledge–related clock pulse. Setup and hold times must be taken into account. During read operations, a master must signal the end of data to the slave by not generating an acknowledge bit on the last byte that was clocked out of the slave. In this case, the slave TPS650231 device must leave the data line high to enable the master to generate the stop condition

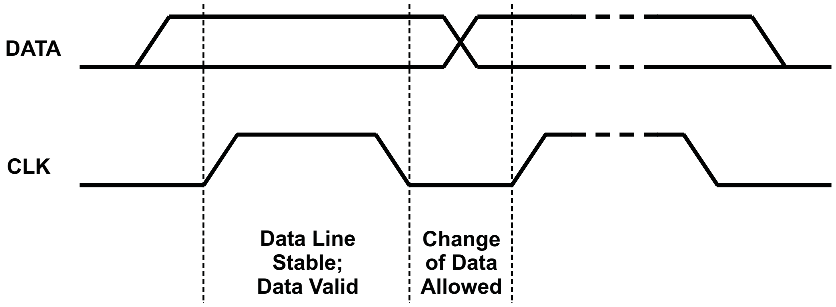


Figure 30. Bit Transfer on the Serial Interface

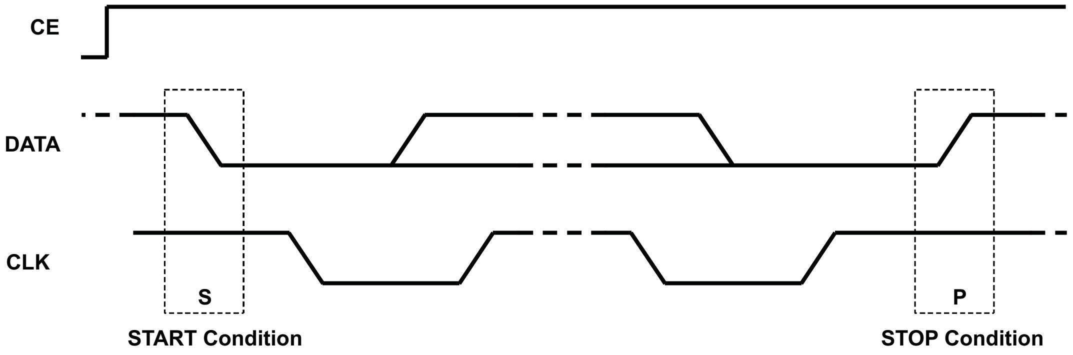
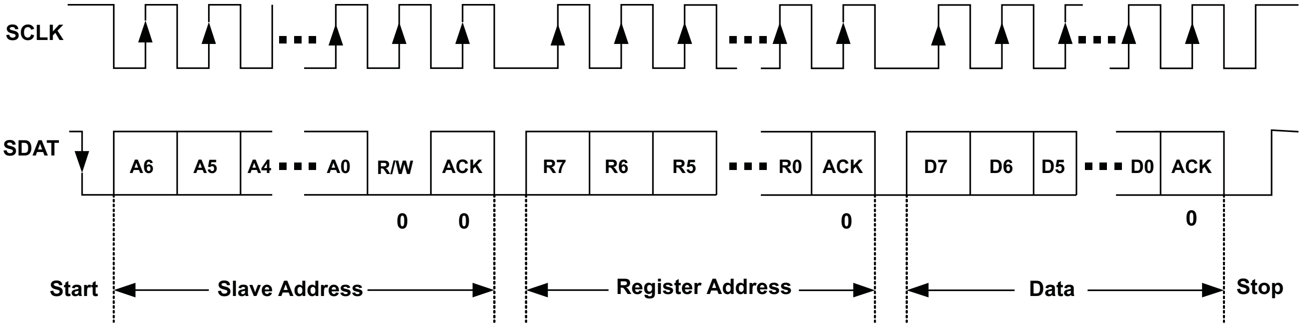


Figure 31. START and STOP Conditions



Note: SLAVE = TPS650231

Figure 32. Serial I/f WRITE to TPS650231 Device

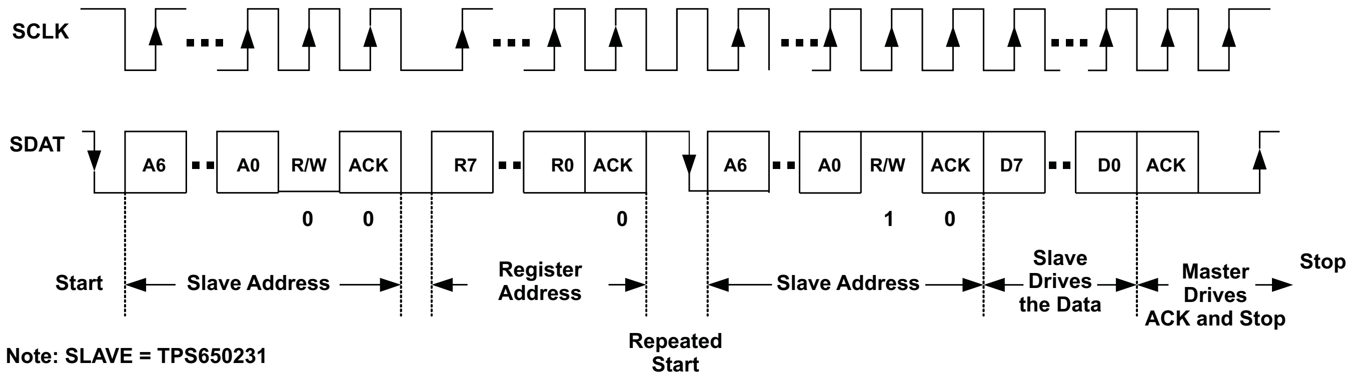


Figure 33. Serial I/f READ from TPS650231: Protocol A

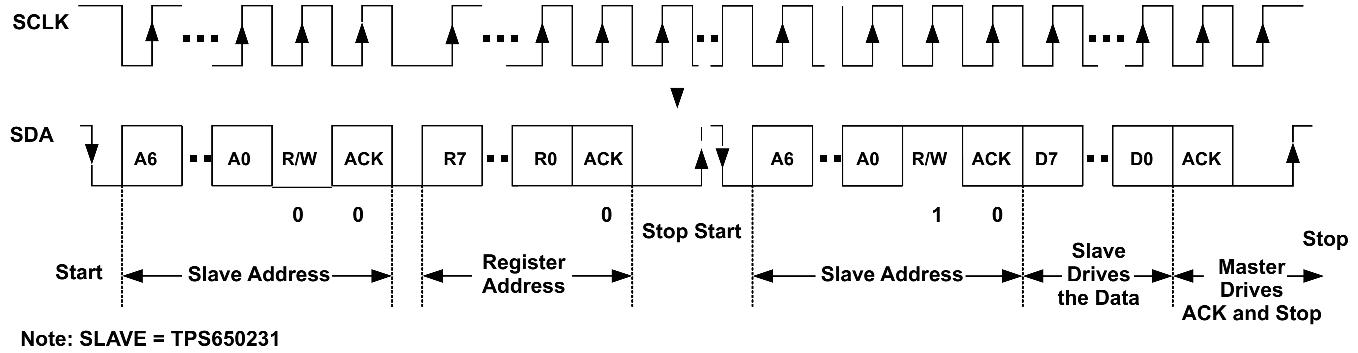


Figure 34. Serial I/f READ from TPS650231: Protocol B

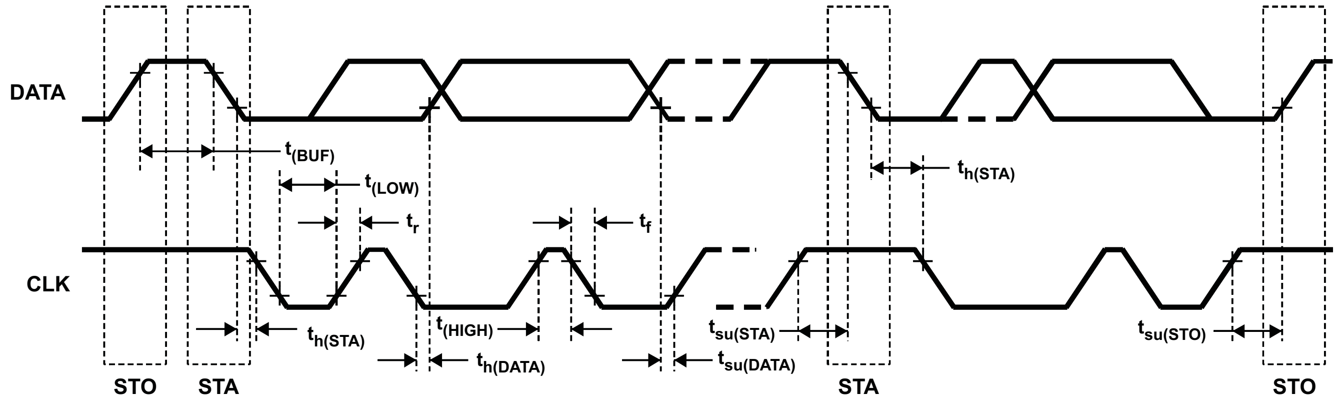


Figure 35. Serial I/f Timing Diagram

	Operating conditions: VINDCDC1 = VINDCDC2 = VINDCDC3 = VCC = VINLDO = 2.5V to 5.5V, VBACKUP = 3.0V, **T_A = -40 °C to +85 °C**	MIN	MAX	UNIT
f_{MAX}	Clock frequency		400	kHz
$t_{wH(HIGH)}$	Clock high time	600		ns
$t_{wL(LOW)}$	Clock low time	1300		ns
t_R	DATA and CLK rise time		300	ns
t_F	DATA and CLK fall time		300	ns
$t_{h(STA)}$	Hold time (repeated) START condition (after this period the first clock pulse is generated)	600		ns
$t_{su(DATA)}$	Setup time for repeated START condition	600		ns
$t_{h(DATA)}$	Data input hold time	100		ns
$t_{su(DATA)}$	Data input setup time	100		ns
$t_{su(STO)}$	STOP condition setup time	600		ns
$t_{(BUF)}$	Bus free time	1300		ns

VERSION. Register Address: 00h (read only)

VERSION	B7	B6	B5	B4	B3	B2	B1	B0
Bit name and function	0	0	1	0	0	0	1	1
Read/Write	R	R	R	R	R	R	R	R

PGOODZ. Register Address: 01h (read only)

PGOODZ	**B7**	**B6**	**B5**	**B4**	**B3**	**B2**	**B1**	**B0**
Bit name and function	PWRFAILZ	LOWBATTZ	PGOODZ VDCDC1	PGOODZ VDCDC2	PGOODZ VDCDC3	PGOODZ LDO2	PGOODZ LDO1	
Set by signal	PWRFAIL	LOWBATT	PGOODZ VDCDC1	PGOODZ VDCDC2	PGOODZ VDCDC3	PGOODZ LDO2	PGOODZ LDO1	
Default value loaded by:	PWRFAILZ	LOWBATTZ	PGOOD VDCDC1	PGOOD VDCDC2	PGOOD VDCDC3	PGOOD LDO2	PGOOD LDO1	
Read/Write	R	R	R	R	R	R	R	R

Bit 7 PWRFAILZ:

0 = indicates that the PWRFAIL_SNS input voltage is above the 1-V threshold.

1 = indicates that the PWRFAIL_SNS input voltage is below the 1-V threshold.

Bit 6 LOWBATTZ:

0 = indicates that the LOWBATT_SNS input voltage is above the 1-V threshold.

1 = indicates that the LOWBATT_SNS input voltage is below the 1-V threshold.

Bit 5 PGOODZ VDCDC1:

0 = indicates that the VDCDC1 converter output voltage is within its nominal range. This bit is zero if the VDCDC1 converter is disabled.

1 = indicates that the VDCDC1 converter output voltage is below its target regulation voltage

Bit 4 PGOODZ VDCDC2:

0 = indicates that the VDCDC2 converter output voltage is within its nominal range. This bit is zero if the VDCDC2 converter is disabled.

1 = indicates that the VDCDC2 converter output voltage is below its target regulation voltage

Bit 3 PGOODZ VDCDC3: .

0 = indicates that the VDCDC3 converter output voltage is within its nominal range. This bit is zero if the VDCDC3 converter is disabled and during a DVM controlled output voltage transition

1 = indicates that the VDCDC3 converter output voltage is below its target regulation voltage

Bit 2 PGOODZ LDO2:

0 = indicates that the LDO2 output voltage is within its nominal range. This bit is zero if LDO2 is disabled.

1 = indicates that LDO2 output voltage is below its target regulation voltage

Bit 1 PGOODZ LDO1

0 = indicates that the LDO1 output voltage is within its nominal range. This bit is zero if LDO1 is disabled.

1 = indicates that the LDO1 output voltage is below its target regulation voltage

MASK. Register Address: 02h (read/write) Default Value: C0h

MASK	B7	B6	B5	B4	B3	B2	B1	B0
Bit name and function	MASK PWRFAILZ	MASK LOWBATTZ	MASK VDCDC1	MASK VDCDC2	MASK VDCDC3	MASK LDO2	MASK LDO1	
Default	1	1	0	0	0	0	0	0
Default value loaded by:	UVLO	UVLO	UVLO	UVLO	UVLO	UVLO	UVLO	
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	

The MASK register can be used to mask particular fault conditions from appearing at the $\overline{\text{INT}}$ pin. MASK<n> = 1 masks PGOODZ<n>.

REG_CTRL. Register Address: 03h (read/write) Default Value: FFh

The REG_CTRL register is used to disable or enable the power supplies via the serial interface. The contents of the register are logically AND'ed with the enable pins to determine the state of the supplies. A UVLO condition resets the REG_CTRL to 0xFF, so the state of the supplies defaults to the state of the enable pin. The REG_CTRL bits are automatically reset to default when the corresponding enable pin is low.

REG_CTRL	B7	B6	B5	B4	B3	B2	B1	B0
Bit name and function			VDCDC1 ENABLE	VDCDC2 ENABLE	VDCDC3 ENABLE	LDO2 ENABLE	LDO1 ENABLE	
Default	1	1	1	1	1	1	1	1
Set by signal			DCDC1_ENZ	DCDC2_ENZ	DCDC3_ENZ	LDO_ENZ	LDO_ENZ	
Default value loaded by:			UVLO	UVLO	UVLO	UVLO	UVLO	
Read/Write			R/W	R/W	R/W	R/W	R/W	

Bit 5 VDCDC1 ENABLE

DCDC1 Enable. This bit is logically AND'ed with the state of the DCDC1_EN pin to turn on the DCDC1 converter. Reset to 1 by a UVLO condition, the bit can be written to 0 or 1 via the serial interface. The bit is reset to 1 when the pin DCDC1_EN is pulled to GND, allowing DCDC1 to turn on when DCDC1_EN returns high.

Bit 4 VDCDC2 ENABLE

DCDC2 Enable. This bit is logically AND'ed with the state of the DCDC2_EN pin to turn on the DCDC2 converter. Reset to 1 by a UVLO condition, the bit can be written to 0 or 1 via the serial interface. The bit is reset to 1 when the pin DCDC2_EN is pulled to GND, allowing DCDC2 to turn on when DCDC2_EN returns high.

Bit 3 VDCDC3 ENABLE

DCDC3 Enable. This bit is logically AND'ed with the state of the DCDC3_EN pin to turn on the DCDC3 converter. Reset to 1 by a UVLO condition, the bit can be written to 0 or 1 via the serial interface. The bit is reset to 1 when the pin DCDC3_EN is pulled to GND, allowing DCDC3 to turn on when DCDC3_EN returns high.

Bit 2 LDO2 ENABLE

LDO2 Enable. This bit is logically AND'ed with the state of the LDO2_EN pin to turn on LDO2. Reset to 1 by a UVLO condition, the bit can be written to 0 or 1 via the serial interface. The bit is reset to 1 when the pin LDO_EN is pulled to GND, allowing LDO2 to turn on when LDO_EN returns high.

Bit 1 LDO1 ENABLE

LDO1 Enable. This bit is logically AND'ed with the state of the LDO1_EN pin to turn on LDO1. Reset to 1 by a UVLO condition, the bit can be written to 0 or 1 via the serial interface. The bit is reset to 1 when the pin LDO_EN is pulled to GND, allowing LDO1 to turn on when LDO_EN returns high.

CON_CTRL. Register Address: 04h (read/write) Default Value: B1h

CON_CTRL	B7	B6	B5	B4	B3	B2	B1	B0
Bit name and function	DCDC2 PHASE1	DCDC2 PHASE0	DCDC3 PHASE1	DCDC3 PHASE0	LOW RIPPLE	FPWM DCDC2	FPWM DCDC1	FPWM DCDC3
Default	1	0	1	1	0	0	0	0
Default value loaded by:	UVLO	UVLO	UVLO	UVLO	UVLO	UVLO	UVLO	UVLO
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

The CON_CTRL register is used to force any or all of the converters into forced PWM operation, when low output voltage ripple is vital. It is also used to control the phase shift between the three converters in order to minimize the input rms current, hence reduce the required input blocking capacitance. The DCDC1 converter is taken as the reference and consequently has a fixed zero phase shift.

CON_CTRL<7:6>	DCDC2 CONVERTER DELAYED BY
00	zero
01	1/4 cycle
10	**1/2 cycle**
11	3/4 cycle

CON_CTRL<5:4>	DCDC3 CONVERTER DELAYED BY
00	zero
01	1/4 cycle
10	1/2 cycle
11	**3/4 cycle**

Bit 3 LOW RIPPLE:
- 0 = PFM mode operation optimized for high efficiency for all converters
- 1 = PFM mode operation optimized for low output voltage ripple for all converters

Bit 2 FPWM DCDC2:
- 0 = DCDC2 converter operates in PWM / PFM mode
- 1 = DCDC2 converter is forced into fixed frequency PWM mode

Bit 1 FPWM DCDC1:
- 0 = DCDC1 converter operates in PWM / PFM mode
- 1 = DCDC1 converter is forced into fixed frequency PWM mode

Bit 0 FPWM DCDC3:
- 0 = DCDC3 converter operates in PWM / PFM mode
- 1 = DCDC3 converter is forced into fixed frequency PWM mode

CON_CTRL2. Register Address: 05h (read/write) Default Value: 40h

CON_CTRL2	B7	B6	B5	B4	B3	B2	B1	B0
Bit name and function	GO	Core adj allowed				DCDC2 discharge	DCDC1 discharge	DCDC3 discharge
Default	0	1	0	0	0	0	0	0
Default value loaded by:	UVLO + DONE	RESET(1)				UVLO	UVLO	UVLO
Read/Write	R/W	R/W				R/W	R/W	R/W

The CON_CTRL2 register can be used to take control the inductive converters.

RESET(1): CON_CTRL2[6] is reset to its default value by one of these events:

- undervoltage lockout (UVLO)
- HOT_RESET pulled low
- RESPWRON active
- VRTC below threshold

Bit 7 GO:

0 = no change in the output voltage for the DCDC1 converter

1 = the output voltage of the DCDC1 converter is changed to the value defined in DEFCORE with the slew rate defined in DEFSLEW. This bit is automatically cleared when the DVM transition is complete. The transition is considered complete in this case when the desired output voltage code has been reached, not when the VDCDC1 output voltage is actually in regulation at the desired voltage.

Bit 6 CORE ADJ Allowed:

0 = the output voltage is set with the I^2C register

1 = DEFDCDC1 is either connected to GND or VCC or an external voltage divider. When connected to GND or VCC, VDCDC1 defaults to 1.2 V or 1.6 V respectively at start-up

Bit 2– 0 0 = the output capacitor of the associated converter is not actively discharged when the converter is disabled

1 = the output capacitor of the associated converter is actively discharged when the converter is disabled. This decreases the fall time of the output voltage at light load

DEFCORE. Register Address: 06h (read/write Default Value: 14h/1Eh

DEFCORE	B7	B6	B5	B4	B3	B2	B1	B0
Bit name and function				CORE4	CORE3	CORE2	CORE1	CORE0
Default	0	0	0	1	DEFDCDC1	DEFDCDC1	DEFDCDC1	DEFDCDC1
Default value loaded by:				RESET(1)	RESET(1)	RESET(1)	RESET(1)	RESET(1)
Read/Write				R/W	R/W	R/W	R/W	R/W

RESET(1): DEFCORE is reset to its default value by one of these events:
- undervoltage lockout (UVLO)
- $\overline{\text{HOT\_RESET}}$ pulled low
- $\overline{\text{RESPWRON}}$ active
- VRTC below threshold

CORE4	CORE3	CORE2	CORE1	CORE0	VDCDC1		CORE4	CORE3	CORE2	CORE1	CORE0	VDCDC1
0	0	0	0	0	0.8 V		1	0	0	0	0	1.2 V
0	0	0	0	1	0.825 V		1	0	0	0	1	1.225 V
0	0	0	1	0	0.85 V		1	0	0	1	0	1.25 V
0	0	0	1	1	0.875 V		1	0	0	1	1	1.275 V
0	0	1	0	0	0.9 V		1	0	1	0	0	1.3 V
0	0	1	0	1	0.925 V		1	0	1	0	1	1.325 V
0	0	1	1	0	0.95 V		1	0	1	1	0	1.35 V
0	0	1	1	1	0.975 V		1	0	1	1	1	1.375 V
0	1	0	0	0	1 V		1	1	0	0	0	1.4 V
0	1	0	0	1	1.025 V		1	1	0	0	1	1.425 V
0	1	0	1	0	1.05 V		1	1	0	1	0	1.45 V
0	1	0	1	1	1.075 V		1	1	0	1	1	1.475 V
0	1	1	0	0	1.1 V		1	1	1	0	0	1.5 V
0	1	1	0	1	1.125 V		1	1	1	0	1	1.525 V
0	1	1	1	0	1.15 V		1	1	1	1	0	1.55 V
0	1	1	1	1	1.175 V		1	1	1	1	1	1.6 V

DEFSLEW. Register Address: 07h (read/write) Default Value: 06h

DEFSLEW	**B7**	**B6**	**B5**	**B4**	**B3**	**B2**	**B1**	**B0**
Bit name and function						SLEW2	SLEW1	SLEW0
Default						1	1	0
Default value loaded by:						UVLO	UVLO	UVLO
Read/Write						R/W	R/W	R/W

SLEW2	**SLEW1**	**SLEW0**	**VDCDC1 SLEW RATE**
0	0	0	0.225 mV/µs
0	0	1	0.45 mV/µs
0	1	0	0.9 mV/µs
0	1	1	1.8 mV/µs
1	0	0	3.6 mV/µs
1	0	1	7.2 mV/µs
1	**1**	**0**	**14.4 mV/µs**
1	1	1	Immediate

LDO_CTRL. Register Address: 08h (read/write) Default Value: set with DEFLDO1 and DEFLDO2

LDO_CTRL	B7	B6	B5	B4	B3	B2	B1	B0
Bit name and function	RSVD	LDO2_2	LDO2_1	LDO2_0	RSVD	LDO1_2	LDO1_1	LDO1_0
Default		DEFLDOx	DEFLDOx	DEFLDOx		DEFLDOx	DEFLDOx	DEFLDOx
Default value loaded by:		UVLO	UVLO	UVLO		UVLO	UVLO	UVLO
Read/Write		R/W	R/W	R/W		R/W	R/W	R/W

The LDO_CTRL registers can be used to set the output voltage of LDO1 and LDO2. LDO_CTRL[7] and LDO_CTRL[3] are reserved and should always be written to **0**.

The default voltage is set with DEFLDO1 and DEFLDO2 pins as described in Table 3.

LDO2_2	LDO2_1	LDO2_0	LDO2 OUTPUT VOLTAGE		LDO1_2	LDO1_1	LDO1_0	LDO1 OUTPUT VOLTAGE
0	0	0	1.05 V		0	0	0	1 V
0	0	1	1.2 V		0	0	1	1.1 V
0	1	0	1.3 V		0	1	0	1.3 V
0	1	1	1.8 V		0	1	1	2.1 V
1	0	0	2.5 V		1	0	0	2.2 V
1	0	1	2.8 V		1	0	1	2.6 V
1	1	0	3.0 V		1	1	0	2.8 V
1	1	1	3.3 V		1	1	1	3.15 V

DESIGN PROCEDURE

Inductor Selection for the DC-DC Converters

Each of the converters in the TPS650231 typically use a 2.2 µH output inductor. Larger or smaller inductor values are used to optimize the performance of the device for specific operation conditions. The selected inductor has to be rated for its dc resistance and saturation current. The dc resistance of the inductance influences directly the efficiency of the converter. Therefore, an inductor with lowest dc resistance should be selected for highest efficiency.

For a fast transient response, a 2.2-µH inductor in combination with a 22-µF output capacitor is recommended.

Equation 4 calculates the maximum inductor current under static load conditions. The saturation current of the inductor should be rated higher than the maximum inductor current as calculated with Equation 4. This is needed because during heavy load transient the inductor current rises above the value calculated under Equation 4.

$$\Delta I_L = Vout \times \frac{1 - \frac{Vout}{Vin}}{L \times f} \qquad (4)$$

$$I_{Lmax} = I_{outmax} + \frac{\Delta I_L}{2} \qquad (5)$$

with:

f = Switching Frequency (2.25 MHz typical)
L = Inductor Value
ΔI_L = Peak-to-Peak inductor ripple current
I_{LMAX} = Maximum Inductor current

The highest inductor current occurs at maximum Vin.

Open core inductors have a soft saturation characteristic, and they can usually handle higher inductor currents versus a comparable shielded inductor.

A more conservative approach is to select the inductor current rating just for the maximum switch current of the TPS650231 (2 A for the VDCDC1 and VDCDC2 converters, and 1.5 A for the VDCDC3 converter). The core material from inductor to inductor differs and has an impact on the efficiency especially at high switching frequencies.

See Table 4 and the typical applications for possible inductors.

Table 4. Tested Inductors

DEVICE	INDUCTOR VALUE	TYPE	COMPONENT SUPPLIER
All Converters	2.2 µH	LPS4012-222LMB	Coilcraft
	2.2 µH	VLCF4020T-2R2N1R7	TDK
For DCDC2 or DCDC3	2.2 µH	LQH32PN2R2NN0	Murata
	2.2 µH	PSI25201T-2R2	Cyntec
For DCDC1	1.5 µH	LQH32PN1R5NN0	Murata

Output Capacitor Selection

The advanced Fast Response voltage mode control scheme of the inductive converters implemented in the TPS650231 allow the use of small ceramic capacitors with a typical value of 10 µF for each converter without having large output voltage under and overshoots during heavy load transients. Ceramic capacitors having low ESR values have the lowest output voltage ripple and are recommended. See Table 5 for recommended components.

If ceramic output capacitors are used, the capacitor RMS ripple current rating always meets the application requirements. Just for completeness, the RMS ripple current is calculated as:

$$I_{RMSCout} = V_{out} \times \frac{1 - \frac{V_{out}}{V_{in}}}{L \times f} \times \frac{1}{2 \times \sqrt{3}} \tag{6}$$

At nominal load current, the inductive converters operate in PWM mode. The overall output voltage ripple is the sum of the voltage spike caused by the output capacitor ESR plus the voltage ripple caused by charging and discharging the output capacitor:

$$\Delta V_{out} = V_{out} \times \frac{1 - \frac{V_{out}}{V_{in}}}{L \times f} \times \left(\frac{1}{8 \times C_{out} \times f} + ESR \right) \tag{7}$$

Where the highest output voltage ripple occurs at the highest input voltage Vin.

At light load currents, the converters operate in PSM and the output voltage ripple is dependent on the output capacitor value. The output voltage ripple is set by the internal comparator delay and the external capacitor. The typical output voltage ripple is less than 1% of the nominal output voltage.

Input Capacitor Selection

Because of the nature of the buck converter having a pulsating input current, a low ESR input capacitor is required for best input voltage filtering and minimizing the interference with other circuits caused by high input voltage spikes. Each dc-dc converter requires a 10-µF ceramic input capacitor on its input pin VINDCDCx. The input capacitor is increased without any limit for better input voltage filtering. The VCC pin is separated from the input for the dc-dc converters. A filter resistor of up to 10R and a 1-µF capacitor is used for decoupling the VCC pin from switching noise. Note that the filter resistor may affect the UVLO threshold since up to 3 mA can flow via this resistor into the VCC pin when all converters are running in PWM mode.

Table 5. Possible Capacitors

CAPACITOR VALUE	CASE SIZE	COMPONENT SUPPLIER	COMMENTS
22 µF	0805	TDK C2012X5R0J226MT	Ceramic
22µF	0805	Taiyo Yuden JMK212BJ226MG	Ceramic
10 µF	0805	Taiyo Yuden JMK212BJ106M	Ceramic
10 µF	0805	TDK C2012X5R0J106M	Ceramic
10 µF	0603	Taiyo Yuden JMK107BJ106	Ceramic

Output Voltage Selection

The DEFDCDC1, DEFDCDC2 and DEFDCDC3 pins are used to set the output voltage for each step-down converter. For DEFDCDC1 and DEFDCDC3 there are default voltages defined when the pin is tied to a logic low or logic high signal. See Table 6for the default voltages if the pins are pulled to GND or to Vcc. If a different voltage is needed, an external resistor divider can be added to the DEFDCDCx pin as shown in Figure 36.

The output voltage of VDCDC1 is set with the I^2C interface. If the voltage is changed from the default, using the DEFCORE register, the output voltage only depends on the register value. Any resistor divider at DEFDCDC1 will not change the voltage set with the register. It is not recommended to change the divider ratio of a resistor divider connected at DEFDCDC1 or DEFDCDC3 during operation as the internal logic may detect a logic high signal in error during the change from a high voltage to a lower voltage and will scale the output to the voltage defined by DEFDCDCx = HIGH. As DEFDCDC2 does not have these default fixed voltages, the resistor divider can be changed during operation.

Table 6.

PIN	LEVEL	DEFAULT OUTPUT VOLTAGE
DEFDCDC1	VCC	1.6 V
	GND	1.2 V
DEFDCDC3	VCC	3.3 V
	GND	1.8 V

This function is not available on the DCDC2 converter. DEFDCDC2 always needs to be connected to a resistive divider as shown below.

Using an external resistor divider at DEFDCDCx:

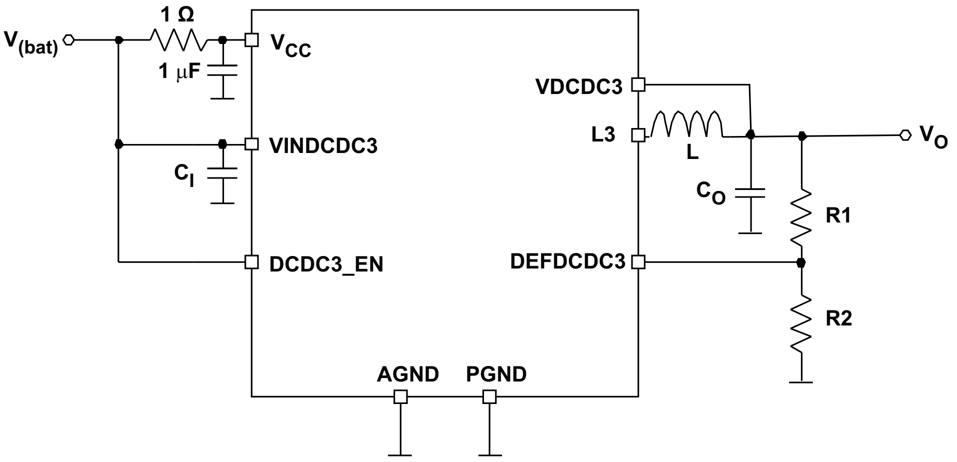


Figure 36. External Resistor Divider

When a resistor divider is connected to DEFDCDCx, the output voltage can be set from 0.6 V up to the input voltage $V_{(bat)}$. The total resistance (R1+R2) of the voltage divider should be kept in the 1-MΩ range in order to maintain a high efficiency at light load.

$V_{(DEFDCDCx)} = 0.6$ V

$$V_{OUT} = V_{DEFDCDCx} \text{ x } \frac{R1 + R2}{R2} \qquad R1 = R2 \text{ x } \left(\frac{V_{OUT}}{V_{DEFDCDCx}} \right) - R2 \tag{8}$$

VRTC Output

It is recommended that a 4.7-µF (minimum) capacitor be added to the VRTC pin.

LDO1 and LDO2

The LDOs in the TPS650231 are general-purpose LDOs which are stable using ceramics capacitors. The minimum output capacitor required is 2.2 µF. The LDOs output voltage can be changed to different voltages between 1 V and 3.3 V using the I^2C interface. The supply voltage for the LDOs needs to be connected to the VINLDO pin, giving the flexibility to connect the lowest voltage available in the system and provides the highest efficiency.

TRESPWRON

This is the input to a capacitor that defines the reset delay time after the voltage at VRTC rises above 2.52 V. The timing is generated by charging and discharging the capacitor with a current of 2 µA between a threshold of 0.25 V and 1 V for 128 cycles. A 1-nF capacitor gives a delay time of 100 ms.

$$t_{(reset)} = 2 \text{ x } 128 \text{ x } \left(\frac{(1\text{ V} - 0.25\text{ V}) \text{ x } C_{(reset)}}{2\ \mu\text{A}} \right) \tag{9}$$

Where:

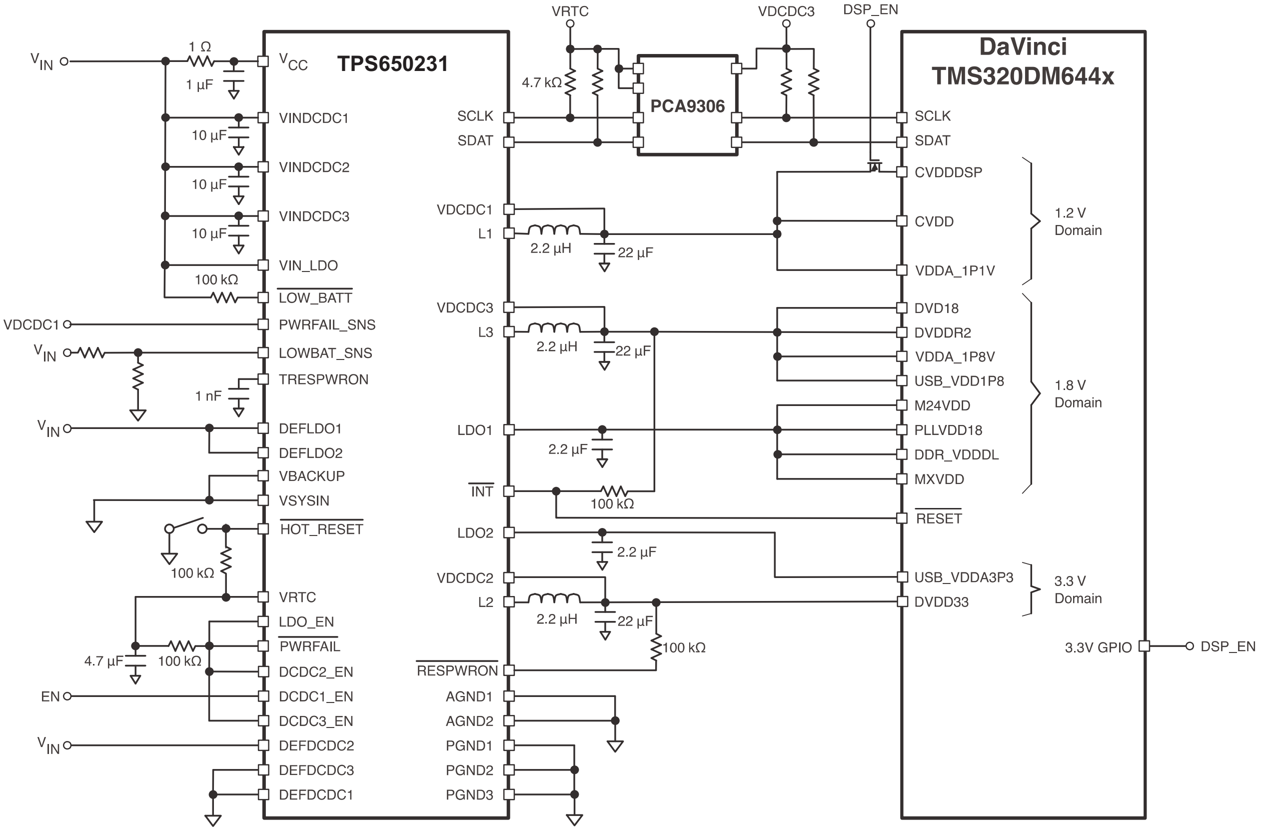
$t_{(reset)}$ is the reset delay time
$C_{(reset)}$ is the capacitor connected to the TRESPWRON pin

V_{CC}-Filter

An RC filter connected at the VCC input is used to keep noise from the internal supply for the bandgap and other analog circuitry. A typical value of 1 Ω and 1 µF is used to filter the switching spikes, generated by the dc-dc converters. A larger resistor than 10 Ω should not be used because the current into VCC of up to 3 mA causes a voltage drop at the resistor causing the undervoltage lockout circuitry connected at VCC internally to switch off too early.

APPLICATION INFORMATION

Typical Configuration for the Texas Instruments® TMS320DM644x DaVinci Processors



Reset Condition of DCDC1

If DEFDCDC1 is connected to ground and DCDC1_EN is pulled high after VINDCDC1 is applied, the output voltage of DCDC1 defaults to 1.225V instead of 1.2V (high by 2%). Figure 37 illustrates the problem.

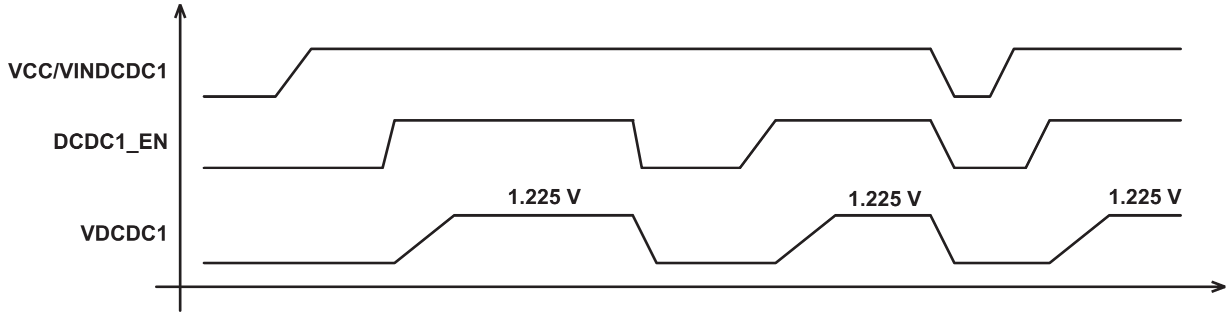


Figure 37. Default DCDC1

Workaround 1: Tie DCDC1_EN to VINDCDC1 (Figure 38)

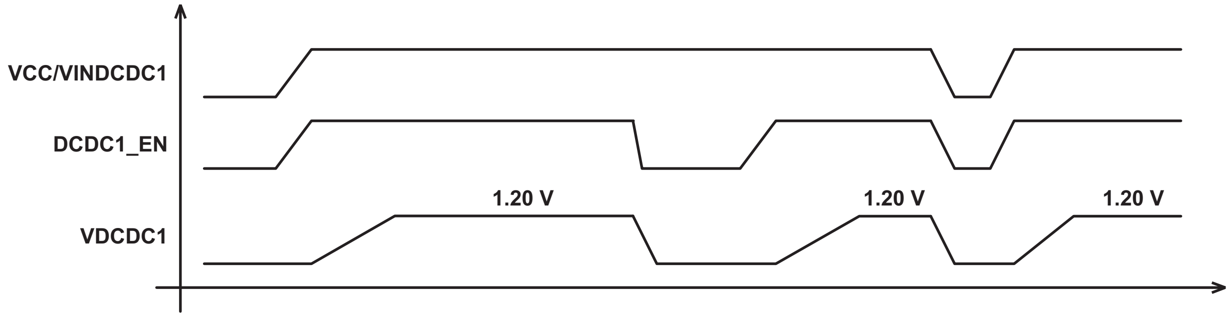


Figure 38. Workaround 1

Workaround 2: Write the correct voltage to the DEF_CORE register via I^2C. This can be done before or after the converter is enabled. If written before the enable, the only bit changed is DEF_CORE[0]. The voltage will be 1.2V, however, when the enable is pulled high (Figure 39).

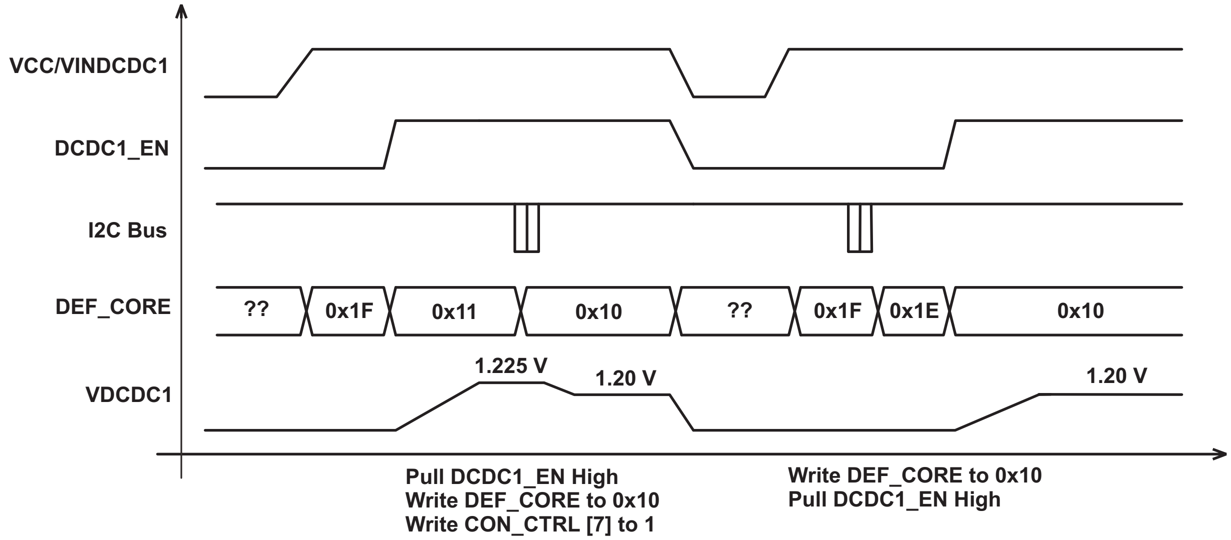


Figure 39. Workaround 2

Workaround 3: Generate a $\overline{\text{HOT\_RESET}}$ after enabling DCDC1 (Figure 40)

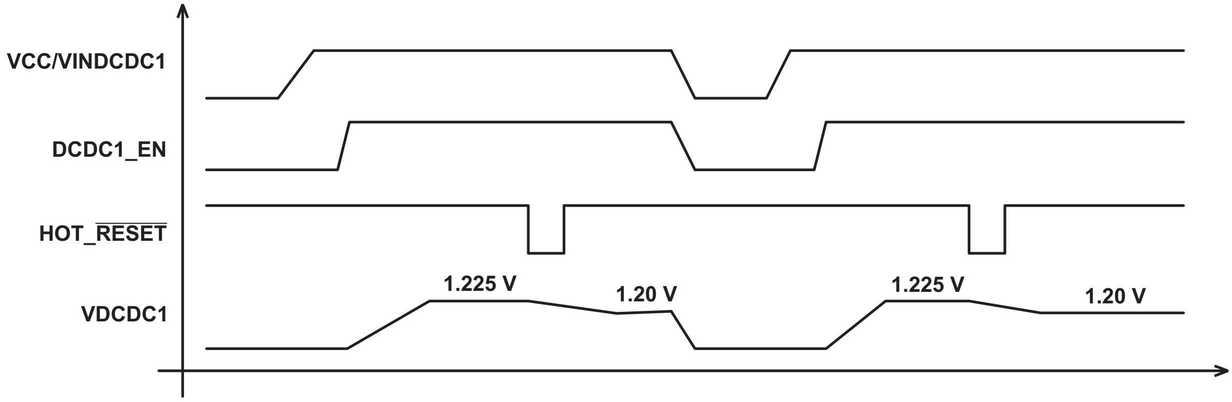


Figure 40. Workaround 3

DIFFERENCES OF TPS650231 VERSUS TPS65023 and TPS65023B

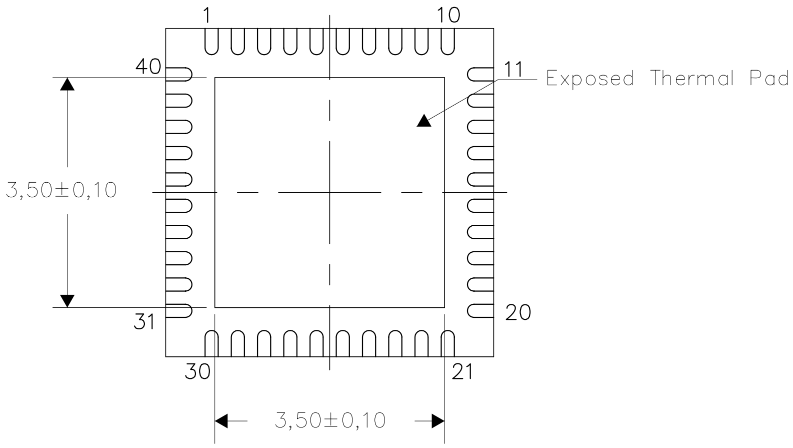
ITEM	DESCRIPTION	TPS65023	TPS65023B	TPS650231
V_{IH}	High level input voltage for the SDAT pin	Minimum 1.3V	Minimum 1.65V; Vcc = 2.5V to 5.25V	Minimum 1.65V; Vcc = 2.5V to 5.25V
V_{IH}	High level input voltage for the SCLK pin	Minimum 1.3V	Minimum 1.4V, Vcc = 2.5V to 5.25V	Minimum 1.4V, Vcc = 2.5V to 5.25V
V_{IL}	Low level input voltage for SCLK and SDAT pin	Maximum 0.4V	Maximum 0.35V	Maximum 0.35V
$t_{h(DATA)}$	Data input hold time	Minimum 300ns	Minimum 100ns	Minimum 100ns
$t_{su(DATA)}$	Data input setup time	Minimum 300ns	Minimum 100ns	Minimum 100ns
	LDO1 voltage for setting LDO1_[2..0] = 011	1.8V	1.8V	2.1V
	DEFDCDC2 pin functionality	1) DEFDCDC2=LOW: Vo=1.8V 2) DEFDCDC2=HIGH: Vo=3.3V 3) 0.6V feedback input	1) DEFDCDC2=LOW: Vo=1.8V 2)DEFDCDC2=HIGH: Vo=3.3V 3)0.6V feedback input	0.6V feedback input only (allows voltage scaling with external resistor divider without restrictions)

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No-Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.

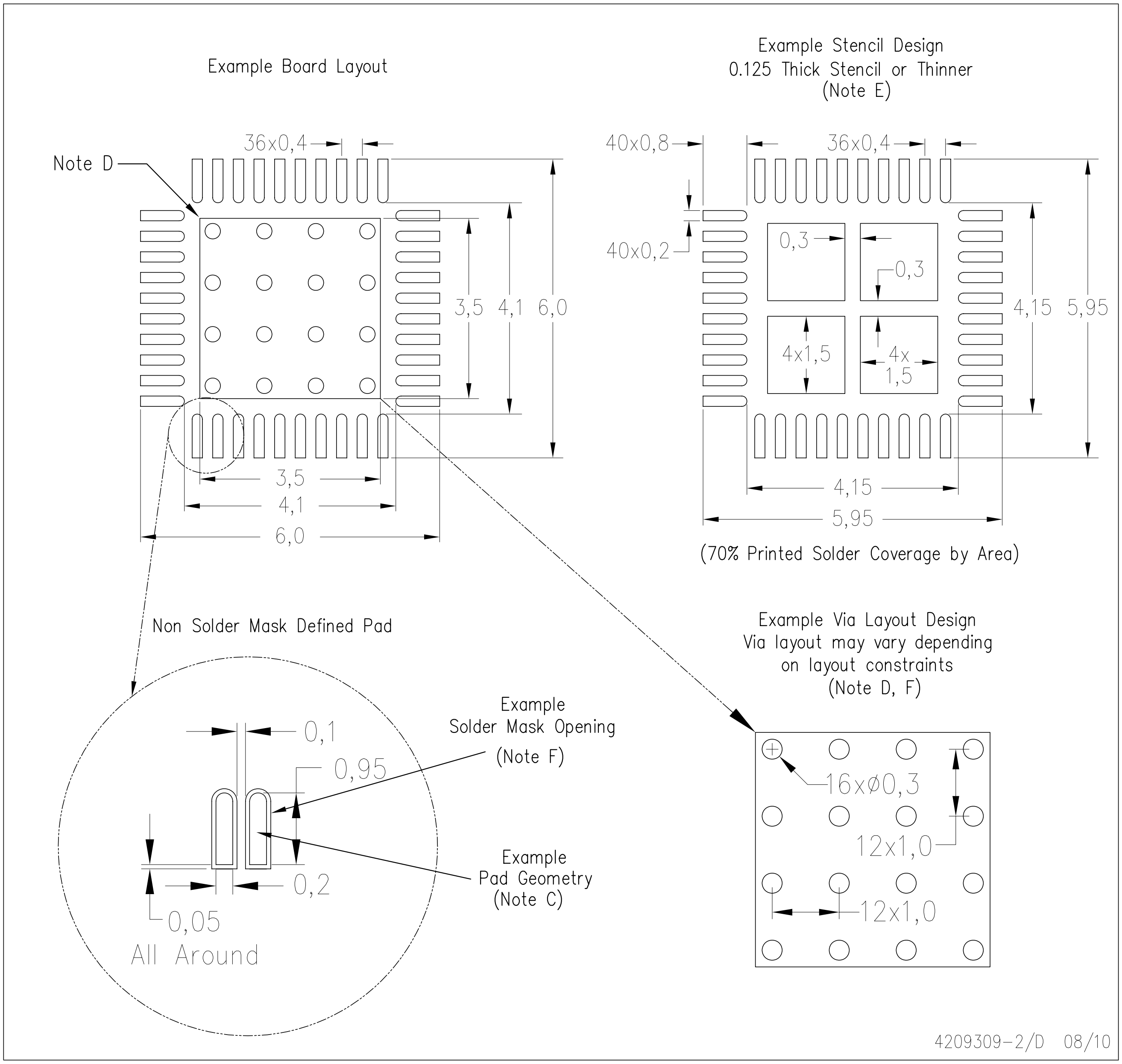


Bottom View

NOTE: All linear dimensions are in millimeters

Exposed Thermal Pad Dimensions

RSB (S–PWQFN–N40) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Publication IPC–7351 is recommended for alternate designs.
- D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat–Pack Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>.
- E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
- F. Customers should contact their board fabrication site for recommended solder mask tolerances and via tenting recommendations for vias placed in the thermal pad.

PACKAGING INFORMATION

Orderable Device	Status [1]	Package Type	Package Drawing	Pins	Package Qty	Eco Plan [2]	Lead/ Ball Finish	MSL Peak Temp [3]	Samples (Requires Login)
TPS650231RSBR	PREVIEW	WQFN	RSB	40	3000	TBD	Call TI	Call TI	Samples Not Available
TPS650231RSBT	PREVIEW	WQFN	RSB	40	250	TBD	Call TI	Call TI	Samples Not Available
TPS650231YFFR	PREVIEW	DSBGA	YFF	49	3000	TBD	Call TI	Call TI	Samples Not Available
TPS650231YFFT	PREVIEW	DSBGA	YFF	49	250	TBD	Call TI	Call TI	Samples Not Available

[1] The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

[2] Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

[3] MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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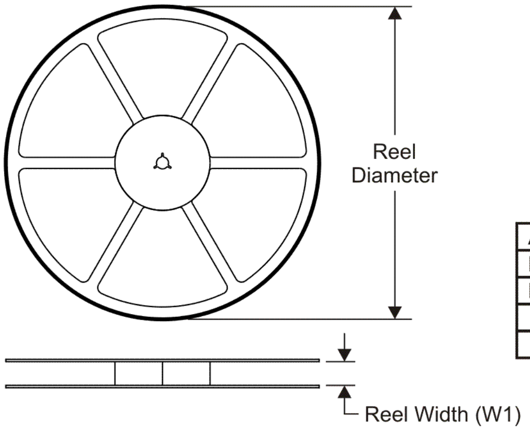
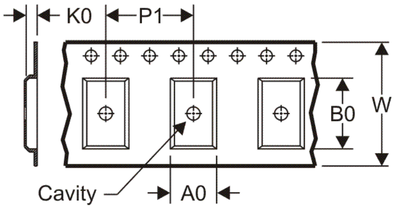
TAPE AND REEL INFORMATION

REEL DIMENSIONS

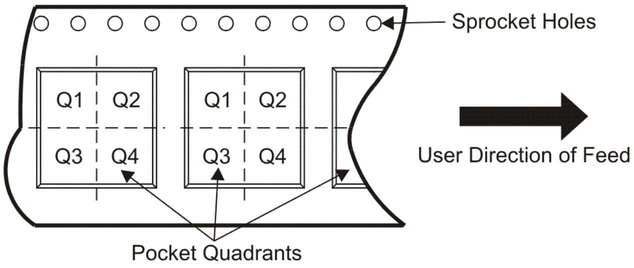


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

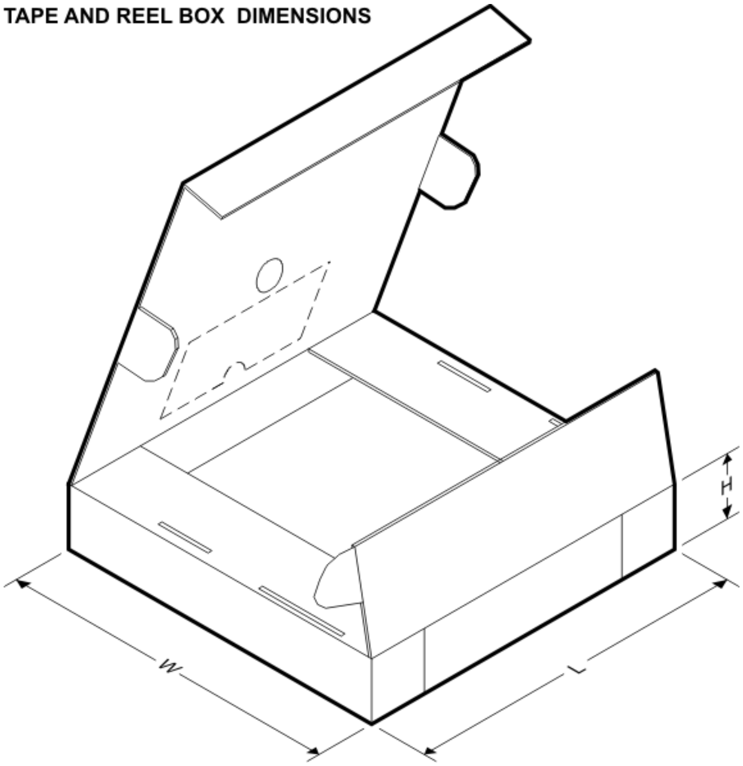
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS650231RSBR	WQFN	RSB	40	3000	330.0	12.4	5.25	5.25	1.1	8.0	12.0	Q2
TPS650231RSBT	WQFN	RSB	40	250	330.0	12.4	5.25	5.25	1.1	8.0	12.0	Q2
TPS650231YFFT	DSBGA	YFF	49	250	180.0	8.4	3.3	3.3	0.75	4.0	8.0	Q1

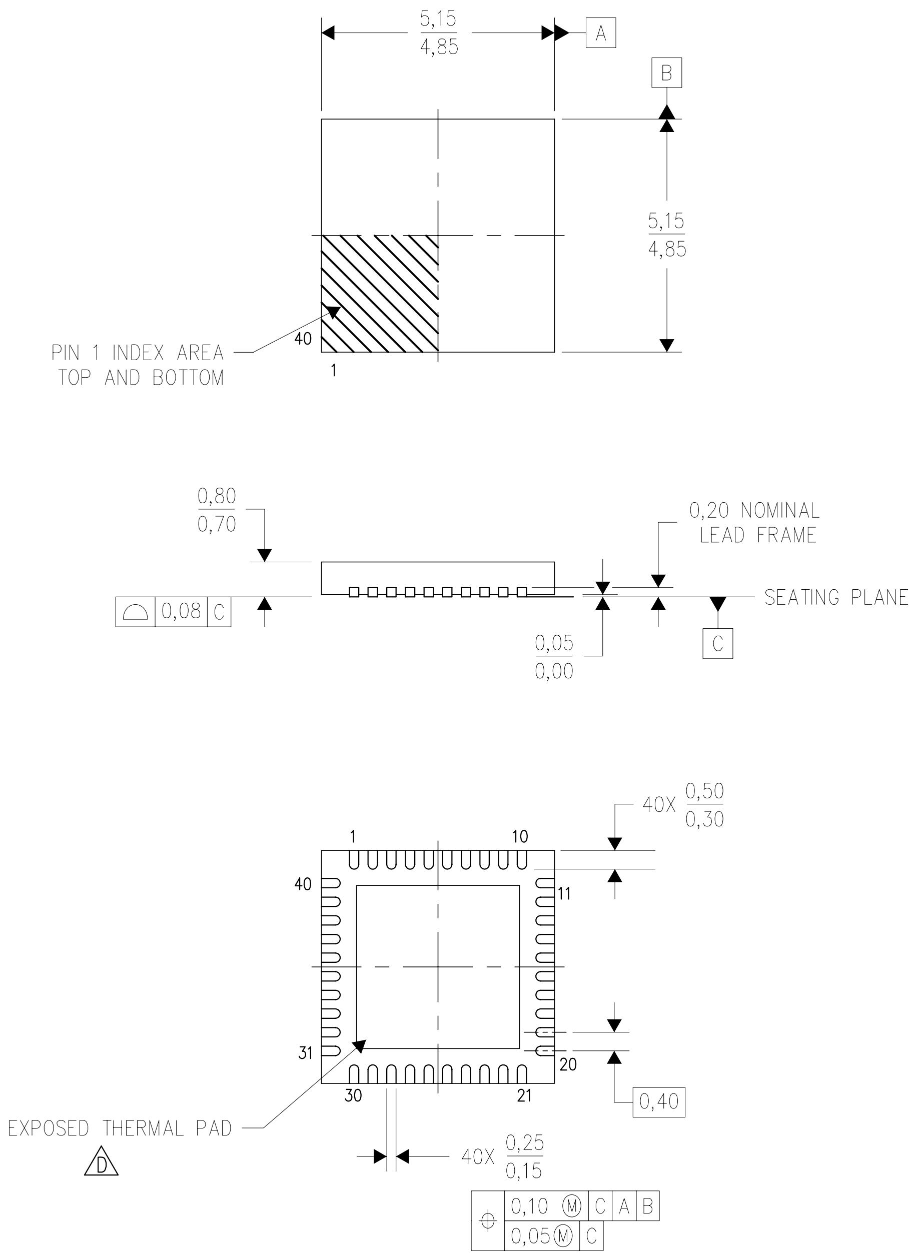
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS650231RSBR	WQFN	RSB	40	3000	340.5	338.1	20.6
TPS650231RSBT	WQFN	RSB	40	250	340.5	338.1	20.6
TPS650231YFFT	DSBGA	YFF	49	250	190.5	212.7	31.8

RSB (S-PWQFN-N40) PLASTIC QUAD FLATPACK NO-LEAD

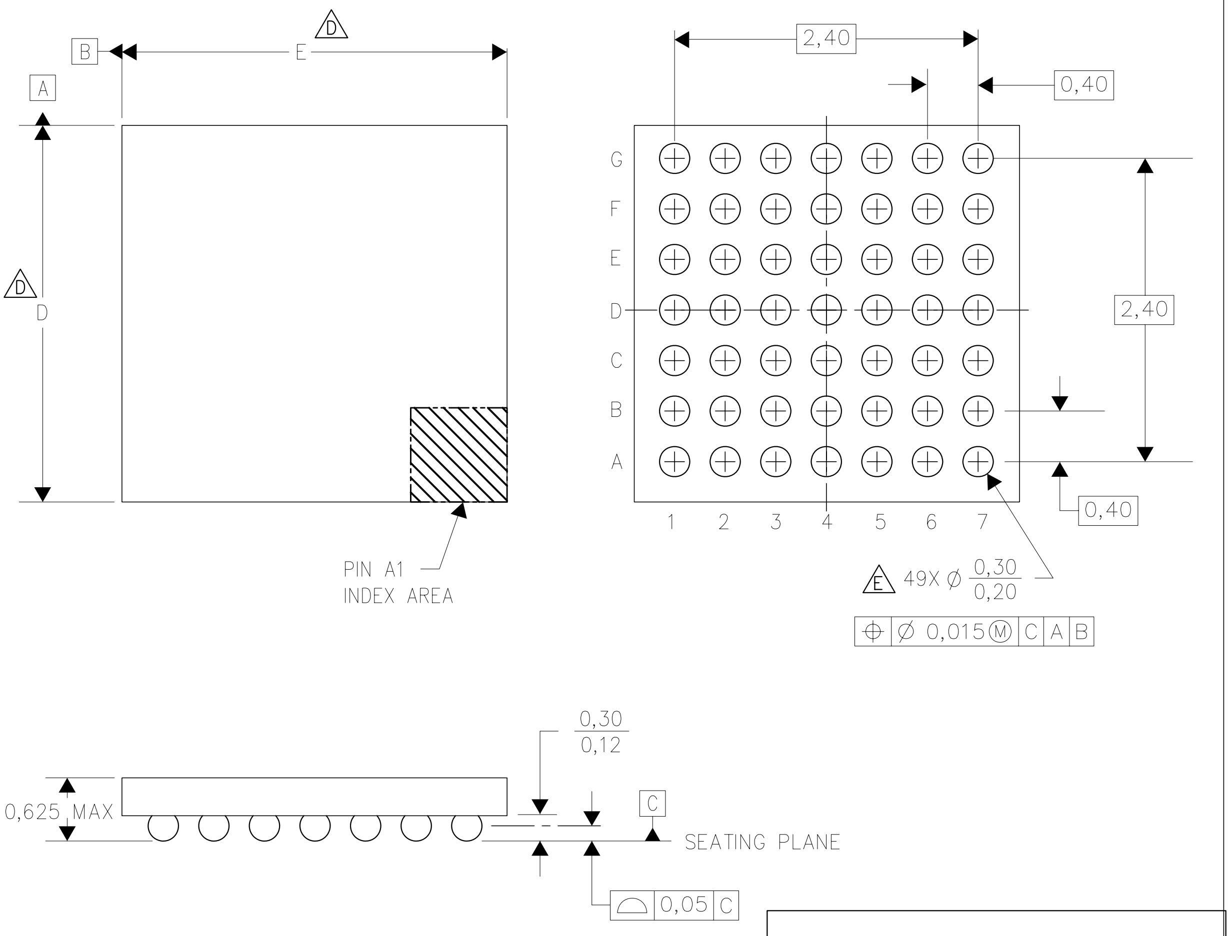


4207182/B 08/10

NOTES:

- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
- B. This drawing is subject to change without notice.
- C. QFN (Quad Flatpack No-Lead) Package configuration.
- D. The package thermal pad must be soldered to the board for thermal and mechanical performance. See the Product Data Sheet for details regarding the exposed thermal pad dimensions.

YFF (R–XBGA–N49) DIE–SIZE BALL GRID ARRAY



X: Max = 3132 µm, Min = 3032 µm

Y: Max = 3116 µm, Min = 3016 µm

4207625–16/Y 05/10

NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
- B. This drawing is subject to change without notice.
- C. NanoFree™ package configuration.
- D. Devices in YFF package can have dimension D ranging from 2.73 to 3.45 mm and dimension E ranging from 2.73 to 3.45 mm. To determine the exact package size of a particular device, refer to the device datasheet or contact a local TI representative.
- E. Reference Product Data Sheet for array population. 7 x 7 matrix pattern is shown for illustration only.
- F. This package contains Pb–free balls.

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