TUSB1211
独立 **USB** 收发器芯片

Data Manual

Literature Number: ZHCS133
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内容

图片列表

图表列表

独立 USB 收发器芯片

查询样品: TUSB1211

1 特性

- **USB2.0 PHY** 收发器芯片，可通过 **ULPI** 接口连接 **USB** 控制器，其完全符合：
  - 通用串行总线规范 **2.0** 版
  - ***USB 2.0*** 规范移动附录 **1.3** 版
  - ***UTMI+*** 低引脚接口 ***(ULPI)*** 规范 **1.1** 版
  - ***ULPI 12*** 引脚 ***SDR*** 接口标准
  - ***USB*** 电池充电规范 ***1.1*** 版
- **USB** 电池充电器检测特性
  - 检测功能符合 **USB** 充电规范 **1.1** 版，包括 **ACA** 检测
  - 其它 **DP** 弱上拉电阻器可用于 **DP/DM** 连接性检测
- **DP/DM** 线路外部组件补偿（**TI** 正在申请专利）
- 完整的 **USB OTG** 物理前端支持主机协商协议 **(HNP)** 与会话请求协议 **(SRP)**
- V_{BUS} 过压保护电路系统可在 **–2 V** 至 **20 V** 的电压范围内保护 V_{BUS} 引脚
- 内部 **5 V** 短路保护功能可防止 **DP**、**DM** 与线缆 **ID** 引脚短路连接至 V_{BUS} 引脚
- **ULPI** 接口：
  - **I/O** 接口 **(1.8V)** 针对无端接 **50** Ω 线路阻抗进行了优化
  - **ULPI** 时钟引脚 **(60 MHz)** 可同时支持输入和输出时钟配置
  - 符合 **ULPI** 标准的全面可编程型寄存器集
- 完全工业级工作温度范围：**–40°C** 至 **85°C**
- 采用 **TFBGA36** 焊球封装
- **SOF** 引脚上的 **USB HS** 帧开始时钟输出特性可用于实现另一个应用（如音频）与 **USB** 数据包流的同步
- 可通过 **ULPI** 连接外设、主机或 **OTG** 控制器设备。适用于具有内建控制器内核的便携式设备或系统 **ASIC**。
- 完整的 **HS-USB** 物理前端：
  - 支持高速 **(480 Mbit/s)**、全速 **(12 Mbit/s)** 和低速 **(1.5 Mbit/s)**
  - 集成型锁相环 **(PLL)** 支持 **2** 个时钟频率 **19.2 MHz/26 MHz**
  - 集成型 **45** Ω **±10%** 高速终端电阻器、**1.5 k**Ω 全速器件上拉电阻器以及 **15 k**Ω 主机终端电阻器
  - 集成型收发路径支持并行至串行和串行至并行数据转换
  - **USB** 数据恢复可恢复频率漂移高达 **±500 ppm** 的 **USB** 数据
  - 可在传输时进行位插入，在接受时删除
  - 非归零反转 **(NRZI)** 编码和解码
  - 支持总线复位、挂起、唤醒以及高速检测握手（啁啾声）
  - **HS USB DP/DM** 阻抗可编程性支持外部组件补偿
- **OTG 1.3** 版：
  - 外部 V_{BUS} 开关或充电泵的控制
  - V_{BUS} 故障检测
  - 支持两种会话请求协议 **(SRP)** 方法：数据脉冲与 V_{BUS} 脉冲
  - 集成型 V_{BUS} 检测器与线缆检测 **(ID)**
- 内部上电复位 **(POR)** 电路
- 高灵活系统集成与极低的流耗，针对便携式设备进行了优化

1.1 说明

TUSB1211 是一款 USB2.0 收发器芯片，可通过 ULPI 接口连接 USB 控制器。 它可在主机与外设模式下支持所有 USB2.0 数据速率（高速 480Mbps、全速 12 Mbps 以及低速 1.5Mbps）。 此外，该器件还支持 UART 模式及原有 ULPI 串行模式。

TUSB1211 还支持 USB 电池充电规范 1.1 版，集成的充电器检测模块可感测和控制 DP/DM 线路，检测 ACA（辅助充电适配器），并控制 ID 线路。 ACA 支持将 USB 充电器或充电下行端口及配件同步连接至便携式 OTG 设备。 配置位可帮助 ACA 不可知原有链路通过 ACA 与连接的配件端口正常通信。

此外，TUSB1211 还支持 USB2.0 规范相关 OTG（1.3 版）可选附件 ，包括主机协商协议 (HNP) 和会话请求协议 (SRP)。

TUSB1211 支持 1.8 V 接口电源电压，其可通过 12 引脚 SDR UTMI 低引脚接口 (ULPI) 连接，从而可支持输入时钟与输出时钟模式。

TUSB1211 集成 3.3 V LDO，可灵活地配合电池供电系统或纯 3.3 V 供电系统工作。 主电源与 3.3 V 电源域都可通过外部开关模式转换器供电来提高能效。

TUSB1211 包含 POR 电路，可检测 V_{BAT} 与 V_{DDIO} 引脚上存在的电源。 TUSB1211 可在低功耗模式下禁用或配置，实现节能。

TUSB1211 可防止外露接口 (DPDM/ID) 上的 5 V 或接地意外短路。 该产品还可应对 V_{BUS} 上高达 20 V 的突波。

TUSB1211 不但集成 480 MHz 高性能低抖动 PLL，而且还支持两个时钟配置。 通过必要的链接配置，TUSB1211 可支持 ULPI 输入及输出时钟模式：在输入时钟模式下，TUSB1211 可通过 ULPI 接口时钟引脚获取 60 MHz 的方波时钟；在输出时钟模式下，TUSB1211 可在 19.2 MHz 或 26 MHz 的 REFCLK 下接收方波参考时钟。 频率可通过配置引脚 CFG 提供给 TUSB1211。 如果系统中已经有了参考时钟，该功能就非常有用。

2 Terminal Description

TFBGA36 PACKAGE
(BOTTOM VIEW)

	1	2	3	4	5	6
F	CHRG_ POL	CHRG_ DET	VBAT	VBUS	REFCLK	SOF
E	CHRG_ EN_N	FAULT	REG3V3	GND	DIR	REG1V5
D	DP	GND	ID	PSW	DXT	STP
C	DM	NC(1)	CS_N	RESET_N	GND	DATA7
B	DATA0	VDDIO	CS	CFG	VDDIO	DATA6
A	DATA1	DATA2	DATA3	CLOCK	DATA4	DATA5

(1) NC = Not Connected

(2) The size of the device should be 3.5 mm ±0.1 mm by 3.5 mm ±0.1 mm. Height is 1.0 mm typical 1.15 mm max including the solder balls. The pitch of the device is 0.5 mm. Ball width 0.3 mm ±0.05 mm.

Figure 2-1. TFBGA36 Package - Bottom View

2.1 Terminal Functions

Table 2-1 provides a description of the signals on the TUSB1211 package; some signals are available on multiple pins.

Table 2-1. Terminal Functions

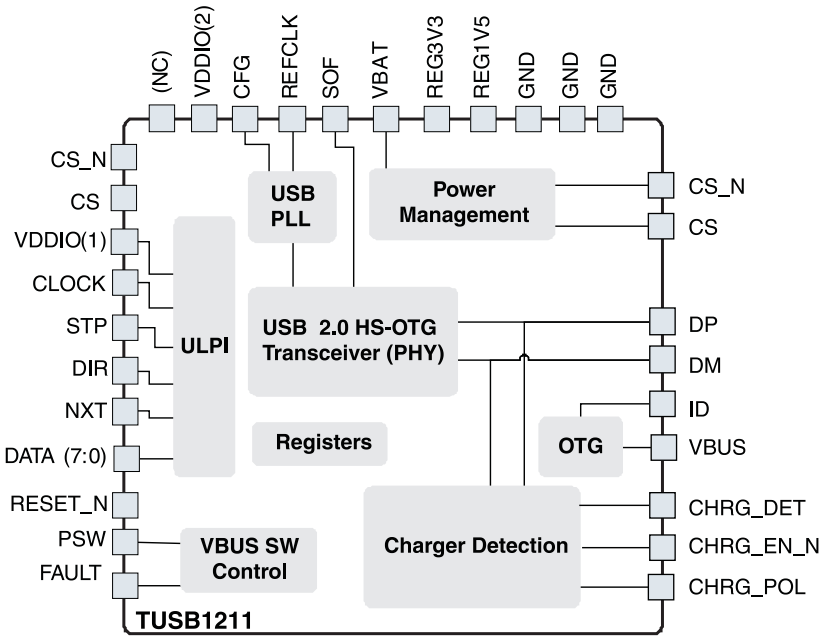
#	PIN(1)	NAME	A/D(2)	TYPE(3)	LEVEL(4)	DESCRIPTION
1	D5	NXT	D	O	V_{DDIO}	ULPI NXT output signal
2	B1	DATA0	D	I/O	V_{DDIO}	ULPI DATA input/output signal synchronized to CLOCK
3	A1	DATA1	D	I/O	V_{DDIO}	ULPI DATA input/output signal synchronized to CLOCK
4	A2	DATA2	D	I/O	V_{DDIO}	ULPI DATA input/output signal synchronized to CLOCK
5	A3	DATA3	D	I/O	V_{DDIO}	ULPI DATA input/output signal synchronized to CLOCK
6	A5	DATA4	D	I/O	V_{DDIO}	ULPI DATA input/output signal synchronized to CLOCK
7	A6	DATA5	D	I/O	V_{DDIO}	ULPI DATA input/output signal synchronized to CLOCK
8	B6	DATA6	D	I/O	V_{DDIO}	ULPI DATA input/output signal synchronized to CLOCK
9	B3	CS	D	I	VDDIO	Active-high chip select pin. When low the IC is in power down and ULPI bus is tri-stated. When high (and CS_N pin iTie to VDDIO if unused.s low) normal operation.
10	E6	REG1V5	A	POWER	V_{DD15}	1.5 V internal LDO output. Connect to external filtering capacitor.
11	C6	DATA7	D	I/O	V_{DDIO}	ULPI DATA input/output signal synchronized to CLOCK
12	B4	CFG	D	I	V_{DDIO}	REFCLK clock frequency configuration pin. Two frequencies are supported: 19.2MHz when 0, or 26MHz when 1.
13	D1	DP	A	I/O	V_{DD33}	DP pin of the USB connector
14	C1	DM	A	I/O	V_{DD33}	DM pin of the USB connector
15	E3	REG3V3	A	POWER	V_{DD33}	3.3 V internal LDO output. Connect to external filtering capacitor.
16	F3	VBAT	A	POWER	V_{BAT}	Input supply voltage or battery source. Nominally 3.3 V to 4.5 V
17	F4	VBUS	A	I/O	V_{BUS}	VBUS pin of the USB connector
18	D3	ID	A	I/O	V_{BUS}	Identification (ID) pin of the USB connector
19	A4	CLOCK	D	I/O	V_{DDIO}	ULPI 60MHz clock on which ULPI data is synchronized. 2 modes are possible: Input Mode: CLOCK defaults as an input (this is the default clock mode) Output Mode: When an input clock is detected on REFCLK pin then CLOCK will change to an output
20	C4	RESET_N	D	I	V_{DDIO}	Active low chip reset pin. Minimum pulse width 100 µs. When low all digital logic (except 32kHz logic required for power-up sequencing and charger detection state-machine) including registers are reset to their default values. ULPI bus is in “ULPI Synchronous mode power-up PLL OFF” state as described in Table14-1. When high normal USB operation.
21	D6	STP	D	I	V_{DDIO}	ULPI STP input signal
22	E5	DIR	D	O	V_{DDIO}	ULPI DIR output signal
23	B5	VDDIO	A	I	V_{DDIO}	External 1.8V supply input for digital I/Os. Connect to external filtering capacitor.
24	B2	VDDIO	A	I	V_{DDIO}	External 1.8V supply input for digital I/Os. Connect to external filtering capacitor.
25	C5	GND	A	GROUND	GND	Ground
26	D2	GND	A	GROUND	GND	Ground
27	E4	GND	A	GROUND	GND	Ground
28	F5	REFCLK	A	I	V_{DDIO}	Reference clock input. Input reference clock frequency must be indicated by CFG pin. Two frequencies are supported: 19.2MHz (when CFG = 0), and 26MHz (when CFG = 1).
29	F6	SOF	D	O	V_{DDIO}	HS USB SOF (Start-Of-Frame) output clock. (feature controlled by SOF_EN bit, disabled and output logic low by default.). HS USB SOF packet rate is 8 kHz
30	C2	NC				Not connected
31	C3	CS_N	D	I	V_{DDIO}	Active-low chip select pin. When high the IC is in power down and ULPI bus is tri-stated. When low (and CS pin is high) normal operation. Tie to GND if unused.
32	E1	CHRG_EN_N	D	I	V_{BAT}	Active low input pin used to enable Battery Charging Detection in Dead Battery Charger Detection mode. This pin is ignored in ACTIVE mode. Connect to GND to activate. Connect to VBAT when charger detection not required
33	E2	FAULT	D	I	V_{BAT}	VBUS fault detector input used as EXTERNALVBUSINDICATOR in TUSB1211. The link must enable VBUS fault detection via the USEEXTERNALVBUSINDICATOR register bit, and the polarity must be set via the INDICATORCOMPLEMENT register bit. INDICATORPASSTHRU bit can be used to qualify FAULT with the internal vbusvalid comparator. Connect to GND if not used. This pin is 5V tolerant.
34	F1	CHRG_POL	D	I	V_{BAT}	When connected to GND then CHRG_DET output pin is active low. When connected to VBAT then CHRG_DET output pin is active high.

(1) Pin = Package Pin coordinate of Figure 2-1
(2) A/D: A = Analog pin, D = Digital pin
(3) TYPE: I = Input pin type, O = Output pin type, I/O = Input/Output pin type, POWER = Power supply pin type, GROUND = Ground type pin
(4) LEVEL = Pin power supply level

Table 2-1. Terminal Functions (continued)

#	PIN(1)	NAME	A/D(2)	TYPE(3)	LEVEL(4)	DESCRIPTION
35	F2	CHRG_DET	D	O	V_{BAT}	When CHRG_POL pin is at GND then CHRG_DET is in active low open-drain mode with external RCHRGDET (100K) connected to VBAT. When CHRG_POL pin is at VBAT then CHRG_DET is in active high open-source mode with external RCHRGDET (100K) connected to GND. This pin is 5V tolerant.
36	D4	PSW	D	O	V_{BAT}	Controls an external, active high, VBUS power switch or charge pump. Open source output on VBAT supply when PSW_OSOD bit is 0 (default), open-drain active-low output when PSW_OSOD bit is 1. Requires an external RPSW (100K) pull down/up resistor to GND/VBAT .

2.2 Block Diagram



3 Electrical Characteristics

3.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

PARAMETER		CONDITIONS	MIN	MAX	UNIT
V_{BAT}	Main battery supply voltage	Continuous	0	5.0	V
	Main battery supply voltage pulsed	The product will have negligible reliability impact for pulsed voltage spikes of 5.5 V for a total (cumulative over lifetime) duration of 5 milliseconds		5.5	V
V_{DDIO}	IO supply voltage	Continuous		1.98	V
	Voltage on any input except V_{DDIO}, V_{BAT}, and V_{BUS} pads	Where V_{DD} represents the voltage applied to the power supply pin associated with the input	–0.3	1.0*V_{DD} + 0.3	V
	DP, DM, ID high voltage short circuit	DP or DM or ID pins short circuited to VBUS supply, in any mode of TUSB1211 operation, continuously for 24hours		5.25	V
	DP, DM, ID low voltage short circuit	DP or DM or ID pins short circuited to GND in any mode of TUSB1211 operation, continuously for 24hours	0		V
	V_{BUS} input		–2	20	V
T_{stg}	Storage temperature range		–55	125	°C
T_A	Ambient temperature range		–40	85	°C
T_J	Junction temperature range	Absolute maximum rating	–40	150	°C

(1) Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

3.2 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{BAT}	Battery supply voltage	VBAT_ACTIVE	2.7	3.6	4.8	V
V_{BAT_CERT}	Battery supply voltage for USB 2.0 compliancy (USB 2.0 certification)	VBAT_CERT	3.15			V
V_{BAT_DB}	Battery supply voltage for charger detect in “dead-battery condition”	VBAT_DB	2.4			V
V_{DDIO}	IO supply voltage	VDDIO_ACTIVE	1.62	1.8	1.95	V
T_A	Ambient temperature range		–40		85	°C
T_J	Junction temperature	For parametric compliance	–40		125	°C

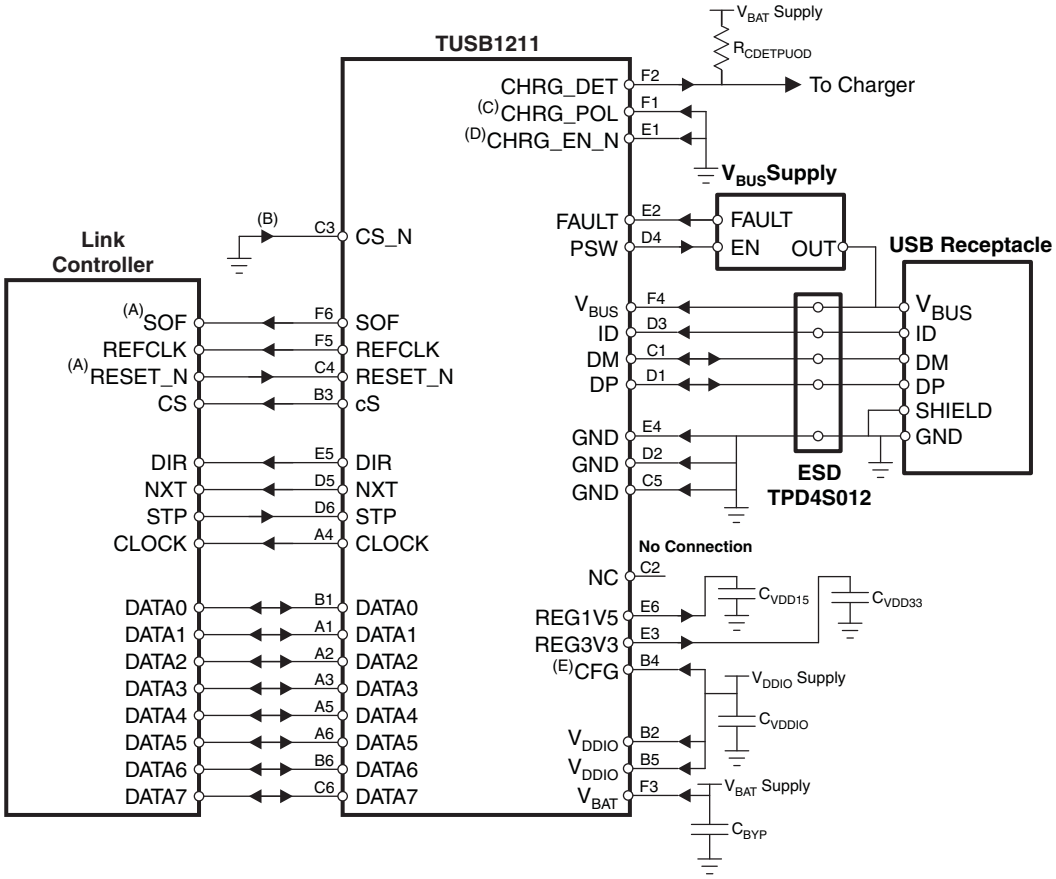
3.3 ESD Electrical Parameters

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
CDM	Charged-Device Model stress voltage (JESD22-C101-A)	All pads			500	V
HBM	Human-Body Model stress voltage (JESD22-A114D)	All pads			2000	V

4 Application Diagram

Figure 4-1 shows the suggested application diagram (Host or OTG, ULPI output-clock mode)



A. Optional: SOF (open if unused); RESET_N (tie to V_{DDIO} if unused)
B. Link controls chip select via CS pin with CS_N at GND. ALternatively, Link may control CS_N pin with CS pin tied to V_{DDIO}.
C. CHRG_DET is active-low (tie CHRG_POL to V_{BAT} for CHRG_DET active high).
D. Dead battery charger detection is enabled (tie CHRG_EN_N to V_{BAT} to disable).
E. CFG tied to V_{DDIO} for 26 MHz input at REFCLK (tie to GND for 19.2 MHz).

Figure 4-1. USB-OTG with ULPI Output Clock

5 Clock System

5.1 USB PLL Reference Clock

The USB PLL block generates the clocks used to synchronize:

- the ULPI interface (60 MHz clock)
- the USB interface (depending on the USB data rate, 480 Mbps, 12 Mbps or 1.5 Mbps)

TUSB1211 requires an external reference clock which is used as an input to the 480MHz USB PLL block. Depending on the clock configuration, this reference clock can be provided either at REFCLK pin or at CLOCK pin.

By default CLOCK pin is configured as an input.

Two clock configurations are possible:

- Input clock configuration (see Section 5.1.1)
- Output clock configuration (see Section 5.1.1)

5.1.1 ULPI Input Clock Configuration

In this mode REFCLK must be externally tied to GND.

CLOCK remains configured as an input.

When the ULPI interface is used in “input clock configuration”, i.e., the 60 MHz ULPI clock is provided to TUSB1211 on CLOCK pin, then this is used as the reference clock for the 480 MHz USB PLL block.

Table 5-1. Electrical Characteristics: CLOCK Input

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
CLOCK input duty cycle		40		60	%
F_{CLOCK} CLOCK nominal frequency			60		MHz
CLOCK input rise/fall time	In % of CLOCK period T_{CLOCK} (= 1/F_{CLOCK})			10	%
CLOCK input frequency accuracy				250	ppm
CLOCK input integrated jitter				600	ps rms

5.1.2 ULPI Output Clock Configuration

In this mode a reference clock must be externally provided on REFCLK pin.

When an input clock is detected on REFCLK pin then CLOCK will automatically change to an output, i.e., 60 MHz ULPI clock is output by TUSB1211 on CLOCK pin.

Two reference clock input frequencies are supported. REFCLK input frequency is communicated to TUSB1211 via a configuration pin, CFG, see F_{REFCLK} in Table 5-2 for frequency correspondence.

TUSB1211 supports square-wave reference clock input only.

Table 5-2. Electrical Characteristics: REFCLK

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
REFCLK input duty cycle		40		60	%
FREFCLK REFCLK nominal frequency	When CFG pin is tied to GND		19.2		MHz
	When CFG pin is tied to V_{DDIO}		26		
REFCLK input rise/fall time	In % of REFCLK period T_{REFCLK} (= 1/F_{REFCLK})			20	%
REFCLK input freq accuracy				250	ppm
REFCLK input integrated jitter				600	ps rms

6 Power Management

This chapter describes the electrical characteristics of the voltage regulators and timing characteristics of the supplies digitally controlled within the TUSB1211.

6.1 Power Consumption

Table 6-1 describes the power consumption depending on the use cases.

Typical power consumption is obtained in nominal operating conditions of TUSB1211.

Table 6-1. Power Consumption

MODE	CONDITIONS	SUPPLY	TYPICAL POWER CONSUMPTION	UNIT
OFF	V_{BAT} = 3.6 V, V_{DDIO} = 1.8 V, CS = 0 V	IV_{BAT}	8	µA
		IV_{DDIO}	1.8	
		I_{TOTAL}	**9.8**	
Suspend	V_{BUS} = 5 V, V_{BAT} = 3.6 V, V_{DDIO} = 1.8 V, VCHRG_EN_N = 0 V, no clock	IV_{BAT}	251	µA
		IV_{DDIO}	21	
		I_{TOTAL}	**272**	
HS USB Mode	V_{BAT} = 3.6 V, V_{DDIO} = 1.8 V, active USB transfer	IV_{BAT}	46.4	mA
		IV_{DDIO}	1.3	
		I_{TOTAL}	**47.7**	
FS USB Mode	V_{BAT} = 3.6 V, V_{DDIO} = 1.8 V, active USB transfer	IV_{BAT}	31.4	mA
		IV_{DDIO}	1.3	
		I_{TOTAL}	**32.7**	

6.2 Power Control

6.2.1 Overview

TUSB1211 can be powered up in two different modes:

- Standard power-up condition

  For this, V_{BAT} and V_{IO} must be present and chip must be selected (CS=1 and CS_N=0). See 9.3.3.1 Standard Power-up Timing Power resources will be configured sequentially until the device reaches the power state.

  USBON . At this time internal power-on-reset signal PORZ will be released and USB PLL will start up. Once PLL is locked, the DIR output pin will be deasserted allowing TUSB1211 to be configured by the USB Link Controller via the ULPI interface.

  Note that by default TUSB1211 will be configured as a Host not providing VBUS as required by register map in ULPI specification Rev1.1.

  This is the case because OTG_CONTROL register bits DRVVBUS and DRVVBUSEXTERNAL bits are 0 by default, and DPPULLDOWN, DMPULLDOWN bits are 1 by default such that the 15 kΩ pulldown resistors at DP/DM pins are enabled by default.

  It is the responsibility of the link to enable external VBUS supply if required in Host mode, or to reconfigure the PHY if required in Device mode.

- Hardware charger detection power-up

  When the chip is not selected (CS=0 or CS_N=1), but VBUS is present and CHRG_EN_N pin is at GND, and VBAT > VBAT_MNTR then TUSB1211 will power-up in Hardware Charger Detection Mode.

  Power resources will be configured sequentially until the device reaches the power state USBON . However since chip is not selected, internal power-on-reset signal PORZ will be not be released and USB PLL will not start up. Instead the device will enter USB Battery charger finite state machine

(FSM) .

7 USB Transceiver (PHY)

The TUSB1211 device includes a universal serial bus (USB) on-the-go (OTG) transceiver that supports USB 480 Mb/s high-speed (HS), 12 Mb/s full-speed (FS), and USB 1.5 Mb/s low-speed (LS) through a 12-pin UTMI+ low pin interface (ULPI).

Table 7-1. Interface Target Frequencies

IO INTERFACE	INTERFACE DESIGNATION		TARGET FREQUENCY
USB	Universal serial bus	High speed	480 Mbits/s
		Full speed	12 Mbits/s
		Low speed	1.5 Mbits/s

7.1 PHY Overview

The PHY is the physical signaling layer of the USB 2.0. It essentially contains all the drivers and receivers required for physical data and protocol signaling on the DP and DM lines.

The PHY interfaces to the USB controller through a standard 12-pin digital interface called UTMI+ low pin interface (ULPI).

The transmitters and receivers inside the PHY are classified into two main classes.

- The full-speed (FS) and low-speed (LS) transceivers. These are the legacy USB1.x transceivers.
- The HS (HS) transceivers

In order to bias the transistors and run the logic, the PHY also contains reference generation circuitry which consists of:

- A PLL which does a frequency multiplication to achieve the 480-MHz low-jitter clock necessary for USB and also the clock required for the switched capacitor resistance block.
- Internal biasing circuitry

Built-in pullup and pulldown resistors are used as part of the protocol signaling.

Apart from this, the PHY also contains circuitry which protects it from accidental short on the DP and DM lines to 5 V or GND.

8 UART Transceiver

By setting CARKITMODE bit in IFC_CTRL register TUSB1211 will enter UART mode. In this mode, the ULPI data bus is redefined as a 2-pin UART interface, which exchanges data through a direct access to the FS/LS analog transmitter at DM pin and receiver at DP pin.

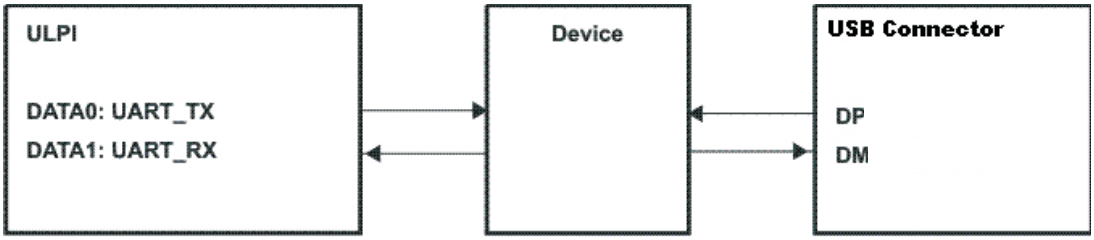


Figure 8-1. USB UART Data Flow

9 USB On-The-Go (OTG) Feature

The on-the-go (OTG) block integrates two main functions:

- ID resistor detection including Accessory Charger Adapter (ACA) detection
- V_{BUS} level detection and SRP pullup/pulldown resistors

10 USB Battery Charger Detection and ACA Feature

In order to support Battery Charging Specification v1.1 April 2009 [BCS v1.1], a charger detection module is included inside TUSB1211 module.

This feature includes:

- Battery charger detection sensing and control on DP/DM lines
- ACA (Accessory Charger Adapter) detection and control on ID line

The detection mechanism aims at distinguishing several types of power sources that can be connected on VBUS line:

- Dedicated Charging Port
- Standard Downstream Port
- Charging Downstream Port

Hardware includes:

- a dedicated voltage referenced pullup on DP line
- a dedicated current controlled pulldown on DM line
- a detection comparator on DM line - a control/detection finite state machine (FSM) including timers
- a charger detection output pin (CHRG_DET) for external charger control
- detection comparators on ID line

ID pin status detection (as defined per OTG v1.3 standard as well as ACA resistor types as described in BCS v1.1) and DP/DM Single-Ended receivers (as defined per USB v2.0 standard) are also used to determine the type of device plugged on USB connector.

USB charger detection is an independent feature, on V_{BAT} supply domain, using CK32K clock.

10.1 USB Battery Charger Detection Modes

There are 3 modes of operation of battery charger detection module:

1. Hardware Charger Detection Mode
2. Software Mode
3. Software FSM Mode

10.2 Accessory Charger Adapter (ACA) Detection

Accessory Charger Adapter (ACA) feature is defined in the USB Battery Charging Specification Rev. 1.1 specification. ACA allows simultaneous connection of a USB Charger or Charging Downstream Port and an Accessory to a portable OTG device (TUSB1211).via only a single USB OTG port.

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