RAD-TOLERANT CLASS-V REGULATING PULSE WIDTH MODULATOR

FEATURES

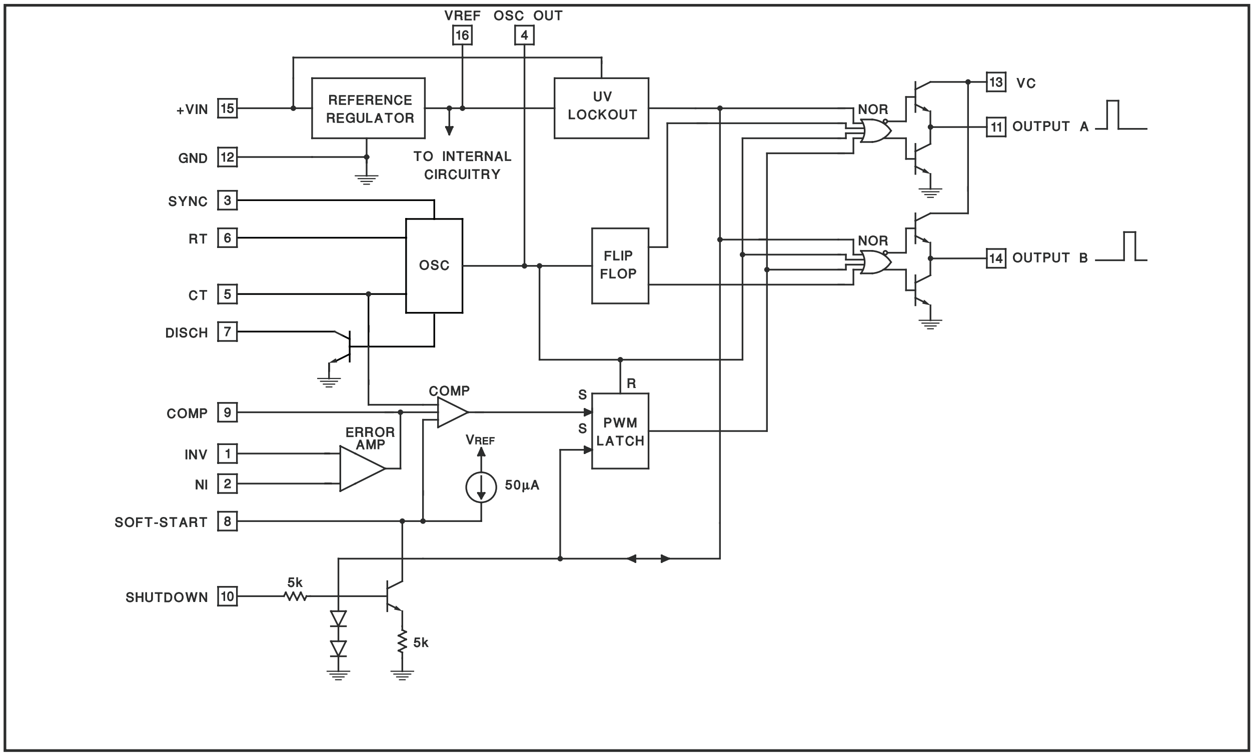
- **QML-V Qualified, SMD 5962-89511**
- **Rad-Tolerant: 30 kRad (Si) TID** (1)
- **8-V to 35-V Operation**
- **5.1-V Buried Zener Reference Trimmed to ±0.75%**
- **100-Hz to 400-kHz Oscillator Range**
- **Separate Oscillator Sync Terminal**
- **Adjustable Deadtime Control**
- **Internal Soft Start**
- **Pulse-by-Pulse Shutdown**
- **Input Undervoltage Lockout With Hysteresis**
- **Latching PWM to Prevent Multiple Pulses**
- **Dual Source/Sink Output Drivers**
- **Low Cross Conduction Output Stage**
- **Tighter Reference Specifications**

(1) Radiation tolerance is a typical value based upon initial device qualification with dose rate = 10 mrad/sec. Radiation Lot Acceptance Testing is available - contact factory for details.

DESCRIPTION

The UC1525B pulse width modulator integrated circuit is designed to offer improved performance and lowered external parts count when used in designing all types of switching power supplies. The on-chip 5.1-V buried zener reference is trimmed to ±0.75%, and the input common-mode range of the error amplifier includes the reference voltage, eliminating external resistors. A sync input to the oscillator allows multiple units to be slaved or a single unit to be synchronized to an external system clock. A single resistor between the CT and the discharge terminals provide a wide range of dead-time adjustment. These devices also feature built-in soft-start circuitry with only an external timing capacitor required. A shutdown terminal controls both the soft-start circuitry and the output stages, providing instantaneous turn off through the PWM latch with pulsed shutdown, as well as soft-start recycle with longer shutdown commands. These functions are also controlled by an undervoltage lockout which keeps the outputs off and the soft-start capacitor discharged for sub-normal input voltages. This lockout circuitry includes approximately 500 mV of hysteresis for jitter-free operation. Another feature of these PWM circuits is a latch following the comparator. Once a PWM pulse has been terminated for any reason, the outputs remain off for the duration of the period. The latch is reset with each clock pulse. The output stages are totem-pole designs capable of sourcing or sinking in excess of 200 mA. The UC1525B output stage features NOR logic, giving a LOW output for an OFF state.

BLOCK DIAGRAM



This device has limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

ORDERING INFORMATION(1)

T_A	PACKAGE(2)	ORDERABLE PART NUMBER	TOP-SIDE MARKING
–55°C to 125°C	FK	5962-8951106V2A	UC1525BFK-SP

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.
(2) Package drawings, thermal data, and symbolization are available at www.ti.com/packaging.

ABSOLUTE MAXIMUM RATINGS[1][2]

over operating free-air temperature range (unless otherwise noted)

$+V_{IN}$	Supply voltage		40 V
V_C	Collector supply voltage		40 V
	Logic inputs		–0.3 V to 5.5 V
V_I	Analog inputs		–0.3 V to V_{IN}
I_O	Output current, source or sink		500 mA
	Reference output current		50 mA
	Oscillator charging current		5 mA
P_D	Power dissipation	T_A = 25°C	1000 mW
		T_C = 25°C	2000 mW
T_J	Operating junction temperature		–55°C to 150°C
T_{stg}	Storage temperature range		–65°C to 150°C
T_{lead}	Lead temperature (soldering, 10 seconds)		300°C

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltages are with respect to ground. Currents are positive into, negative out of the specified terminal.

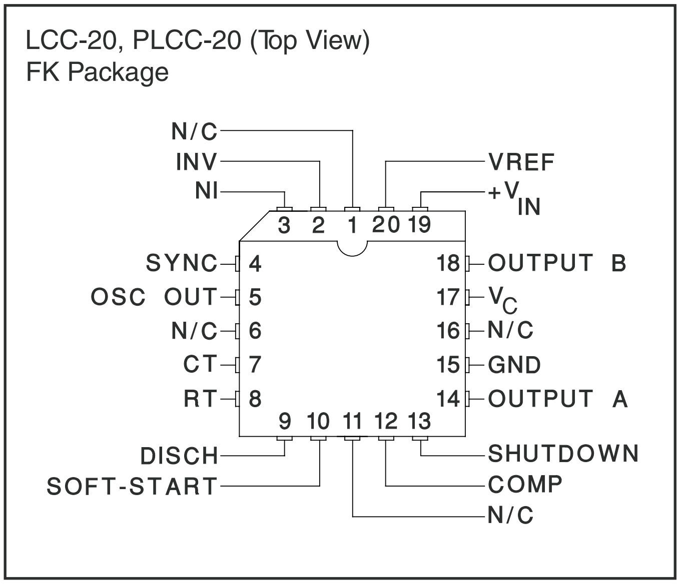
RECOMMENDED OPERATING CONDITIONS[1]

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
$+V_{IN}$	Input voltage	8	35	V
V_C	Collector supply voltage	4.5	35	V
	Sink/source load current (steady state)	0	100	mA
	Sink/source load current (peak)	0	400	mA
	Reference load current	0	20	mA
	Oscillator frequency range	0.1	400	kHz
	Oscillator timing resistor	2	150	kΩ
	Oscillator timing capacitor	0.001	0.1	µF
	Dead time resistor range	0	500	Ω

(1) Range over which the device is functional and parameter limits are specified.

CONNECTION DIAGRAM



ELECTRICAL CHARACTERISTICS

V_{IN} = 20 V, T_A = T_J = –55°C to 125°C (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Reference Section					
Output voltage	T_J = 25°C	5.062	5.10	5.138	V
Line regulation	V_{IN} = 8 V to 35 V		5	10	mV
Load regulation	I_L = 0 mA to 20 mA		7	15	mV
Temperature stability(1)	Over operating range		10	50	mV
Total output variation	Over line, load, and temperature	5.036		5.164	V
Short-circuit current	V_{REF} = 0 V, T_J = 25°C		80	100	mA
Output noise voltage(1)	10 Hz ≤ f ≤ 10 kHz, T_J = 25°C		40	200	µVrms
Oscillator Section					
Initial accuracy(2)	T_J = 25°C		±2	±6	%
Voltage stability(2)	V_{IN} = 8 V to 35 V		±0.3	±1	%
Temperature stability(1)(2)	Over operating range		±3	±6	%
Minimum frequency	R_T = 200 kΩ, C_T = 0.1 µF			120	Hz
Maximum frequency	R_T = 2 kΩ, C_T = 470 pF	400			kHz
Current mirror	I_{RT} = 2 mA	1.7	2.	2.2	mA
Clock amplitude(2)		3	3.5		V
Clock width(2)	T_J = 25°C	0.3	0.5	1	µs
Sync threshold		1.2	2	2.8	V
Sync input current	Sync = 3.5 V		1	2.5	mA

(1) Parameters ensured by design and/or characterization, if not production tested.
(2) Tested at f_{osc} = 40 kHz (R_T = 3.6 kΩ, C_T = 0.01 µF, R_D = 0 Ω).
Approximate oscillator frequency is defined by: f = 1/(C_T (0.7 x R_T + 3R_D)).

ELECTRICAL CHARACTERISTICS (continued)

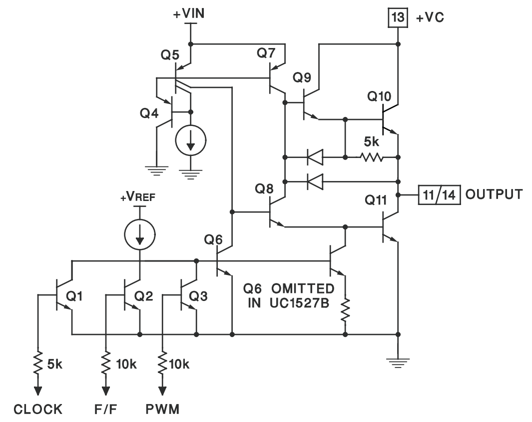
V_{IN} = 20 V, T_A = T_J = –55°C to 125°C (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Error Amplifier Section (V_{CM} = 5.1 V)					
Input offset voltage			0.5	5	mV
Input bias current			1	10	µA
Input offset current				1	µA
DC open loop gain	R_L ≥ 10 MΩ	60	75		dB
Gain-bandwidth product (3)	A_V = 0 dB, T_J = 25°C	1	2		MHz
Ouput low level			0.2	0.5	V
Output high level		3.8	5.6		V
Common mode rejection	V_{CM} = 1.5 V to 5.2 V	60	75		dB
Supply voltage rejection	V_{IN} = 8 V to 35 V	50	60		dB
PWM Comparator					
Minimum duty cycle				0	%
Maximum duty cycle (4)		45	49		%
Input threshold (4)	Zero duty cycle	0.7	0.9		V
Input threshold (4)	Maximum duty cycle		3.3	3.6	V
Input bias current			0.05		µA
Shutdown Section					
Soft start current	$V_{SHUTDOWN}$ = 0 V, $V_{SOFTSTART}$ = 0 V	25	50	80	µA
Soft start low level	$V_{SHUTDOWN}$ = 2.5 V		0.4	0.7	V
Shutdown threshold	To outputs, $V_{SOFTSTART}$ = 5.1 V, T_J = 25°C	0.6	0.8	1	V
Shutdown input current	$V_{SHUTDOWN}$ = 2.5 V		0.4	1	mA
Shutdown delay (3)	$V_{SHUTDOWN}$ = 2.5 V, T_J = 25°C		0.2	0.5	µs
Output Drivers (Each OUtput) (V_C = 20 V)					
Output low level	I_{SINK} = 20 mA		0.2	0.4	V
	I_{SINK} = 100 mA		1	2	
Output high level	I_{SOURCE} = 20 mA	18	19		V
	I_{SOURCE} = 100 mA	17	18		
Undervoltage lockout	V_{COMP} and $V_{SOFTSTART}$ = High	6	7	8	V
Collector leakage	V_C = 35 V			200	µA
Rise time (3)	C_L = 1 nF, T_J = 25°C		100	600	ns
Fall time (3)	C_L = 1 nF, T_J = 25°C		50	300	ns
Cross conduction charge	Per cycle, T_J = 25°C		30		nc
Total Standby Current					
Supply current	V_{IN} = 35 V		14	20	mA

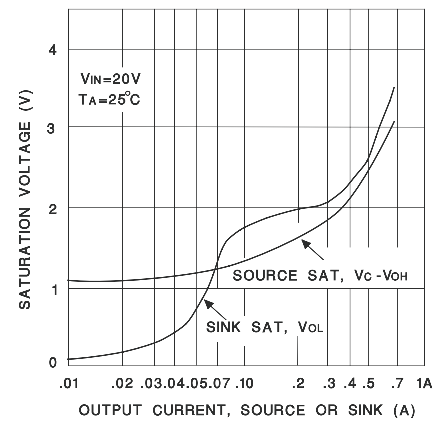
(3) Parameters ensured by design and/or characterization, if not production tested.
(4) Tested at f_{osc} = 40 kHz (R_T = 3.6 kΩ, C_T = 0.01 µF, R_D = 0 Ω).
Approximate oscillator frequency is defined by: $f = 1/(C_T\ (0.7 \times R_T + 3R_D))$.

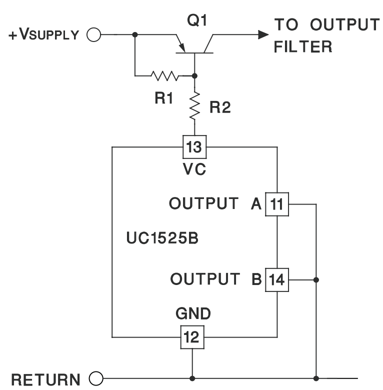
PRINCIPLES OF OPERATION AND TYPICAL CHARACTERISTICS

Output Circuit (½ Circuit Shown)

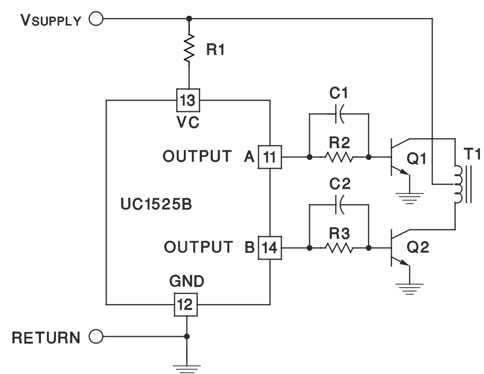


Output Saturation Characteristics

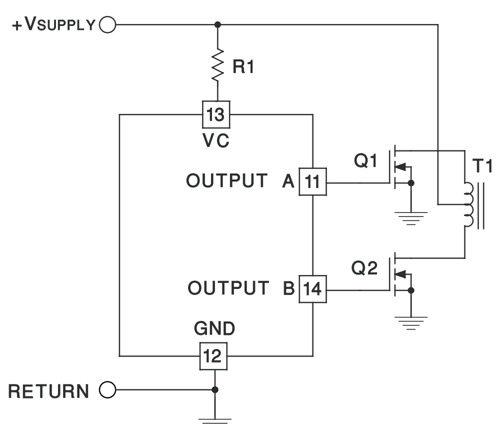




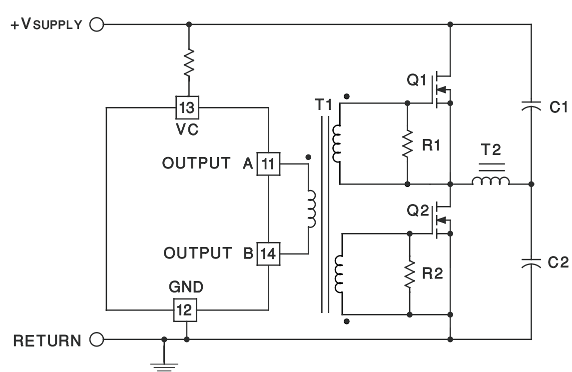
For single ended supplies, the driver outputs are grounded. The VC terminal is switched to ground by the totem-pole source transistors on alternate oscillator cycles.



In conventional push-pull bipolar designs, forward base drive is controlled by R1-R3. Rapid turn-off times for the power devices are acheived with speed-up capacitors C, and C2.



The low source impedance of the output drivers provides rapid charging of power FET input capacitance while minimizing external components.



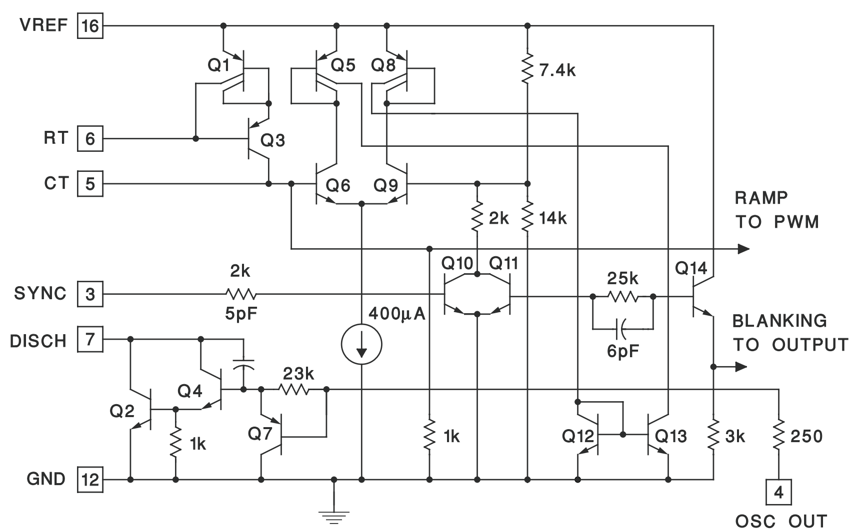
Low power transformers can be driven directly by the UC1525B. Automatic reset occurs during dead time, when both ends of the primary winding are switched to ground.

PRINCIPLES OF OPERATION AND TYPICAL CHARACTERISTICS (continued)

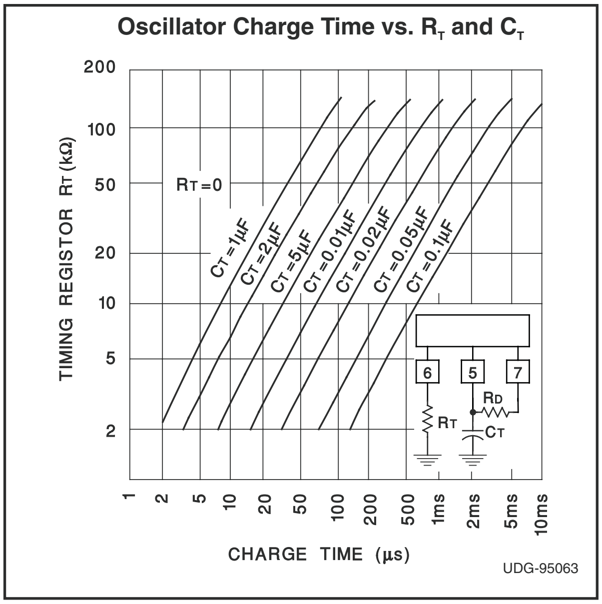
Since both the compensation and soft-start terminals (Pins 9 and 8) have current source pullups, either can readily accept a pulldown signal, which only has to sink a maximum of 100 µA to turn off the outputs. This is subject to the added requirement of discharging whatever external capacitance may be attached to these pins.

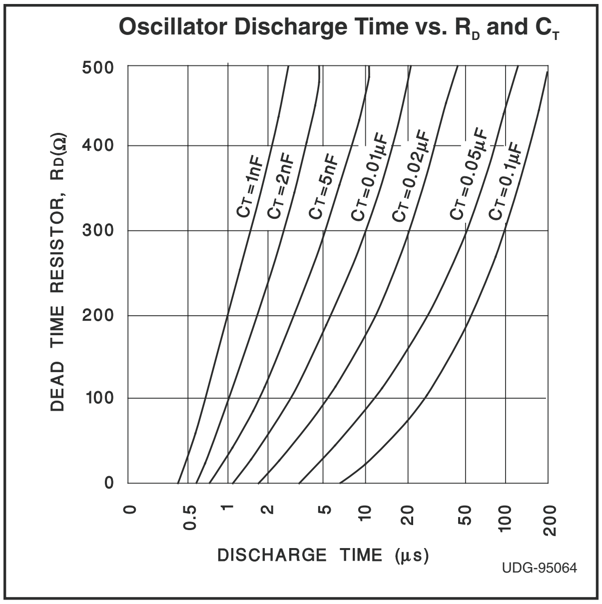
An alternate approach is the use of the shutdown circuitry of Pin 10, which has been improved to enhance the available shutdown options. Activating this circuit by applying a positive signal on Pin 10 performs two functions: the PWM latch is immediately set providing the fastest turn-off signal to the external soft-start capacitor. If the shutdown command is short, the PWM signal is terminated without significant discharge of the soft-start capacitor, thus, allowing, for example, a convenient implementation of pulse-by-pulse current limiting. Holding Pin 10 high for a longer duration, however, ultimately discharges this external capacitor, recycling slow turn-on upon release.

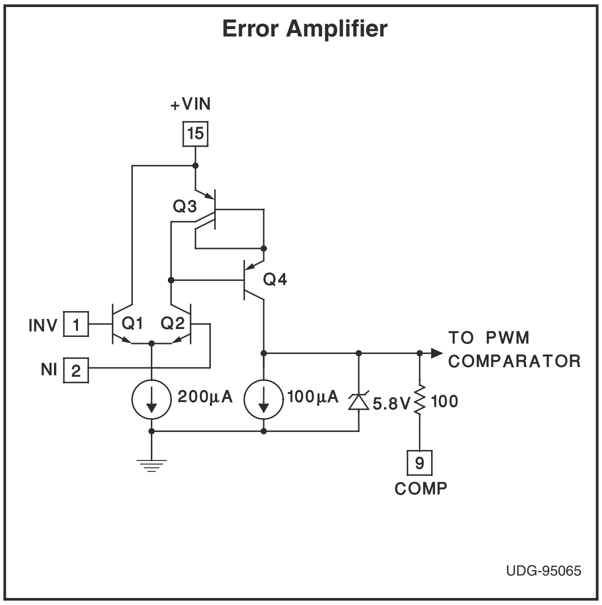
Oscillator Schematic

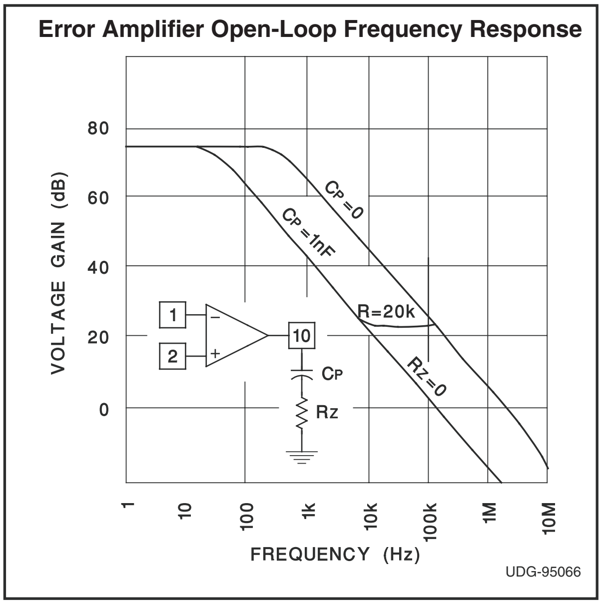


PRINCIPLES OF OPERATION AND TYPICAL CHARACTERISTICS (continued)



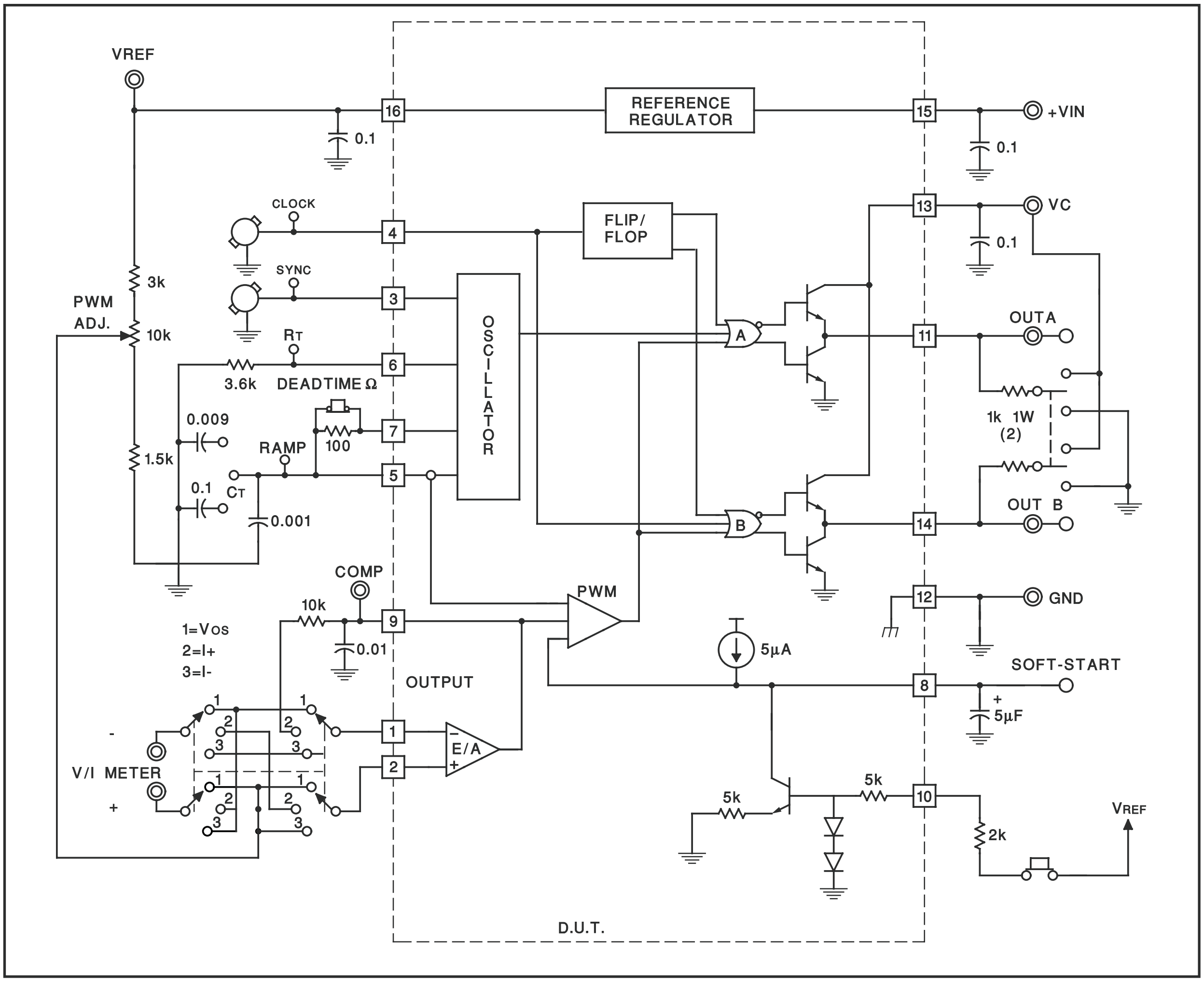






PRINCIPLES OF OPERATION AND TYPICAL CHARACTERISTICS (continued)

LAB TEST FIXTURE



PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)
5962-8951105V2A	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type
5962-8951105VEA	ACTIVE	CDIP	J	16	1	TBD	A42	N / A for Pkg Type
5962-8951106V2A	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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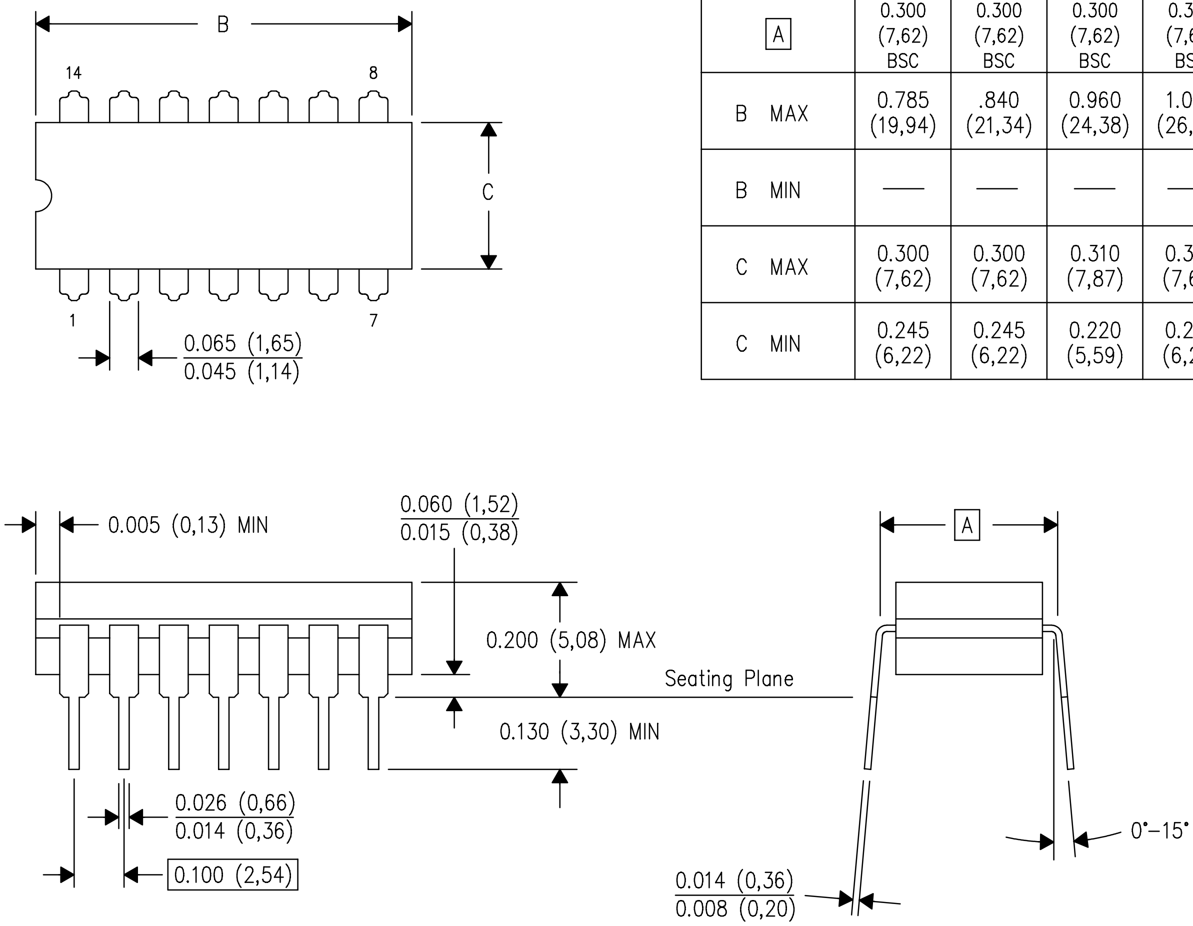
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF UC1525B-SP :
- Catalog: UC1525B

NOTE: Qualified Version Definitions:
- Catalog - TI's standard catalog product

14 LEADS SHOWN

PINS ** / DIM	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)

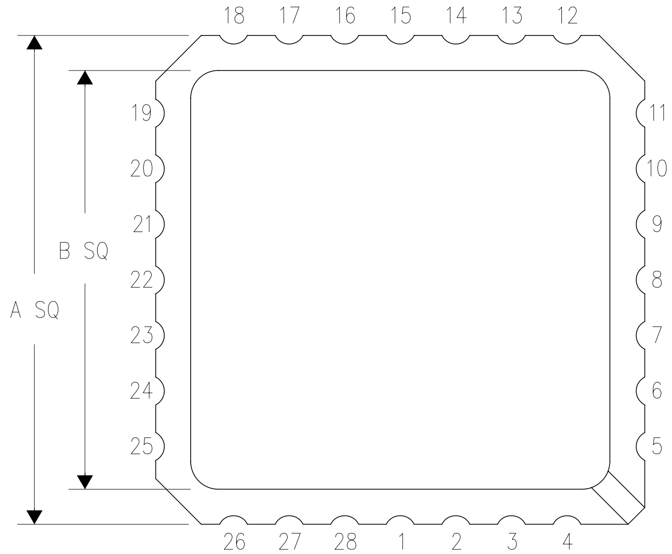


4040083/F 03/03

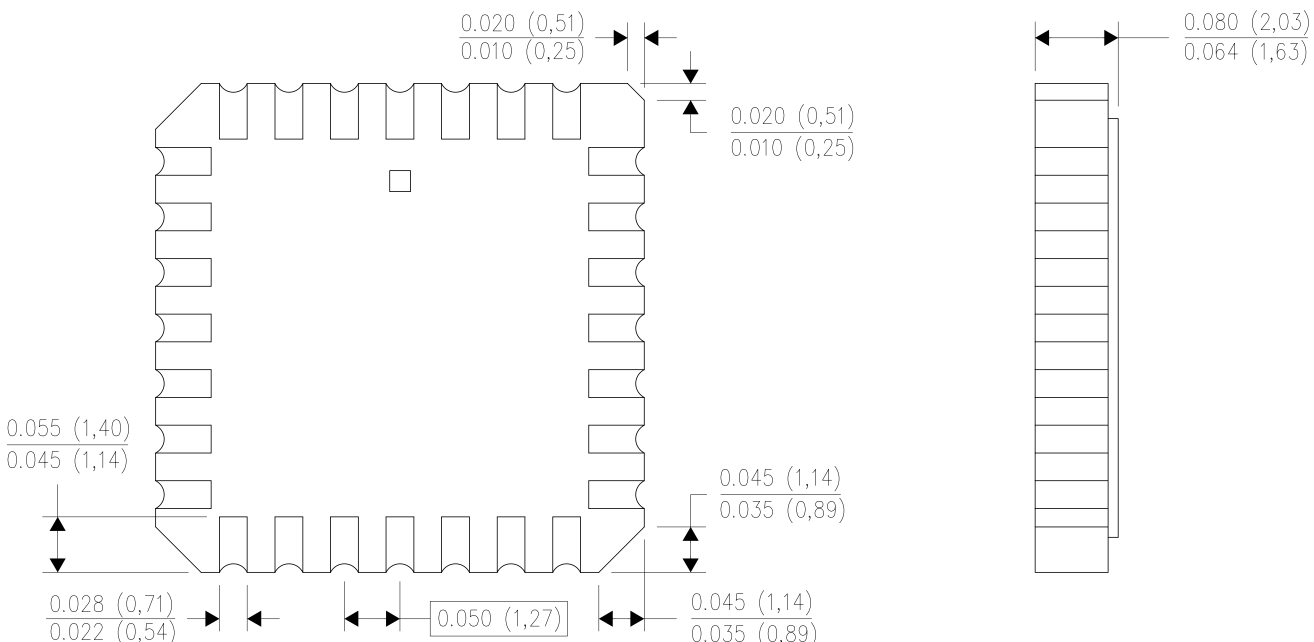
NOTES:
- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. This package is hermetically sealed with a ceramic lid using glass frit.
- D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
- E. Falls within MIL STD 1835 GDIP1–T14, GDIP1–T16, GDIP1–T18 and GDIP1–T20.

FK (S–CQCC–N**) LEADLESS CERAMIC CHIP CARRIER

28 TERMINAL SHOWN



NO. OF TERMINALS **	A		B	
	MIN	MAX	MIN	MAX
20	0.342 (8,69)	0.358 (9,09)	0.307 (7,80)	0.358 (9,09)
28	0.442 (11,23)	0.458 (11,63)	0.406 (10,31)	0.458 (11,63)
44	0.640 (16,26)	0.660 (16,76)	0.495 (12,58)	0.560 (14,22)
52	0.740 (18,78)	0.761 (19,32)	0.495 (12,58)	0.560 (14,22)
68	0.938 (23,83)	0.962 (24,43)	0.850 (21,6)	0.858 (21,8)
84	1.141 (28,99)	1.165 (29,59)	1.047 (26,6)	1.063 (27,0)



4040140/D 01/11

NOTES:
- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. This package can be hermetically sealed with a metal lid.
- D. Falls within JEDEC MS–004