耐辐射 V 类, 无刷 DC 电机控制

查询样品: UC1625-SP

特性

- 经QML-V 标准认证，SMD 5962-91689
- 耐辐射: 40 kRad (Si) TID (1)
- 直接驱动功率场效应管（MOSFET）或者达灵顿功率管（Darlington）
- 50-V 开路集电极高层驱动器
- 锁存软启动
- 装有理想二极管的高速电流感应放大器
- 逐脉冲和平均电流感应
- 过压及欠压保护
- 用于安全方向反转的方向闩
- 转速计
- 修整参考源 30 mA
- 可编程交叉传导保护
- 两象限和四象限运算

(1) 辐射容限是基于初始器件鉴定 （放射量率 = 10 mrad/sec） 的典型值。 可提供辐射批量接受测试——详情请与厂家联系。

说明/订购信息

UC1625 电机控制器在一个封装内集成了高性能无刷dc电机控制所需的大多数功能。 当与外部功率场效应管（MOSFET）或者达灵顿功率管（Darlington）耦合的时候，此器件在电压或者电流模式下件执行固定频率PWM 电机控制的同时执行闭环速度控制和具有智能噪音抑制功能的刹车，安全方向反转，和交叉传导保护。

虽然额定工作电压范围是 10 V至 18V，UC1625 可借助于外部电平位移组件来控制具有更高电源电压的器件。 UC1625 含有用于低侧功率器件的快速、高电流推挽驱动器和用于高侧功率器件或者电平位移电路的 50 V开路集电极输出。

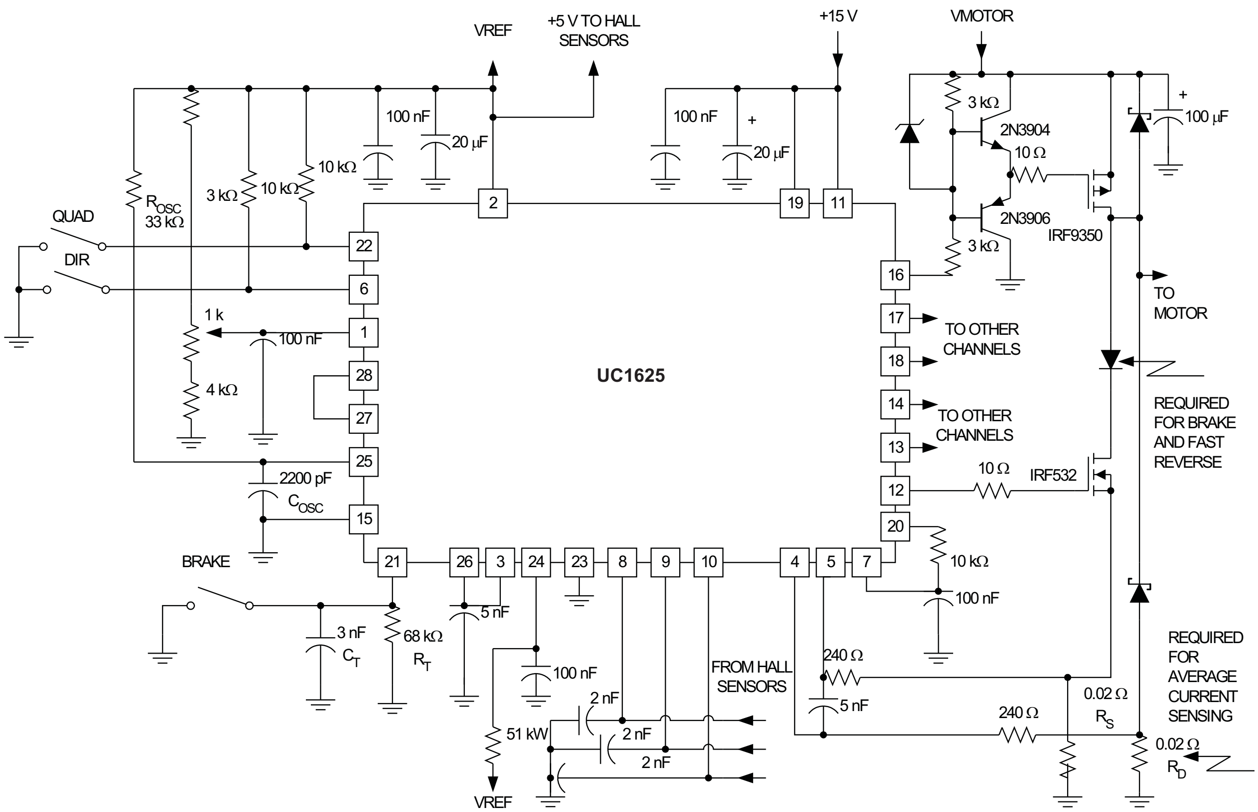
UC1625 额定军用工作温度范围是 -55°C 至 125°C。

ORDERING INFORMATION(1)

T_A	PACKAGE(2)	ORDERABLE PART NUMBER	TOP-SIDE MARKING
–55°C to 125°C	CDIP – JT	5962-9168902VYA	5962-9168902VYA UC1625-SP

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.
(2) Package drawings, thermal data, and symbolization are available at www.ti.com/packaging.

Typical Application



ABSOLUTE MAXIMUM RATINGS(1) (2)

over operating free-air temperature range (unless otherwise noted)

		VALUE	UNIT
VCC	Supply voltage	20	V
PWR VCC		20	
	PWM IN	–0.3 to 6	
	E/A IN(+), E/A IN(–)	–0.3 to 12	
	ISENSE1, ISENSE2	–1.3 to 6	
	OV-COAST, DIR, SPEED-IN, SSTART, QUAD SEL	–0.3 to 8	
	H1, H2, H3	–0.3 to 12	
	PU Output Voltage	–0.3 to 50	
PU	Output current	+200 continuous	mA
PD		±200 continuous	
E/A		±10	
I_{SENSE}		–10	
TACH OUT		±10	
VREF		–50 continuous	
T_J	Maximum Junction Temperature	150	°C

(1) Currents are positive into and negative out of the specified terminal.
(2) Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability. These are stress ratings only and functional operation of the device at these or any other conditions beyond those specified is not implied.

RECOMMENDED OPERATING CONDITIONS

over operating temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{CC}	Supply Voltage	10		18	V
PU	Output Current			+85 continuous	mA
PD				±85 continuous	mA
T_A	Operating temperature range	-55		125	°C

Table 1. THERMAL RATINGS TABLE

PACKAGE	$R_{\theta JA}$(°C/W) (Junction-to-ambient thermal resistance)	$R_{\theta JC}$(°C/W) (Junction-to-case thermal resistance)
DIL-28 (JT)	43.1	4.95

Figure 1. CONNECTION DIAGRAM

ELECTRICAL CHARACTERISTICS

Unless otherwise stated, these specifications apply over the full temperature range, typical values at T_A = 25°C; Pwr V_{CC} = V_{CC} = 12 V; R_{OSC} = 20 kΩ to V_{REF}; C_{OSC} = 2 nF; R_{TACH} = 33 kΩ; C_{TACH} = 10 nF; and all outputs unloaded. T_A = T_J.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Overall						
	Supply current	-55°C to 125°C		14.5	30.0	mA
	VCC turn-on threshold		8.65	8.95	9.55	V
	VCC turn-off threshold		7.75	8.05	8.55	
Overvoltage/Coast						
	OV-COAST inhibit threshold	-55°C to 125°C	1.65	1.75	1.85	V
	OV-COAST restart threshold		1.535	1.65	1.75	
	OV-COAST hysteresis		0.05	0.10	0.155	
	OV-COAST input current		–10	–1	10	µA
Logic Inputs						
	H1, H2, H3 low threshold	-55°C to 125°C	0.8	1.0	1.25	V
	H1, H2, H3 high threshold		1.6	1.9	2.0	
	H1, H2, H3 input current	-55°C to 125°C, to 0 V	–400	–250	–120	µA
	QUAD SEL, dir thresholds	-55°C to 125°C	0.8	1.4	3.0	V
	QUAD SEL hysteresis			70	130	mV
	DIR hysteresis		0.4	0.6	0.9	V
	QUAD SEL input current		–30	50	150	µA
	DIR input current		–30	–1	30	
PWM Amp/Comparator						
	E/A IN(+), E/A IN(–) input current	To 2.5 V	–5.0	–0.1	5.0	µA
	PWM IN input current	To 2.5 V	0	3	30	
	Error amp input offset	0 V < $V_{COMMON\text{-}MODE}$ < 3 V	–10		10	mV
	Error amp voltage gain		70	90		dB
	E/A OUT range	25°C to 125°C	0.25		3.50	V
		-55°C	0.25		4.2	
S_{START}	Pullup current	To 0 V, 25°C	-16	–10	–5	µA
		To 0 V , -55°C to 125°C	–17.5		-5	
	Discharge current	To 2.5 V	0.1	0.4	3.0	mA
	Restart threshold		0.1	0.2	0.3	V
Current Amp						
	Gain	I_{SENSE1} = 0.3 V, I_{SENSE2} = 0.5 V to 0.7 V	1.75	1.95	2.15	V/V
	Level shift	I_{SENSE1} = 0.3 V, I_{SENSE2} = 0.3 V	2.4	2.5	2.65	V
	Peak current threshold	I_{SENSE1} = 0 V, force I_{SENSE2}	0.14	0.20	0.26	
	Over current threshold		0.26	0.30	0.36	
	I_{SENSE1}, I_{SENSE2} input current	To 0 V	–850	–320	0	µA
	I_{SENSE1}, I_{SENSE2} offset current		-12	±2	12	
	Range I_{SENSE1}, I_{SENSE2}		–1		2	V
Tachometer/Brake						
	TACH-OUT high level	-55°C to 125°C, 10 kΩ to 2.5 V	4.7	5	5.3	V
	TACH-OUT low level				0.2	
	On time		170	220	280	µs
	On time change with temp	-55°C to 125°C		0.1%		
	RC-BRAKE input current	To 0 V	–4.0	–1.9		mA

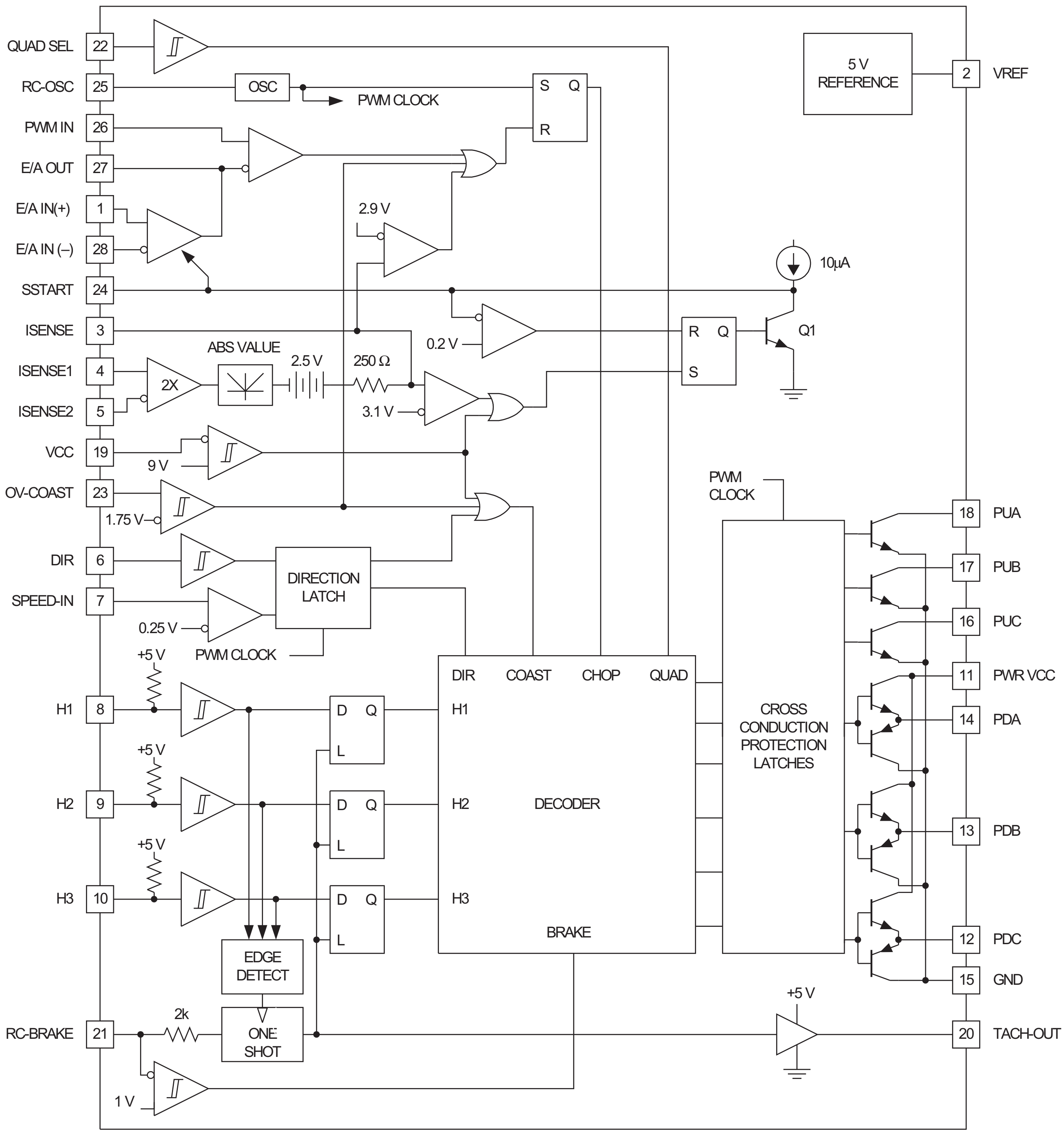
ELECTRICAL CHARACTERISTICS (continued)

Unless otherwise stated, these specifications apply over the full temperature range, typical values at T_A = 25°C; Pwr V_{CC} = V_{CC} = 12 V; R_{OSC} = 20 kΩ to V_{REF}; C_{OSC} = 2 nF; R_{TACH} = 33 kΩ; C_{TACH} = 10 nF; and all outputs unloaded. T_A = T_J.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
	Threshold to brake, RC-brake	-55°C to 125°C	0.8	1.0	1.2	V
	Brake hysteresis, RC-brake			0.09	0.4	
	SPEED-IN threshold		220	257	290	mV
	SPEED-IN input current		–30	–5	30	µA
Low-Side Drivers(1)						
	Voh, –1 mA, down from V_{CC}	-55°C to 125°C		1.60	2.50	V
	Voh, –50 mA, down from V_{CC}			1.75	2.45	
	Vol, 1 mA			0.05	0.4	
	Vol, 50 mA			0.36	0.9	
	Rise/fall time	10% to 90% slew time, into 1 nF		50	500	ns
High-Side Drivers						
	Vol, 1 mA	-55°C to 125°C		0.1	0.4	V
	Vol, 50 mA			1.0	1.8	
	Leakage current	Output voltage = 50 V			30	µA
	Fall time	10% to 90% slew time, 50 mA load		50		ns
Oscillator						
	Frequency	-55°C to 125°C	30		80	kHz
Reference						
	Output voltage	Iref = 0 mA, 25°C	4.85	5.0	5.15	V
		-55°C to 125°C	4.7	5.0	5.3	
	Load regulation	0 mA to –20 mA load	–40	–5		mV
	Line regulation	10 V to 18 V V_{CC}	–10	–1	10	
	Short circuit current	-55°C to 125°C	20	100	150	mA
Miscellaneous						
	Output turn-on delay			1		µs
	Output turn-off delay			1		

(1) Current available from these pins can peak as high as 0.5 A.

Block Diagram



DEVICE INFORMATION

Terminal Functions

TERMINAL		DESCRIPTION
NAME	NO.	
DIR, SPEED-IN	6, 7	The position decoder logic translates the Hall signals and the DIR signal to the correct driver signals (PUs and PDs). To prevent output stage damage, the signal on DIR is first loaded into a direction latch, then shifted through a two-bit register. As long as SPEED-IN is less than 250 mV, the direction latch is transparent. When SPEED-IN is higher than 250 mV, the direction latch inhibits all changes indirection. SPEED-IN can be connected to TACH-OUT through a filter, so that the direction latch is only transparent when the motor is spinning slowly, and has too little stored energy to damage power devices. Additional circuitry detects when the input and output of the direction latch are different, or when the input and output of the shift register are different, and inhibits all output drives during that time. This can be used to allow the motor to coast to a safe speed before reversing. The shift register ensures that direction can not be changed instantaneously. The register is clocked by the PWM oscillator, so the delay between direction changes is always going to be between one and two oscillator periods. At 40 kHz, this corresponds to a delay of between 25 µs and 50 µs. Regardless of output stage, 25 µs deadtime should be adequate to ensure no overlap cross-conduction. Toggling DIR causes an output pulse on TACH-OUT regardless of motor speed.
E/A IN(+), E/A IN(–), E/A OUT, PWM IN	1, 28, 27, 26	E/A IN(+) and E/A IN(–) are not internally committed to allow for a wide variety of uses. They can be connected to the ISENSE, to TACH-OUT through a filter, to an external command voltage, to a D/A converter for computer control, or to another op amp for more elegant feedback loops. The error amplifier is compensated for unity gain stability, so E/A OUT can be tied to E/A IN(–) for feedback and major loop compensation. E/A OUT and PWM In drive the PWM comparator. For voltage-mode PWM systems, PWM In can be connected to RC-OSC. The PWM comparator clears the PWM latch, commanding the outputs to chop. The error amplifier can be biased off by connecting E/A IN(–) to a higher voltage than /EA IN(+). When biased off, E/A OUT appears to the application as a resistor to ground. E/A OUT can then be driven by an external amplifier.
GND	15	All thresholds and outputs are referred to the GND pin except for the PD and PU outputs.
H1, H2, H3	8, 9, 10	The three shaft position sensor inputs consist of hysteresis comparators with input pullup resistors. Logic thresholds meet TTL specifications and can be driven by 5-V CMOS, 12-V CMOS, NMOS, or open-collectors. Connect these inputs to motor shaft position sensors that are positioned 120 electrical degrees apart. If noisy signals are expected, zener clamp and filter these inputs with 6-V zeners and an RC filter. Suggested filtering components are 1 kΩ and 2 nF. Edge skew in the filter is not a problem, because sensors normally generate modified gray code with only one output changing at a time, but rise and fall times must be shorter than 20 µs for correct tachometer operation. Motors with 60 electrical degree position sensor coding can be used if one or two of the position sensor signals is inverted.
ISENSE1, ISENSE2, ISENSE	3, 4, 5	The current sense amplifier has a fixed gain of approximately two. It also has a built-in level shift of approximately 2.5 V. The signal appearing on ISENSE is: $I_{SENSE} = 2.5\text{ V} + (2 \times ABS\ (I_{SENSE1} - I_{SENSE2}))$ I_{SENSE1} and I_{SENSE2} are interchangeable and can be used as differential inputs. The differential signal applied can be as high as ±0.5 V before saturation. If spikes are expected on ISENSE1 or ISENSE2, they are best filtered by a capacitor from ISENSE to ground. Filtering this way allows fast signal inversions to be correctly processed by the absolute value circuit. The peak-current comparator allows the PWM to enter a current-limit mode with current in the windings never exceeding approximately 0.2 V / R_{SENSE}. The overcurrent comparator provides a fail-safe shutdown in the unlikely case of current exceeding 0.3 V / R_{SENSE}. Then, softstart is commanded, and all outputs are turned off until the high current condition is removed. It is often essential to use some filter driving ISENSE1 and ISENSE2 to reject extreme spikes and to control slew rate. Reasonable starting values for filter components might be 250-Ω series resistors and a 5-nF capacitor between ISENSE1 and ISENSE2. Input resistors should be kept small and matched to maintain gain accuracy.
OV-COAST	23	This input can be used as an over-voltage shut-down input, as a coast input, or both. This input can be driven by TTL, 5-V CMOS, or 12-V CMOS.

Terminal Functions (continued)

TERMINAL		DESCRIPTION
NAME	NO.	
PDA, PDB, PDC	12, 13, 14	These outputs can drive the gates of N-channel power MOSFETs directly or they can drive the bases of power Darlingtons if some form of current limiting is used. They are meant to drive low-side power devices in high-current output stages. Current available from these pins can peak as high as 0.5 A. These outputs feature a true totem-pole output stage. Beware of exceeding device power dissipation limits when using these outputs for high continuous currents. These outputs pull high to turn a “low-side” device on (active high).
PUA, PUB, PUC	16, 17, 18	These outputs are open-collector, high-voltage drivers that are meant to drive high-side power devices in high-current output stages. These are active low outputs, meaning that these outputs pull low to command a high-side device on. These outputs can drive low-voltage PNP Darlingtons and P-channel MOSFETs directly, and can drive any high-voltage device using external charge pump techniques, transformer signal coupling, cascode level-shift transistors, or opto-isolated drive (high-speed opto devices are recommended). (See applications).
PWR VCC	11	This supply pin carries the current sourced by the PD outputs. When connecting PD outputs directly to the bases of power Darlingtons, the PWR VCC pin can be current limited with a resistor. Darlington outputs can also be "Baker Clamped" with diodes from collectors back to PWR VCC. (See Applications)
QUAD SEL	22	The device can chop power devices in either of two modes, referred to as “two-quadrant” (Quad Sellow) and “four quadrant” (Quad Sel high). When two-quadrant chopping, the pulldown power devices are chopped by the output of the PWM latch while the pullup drivers remain on. The load chops into one commutation diode, and except for back-EMF, will exhibit slow discharge current and faster charge current. Two-quadrant chopping can be more efficient than four-quadrant. When four-quadrant chopping, all power drivers are chopped by the PWM latch, causing the load current to flow into two diodes during chopping. This mode exhibits better control of load current when current is low, and is preferred in servo systems for equal control over acceleration and deceleration. The QUAD SEL input has no effect on operation during braking.
RC-BRAKE	21	Each time the TACH-OUT pulses, the capacitor tied to RC-BRAKE discharges from approximately 3.33 V down to 1.67 V through a resistor. The tachometer pulse width is approximately T = 0.67 R_T C_T, where R_T and C_T are a resistor and capacitor from RC-BRAKE to ground. Recommended values for R_T are 10 kΩ to 500 kΩ, and recommended values for C_T are 1 nF to 100 nF, allowing times between 5 µs and 10 ms. Best accuracy and stability are achieved with values in the centers of those ranges. RC-BRAKE also has another function. If RC-BRAKE pin is pulled below the brake threshold, the device enters brake mode. This mode consists of turning off all three high-side devices, enabling all three low-side devices, and disabling the tachometer. The only things that inhibit low-side device operation in braking are low-supply, exceeding peak current, OV-COAST command, and the PWM comparator signal. The last of these means that if current sense is implemented such that the signal in the current sense amplifier is proportional to braking current, the low-side devices will brake the motor with current control. (See applications) Simpler current sense connections results in uncontrolled braking and potential damage to the power devices.
RC-OSC	25	The UC1625 can regulate motor current using fixed-frequency pulse width modulation (PWM). The RC-OSC pin sets oscillator frequency by means of timing resistor R_{OSC} from the RC-OSC pin to VREF and capacitor COSC from RC-OSC to Gnd. Resistors 10 kΩ to 100 kΩ and capacitors 1 nF to 100 nF works the best, but frequency should always be below 500 kHz. Oscillator frequency is approximately: F = 2/(R_{OSC} x C_{OSC}) Additional components can be added to this device to cause it to operate as a fixed off-time PWM rather than a fixed frequency PWM, using the RC-OSC pin to select the monostable time constant. The voltage on the RC-OSC pin is normally a ramp of about 1.2 V peak-to-peak, centered at approximately 1.6 V. This ramp can be used for voltage-mode PWM control, or can be used for slope compensation in current-mode control.

Terminal Functions (continued)

TERMINAL		DESCRIPTION
NAME	NO.	
SSTART	24	Any time that VCC drops below threshold or the sensed current exceeds the over-current threshold, the soft-start latch is set. When set, it turns on a transistor that pulls down on SSTART. Normally, a capacitor is connected to this pin, and the transistor will completely discharge the capacitor. A comparator senses when the NPN transistor has completely discharged the capacitor, and allows the soft-start latch to clear when the fault is removed. When the fault is removed, the soft-start capacitor charges from the on-chip current source. SSTART clamps the output of the error amplifier, not allowing the error amplifier output voltage to exceed SSTART regardless of input. The ramp on RC-OSC can be applied to PWM In and compared to E/A OUT. With SSTART discharged below 0.2 V and the ramp minimum being approximately 1.0 V, the PWM comparator keeps the PWM latch cleared and the outputs off. As SSTART rises, the PWM comparator begins to duty-cycle modulate the PWM latch until the error amplifier inputs overcome the clamp. This provides for a safe and orderly motor start-up from an off or fault condition. A 51-kΩ resister is added between VREF and SSTART to ensure switching.
TACH-OUT	20	Any change in the H1, H2, or H3 inputs loads data from these inputs into the position sensor latches. At the same time data is loaded, a fixed-width 5-V pulse is triggered on TACH-OUT. The average value of the voltage on TACH-OUT is directly proportional to speed, so this output can be used as a true tachometer for speed feedback with an external filter or averaging circuit which usually consists of a resistor and capacitor. Whenever TACH-OUT is high, the position latches are inhibited, such that during the noisiest part of the commutation cycle, additional commutations are not possible. Although this effectively sets a maximum rotational speed, the maximum speed can be set above the highest expected speed, preventing false commutation and chatter.
VCC	19	This device operates with supplies between 10 V and 18 V. Under-voltage lockout keeps all outputs off below 7.5 V, insuring that the output transistors never turn on until full drive capability is available. Bypass VCC to ground with an 0.1-μF ceramic capacitor. Using a 10-μF electrolytic bypass capacitor as well can be beneficial in applications with high supply impedance.
VREF	2	This pin provides regulated 5 V for driving Hall-effect devices and speed control circuitry. VREF reaches 5 V before VCC enables, ensuring that Hall-effect devices powered from VREF becomes active before the UC1625 drives any output. For proper performance VREF should be bypassed with at least a 0.1-μF capacitor to ground.

TYPICAL CHARACTERISTICS

Oscillator Frequency vs C_{OSC} and R_{OSC}

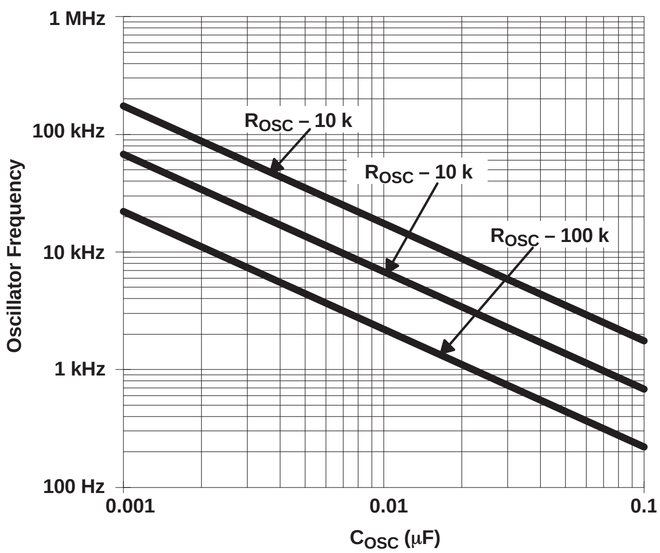


Figure 2.

Tachometer on Time vs RT and CT

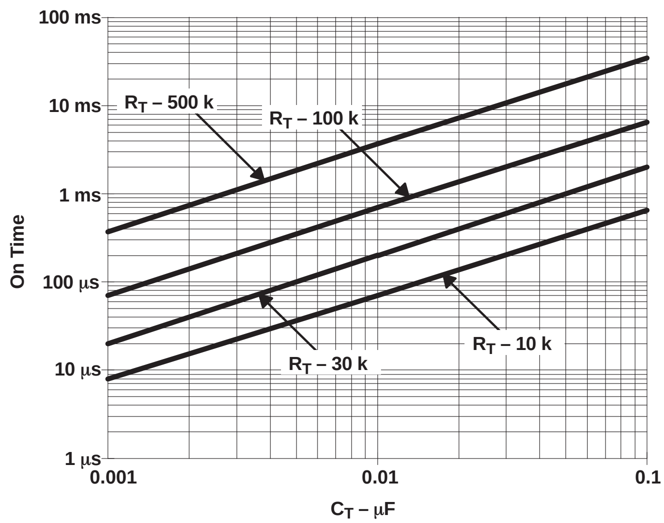


Figure 3.

TYPICAL CHARACTERISTICS (continued)

Supply Current vs Temperature

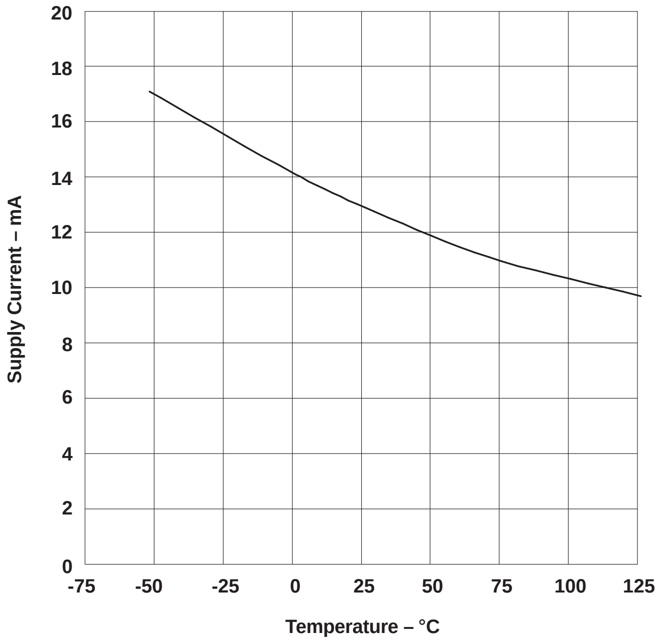


Figure 4.

Soft-Start Pullup Current vs Temperature

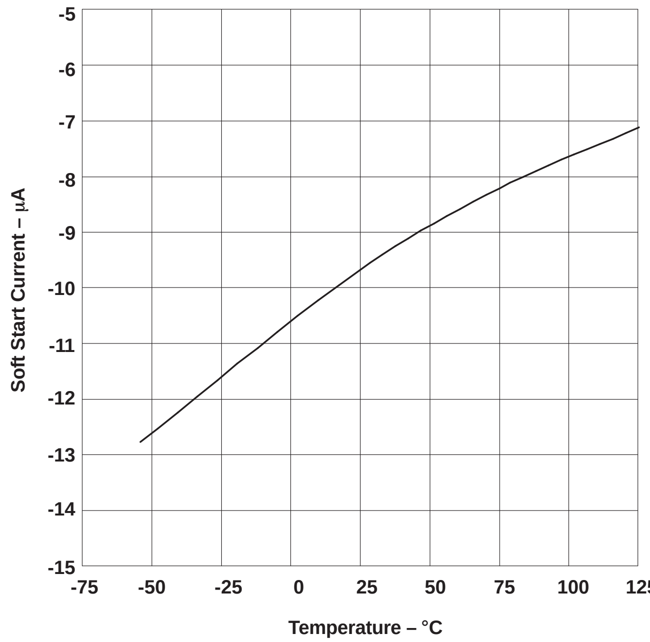


Figure 5.

Soft-Start Discharge Current vs Temperature

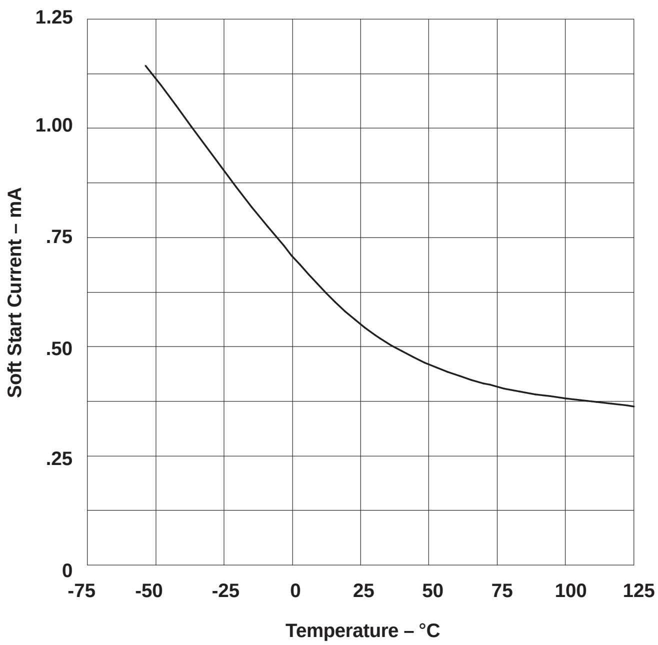


Figure 6.

Current Sense Amplifier Transfer Function vs $I_{SENSE2} - I_{SENSE1}$

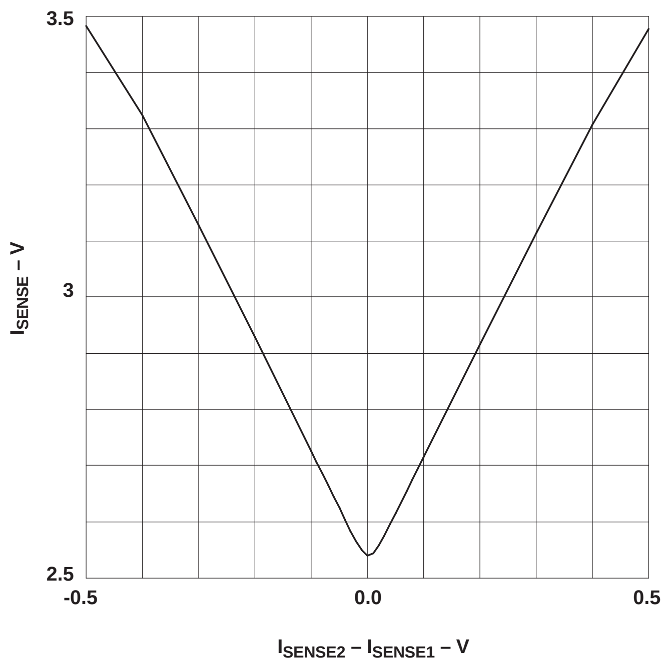


Figure 7.

APPLICATION INFORMATION

Cross Conduction Prevention

The UC1625 inserts delays to prevent cross conduction due to overlapping drive signals. However, some thought must always be given to cross conduction in output stage design because no amount of dead time can prevent fast slewing signals from coupling drive to a power device through a parasitic capacitance.

The UC1625 contains input latches that serve as noise blanking filters. These latches remain transparent through any phase of a motor rotation and latch immediately after an input transition is detected. They remain latched for two cycles of the PWM oscillator. At a PWM oscillator speed of 20 kHz, this corresponds to 50 µs to 100 µs of blank time which limits maximum rotational speed to 100 kRPM for a motor with six transitions per rotation or 50 kRPM for a motor with 12 transitions per rotation.

This prevents noise generated in the first 50 µs of a transition from propagating to the output transistors and causing cross-conduction or chatter.

The UC1625 also contains six flip flops corresponding to the six output drive signals. One of these flip flops is set every time that an output drive signal is turned on, and cleared two PWM oscillator cycles after that drive signal is turned off. The output of each flip flop is used to inhibit drive to the opposing output (Figure 8). In this way, it is impossible to turn on driver PUA and PDA at the same time. It is also impossible for one of these drivers to turn on without the other driver having been off for at least two PWM oscillator clocks.

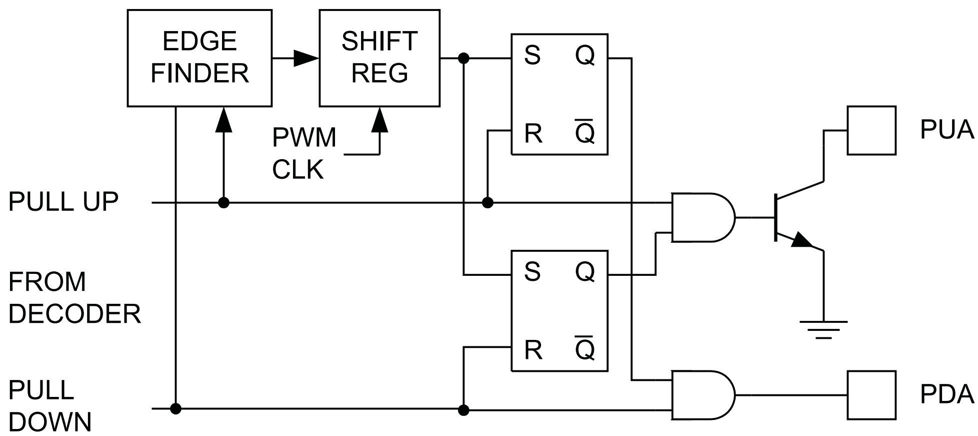


Figure 8. Cross Conduction Prevention

Power Stage Design

The UC1625 is useful in a wide variety of applications, including high-power in robotics and machinery. The power output stages used in such equipment can take a number of forms, according to the intended performance and purpose of the system. Figure 9 show four different power stages with the advantages and disadvantages of each.

For high-frequency chopping, fast recovery circulating diodes are essential. Six are required to clamp the windings. These diodes should have a continuous current rating at least equal to the operating motor current, since diode conduction duty-cycle can be high. For low-voltage systems, Schottky diodes are preferred. In higher voltage systems, diodes such as Microsemi UHVP high voltage platinum rectifiers are recommended.

In a pulse-by-pulse current control arrangement, current sensing is done by resistor R_S, through which the transistor's currents are passed (Fig. A, B, and C). In these cases, R_D is not needed. The low-side circulating diodes go to ground and the current sense terminals of the UC1625 (I_{SENSE1} and I_{SENSE2}) are connected to R_S through a differential RC filter. The input bias current of the current sense amplifier causes a common mode offset voltage to appear at both inputs, so for best accuracy, keep the filter resistors below 2 kΩ and matched.

The current that flows through R_S is discontinuous because of chopping. It flows during the on time of the power stage and is zero during the off time. Consequently, the voltage across R_S consists of a series of pulses, occurring at the PWM frequency, with a peak value indicative of the peak motor current.

To sense average motor current instead of peak current, add another current sense resistor (R_D in Fig. D) to measure current in the low-side circulating diodes, and operate in four quadrant mode (pin 22 high). The negative voltage across R_D is corrected by the absolute value current sense amplifier. Within the limitations imposed by Table 2, the circuit of Fig. B can also sense average current.

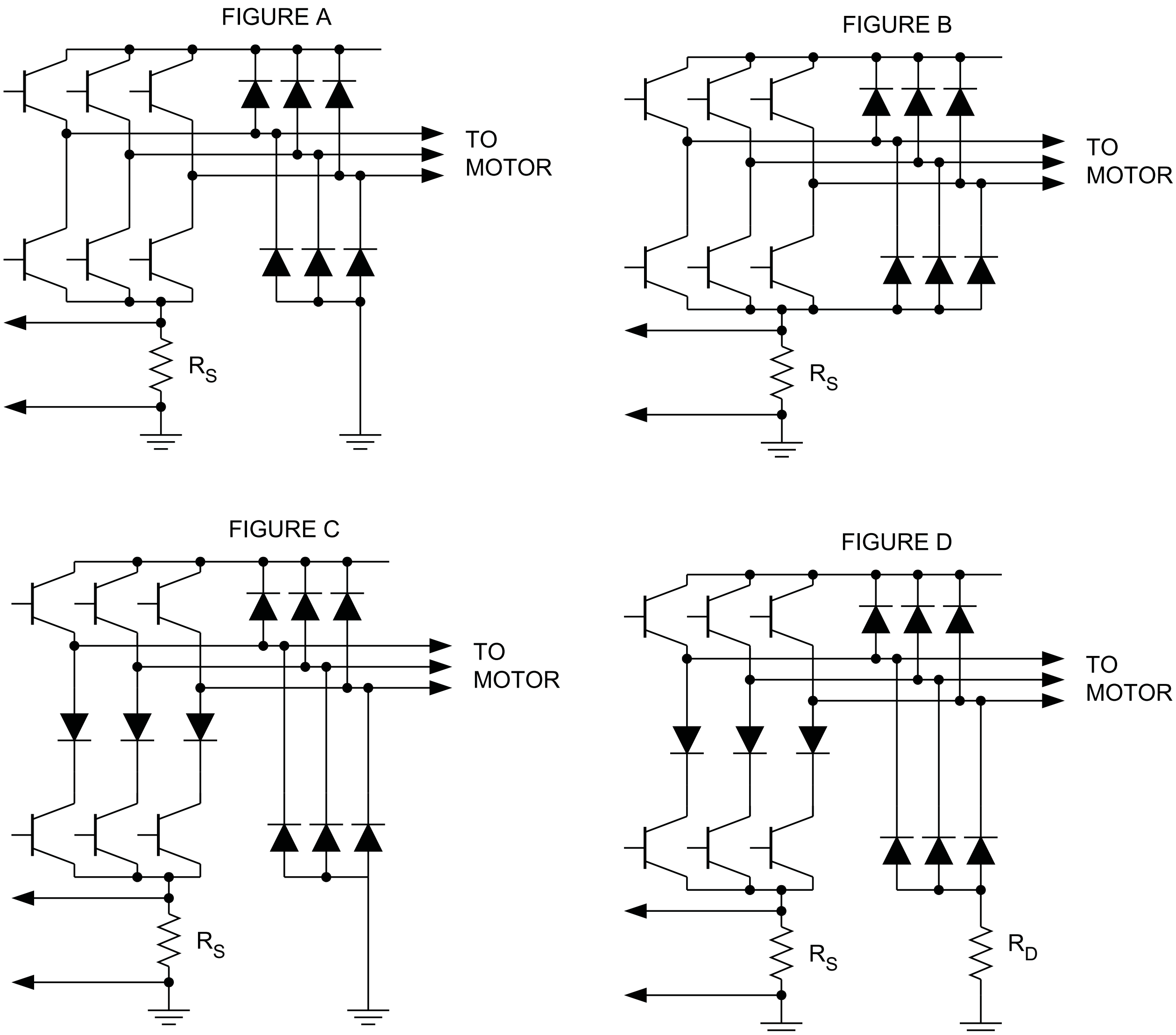


Figure 9. Four Power Stage Designs

Table 2. Imposed Limitations for Figure 9

	2 QUADRANT	4 QUADRANT	SAFE BRAKING	POWER REVERSE	CURRENT SENSE	
					Pulse-by-Pulse	Average
Figure A	Yes	No	No	N0	Yes	No
Figure B	Yes	Yes	No	In 4-quad mode only	Yes	Yes
Figure C	Yes	Yes	Yes	In 4-quad mode only	Yes	No
Figure D	Yes	Yes	Yes	In 4-quad mode only	Yes	Yes

For drives where speed is critical, P-channel MOSFETs can be driven by emitter followers as shown in Figure 10. Here, both the level shift NPN and the PNP must withstand high voltages. A zener diode is used to limit gate-source voltage on the MOSFET. A series gate resistor is not necessary, but always advisable to control overshoot and ringing.

High-voltage optocouplers can quickly drive high-voltage MOSFETs if a boost supply of at least 10 V greater than the motor supply is provided (See Figure 11) To protect the MOSFET, the boost supply should not be higher than 18 V above the motor supply.

For under 200-V 2-quadrant applications, a power NPN driven by a small P-Channel MOSFET performs well as a high-side driver as in Figure 12. A high voltage small-signal NPN is used as a level shift and a high voltage low-current MOSFET provides drive. Although the NPN does not saturate if used within its limitations, the base-emitter resistor on the NPN is still the speed-limiting component.

Figure 13 shows a power NPN Darlington drive technique using a clamp to prevent deep saturation. By limiting saturation of the power device, excessive base drive is minimized and turn-off time is kept fairly short. Lack of base series resistance also adds to the speed of this approach.

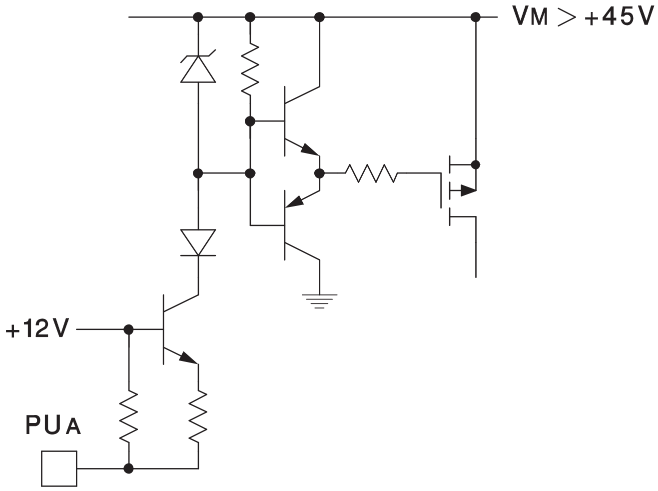


Figure 10. Fast High-Side P-Channel Driver

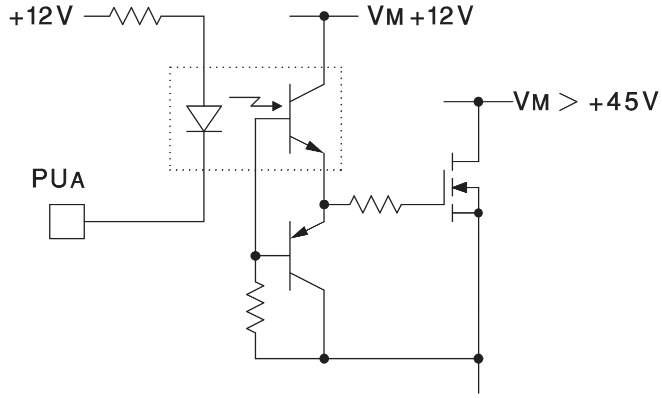


Figure 11. Optocoupled N-Channel High-Side Driver

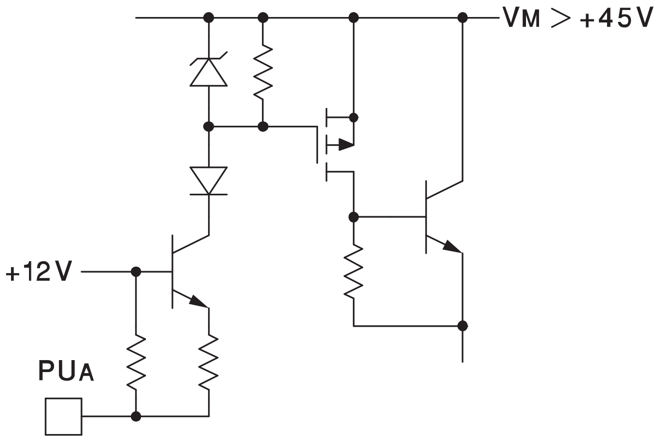


Figure 12. Power NPN High-Side Driver

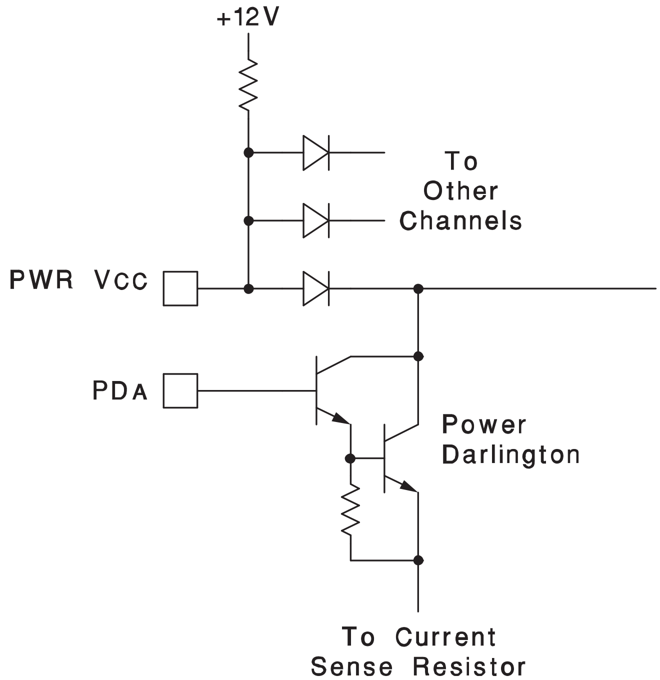


Figure 13. Power NPN Low-Side Driver

Fast High-Side N-Channel Driver with Transformer Isolation

A small pulse transformer can provide excellent isolation between the UC1625 and a high-voltage N-Channel MOSFET while also coupling gate drive power. In this circuit (shown in Figure 14), a UC3724 is used as a transformer driver/encoder that duty-cycle modulates the transformer with a 150-kHz pulse train. The UC3725 rectifies this pulse train for gate drive power, demodulates the signal, and drives the gate with over 2-A peak current.

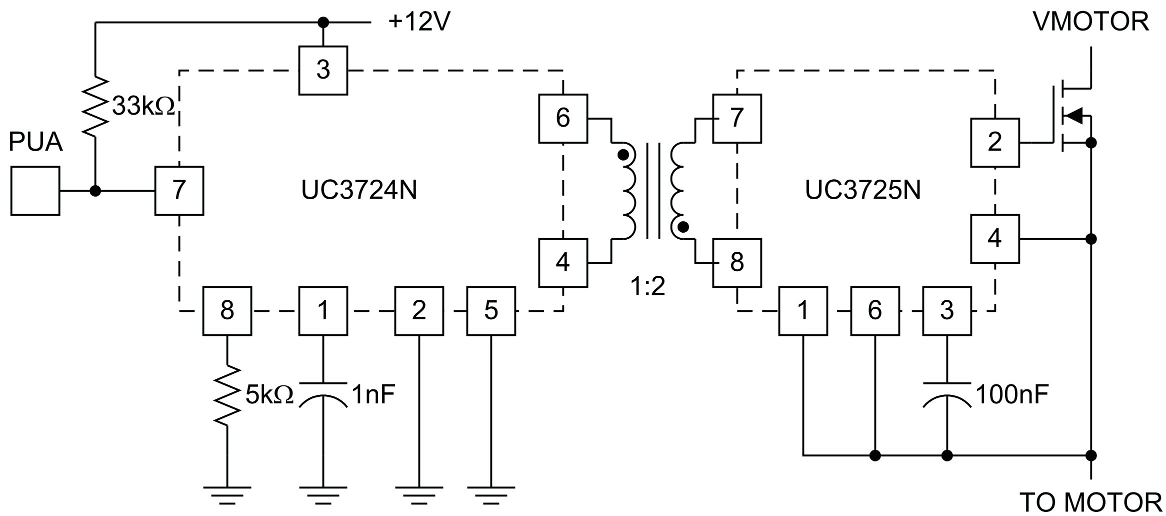


Figure 14. Fast High-Side N-Channel Driver with Transformer Isolation

Both the UC3724 and the UC3725 can operate up to 500 kHz if the pulse transformer is selected appropriately. To raise the operating frequency, either lower the timing resistor of the UC3724 (1 kΩ min), lower the timing capacitor of the UC3724 (500 pF min) or both.

If there is significant capacitance between transformer primary and secondary, together with very high output slew rate, then it may be necessary to add clamp diodes from the transformer primary to 12 V and ground. General purpose small signal switching diodes such as 1N4148 are normally adequate.

The UC3725 also has provisions for MOSFET current limiting. See the UC3725 data sheet for more information on implementing this.

Computational Truth Table

Table 3 shows the outputs of the gate drive and open collector outputs for given hall input codes and direction signals. Numbers at the top of the columns are pin numbers.

These devices operate with position sensor encoding that has either one or two signals high at a time, never all low or all high. This coding is sometimes referred to as "120° Coding" because the coding is the same as coding with position sensors spaced 120 magnetic degrees about the rotor. In response to these position sense signals, only one low-side driver turns on (go high) and one high-side driver turns on (pull low) at any time.

Table 3. Computational Truth Table

INPUTS				OUTPUTS					
DIR	H1	H2	H3	Low-Side			High-Side		
6	8	9	10	12	13	14	16	17	18
1	0	0	1	L	H	L	L	H	H
1	0	1	1	L	L	H	L	H	H
1	0	1	0	L	L	H	H	L	H
1	1	1	0	H	L	L	H	L	H
1	1	0	0	H	L	L	H	H	L
1	1	0	1	L	H	L	H	H	L
0	1	0	1	L	L	H	H	L	H
0	1	0	0	L	L	H	L	H	H
0	1	1	0	L	H	L	L	H	H
0	0	1	0	L	H	L	H	H	L
0	0	1	1	H	L	L	H	H	L
0	0	0	1	H	L	L	H	L	H
X	1	1	1	L	L	L	H	H	H
X	0	0	0	L	L	L	H	H	H

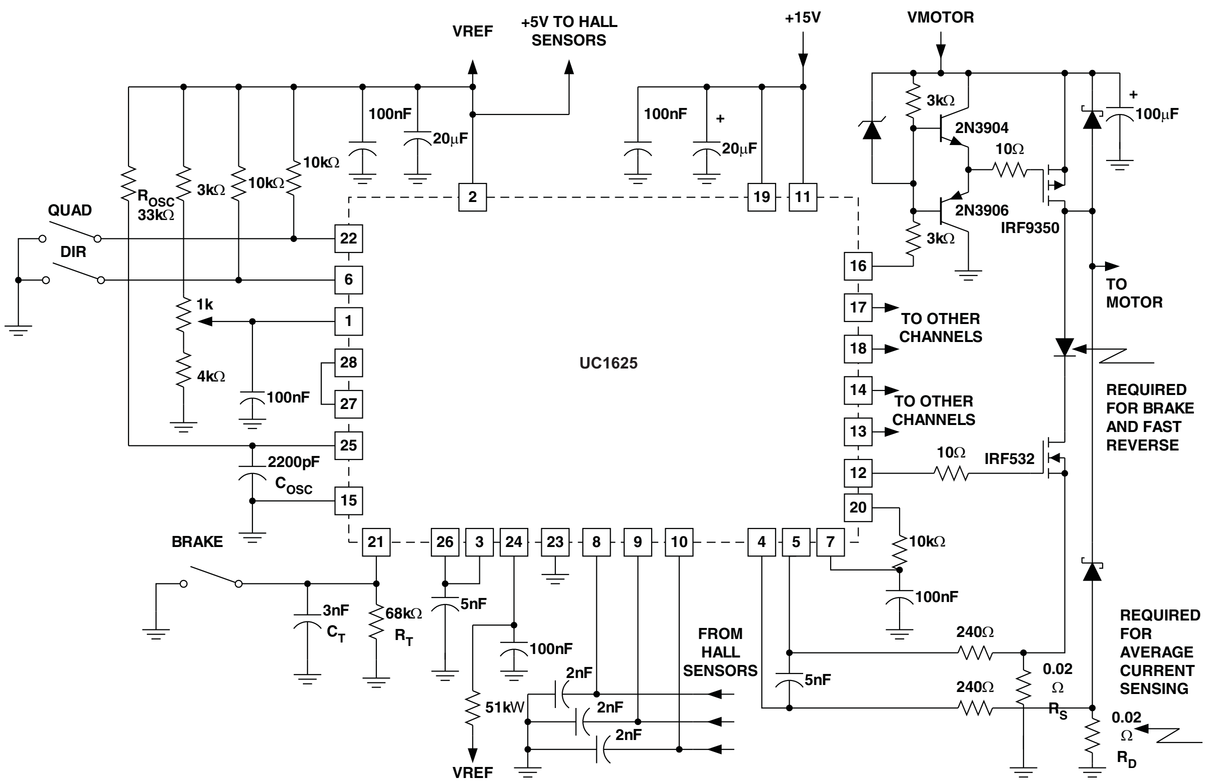


Figure 15. 45-V/8-A Brushless DC Motor Drive Circuit

N-Channel power MOSFETs are used for low-side drivers, while P-Channel power MOSFETs are shown for high-side drivers. Resistors are used to level shift the UC1625 open-collector outputs, driving emitter followers into the MOSFET gate. A 12-V zener clamp insures that the MOSFET gate-source voltage never exceeds 12 V. Series 10-Ω gate resistors tame gate reactance, preventing oscillations and minimizing ringing.

The oscillator timing capacitor should be placed close to pins 15 and 25, to keep ground current out of the capacitor. Ground current in the timing capacitor causes oscillator distortion and slaving to the commutation signal.

The potentiometer connected to pin 1 controls PWM duty cycle directly, implementing a crude form of speed control. This control is often referred to as "voltage mode" because the potentiometer position sets the average motor voltage. This controls speed because steady-state motor speed is closely related to applied voltage.

Pin 20 (Tach-Out) is connected to pin 7 (SPEED IN) through an RC filter, preventing direction reversal while the motor is spinning quickly. In two-quadrant operation, this reversal can cause kinetic energy from the motor to be forced into the power MOSFETs.

A diode in series with the low-side MOSFETs facilitates PWM current control during braking by insuring that braking current will not flow backwards through low-side MOSFETs. Dual current-sense resistors give continuous current sense, whether braking or running in four-quadrant operation, an unnecessary luxury for two-quadrant operation.

The 68-kΩ and 3-nF tachometer components set maximum commutation time at 140 µs. This permits smooth operation up to 35,000 RPM for four-pole motors, yet gives 140 µs of noise blanking after commutation.

PACKAGING INFORMATION

Orderable Device	Status [(1)]	Package Type	Package Drawing	Pins	Package Qty	Eco Plan [(2)]	Lead/ Ball Finish	MSL Peak Temp [(3)]	Samples (Requires Login)
5962-9168902VYA	ACTIVE	CDIP	JT	28	1	TBD	A42	N / A for Pkg Type	

[(1)] The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

[(2)] Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

[(3)] MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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OTHER QUALIFIED VERSIONS OF UC1625-SP :

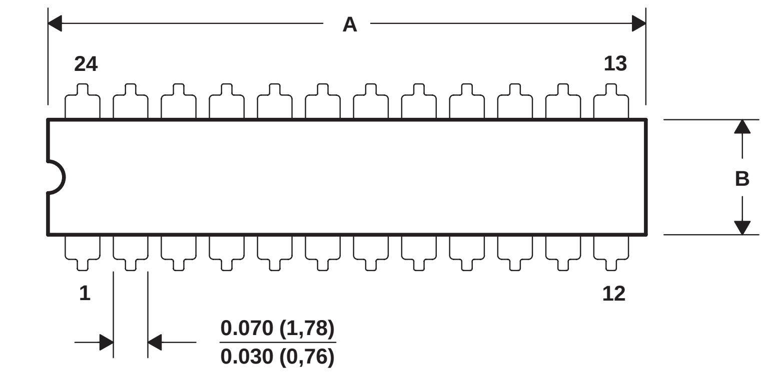
- Catalog: UC1625

NOTE: Qualified Version Definitions:

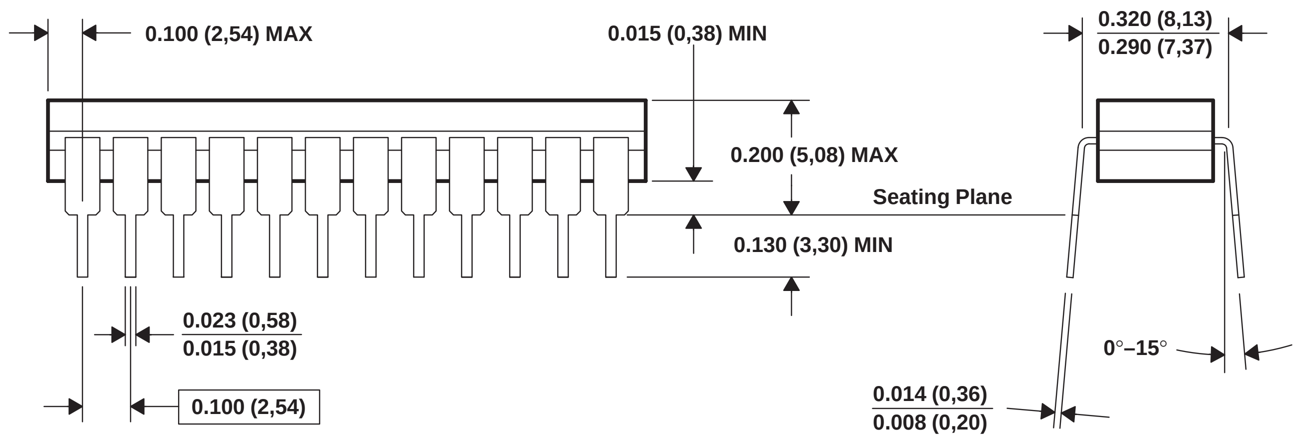
- Catalog - TI's standard catalog product

JT (R-GDIP-T)** **CERAMIC DUAL-IN-LINE**

24 LEADS SHOWN



PINS ** / DIM	24	28
A MAX	1.280 (32,51)	1.460 (37,08)
A MIN	1.240 (31,50)	1.440 (36,58)
B MAX	0.300 (7,62)	0.291 (7,39)
B MIN	0.245 (6,22)	0.285 (7,24)



4040110/C 08/96

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package can be hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for terminal identification.
E. Falls within MIL STD 1835 GDIP3-T24, GDIP4-T28, and JEDEC MO-058 AA, MO-058 AB

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