INTEGRATED CIRCUITS
UNITRODE

UC1851
UC2851
UC3851

Programmable, Off-Line, PWM Controller

FEATURES

- All Control, Driving, Monitoring, and Protection Functions Included
- Low-Current Off Line Start Circuit
- Voltage Feed Forward or Current Mode Control
- High Current Totem Pole Output
- 50% Absolute Max Duty Cycle
- PWM Latch for Single Pulse Per Period
- Pulse-by-Pulse Current Limiting plus Shutdown for Over-Current Fault
- No Start-Up or Shutdown Transients
- Slow Turn-On Both Initially and After Fault Shutdown
- Shutdown Upon Over or Under Voltage Sensing
- Latch Off or Continuous Retry After Fault
- 1% Reference Accuracy
- 500kHz Operation
- 18 Pin DIL or 20 Pin PLCC Package

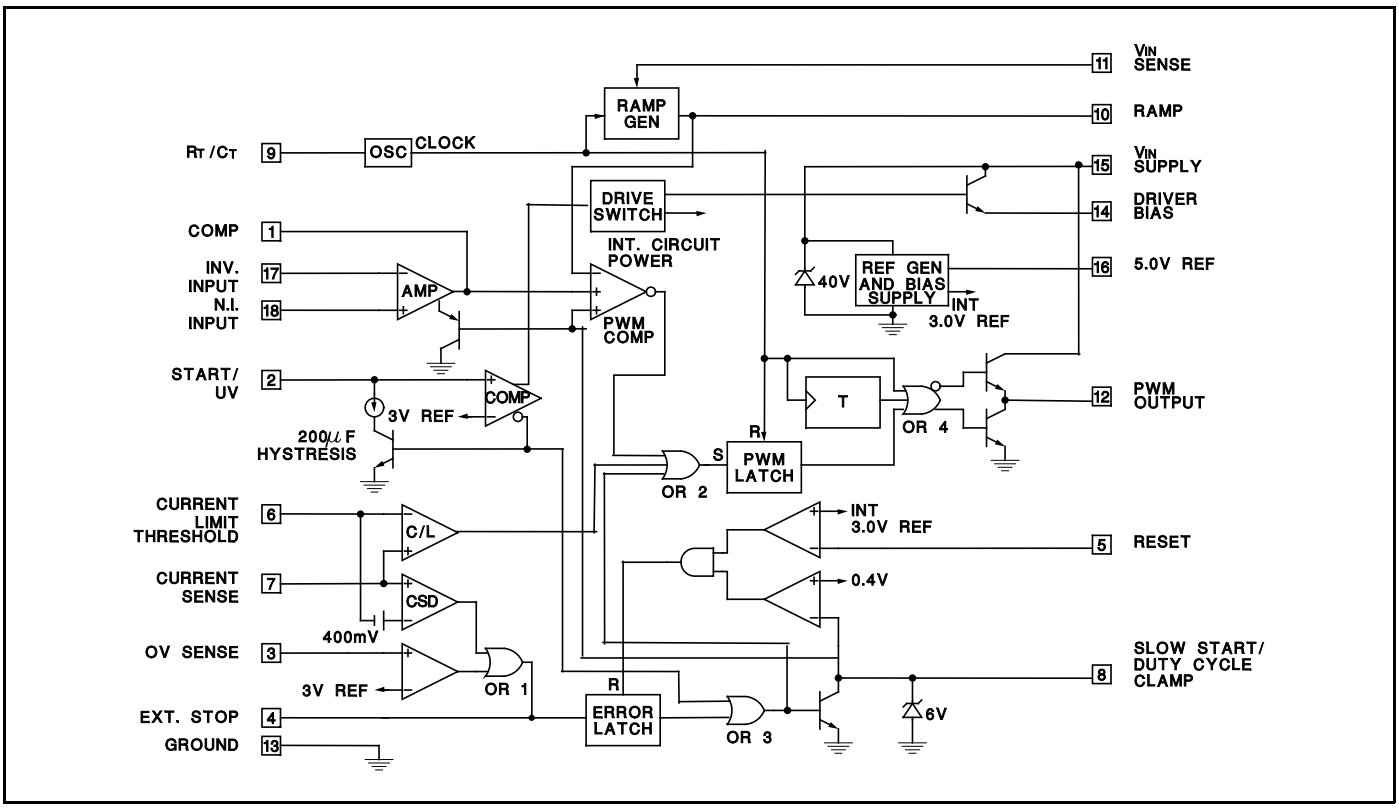
DESCRIPTION

The UC1851 family of PWM controllers are optimized for off-line primary side control. These devices include a high current totem pole output stage and a toggle flip-flop for absolute 50% duty cycle limiting. In all other respects this line of controllers is pin for pin compatible with the UC1841 series. Inclusion of all major housekeeping functions in these high performance controllers makes them ideal for use in cost sensitive applications.

Important features of these controllers include low current start-up, linear feed-forward for constant volt-second operation, and compatibility with both voltage or current mode control. In addition, these devices include a programmable start threshold, as well as programmable over-voltage, under-voltage, and over current fault thresholds. The fault latch on these devices can be configured for automatic restart, or latched off response to a fault.

These devices are packaged in 18-pin plastic or ceramic dual-in-line packages, or for surface mount applications, a 20 Pin PLCC. The UC1851 is characterized for -55°C to +125°C operation while the UC2851 and UC3851 are designed for -40°C to +85°C and 0°C to +70°C, respectively.

BLOCK DIAGRAM



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ABSOLUTE MAXIMUM RATINGS (Note 1)

Supply Voltage, +V_{IN} (Pin 15)
- Voltage Driven . . . . . +32V
- Current Driven, 100mA maximum . . . . . Self-limiting

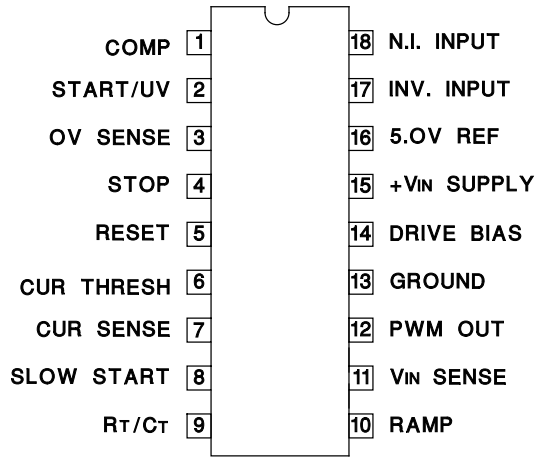
PWM Output Voltage (Pin 12) 40V
PWM Output Current, Steady-State (Pin 12) 400mA
PWM Output Peak Energy Discharge 20µJoules
Driver Bias Current (Pin 14) . . . . . -200mA
Reference Output Current (Pin 16) . . . . . -50mA
Slow-Start Sink Current (Pin 8) 20mA
V_{IN} Sense Current (Pin 11) 10mA
Current Limit Inputs (Pins 6 & 7) . . . . . -0.5 to +5.5V
Stop Input (Pin 4) . . . . . -0.3 to +5.5V

Comparator Inputs
(Pins 1–7, 9–11, 16) . . . . . Internally clamped at 12V
Power Dissipation at T_A = 25°C (Note 3) 1000mW
Power Dissipation at T_C = 25°C (Note 3) 2000mW
Operating Junction Temperature . . . . . -55°C to +150°C
Storage Temperature Range . . . . . -65°C to +150°C
Lead Temperature (Soldering, 10 sec) . . . . . +300°C

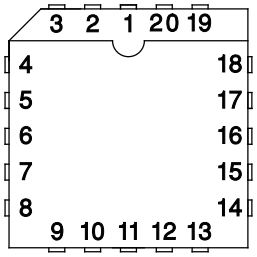
Note 1: All voltages are with respect to ground, Pin 13. Currents are positive-into, negative-out of the specified terminal
Note 2: All pin numbers are referenced to DIL-18 package.
Note 3: Consult Packaging Section of Databook for thermal limitations and considerations of package.

CONNECTION DIAGRAMS

DIL-18, SOIC-18 (TOP VIEW)
J or N, DW Package



PLCC-20, LCC-20
(TOP VIEW)
Q, L PACKAGE



PACKAGE PIN FUNCTIONS	
FUNCTION	PIN
COMP	1
START/UV	2
OV SENSE	3
STOP	4
RESET	5
CUR THRESH	7
CUR SENSE	8
SLOW START	9
RT/CT	10
RAMP	11
VIN SENSE	12
PWM OUT	13
GROUND	14
DRIVE BIAS	15
+VIN SUPPLY	17
5.0V REF	18
INV. INPUT	19
N.I. INPUT	20

ELECTRICAL CHARACTERISTICS:

Unless otherwise stated, these specifications apply for T_A = -55°C to +125°C for the UC1851, -40°C to +85°C for the UC2851, and 0°C to 70°C for the UC3851; V_{IN} = 20V, R_T = 20kΩ, C_T = .001 mfd, R_R = 10kΩ, C_R = .001mfd. Current Limit Threshold = 200mV, T_A = T_J.

PARAMETER	TEST CONDITIONS	UC1851 / UC2851			UC3851			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
Power Inputs								
Start-Up Current	V_{IN} = 30V, Pin 2 = 2.5V		4.5	6		4.5	6	mA
Operating Current	V_{IN} = 30V, Pin 2 = 3.5V		15	21		15	21	mA
Supply OV Clamp	V_{IN} = 20mA	33	39	45	33	39	45	V
Reference Section								
Reference Voltage	T_J = 25°C	4.95	5.0	5.05	4.9	5.0	5.1	V
Line Regulation	V_{IN} = 8 to 30V		10	15		10	20	mV
Load Regulation	I_L = 0 to 10mA		10	20		10	30	mV
Total Ref Variation	Over Operating Temperature Range	4.9		5.1	4.85		5.15	V
Short Circuit Current	V_{REF} = 0, T_J = 25°C		-80	-100		-80	-100	mA
Oscillator								
Nominal Frequency	T_J = 25°C	47	50	53	45	50	55	kHz
Voltage Stability	V_{IN} = 8 to 30V		0.5	1		0.5	1	%
Total Ref Variation	Over Operating Temperature Range	45		55	43		57	kHz
Maximum Frequency	R_T = 2kΩ, C_T = 330pF	500			500			kHz

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ELECTRICAL CHARACTERISTICS: Unless otherwise stated, these specifications apply for T_A = -55°C to +125°C for the UC1851, -40°C to +85°C for the UC2851, and 0°C to 70°C for the UC3851; V_{IN} = 20V, R_T = 20kΩ, C_T = .001 mfd, R_R = 10kΩ, C_R = .001mfd. Current Limit Threshold = 200mV, T_A = T_J.

PARAMETER	TEST CONDITIONS	UC1851 / UC2851			UC3851			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
Ramp Generator								
Ramp Current, Minimum	I_{SENSE} = –10µA		-11	-14		-11	-14	µA
Ramp Current, Maximum	I_{SENSE} = 1.0mA	-0.9	-.95		-0.9	-.95		mA
Ramp Valley		0.3	0.4	0.6	0.3	0.4	0.6	V
Ramp Peak	Clamping Level	3.9	4.2	4.5	3.9	4.2	4.5	V
Error Amplifier								
Input Offset Voltage	V_{CM} = 5.0V		0.5	5		2	10	mV
Input Bias Current			0.5	2		1	5	µA
Input Offset Current				0.5			0.5	µA
Open Loop Gain	ΔV_O = 1 to 3V	60	66		60	66		dB
Output Swing (Max Output ≤ Ramp Peak - 100mV)	Minimum Total Range	0.3		3.5	0.3		3.5	V
CMRR	V_{CM} = 1.5 to 5.5V	70	80		70	80		dB
PSRR	V_{IN} = 8 to 30V	70	80		70	80		dB
Short Circuit Current	V_{COMP} = 0V		-4	-10		-4	-10	mA
Gain Bandwidth (Note 1)	T_J = 25°C, A_{VOL} = 0dB	1	2		1	2		MHz
Slew Rate (Note 1)	T_J = 25°C, A_{VCL} = 0dB		0.8			0.8		V/µs
PWM Section								
Continuous Duty Cycle Range (other than zero) (Note 1)	Minimum Total Continuous Range Ramp Peak < 4.2V	2		46	2		46	%
Output High Level	I_{SOURCE} = 20mA	18	18.5		18	18.5		V
	I_{SOURCE} = 200mA	17	18.5		17	18.5		V
Rise Time (Note 1)	T_J = 25°C, C_L = 1nF		50	150		50	150	ns
Fall Time (Note 1)	T_J = 25°C, C_L = 1nF		50	150		50	150	ns
Output Saturation	I_{OUT} = 20mA		0.2	0.4		0.2	0.4	V
	I_{OUT} = 200mA		1.7	2.2		1.7	2.2	V
Comparator Delay (Note 1)	Pin 8 to Pin 12, T_J = 25°C, R_L = 1kΩ		300	500		300	500	ns
Sequencing Functions								
Comparator Thresholds	Pins 2, 3, 5	2.8	3.0	3.2	2.8	3.0	3.2	V
Input Bias Current	Pins 3, 5 = 0V		-1.0	-4.0		-1.0	-4.0	µA
Input Leakage	Pins 3, 5 = 10V		0.1	2.0		0.1	2.0	µA
Start/UV Hysteresis Current	Pin 2 = 2.5V	170	200	220	170	200	230	µA
Ext. Stop Threshold	Pin 4	0.8	1.6	2.4	0.8	1.6	2.4	V
Error Latch Activate Current	Pin 4 = 0V, Pin 3 > 3V		-120	-200		-120	-200	µA
Driver Bias Saturation Voltage, V_{IN}-V_{OH}	I_B = -50mA		2	3		2	3	V
Driver Bias Leakage	V_B = 0V		-0.1	-10		-0.1	-10	µA
Slow-Start Saturation	I_S = 10mA		0.2	0.5		0.2	0.5	V
Slow-Start Leakage	V_S = 4.5V		0.1	2.0		0.1	2.0	µA
Current Control								
Current Limit Offset			0	5		0	10	mV
Current Shutdown Offset		370	400	430	360	400	440	mV
Input Bias Current	Pin 7 = 0V		-2	-5		-2	-5	µA
Common Mode Range (Note 1)		-0.4		3.0	-0.4		3.0	V
Current Limit Delay (Note 1)	T_J = 25°C, Pin 7 to 12, R_L = 1k		200	400		200	400	ns

Note 1:Guaranteed by design. Not 100% tested in production.

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FUNCTIONAL DESCRIPTION

PWM CONTROL	
1. Oscillator	Generates a fixed-frequency internal clock from an external R_T and C_T. Frequency = $\frac{K_C}{R_T C_T}$ where K_C is a first-order correction factor $\approx$ 0.3 log (C_T x 10^{12}).
2. Ramp Generator:	Develops linear ramp with slope defined externally by $\frac{dV}{dT} = \frac{\text{sense voltage}}{R_R C_R}$. C_R is normally selected $\leq C_T$ and its value will have some effect upon valley duty cycle. Limiting the minimum value for I_{SENSE} into pin 11 will establish a maximum duty cycle clamp. C_R terminal can be used as an input port for current mode control.
3. Error Amplifier	Conventional operational amplifier for closed-loop gain and phase compensation. Low output impedance; unity-gain stable. The output is held low by the slow start voltage at turn on in order to minimize overshoot.
4. Reference Generator:	Precision 5.0V for internal and external usage to 50mA. Tracking 3.0V reference for internal usage only with nominal accuracy of ±2%. 40V clamp zener for chip OV protection, 100mA maximum current.
5. PWM Comparator:	Generates output pulse which starts at termination of clock pulse and ends when the ramp input crosses the lowest of two positive inputs.
6. PWM Latch:	Terminates the PWM output pulse when set by inputs from either the PWM comparator, the pulse-by-pulse comparator, or the error latch. Resets with each internal clock pulse.
7. PWM Output Switch:	Totem pole output stage capable of sourcing and sinking 1 amp peak current. The active "on" state is high.
SEQUENCING FUNCTIONS	
1. Start/UV Sense:	With an increasing voltage, this comparator generates a turn-on signal and releases the slow start clamp at a start threshold. With a decreasing voltage, it generates a turn-off command at a lower level separated by a 200µA hysteresis current.
2. Drive Switch:	Disables most of the chip to hold internal current consumption low, and Driver Bias OFF, until input voltage reaches start threshold.
3. Driver Bias:	Supplies drive to external circuitry upon start-up.
4. Slow Start:	Clamps low to hold PWM OFF. Upon release, rises with rate controlled by $R_S C_S$ for slow increase of output pulse width. Can also be used as an alternate maximum duty cycle clamp with an external voltage divider.
PROTECTION FUNCTIONS	
1. Error Latch:	When set by momentary input, this latch insures immediate PWM shutdown and hold off until reset. Inputs to Error Latch are: a. OV > 3.2V (Typically 3V) b. Stop > 2.4V (Typically 1.6V) c. Current Sense 400mV over threshold. (Typical). Error Latch resets when slow start voltage falls to 0.4V if Reset Pin < 2.8V. With Pin 5 > 3.2V, Error Latch will remain set.
2. Current Limiting:	Differential input comparator terminates individual output pulses each time sense voltage rises above threshold. When sense voltage rises to 400mV (typical) above threshold, a shutdown signal is sent to Error Latch.
3. External Stop:	A voltage over 2.4 will set the Error Latch and hold the output off. A voltage less than 0.8V will defeat the error latch and prevent shutdown. A capacitor here will slow the action of the error latch for transient protection by providing a Typical Delay of 13ms/µF.

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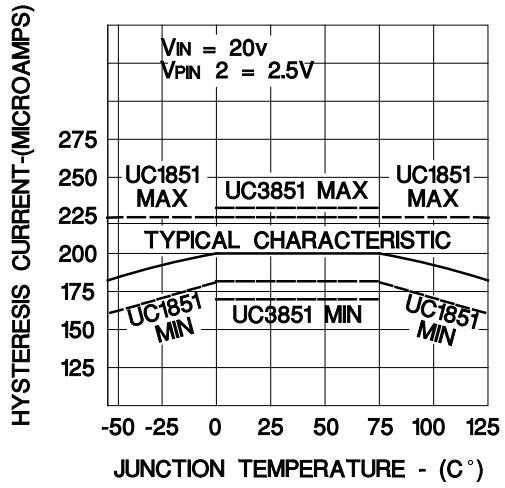
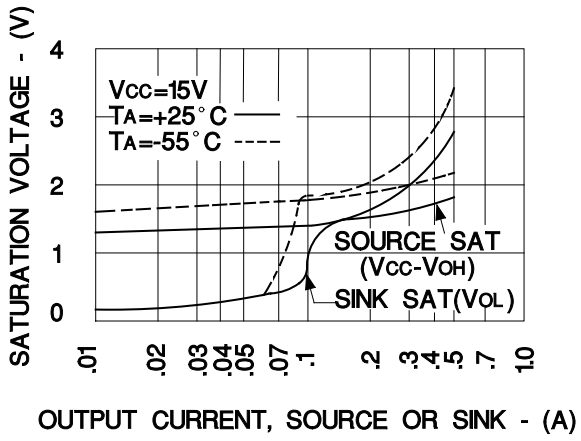
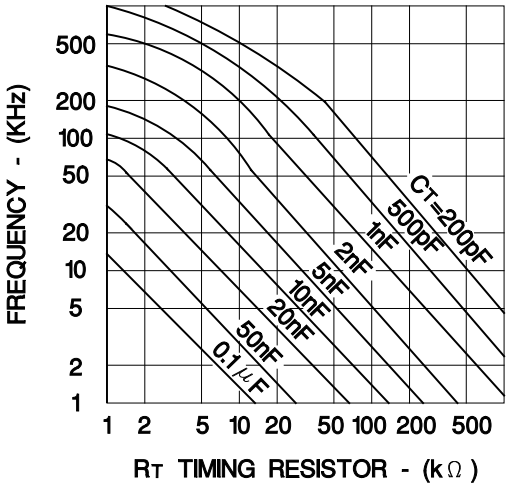
Start/UV Hysteresis Current



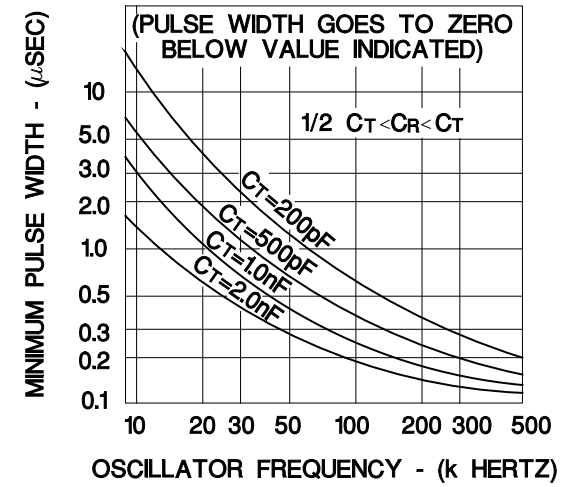
Output Saturation Characteristics



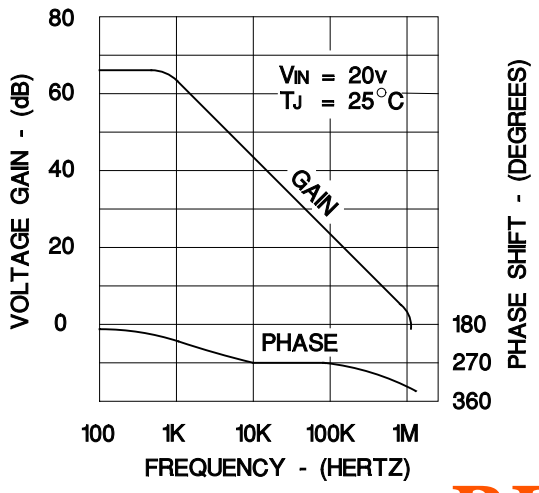
Oscillator Frequency



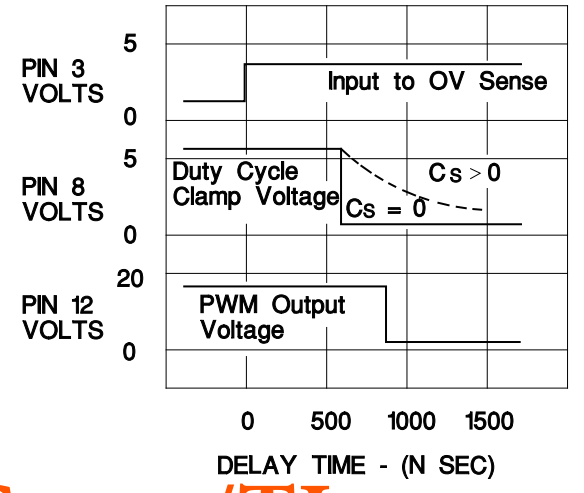
PWM Output Minimum Pulse Width



Error Amplifier Open-Loop Gain and Phase



Shutdown Timing



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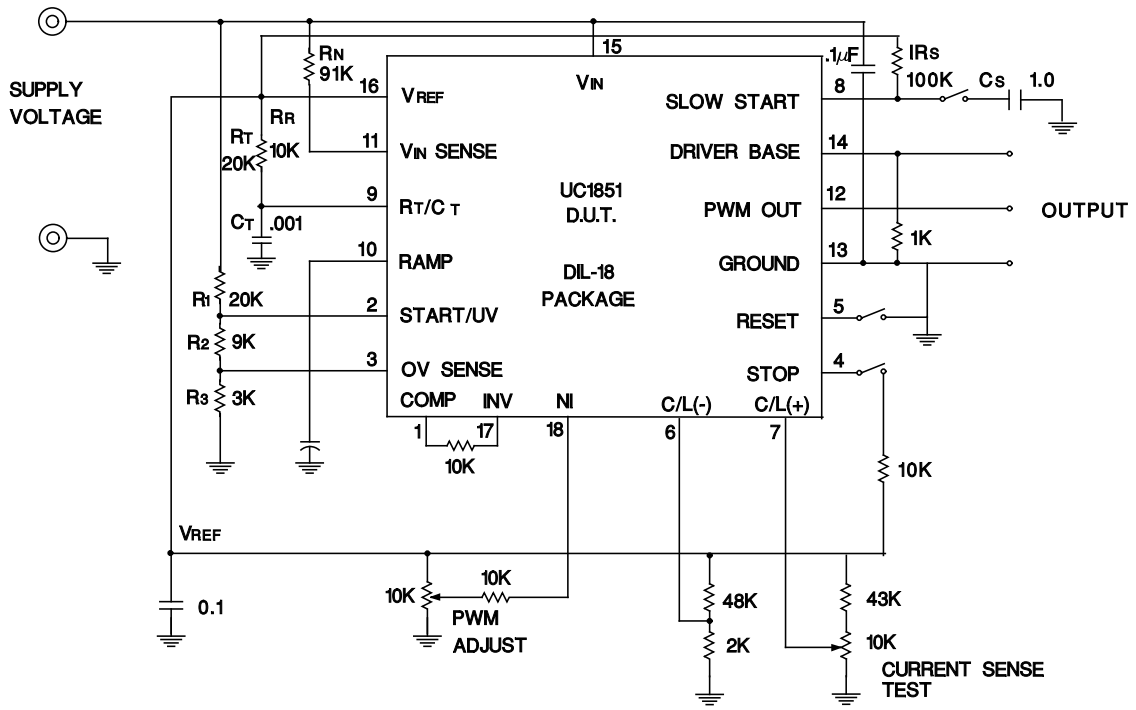
OPEN-LOOP CIRCUIT



Nominal Frequency = $\frac{1}{R_T C_T}$ = 50kHz

Start Voltage = $3\left(\frac{R1+R2+R3}{R2+R3}\right)$ +0.2R1 = 12V

UV Fault Voltage = $3\left(\frac{R1+R2+R3}{R2+R3}\right)$ = 8V

OV Fault Voltage = $3\left(\frac{R1+R2+R3}{R3}\right)$ = 32V

Current Limit = 200mV

Current Fault Voltage = 600mV

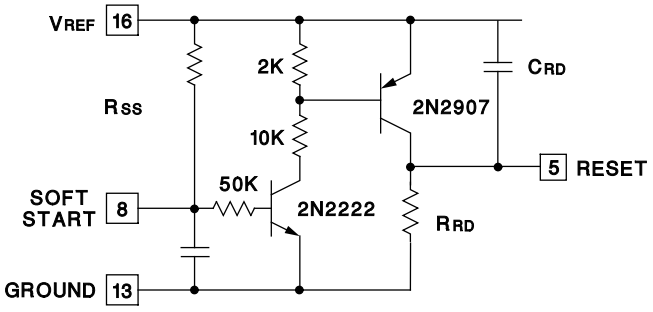
Duty Cycle Clamp = 50%

@VIN = 15V, Duty Cycle = 48%

@VIN = 30V, Duty Cycle = 24%

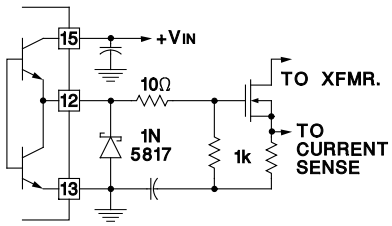
High Peak currents associated with capacitive loads necessitate careful grounding techniques. Timing and bypass capacitors should be connected close to pin 13 in a single ground point.

Programmable Soft Start and Restart Delay Circuit

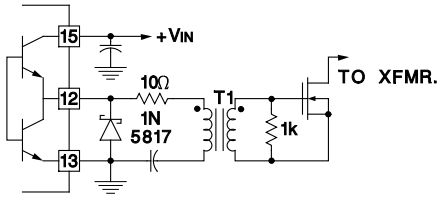


For further application information see UC1840/UC1841 Data Sheets

UC1851 Power MOSFET Drive Interface



(A) DIRECT DRIVE



(B) TRANSFORMER COUPLED

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)
5962-9558601MVA	OBSOLETE	CDIP	J	18		TBD	Call TI	Call TI
UC1851J	OBSOLETE	CDIP	J	18		TBD	Call TI	Call TI
UC1851J883B	OBSOLETE	CDIP	J	18		TBD	Call TI	Call TI
UC2851DW	ACTIVE	SOIC	DW	18	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
UC2851DWG4	ACTIVE	SOIC	DW	18	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
UC2851N	ACTIVE	PDIP	N	18	20	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type
UC2851NG4	ACTIVE	PDIP	N	18	20	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type
UC3851DW	ACTIVE	SOIC	DW	18	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
UC3851DWG4	ACTIVE	SOIC	DW	18	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
UC3851DWTR	ACTIVE	SOIC	DW	18	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
UC3851DWTRG4	ACTIVE	SOIC	DW	18	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
UC3851N	ACTIVE	PDIP	N	18	20	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type
UC3851NG4	ACTIVE	PDIP	N	18	20	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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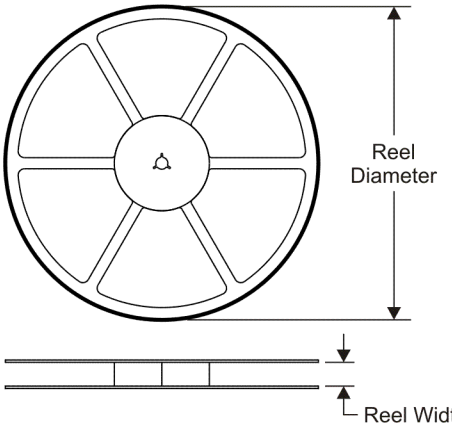
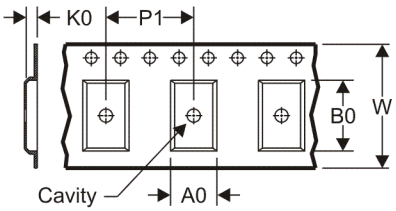
TAPE AND REEL INFORMATION

REEL DIMENSIONS

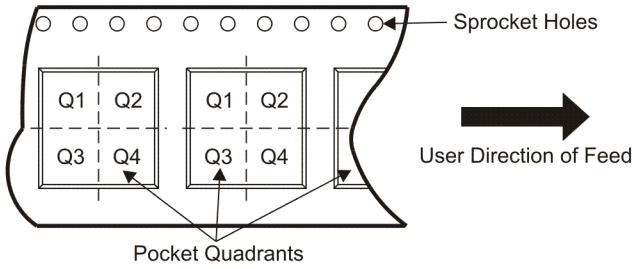


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
UC3851DWTR	SOIC	DW	18	2000	330.0	24.4	10.9	12.0	2.7	12.0	24.0	Q1

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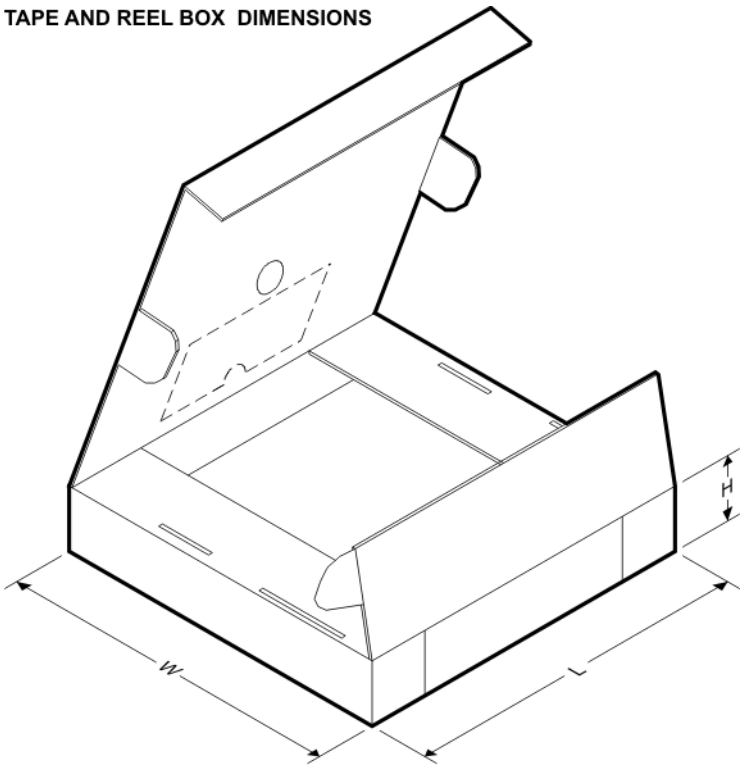
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
UC3851DWTR	SOIC	DW	18	2000	346.0	346.0	41.0

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