application INFO available

UC1842A/3A/4A/5A
UC2842A/3A/4A/5A
UC3842A/3A/4A/5A

Current Mode PWM Controller

FEATURES

- Optimized for Off-line and DC to DC Converters
- Low Start Up Current (<0.5mA)
- Trimmed Oscillator Discharge Current
- Automatic Feed Forward Compensation
- Pulse-by-Pulse Current Limiting
- Enhanced Load Response Characteristics
- Under-Voltage Lockout With Hysteresis
- Double Pulse Suppression
- High Current Totem Pole Output
- Internally Trimmed Bandgap Reference
- 500kHz Operation
- Low Ro Error Amp

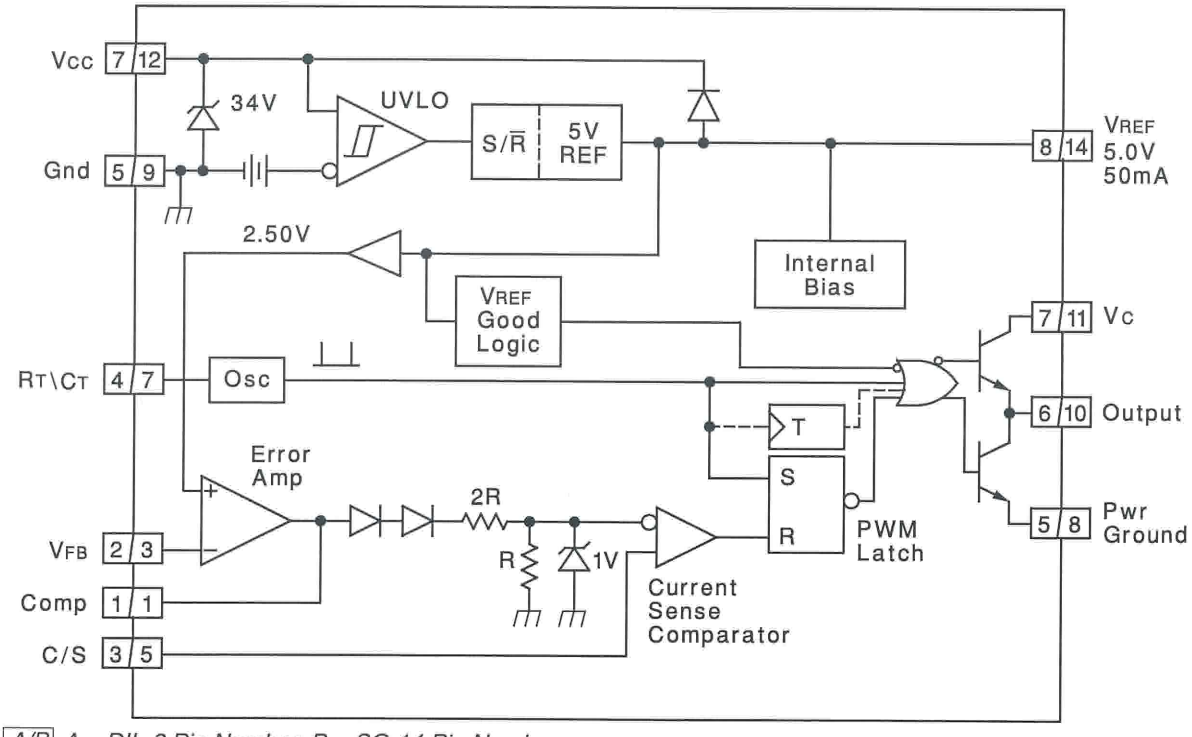
DESCRIPTION

The UC1842A/3A/4A/5A family of control ICs is a pin for pin compatible improved version of the UC3842/3/4/5 family. Providing the necessary features to control current mode switched mode power supplies, this family has the following improved features. Start up current is guaranteed to be less than 0.5mA. Oscillator discharge is trimmed to 8.3mA. During under voltage lockout, the output stage can sink at least 10mA at less than 1.2V for Vcc over 5V.

The difference between members of this family are shown in the table below.

Part #	UVLO On	UVLO Off	Maximum Duty Cycle
UC1842A	16.0V	10.0V	<100%
UC1843A	8.5V	7.9V	<100%
UC1844A	16.0V	10.0V	<50%
UC1845A	8.5V	7.9V	<50%

BLOCK DIAGRAM



Note 1: A/B A = DIL-8 Pin Number. B = SO-14 Pin Number.
Note 2: Toggle flip flop used only in 1844A and 1845A.

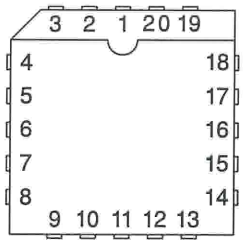
CONNECTION DIAGRAMS

ABSOLUTE MAXIMUM RATINGS (Note 1)

Supply Voltage (Low Impedance Source) 30V
Supply Voltage (I_{CC} mA) . . . . . Self Limiting
Output Current . . . . . ±1A
Output Energy (Capacitive Load) 5µJ
Analog Inputs (Pins 2, 3) . . . . . -0.3V to +6.3V
Max negative voltage all pins . . . . . -0.3V
For 14 and 20 pin packages . . . . . (V_C - V_{CC}) > -0.3V
Error Amp Output Sink Current 10mA
Power Dissipation at $T_A \leq 25°C$ (DIL-8) 1W
Storage Temperature Range . . . . . -65°C to +150°C
Junction Temperature Range . . . . . -55°C to +150°C
Lead Temperature (Soldering, 10 Seconds) . . . . . 300°C

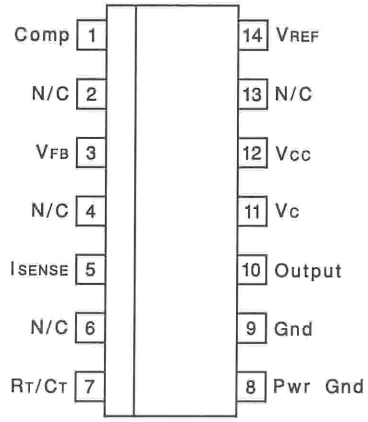
Note 1. All voltages are with respect to Ground, Pin 5. Currents are positive into, negative out of the specified terminal. Consult Packaging Section of Databook for thermal limitations and considerations of packages. Pin numbers refer to DIL package only. The GND pins and the PGND pins must be connected to each other with short thick traces.

PLCC-20, LCC-20 (TOP VIEW)
Q, L Packages

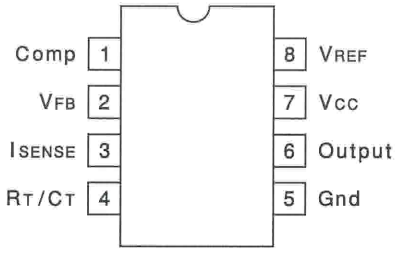


PACKAGE PIN FUNCTION	
FUNCTION	PIN
N/C	1
Comp	2
N/C	3-4
V_{FB}	5
N/C	6
I_{SENSE}	7
N/C	8-9
R_T/C_T	10
N/C	11
Pwr Gnd	12
Gnd	13
N/C	14
Output	15
N/C	16
V_C	17
V_{CC}	18
N/C	19
V_{REF}	20

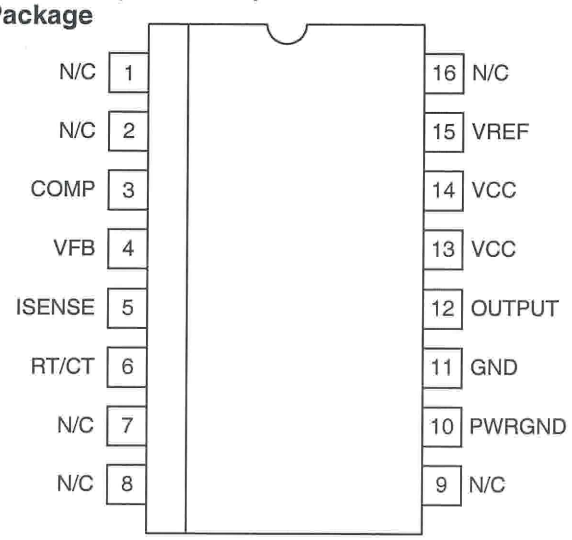
SOIC-14 (TOP VIEW)
D Package



DIL-8, SOIC-8 (TOP VIEW)
J or N, D8 Package



SOIC-WIDE16 (TOP VIEW)
DW Package



THERMAL CHARACTERISTICS

Over operating free-air temperature range (unless otherwise noted)

PACKAGE		θ_{JC}	θ_{JA}
DIL - 8	J	28(1)	125 - 160
	N	25	110(2)
SOIC - 8	D8	42	84 - 160(2)
SOIC - 14	D14	35	50 - 120(2)
CFP - 14	W	5.49 °C/W	175.4 °C/W
PLCC - 20	Q	34	43 - 75(2)
SOIC Wide 16	DW	27	50 - 100(2)
LLC - 20	L	20(3)	70 - 80

(1) θ_{JC} data values stated were derived from MIL-STD-1835B.
(2) Specified θ_{JA} (junction to ambient) is for devices mounted to 5 in^2 FR4 PC board with one ounce copper where noted. When resistance range is given, lower values are for 5 in^2. Test PWB was 0.062 in thick and typically used 0.635-mm trace widths for power packages and 1.3-mm trace widths for non-power packages with 100 x 100-mil probe land area at the end of each trace.
(3) θ_{JC} data values stated were derived from MIL-STD-1835B. MIL-STD-1835B states that "The baseline values shown are worse case (mean+2s) for a 60 x 60 mil microcircuit device silicon die and applicable for devices with die sizes up to 144000 square mils. For device sizes greater than 14400 square mils use the following values; dual-in-line, 11°C/W; flat pack, 10°C/W; pin grid array, 10°C/W".

DISSIPATION RATINGS

PACKAGE	$T_A \leq 25°C$ POWER RATINGc	DERATING FACTOR ABOVE $T_A \leq 25°C$	$T_A \leq 70°C$ POWER RATING	$T_A \leq 80°C$ POWER RATING	$T_A \leq 125°C$ POWER RATING
W	700 mW	5.5 mW/°C	452 mW	370 mW	150 mW

ELECTRICAL CHARACTERISTICS Unless otherwise stated, these specifications apply for –55°C ≤ T_A ≤ 125°C for the UC184xA; –40°C ≤ T_A ≤ 125°C for the UC284xAQ; –40°C ≤ T_A ≤ 85°C for the UC284xA; 0 ≤ T_A ≤ 70°C for the UC384xA; V_{CC} = 15V (Note 5); R_T = 10k; C_T = 3.3nF; T_A = T_J; Pin numbers refer to DIL-8.

PARAMETER	TEST CONDITIONS	UC184xA\UC284xA			UC384xA			UNITS
		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
Reference Section								
Output Voltage	T_J = 25°C, I_O = 1mA	4.95	5.00	5.05	4.90	5.00	5.10	V
Line Regulation	12 ≤ V_{IN} 25V		6	20		6	20	mV
Load Regulation	1 ≤ I_O ≤ 20mA		6	25		6	25	mV
Temp. Stability	(Note 2, Note 7)		0.2	0.4		0.2	0.4	mV/°C
Total Output Variation	Line, Load, Temp.	4.9		5.1	4.82		5.18	V
Output Noise Voltage	10Hz ≤ f ≤ 10kHz T_J = 25°C (Note 2)		50			50		µV
Long Term Stability	T_A = 125°C, 1000Hrs. (Note 2)		5	25		5	25	mV
Output Short Circuit		-30	-100	-180	-30	-100	-180	mA
Oscillator Section								
Initial Accuracy	T_J = 25°C (Note 6)	47	52	57	47	52	57	kHz
Voltage Stability	12 ≤ V_{CC} ≤ 25V		0.2	1		0.2	1	%
Temp. Stability	T_{MIN} ≤ T_A ≤ T_{MAX} (Note 2)		5			5		%
Amplitude	$V_{PIN\ 4}$ peak to peak (Note 2)		1.7			1.7		V
Discharge Current	T_J = 25°C, $V_{PIN\ 4}$ = 2V (Note 8)	7.8	8.3	8.8	7.8	8.3	8.8	mA
	$V_{PIN\ 4}$ = 2V (Note 8)	7.5		8.8	7.6		8.8	mA
Error Amp Section								
Input Voltage	$V_{PIN\ 1}$ = 2.5V	2.45	2.50	2.55	2.42	2.50	2.58	V
Input Bias Current			-0.3	-1		-0.3	-2	µA
A_{VOL}	2 ≤ V_O ≤ 4V	65	90		65	90		dB
Unity Gain Bandwidth	T_J = 25°C (Note 2)	0.7	1		0.7	1		MHz
PSRR	12 ≤ V_{CC} ≤ 25V	60	70		60	70		dB
Output Sink Current	$V_{PIN\ 2}$ = 2.7V, $V_{PIN\ 1}$ = 1.1V	2	6		2	6		mA
Output Source Current	$V_{PIN\ 2}$ = 2.3V, $V_{PIN\ 1}$ = 5V	-0.5	-0.8		-0.5	-0.8		mA
V_{OUT} High	$V_{PIN\ 2}$ = 2.3V, R_L = 15k to ground	5	6		5	6		V
V_{OUT} Low	$V_{PIN\ 2}$ = 2.7V, R_L = 15k to Pin 8		0.7	1.1		0.7	1.1	V
Current Sense Section								
Gain	(Note 3, Note 4)	2.85	3	3.15	2.85	3	3.15	V/V
Maximum Input Signal	$V_{PIN\ 1}$ = 5V (Note 3)	0.9	1	1.1	0.9	1	1.1	V
PSRR	12 ≤ V_{CC} ≤ 25V (Note 3)		70			70		dB
Input Bias Current			-2	-10		-2	-10	µA
Delay to Output	$V_{PIN\ 3}$ = 0 to 2V (Note 2)		150	300		150	300	ns
Output Section								
Output Low Level	I_{SINK} = 20mA		0.1	0.4		0.1	0.4	V
	I_{SINK} = 200mA		1.5	2.2		1.5	2.2	V
Output High Level	I_{SOURCE} = 20mA	13	13.5		13	13.5		V
	I_{SOURCE} = 200mA	12	13.5		12	13.5		V
Rise Time	T_J = 25°C, C_L = 1nF (Note 2)		50	150		50	150	ns
Fall Time	T_J = 25°C, C_L = 1nF (Note 2)		50	150		50	150	ns
UVLO Saturation	V_{CC} = 5V, I_{SINK} = 10mA		0.7	1.2		0.7	1.2	V

ELECTRICAL CHARACTERISTICS Unless otherwise stated, these specifications apply for –55°C ≤ T_A ≤ 125°C for the UC184xA; –40°C ≤ T_A ≤ 125°C for the UC284xAQ; –40°C ≤ T_A ≤ 85°C for the UC284xA; 0 ≤ T_A ≤ 70°C for the UC384xA; V_{CC} = 15V (Note 5); R_T = 10k; C_T = 3.3nF; T_A = T_J; Pin numbers refer to DIL-8.

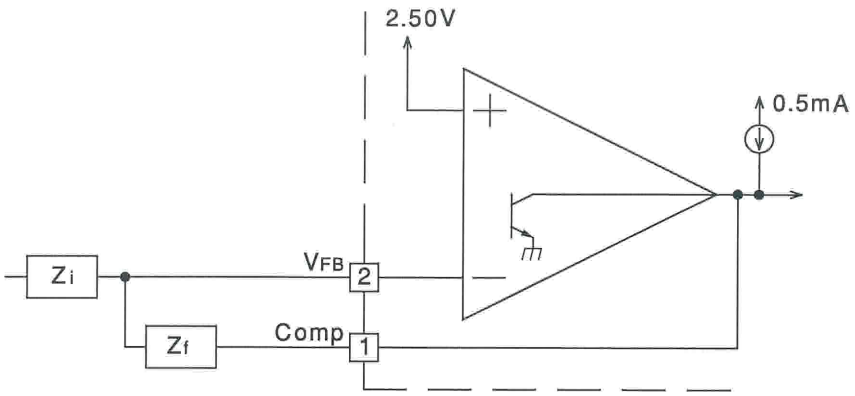
PARAMETER	TEST CONDITIONS	UC184xA\UC284xA			UC384xA			UNITS
		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
Under-Voltage Lockout Section								
Start Threshold	x842A/4A	15	16	17	14.5	16	17.5	V
	x843A/5A	7.8	8.4	9.0	7.8	8.4	9.0	V
Min. Operation Voltage After	x842A/4A	9	10	11	8.5	10	11.5	V
Turn On	x843A/5A	7.0	7.6	8.2	7.0	7.6	8.2	V
PWM Section								
Maximum Duty Cycle	x842A/3A	94	96	100	94	96	100	%
	x844A/5A	47	48	50	47	48	50	%
Minimum Duty Cycle				0			0	%
Total Standby Current								
Start-Up Current			0.3	0.5		0.3	0.5	mA
Operating Supply Current	$V_{PIN\ 2}$ = $V_{PIN\ 3}$ = 0V		11	17		11	17	mA
V_{CC} Zener Voltage	I_{CC} = 25mA	30	34		30	34		V

Note 2: *Ensured by design, but not 100% production tested.*
Note 3: *Parameter measured at trip point of latch with V_{PIN2} = 0.*
Note 4: *Gain defined as: $A = \frac{\Delta VPIN\ 1}{\Delta VPIN\ 3}$; 0 ≤ $V_{PIN\ 3}$ ≤ 0.8V.*
Note 5: *Adjust V_{CC} above the start threshold before setting at 15V.*
Note 6: *Output frequency equals oscillator frequency for the UC1842A and UC1843A. Output frequency is one half oscillator frequency for the UC1844A and UC1845A.*
Note 7: *"Temperature stability, sometimes referred to as average temperature coefficient, is described by the equation:*

$$\text{Temp Stability} = \frac{VREF\ (max) - VREF\ (min)}{TJ\ (max) - TJ\ (min)}$$

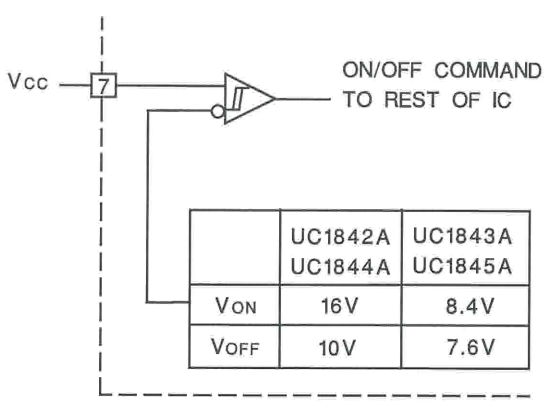
V_{REF} (max) and V_{REF} (min) are the maximum & minimum reference voltage measured over the appropriate temperature range. Note that the extremes in voltage do not necessarily occur at the extremes in temperature."
Note 8: *This parameter is measured with R_T = 10kΩ to V_{REF}. This contributes approximately 300μA of current to the measurement. The total current flowing into the R_T/C pin will be approximately 300μA higher than the measured value.*

Error Amp Configuration

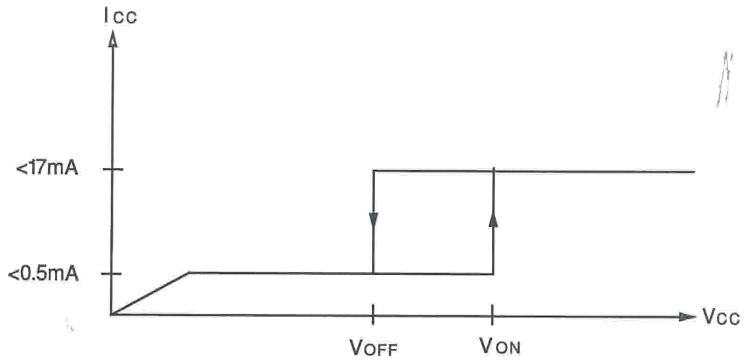


Error Amp can Source and Sink up to 0.5mA, and Sink up to 2mA.

Under-Voltage Lockout

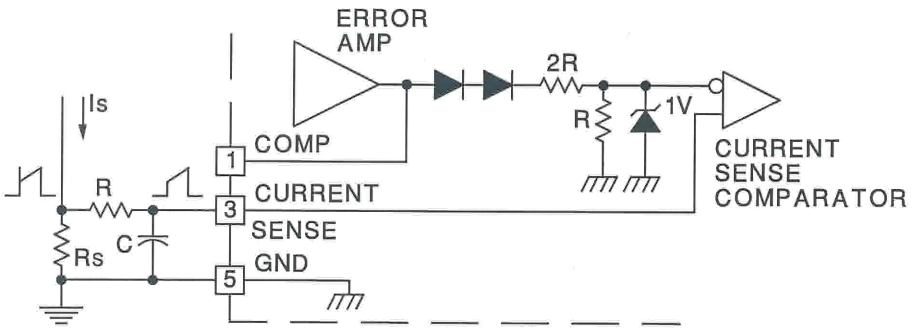


	UC1842A UC1844A	UC1843A UC1845A
VON	16V	8.4V
VOFF	10V	7.6V



During UVLO, the Output is low.

Current Sense Circuit

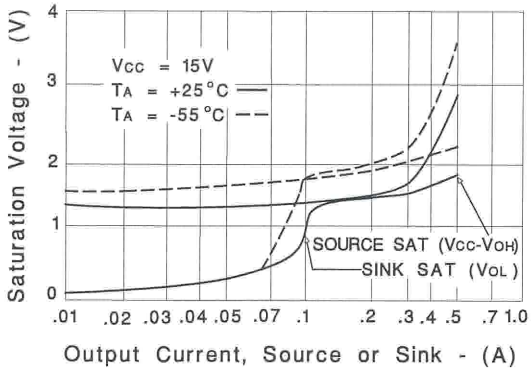


Peak Current (Is) is Determined By The Formula

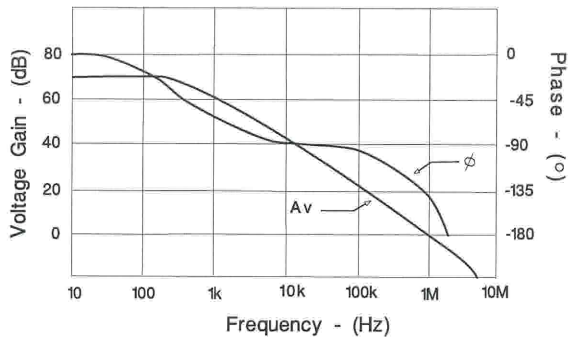
$$I_{SMAX} \approx \frac{1.0V}{RS}$$

A small RC filter may be required to suppress switch transients.

Output Saturation Characteristics

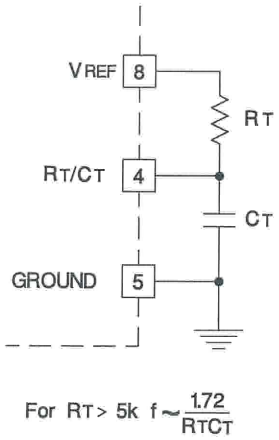


Error Amplifier Open-Loop Frequency Response

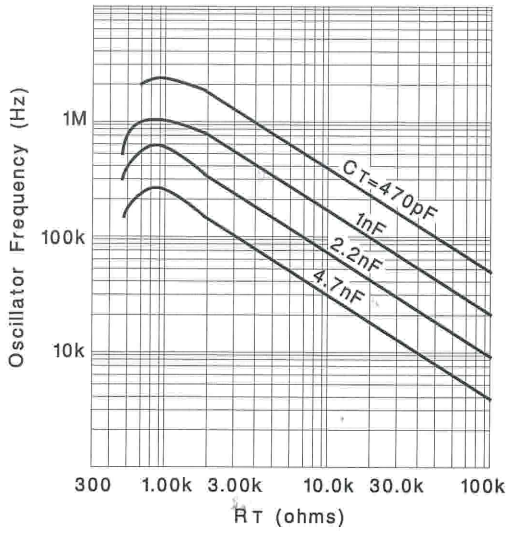


APPLICATIONS DATA (cont.)

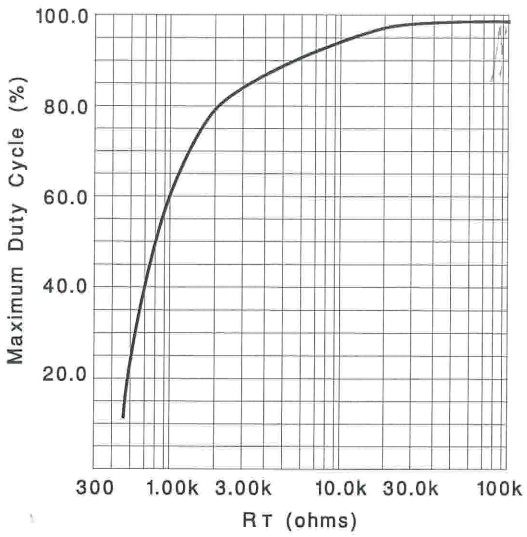
Oscillator Section



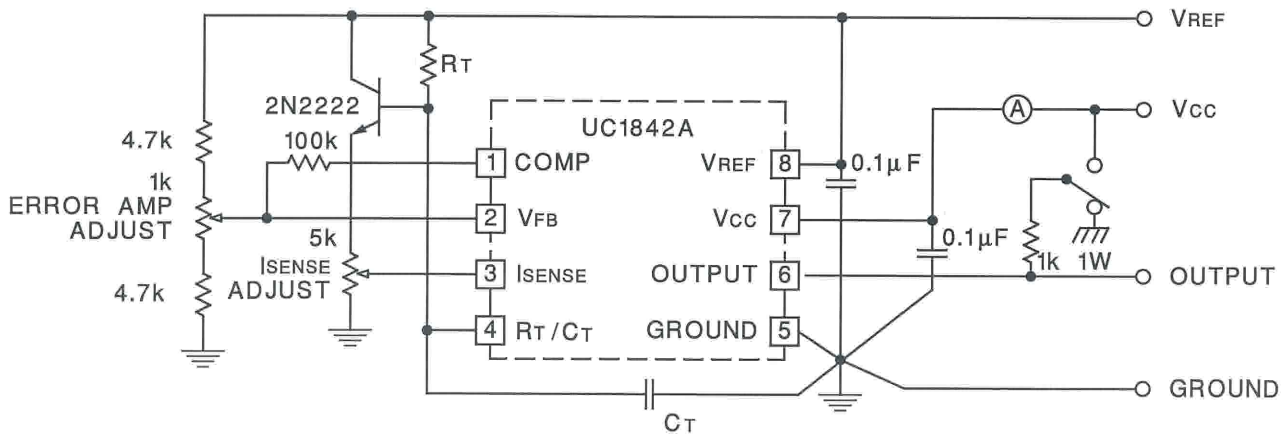
Oscillator Frequency vs Timing Resistance



Maximum Duty Cycle vs Timing Resistor

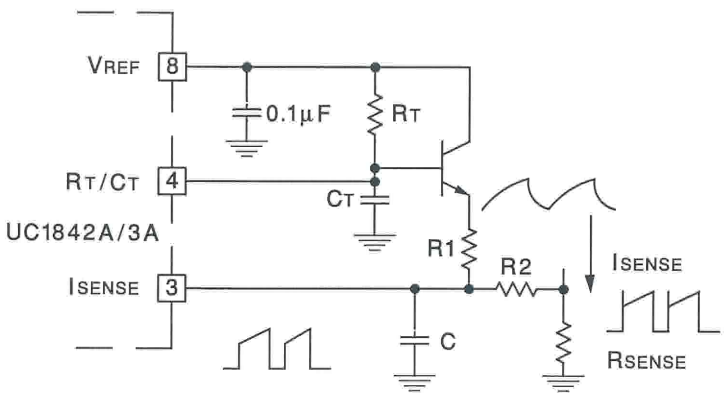


Open-Loop Laboratory Test Fixture



High peak currents associated with capacitive loads necessitate careful grounding techniques. Timing and bypass capacitors should be connected close to pin 5 in a single point ground. The transistor and 5k potentiometer are used to sample the oscillator waveform and apply an adjustable ramp to pin 3.

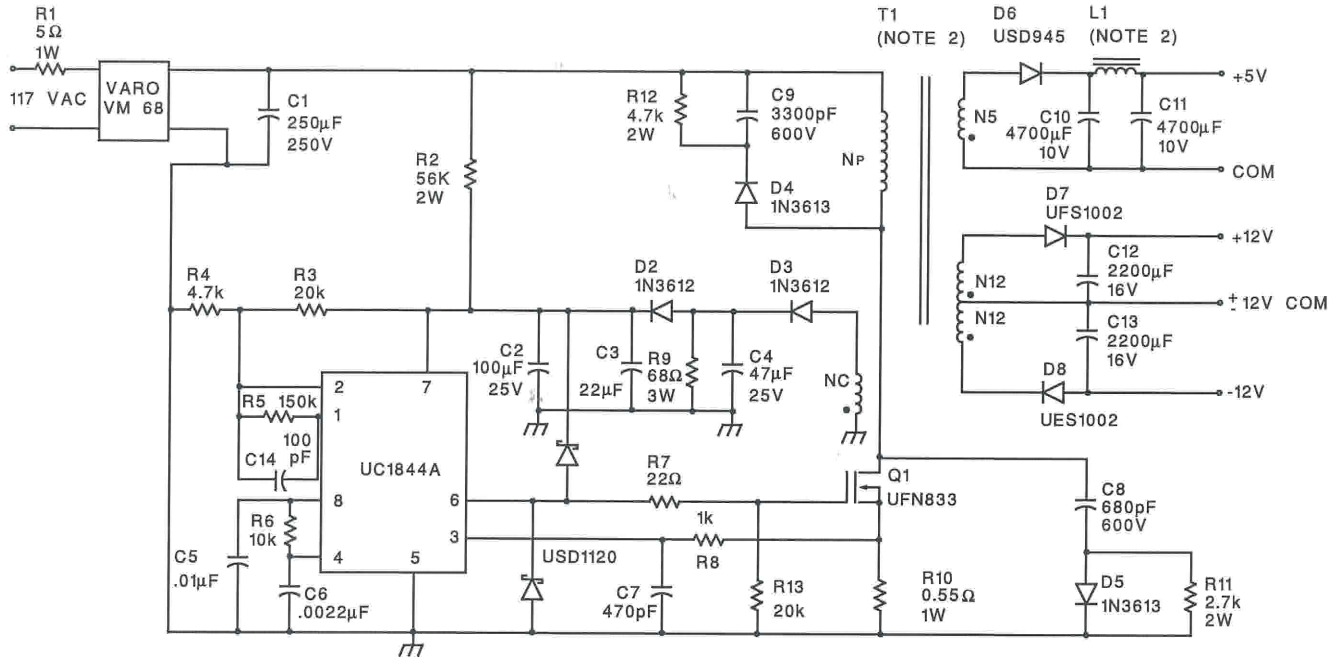
Slope Compensation



A fraction of the oscillator ramp can be resistively summed with the current sense signal to provide slope compensation for converters requiring duty cycles over 50%.
Note that capacitor, C, forms a filter with R2 to suppress the leading edge switch spikes.

APPLICATIONS DATA (cont.)

Off-line Flyback Regulator



Power Supply Specifications

1. Input Voltage		*95VAC to 130VA (50 Hz/60Hz)*
2. Line Isolation		*3750V*
3. Switching Frequency		*40kHz*
4. Efficiency	*Full Load*	*70%*

5. Output Voltage:
A. +5V, ±5%; 1A to 4A load
Ripple voltage: 50mV P-P Max
B. +12V, ±3%; 0.1A to 0.3A load
Ripple voltage: 100mV P-P Max
C. -12V ,±3%; 0.1A to 0.3A load
Ripple voltage: 100mV P-P Max

REVISION HISTORY

Revision B (September 2009) to revision C (August 2010):

Corrected I_{SINK} voltage, page 4, 15 V to 1.5 V in two places.

Revision C (August 2010 to revision D (July 2011):

Updated Abs Max Table with Max negative voltage and GND pin notes.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/ Ball Finish	MSL Peak Temp (3)	Samples (Requires Login)
5962-8670405PA	ACTIVE	CDIP	JG	8	1	TBD	Call TI	Call TI	
5962-8670405XA	ACTIVE	LCCC	FK	20	1	TBD	Call TI	Call TI	
5962-8670406PA	ACTIVE	CDIP	JG	8	1	TBD	Call TI	Call TI	
5962-8670406XA	ACTIVE	LCCC	FK	20	1	TBD	Call TI	Call TI	
5962-8670407PA	ACTIVE	CDIP	JG	8	1	TBD	Call TI	Call TI	
5962-8670407XA	ACTIVE	LCCC	FK	20	1	TBD	Call TI	Call TI	
5962-8670408PA	ACTIVE	CDIP	JG	8	1	TBD	Call TI	Call TI	
5962-8670408XA	ACTIVE	LCCC	FK	20	1	TBD	Call TI	Call TI	
UC1842AJ	ACTIVE	CDIP	JG	8	1	TBD	A42	N / A for Pkg Type	
UC1842AJ883B	ACTIVE	CDIP	JG	8	1	TBD	A42	N / A for Pkg Type	
UC1842AL883B	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	
UC1843AJ	ACTIVE	CDIP	JG	8	1	TBD	A42	N / A for Pkg Type	
UC1843AJ883B	ACTIVE	CDIP	JG	8	1	TBD	A42	N / A for Pkg Type	
UC1843AL883B	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	
UC1844AJ	ACTIVE	CDIP	JG	8	1	TBD	A42	N / A for Pkg Type	
UC1844AJ883B	ACTIVE	CDIP	JG	8	1	TBD	A42	N / A for Pkg Type	
UC1844AL883B	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	
UC1845AJ	ACTIVE	CDIP	JG	8	1	TBD	A42	N / A for Pkg Type	
UC1845AJ883B	ACTIVE	CDIP	JG	8	1	TBD	A42	N / A for Pkg Type	
UC1845AL883B	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	
UC2842AD	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
UC2842AD8	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
UC2842AD8G4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
UC2842AD8TR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
UC2842AD8TRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/ Ball Finish	MSL Peak Temp (3)	Samples (Requires Login)
UC2842ADG4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
UC2842ADTR	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
UC2842ADTRG4	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
UC2842ADW	ACTIVE	SOIC	DW	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	
UC2842ADWG4	ACTIVE	SOIC	DW	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	
UC2842ADWTR	ACTIVE	SOIC	DW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	
UC2842ADWTRG4	ACTIVE	SOIC	DW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	
UC2842AJ	OBSOLETE	CDIP	JG	8		TBD	Call TI	Call TI	
UC2842AN	ACTIVE	PDIP	P	8	50	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type	
UC2842ANG4	ACTIVE	PDIP	P	8	50	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type	
UC2843AD	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
UC2843AD8	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
UC2843AD8G4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
UC2843AD8TR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
UC2843AD8TRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
UC2843ADG4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
UC2843ADTR	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
UC2843ADTRG4	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
UC2843AJ	OBSOLETE	CDIP	JG	8		TBD	Call TI	Call TI	

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/ Ball Finish	MSL Peak Temp (3)	Samples (Requires Login)
UC2843AN	ACTIVE	PDIP	P	8	50	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type	
UC2843ANG4	ACTIVE	PDIP	P	8	50	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type	
UC2843AQ	ACTIVE	PLCC	FN	20	46	Green (RoHS & no Sb/Br)	CU SN	Level-2-260C-1 YEAR	
UC2843AQG3	ACTIVE	PLCC	FN	20	46	Green (RoHS & no Sb/Br)	CU SN	Level-2-260C-1 YEAR	
UC2844AD	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
UC2844AD8	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
UC2844AD8G4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
UC2844AD8TR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
UC2844AD8TRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
UC2844ADG4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
UC2844ADTR	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
UC2844ADTRG4	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
UC2844AN	ACTIVE	PDIP	P	8	50	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type	
UC2844ANG4	ACTIVE	PDIP	P	8	50	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type	
UC2844AQD	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
UC2844AQD8	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
UC2844AQD8R	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
UC2844AQDR	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/ Ball Finish	MSL Peak Temp (3)	Samples (Requires Login)
UC2845AD	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
UC2845AD8	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
UC2845AD8G4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
UC2845AD8TR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
UC2845AD8TRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
UC2845ADG4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
UC2845ADTR	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
UC2845ADTRG4	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
UC2845ADW	ACTIVE	SOIC	DW	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	
UC2845ADWG4	ACTIVE	SOIC	DW	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	
UC2845AN	ACTIVE	PDIP	P	8	50	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type	
UC2845ANG4	ACTIVE	PDIP	P	8	50	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type	
UC3842AD	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
UC3842AD8	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
UC3842AD8G4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
UC3842AD8TR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
UC3842AD8TRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
UC3842ADG4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/ Ball Finish	MSL Peak Temp (3)	Samples (Requires Login)
UC3842ADTR	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
UC3842ADTRG4	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
UC3842ADW	ACTIVE	SOIC	DW	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	
UC3842ADWG4	ACTIVE	SOIC	DW	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	
UC3842AN	ACTIVE	PDIP	P	8	50	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type	
UC3842ANG4	ACTIVE	PDIP	P	8	50	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type	
UC3842J	ACTIVE	CDIP	JG	8	1	TBD	A42	N / A for Pkg Type	
UC3843AD	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
UC3843AD8	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
UC3843AD8G4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
UC3843AD8TR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
UC3843AD8TRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
UC3843ADG4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
UC3843ADTR	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
UC3843ADTRG4	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
UC3843AN	ACTIVE	PDIP	P	8	50	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type	
UC3843ANG4	ACTIVE	PDIP	P	8	50	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type	
UC3844AD	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/ Ball Finish	MSL Peak Temp (3)	Samples (Requires Login)
UC3844AD8	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
UC3844AD8G4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
UC3844AD8TR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
UC3844AD8TRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
UC3844ADG4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
UC3844ADTR	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
UC3844ADTRG4	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
UC3844AN	ACTIVE	PDIP	P	8	50	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type	
UC3844ANG4	ACTIVE	PDIP	P	8	50	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type	
UC3845AD	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
UC3845AD8	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
UC3845AD8G4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
UC3845AD8TR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
UC3845AD8TRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
UC3845ADG4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
UC3845ADTR	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
UC3845ADTRG4	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
UC3845AN	ACTIVE	PDIP	P	8	50	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type	

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/ Ball Finish	MSL Peak Temp (3)	Samples (Requires Login)
UC3845ANG4	ACTIVE	PDIP	P	8	50	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type	

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

OTHER QUALIFIED VERSIONS OF UC1842A, UC1843A, UC1844A, UC1845A, UC2843A, UC3842A, UC3842M, UC3843A, UC3844A, UC3845A :

- Catalog: UC3842A, UC3843A, UC3844A, UC3845A, UC3842, UC3845AM
- Automotive: UC2843A-Q1
- Enhanced Product: UC1842A-EP, UC1843A-EP, UC1844A-EP, UC1845A-EP, UC1842A-EP, UC1843A-EP, UC1844A-EP, UC1845A-EP
- Military: UC1842A, UC1843A, UC1844A, UC1845A

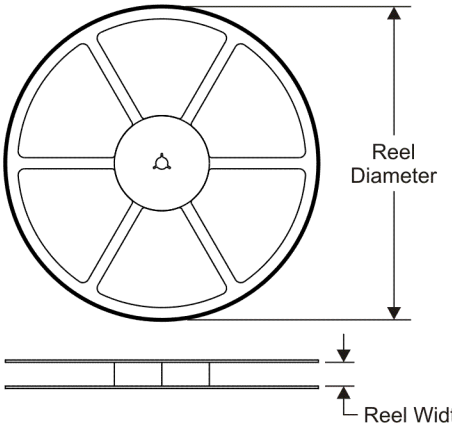
- Space: UC1842A-SP, UC1843A-SP, UC1844A-SP, UC1845A-SP, UC1842A-SP, UC1843A-SP, UC1844A-SP, UC1845A-SP

NOTE: Qualified Version Definitions:

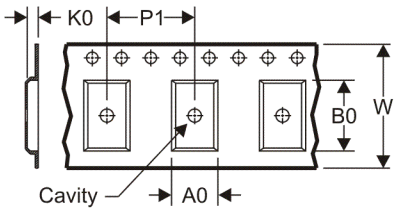
- Catalog - TI's standard catalog product
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects
- Enhanced Product - Supports Defense, Aerospace and Medical Applications
- Military - QML certified for Military and Defense Applications
- Space - Radiation tolerant, ceramic packaging and qualified for use in Space-based application

TAPE AND REEL INFORMATION

REEL DIMENSIONS

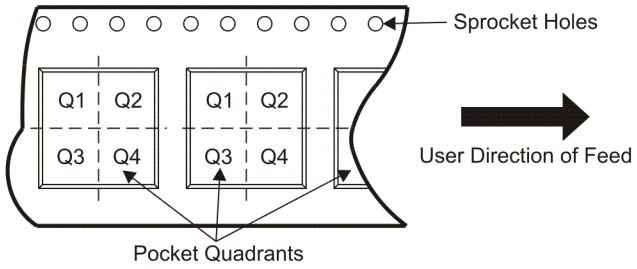


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

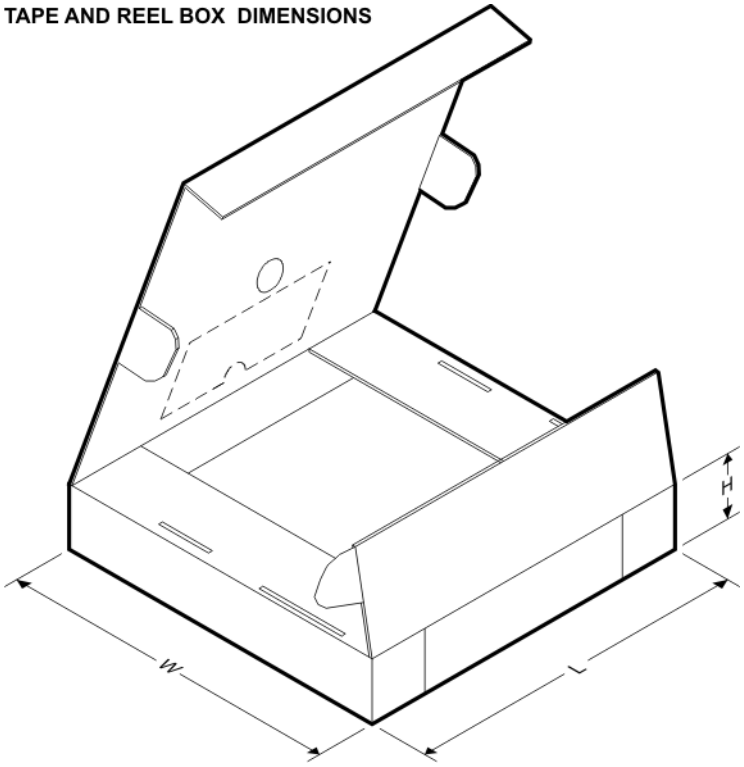
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
UC2842AD8TR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
UC2842ADTR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
UC2842ADWTR	SOIC	DW	16	2000	330.0	16.4	10.85	10.8	2.7	12.0	16.0	Q1
UC2843AD8TR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
UC2843ADTR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
UC2844AD8TR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
UC2844ADTR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
UC2844AQD8R	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	4.0	12.0	Q1
UC2845AD8TR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
UC2845ADTR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
UC3842AD8TR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
UC3842ADTR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
UC3843AD8TR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
UC3843ADTR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
UC3844AD8TR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
UC3844ADTR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
UC3845AD8TR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
UC3845ADTR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS

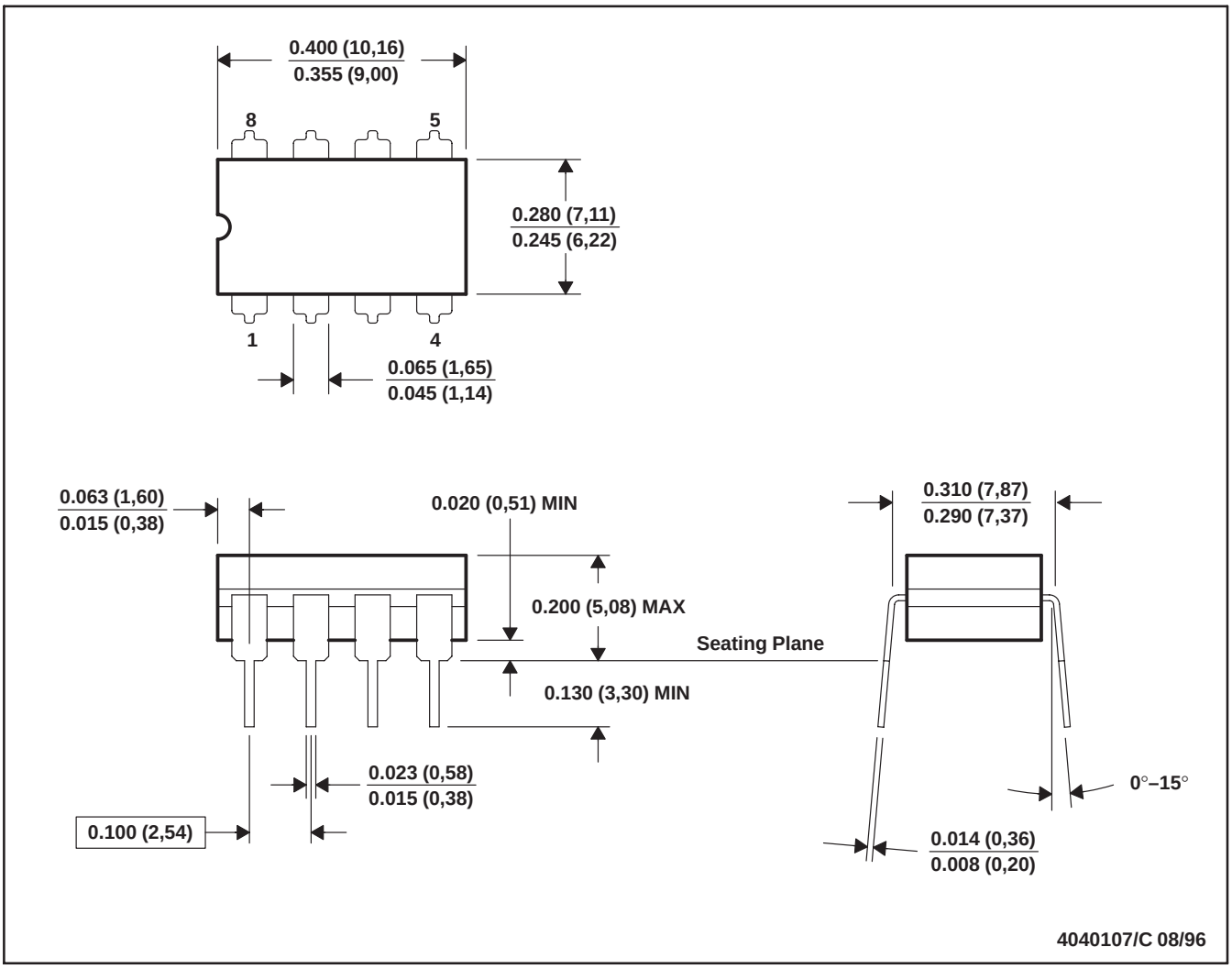


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
UC2842AD8TR	SOIC	D	8	2500	340.5	338.1	20.6
UC2842ADTR	SOIC	D	14	2500	333.2	345.9	28.6
UC2842ADWTR	SOIC	DW	16	2000	346.0	346.0	33.0
UC2843AD8TR	SOIC	D	8	2500	340.5	338.1	20.6
UC2843ADTR	SOIC	D	14	2500	333.2	345.9	28.6
UC2844AD8TR	SOIC	D	8	2500	340.5	338.1	20.6
UC2844ADTR	SOIC	D	14	2500	333.2	345.9	28.6
UC2844AQD8R	SOIC	D	8	2500	367.0	367.0	35.0
UC2845AD8TR	SOIC	D	8	2500	340.5	338.1	20.6
UC2845ADTR	SOIC	D	14	2500	333.2	345.9	28.6
UC3842AD8TR	SOIC	D	8	2500	340.5	338.1	20.6
UC3842ADTR	SOIC	D	14	2500	333.2	345.9	28.6
UC3843AD8TR	SOIC	D	8	2500	340.5	338.1	20.6
UC3843ADTR	SOIC	D	14	2500	333.2	345.9	28.6
UC3844AD8TR	SOIC	D	8	2500	340.5	338.1	20.6
UC3844ADTR	SOIC	D	14	2500	333.2	345.9	28.6
UC3845AD8TR	SOIC	D	8	2500	340.5	338.1	20.6
UC3845ADTR	SOIC	D	14	2500	333.2	345.9	28.6

MCER001A – JANUARY 1995 – REVISED JANUARY 1997

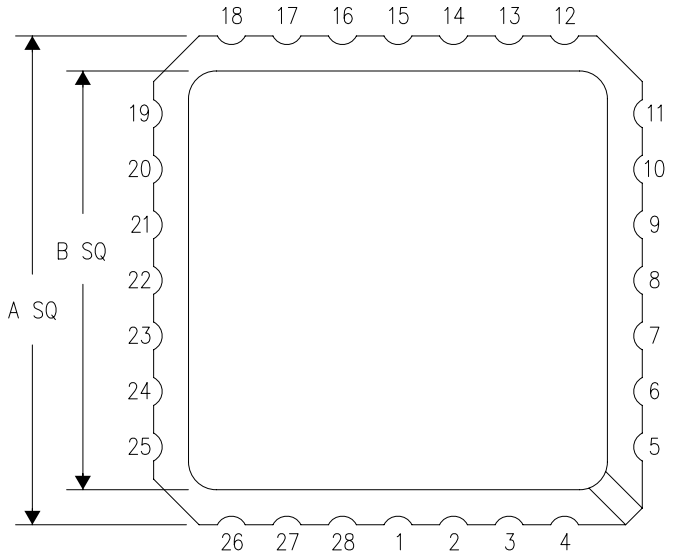
JG (R-GDIP-T8) **CERAMIC DUAL-IN-LINE**



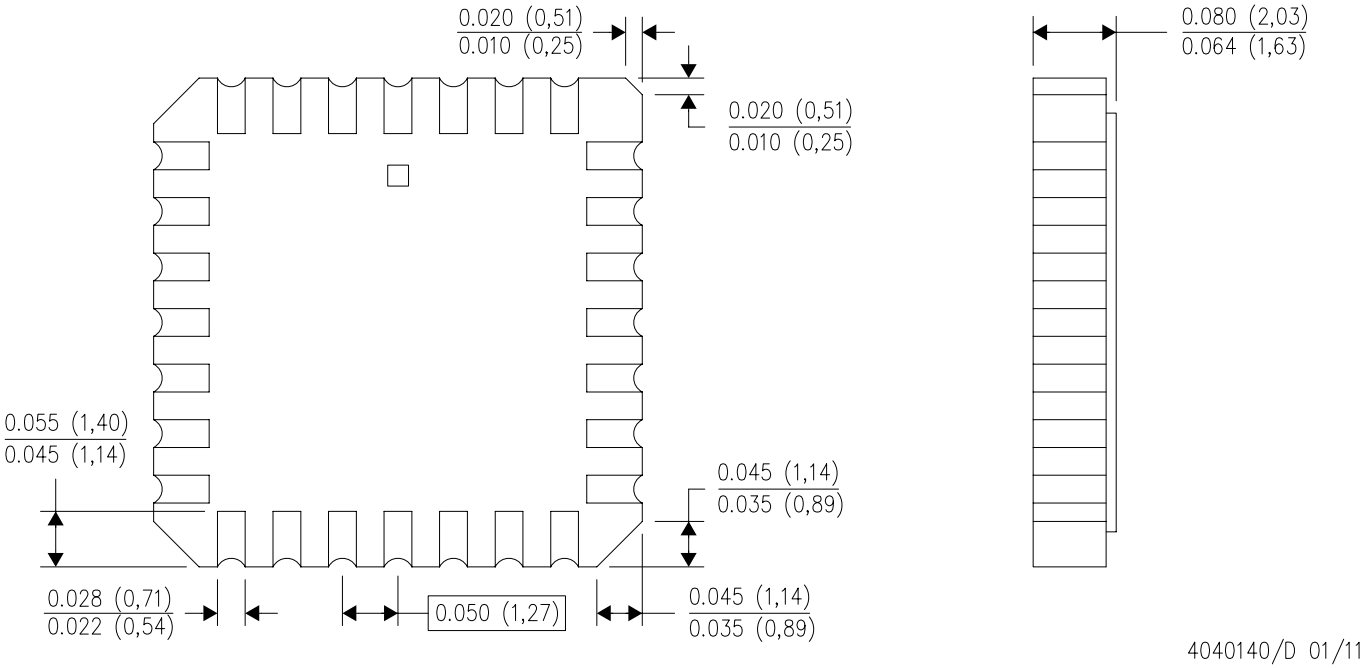
NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package can be hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for terminal identification.
E. Falls within MIL STD 1835 GDIP1-T8

FK (S–CQCC–N**) LEADLESS CERAMIC CHIP CARRIER

28 TERMINAL SHOWN



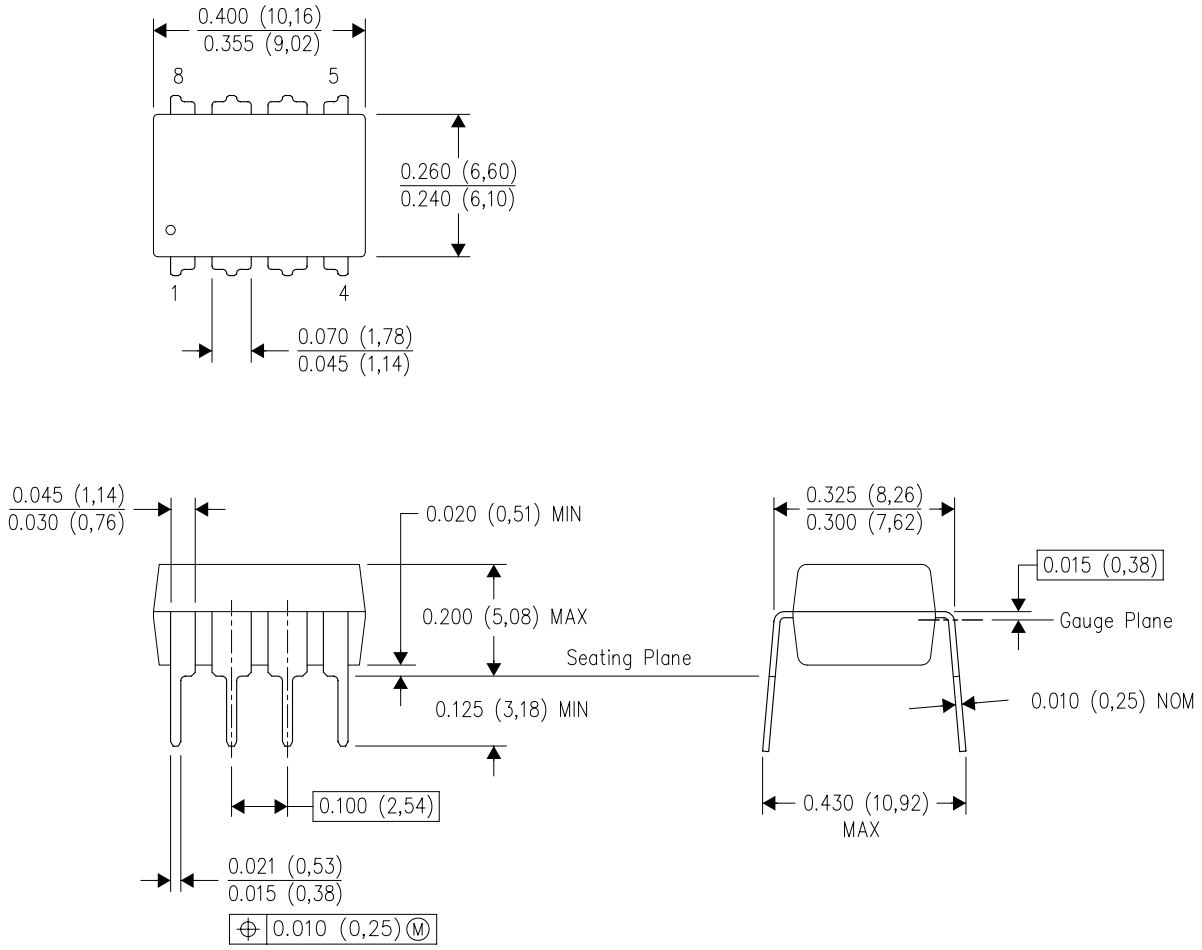
NO. OF TERMINALS **	A		B	
	MIN	MAX	MIN	MAX
20	0.342 (8,69)	0.358 (9,09)	0.307 (7,80)	0.358 (9,09)
28	0.442 (11,23)	0.458 (11,63)	0.406 (10,31)	0.458 (11,63)
44	0.640 (16,26)	0.660 (16,76)	0.495 (12,58)	0.560 (14,22)
52	0.740 (18,78)	0.761 (19,32)	0.495 (12,58)	0.560 (14,22)
68	0.938 (23,83)	0.962 (24,43)	0.850 (21,6)	0.858 (21,8)
84	1.141 (28,99)	1.165 (29,59)	1.047 (26,6)	1.063 (27,0)



4040140/D 01/11

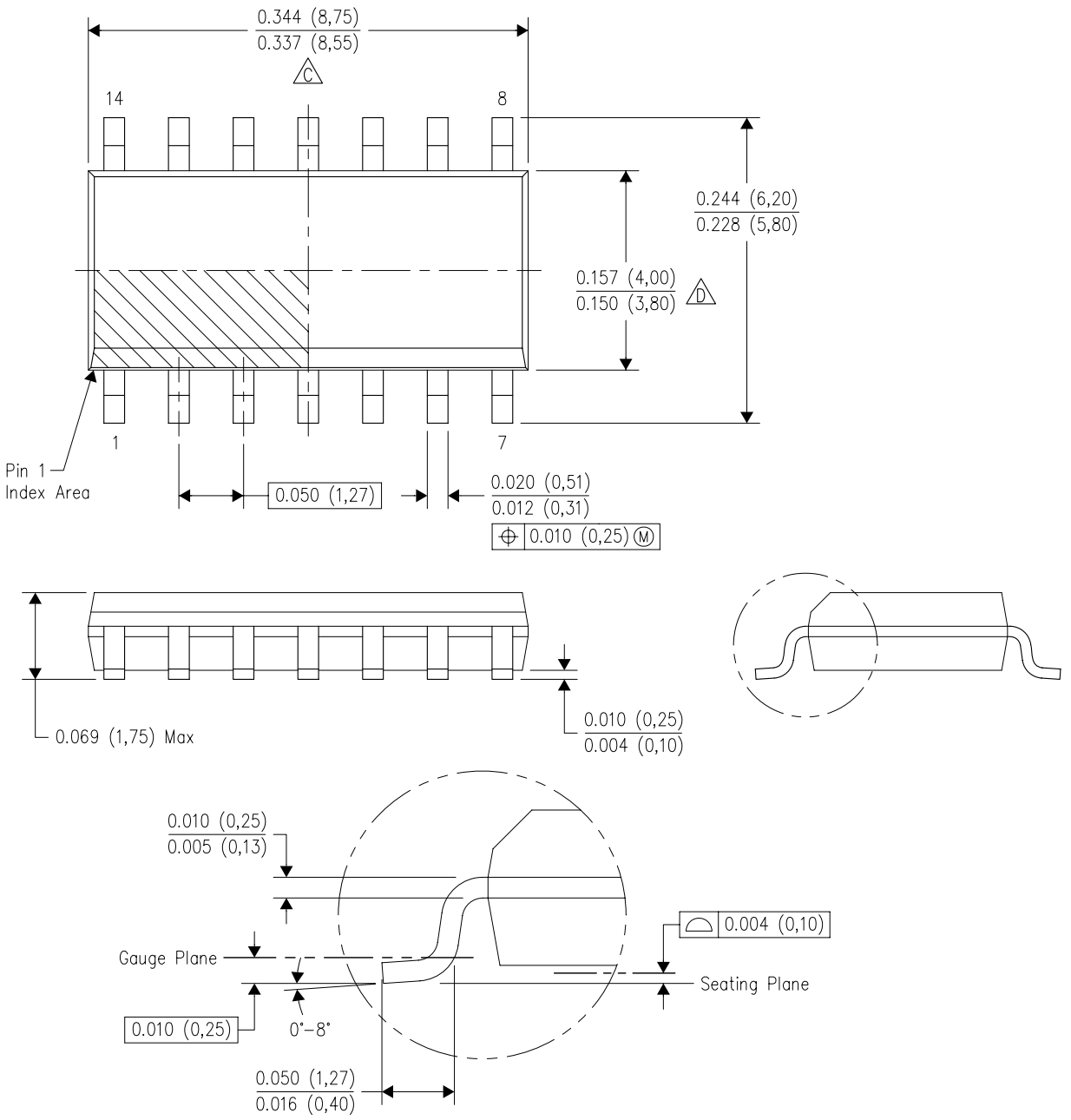
NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package can be hermetically sealed with a metal lid.
D. Falls within JEDEC MS–004

P (R–PDIP–T8) PLASTIC DUAL–IN–LINE PACKAGE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001 variation BA.

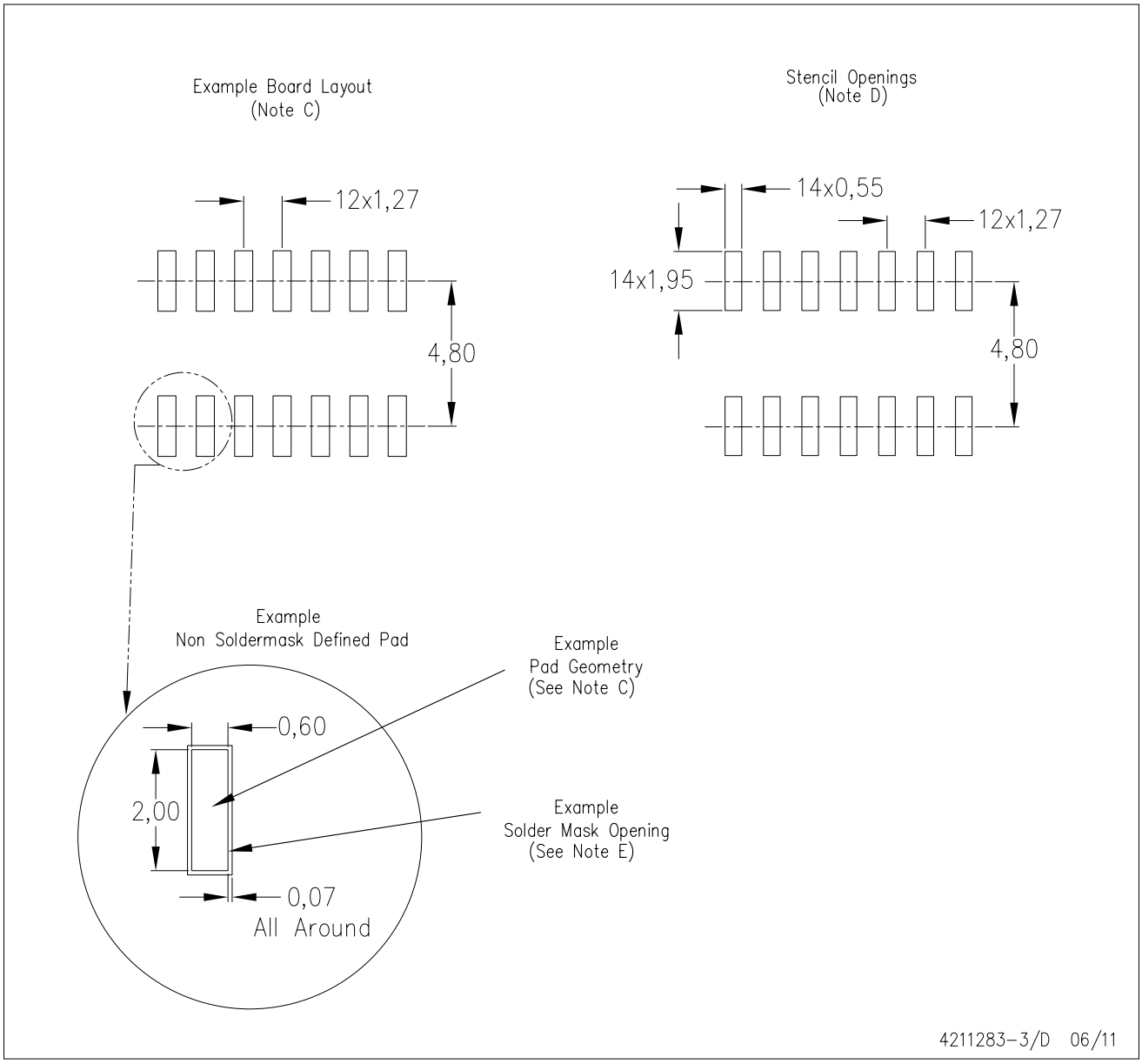
D (R–PDSO–G14) PLASTIC SMALL OUTLINE



4040047–5/M 06/11

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AB.

D (R–PDSO–G14) PLASTIC SMALL OUTLINE



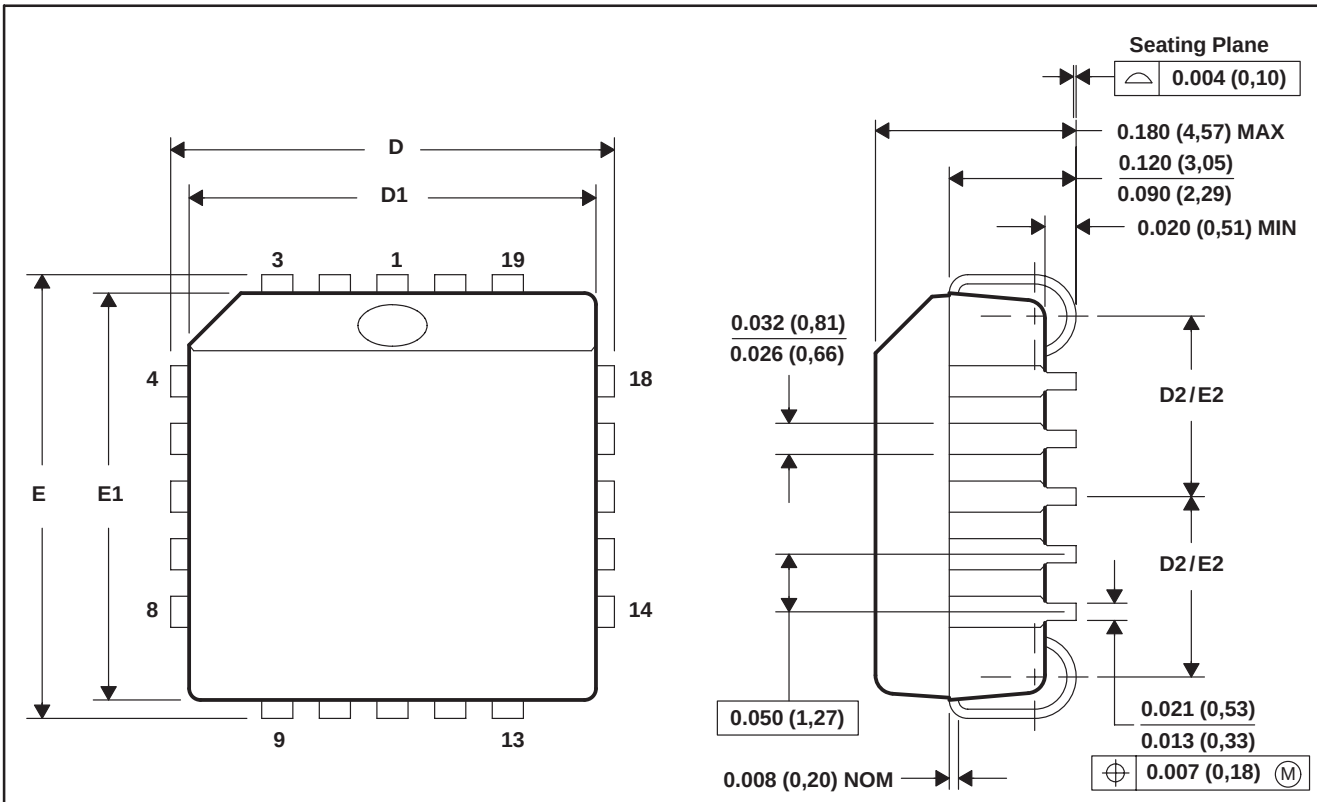
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

MPLC004A – OCTOBER 1994

FN (S-PQCC-J**)

PLASTIC J-LEADED CHIP CARRIER

20 PIN SHOWN

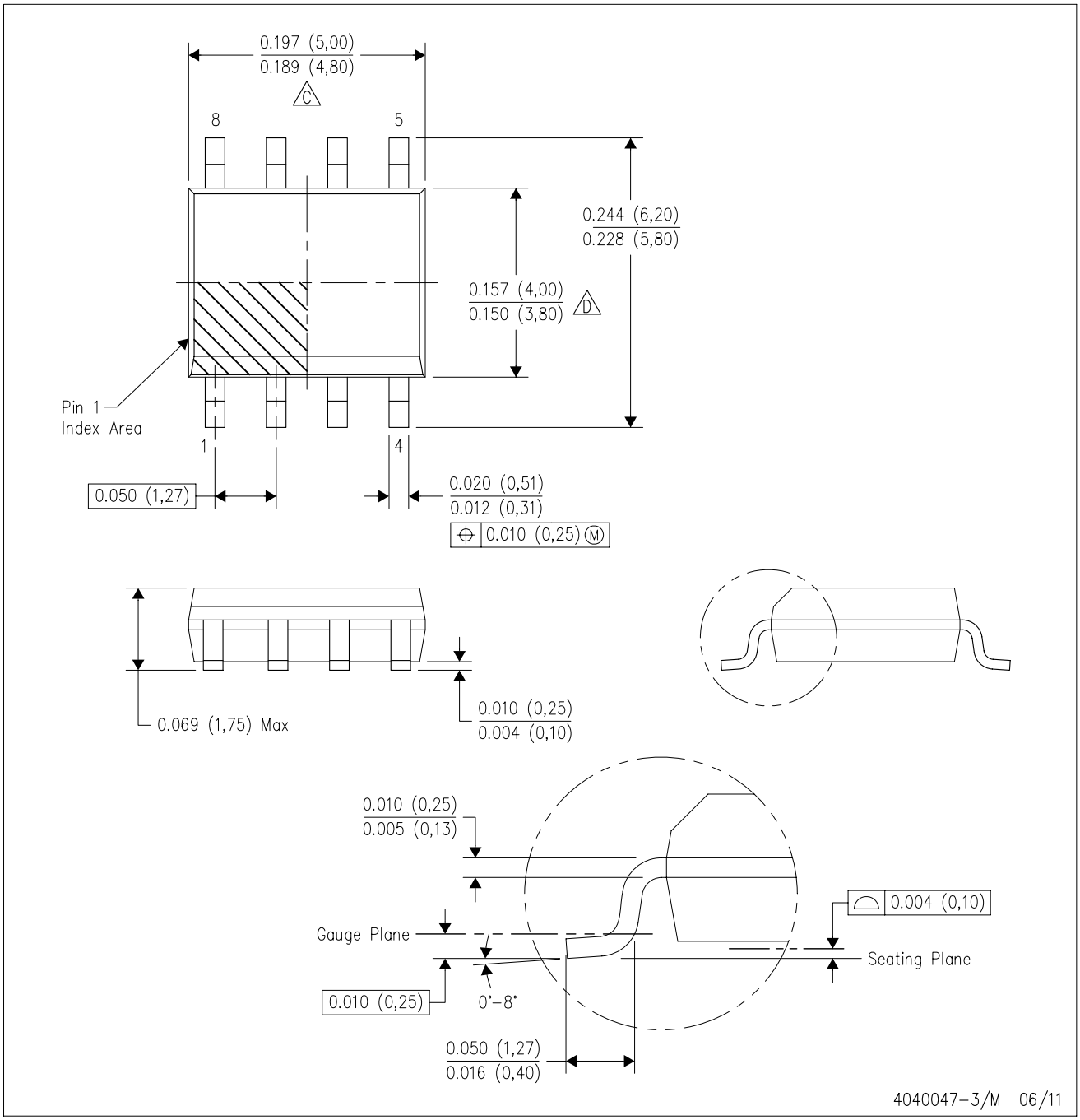


NO. OF PINS **	D/E		D1/E1		D2/E2	
	MIN	MAX	MIN	MAX	MIN	MAX
20	0.385 (9,78)	0.395 (10,03)	0.350 (8,89)	0.356 (9,04)	0.141 (3,58)	0.169 (4,29)
28	0.485 (12,32)	0.495 (12,57)	0.450 (11,43)	0.456 (11,58)	0.191 (4,85)	0.219 (5,56)
44	0.685 (17,40)	0.695 (17,65)	0.650 (16,51)	0.656 (16,66)	0.291 (7,39)	0.319 (8,10)
52	0.785 (19,94)	0.795 (20,19)	0.750 (19,05)	0.756 (19,20)	0.341 (8,66)	0.369 (9,37)
68	0.985 (25,02)	0.995 (25,27)	0.950 (24,13)	0.958 (24,33)	0.441 (11,20)	0.469 (11,91)
84	1.185 (30,10)	1.195 (30,35)	1.150 (29,21)	1.158 (29,41)	0.541 (13,74)	0.569 (14,45)

4040005/B 03/95

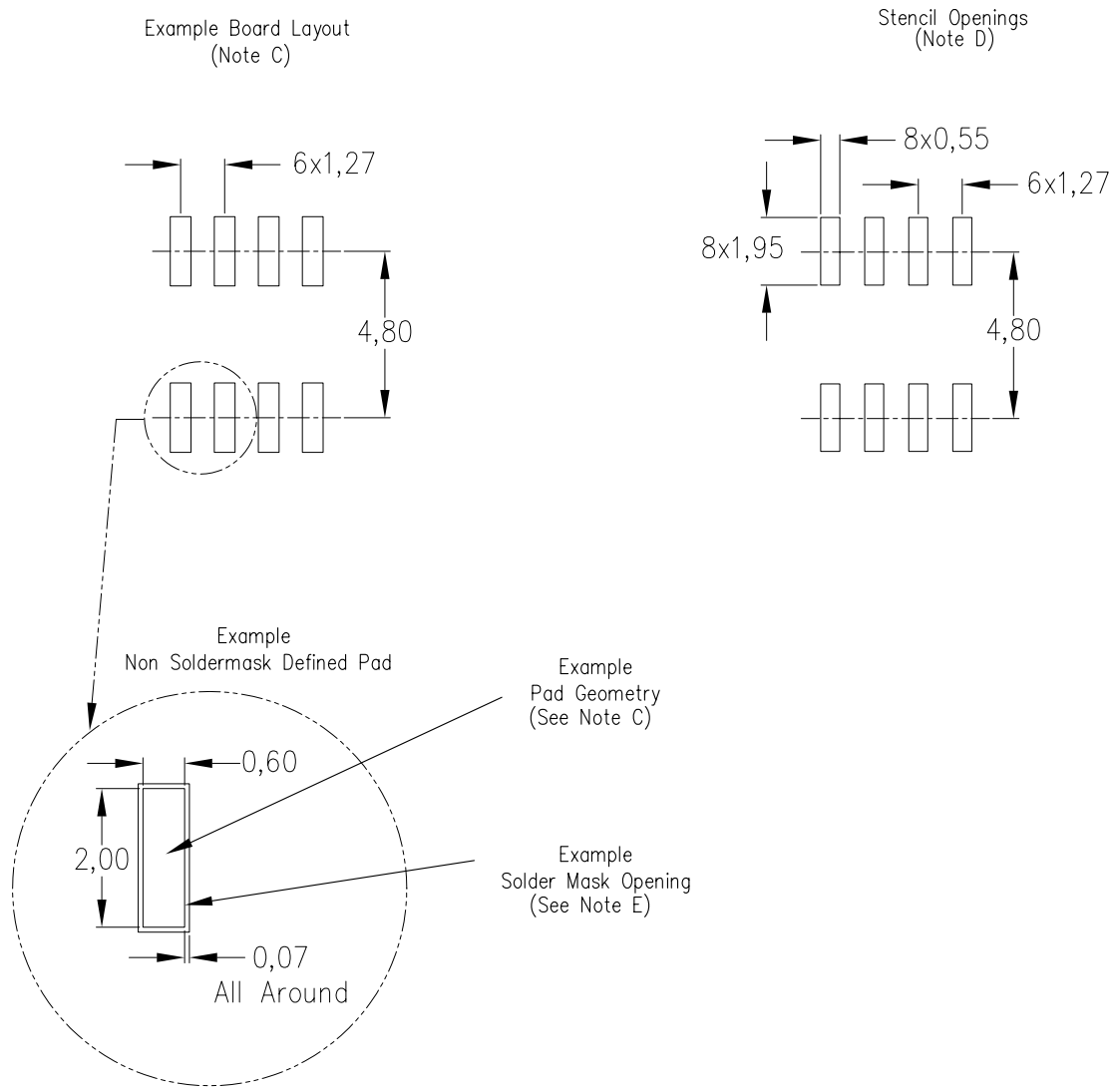
NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS-018

D (R–PDSO–G8) PLASTIC SMALL OUTLINE



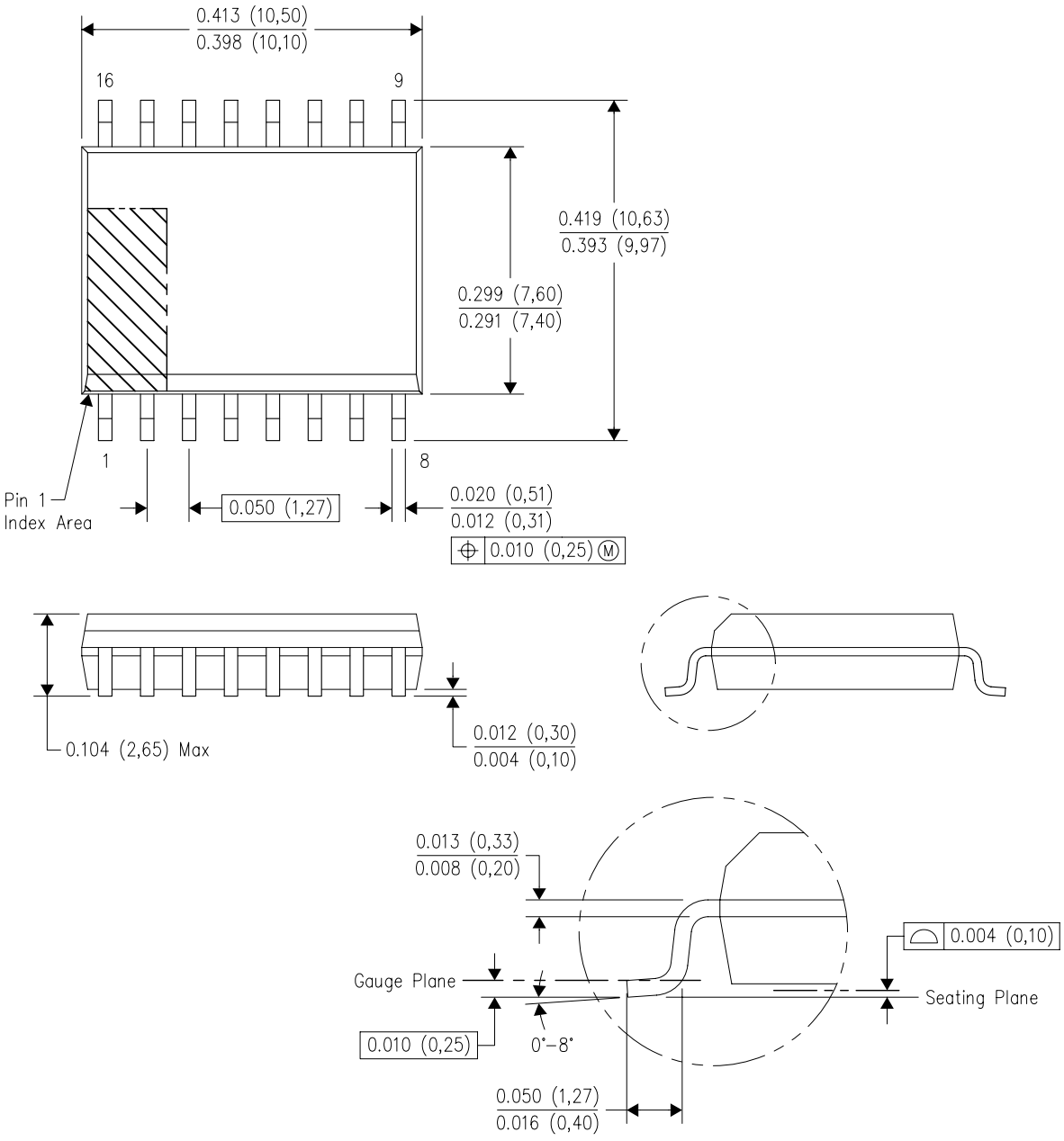
NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AA.

D (R–PDSO–G8) PLASTIC SMALL OUTLINE



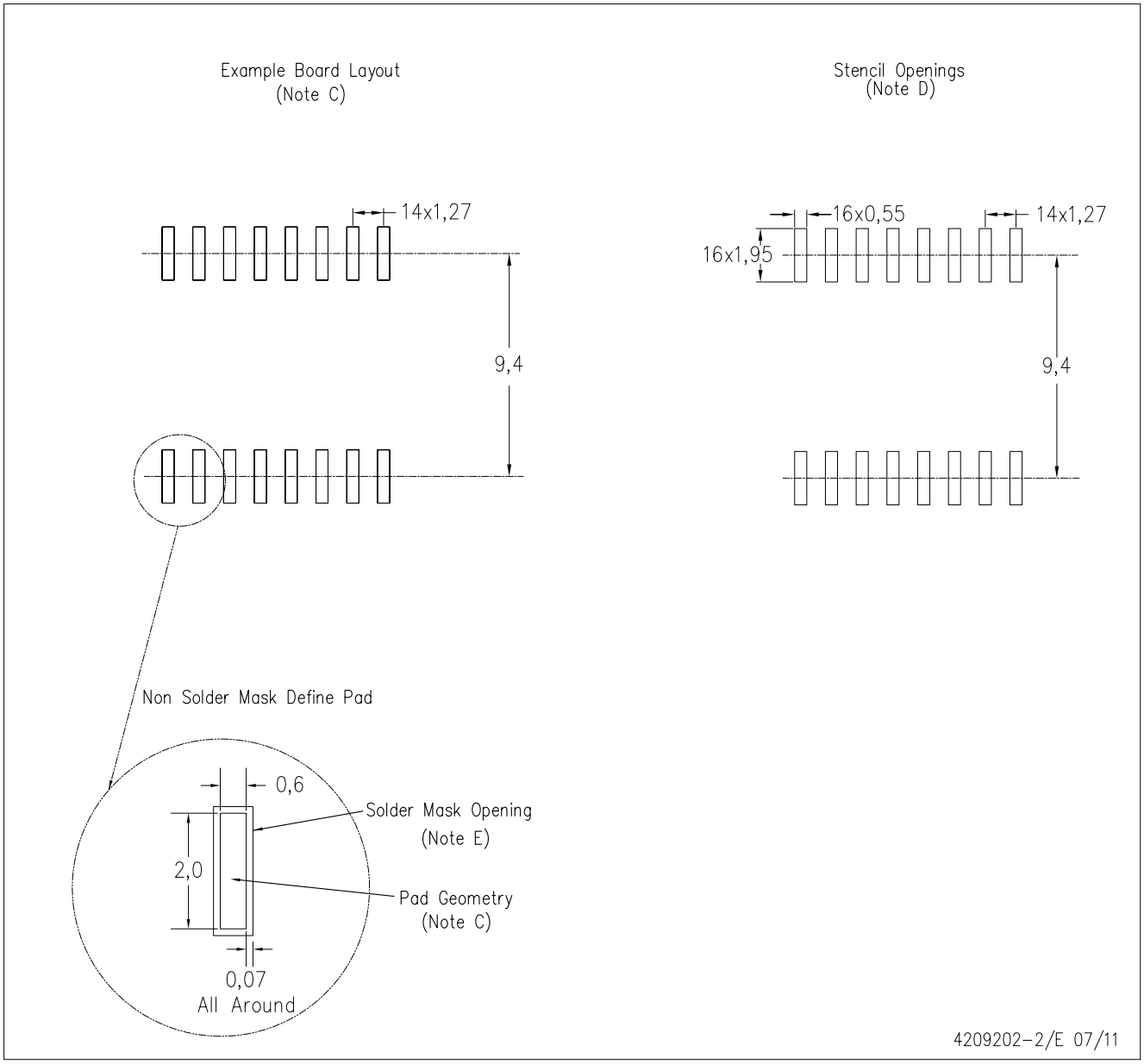
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

DW (R–PDSO–G16) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in inches (millimeters). Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
D. Falls within JEDEC MS–013 variation AA.

DW (R–PDSO–G16) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Refer to IPC7351 for alternate board design.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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