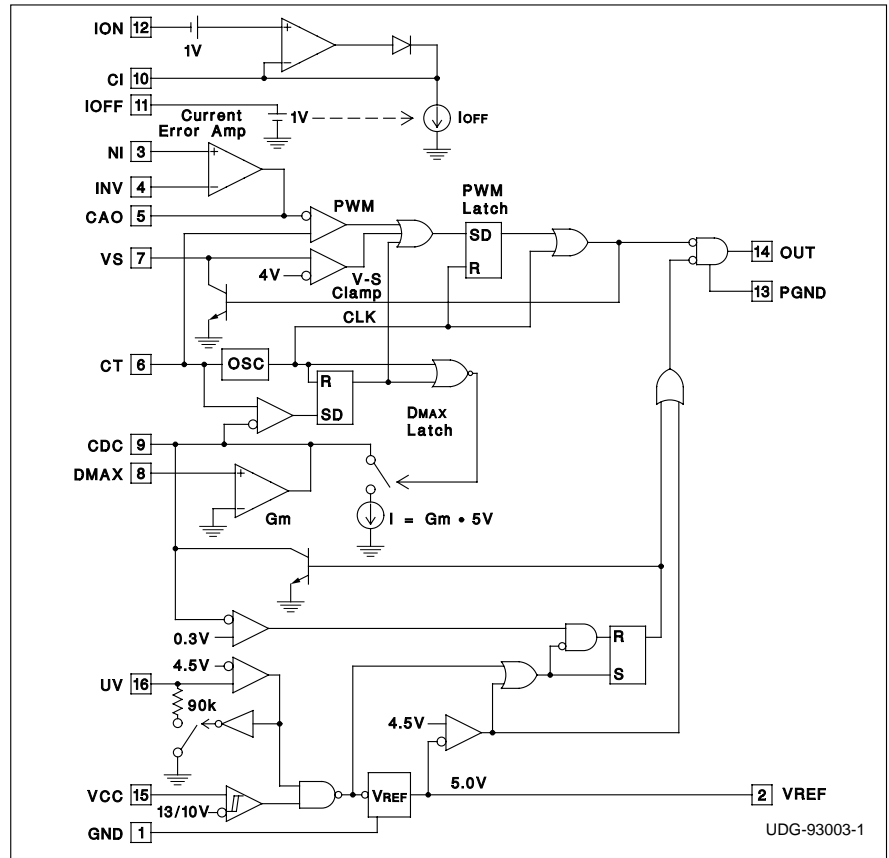


Average Current Mode PWM Controller

FEATURES

- Practical Primary Side Control of Isolated Power Supplies with DC Control of Secondary Side Current
- Accurate Programmable Maximum Duty Cycle Clamp
- Maximum Volt-Second Product Clamp to Prevent Core Saturation
- Practical Operation Up to 1MHz
- High Current (2A Pk) Totem Pole Output Driver
- Wide Bandwidth (8MHz) Current Error Amplifier
- Under Voltage Lockout Monitors VCC, VIN and VREF
- Output Active Low During UVLO
- Low Startup Current (500µA)
- Precision 5V Reference (1%)

BLOCK DIAGRAM



DESCRIPTION

The UC3848 family of PWM control ICs makes primary side average current mode control practical for isolated switching converters. Average current mode control insures that both cycle by cycle peak switch current and maximum average inductor current are well defined and will not run away in a short circuit situation. The UC3848 can be used to control a wide variety of converter topologies.

In addition to the basic functions required for pulse width modulation, the UC3848 implements a patented technique of sensing secondary current in an isolated buck derived converter from the primary side. A current waveform synthesizer monitors switch current and simulates the inductor current down slope so that the complete current waveform can be constructed on the primary side without actual secondary side measurement. This information on the primary side allows for full DC control of output current.

The UC3848 circuitry includes a precision reference, a wide bandwidth error amplifier for average current control, an oscillator to generate the system clock, latching PWM comparator and logic circuits, and a high current

output driver. The current error amplifier easily interfaces with an optoisolator from a secondary side voltage sensing circuit.

A full featured undervoltage lockout (UVLO) circuit is contained in the UC3848. UVLO monitors the supply voltage to the controller (VCC), the reference voltage (VREF), and the input line voltage (VIN). All three must be good before soft start commences. If either VCC or VIN is low, the supply current required by the chip is only 500µA and the output is actively held low.

Two on board protection features set controlled limits to prevent transformer core saturation. Input voltage is monitored and pulse width is constrained to limit the maximum volt-second product applied to the transformer. A unique patented technique limits maximum duty cycle within 3% of a user programmed value.

These two features allow for more optimal use of transformers and switches, resulting in reduced system size and cost.

Patents embodied in the UC3848 belong to Lambda Electronics Incorporated and are licensed for use in applications employing these devices.

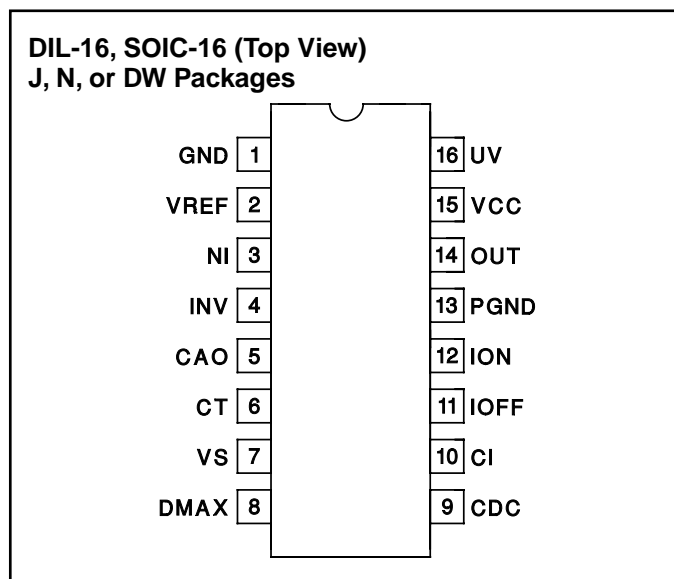
ABSOLUTE MAXIMUM RATINGS

Supply Voltage (Pin 15)	22V
Output Current, Source or Sink (Pin 14)	
DC	0.5A
Pulse (0.5 s)	2.2A
Power Ground to Ground (Pin 1 to Pin 13)	$\pm 0.2V$
Analog Input Voltages	
(Pins 3, 4, 7, 8, 12, 16)	-0.3 to 7V
Analog Input Currents, Source or Sink	
(Pins 3, 4, 7, 8, 11, 12, 16)	1mA

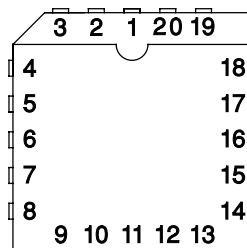
Analog Output Currents, Source or Sink (Pins 5 & 10)	5mA
Power Dissipation at $T_A = 60^\circ C$	1W
Storage Temperature Range	$-65^\circ C$ to $+150^\circ C$
Lead Temperature (Soldering 10 seconds)	$+300^\circ C$

Notes: All voltages are with respect to ground (DIL and SOIC Pin 1). Currents are positive into the specified terminal. Pin numbers refer to the 16 pin DIL and SOIC packages. Consult Packaging Section of Databook for thermal limitations and considerations of packages.

CONNECTION DIAGRAMS



**PLCC-20 & LCC-20
(Top View)
Q & L Packages**



PACKAGE PIN FUNCTION	
FUNCTION	PIN
N/C	1
GND	2
VREF	3
NI	4
INV	5
N/C	6
CAO	7
CT	8
VS	9
DMAX	10
N/C	11
CDC	12
CI	13
IOFF	14
ION	15
N/C	16
PGND	17
OUT	18
VCC	19
UV	20

THERMAL RATINGS TABLE

Package	Θ_{JA}	Θ_{JC}
DIL-16J	80-120	28 ⁽²⁾
DIL-16N	90 ⁽¹⁾	45
SOIC-16DW	50-100 ⁽¹⁾	27
PLCC-20	43-75 ⁽¹⁾	34
LCC-20	70-80	20 ⁽²⁾⁽³⁾

(1) Specified Θ_{JA} (junction to ambient) is for devices mounted to 5in² FR4 PC board with one ounce copper where noted. When resistance range is given, lower values are for 5in² aluminum PC board. Test PWB was 0.062in thick and typically used 0.635mm trace widths for power packages and 1.3mm trace widths for non-power packages with 100 x 100 mil probe land area at the end of each trace.

(2) Θ_{JC} data values stated were derived from MIL-STD-1835B. MIL-STD-1835B states that the baseline values shown are worst case (mean +2s) for a 60 x 60mil microcircuit device silicon die and applicable for devices with die sizes up to 14400 square mils. For device die sizes greater than 14400 square mils use the following values; dual-in-line, 11°C/W; flat pack 10°C/W; pin grid array, 10°C/W.

(3) Θ_{JC} estimated for backside of device, through the metgalized thermal condition pads.

ELECTRICAL CHARACTERISTICS: Unless otherwise stated, all specifications are over the junction temperature range of -55°C to $+125^{\circ}\text{C}$ for the UC1848, -40°C to $+85^{\circ}\text{C}$ for the UC2848, and 0°C to $+70^{\circ}\text{C}$ for the UC3848. Test conditions are: $V_{CC} = 12\text{V}$, $C_T = 400\text{pF}$, $C_I = 100\text{pF}$, $I_{OFF} = 100\mu\text{A}$, $C_{DC} = 100\text{nF}$, $C_{vs} = 100\text{pF}$, and $I_{vs} = 400\mu\text{A}$, $T_A = T_J$.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Real Time Current Waveform Synthesizer					
Ion Amplifier					
Offset Voltage		0.95	1	1.05	V
Slew Rate (Note 1)		20	25		V/ μs
lib			-2	-20	μA
IOFF Current Mirror					
Input Voltage		0.95	1	1.05	V
Current Gain		0.9	1	1.1	A/A
Current Error Amplifier					
A_{VOL}		60	100		dB
V_{io}	$12\text{V} \leq V_{CC} \quad 20\text{V}, 0\text{V} \quad V_{CM} \quad 5\text{V}$			10	mV
lib			-0.5	-3	μA
V_{oh}	$I_o = -200\mu\text{A}$	3	3.3		V
V_{ol}	$I_o = 200\mu\text{A}$		0.3	0.6	V
Source Current	$V_o = 1\text{V}$	1.4	1.6	2.0	mA
GBW Product	$f = 200\text{kHz}$	5	8		MHz
Slew Rate (Note 1)		8	10		V/ μs
Oscillator					
Frequency	$T_A = 25^{\circ}\text{C}$	240	250	260	kHz
		235		265	kHz
Ramp Amplitude		1.5	1.65	1.8	V
Duty Cycle Clamp					
Max Duty Cycle	$V(D_{MAX}) = 0.75 \cdot V_{REF}$	73.5	76.5	79.5	%
Volt Second Clamp					
Max On Time		900		1100	ns
VCC Comparator					
Turn-on Threshold			13	14	V
Turn-off Threshold		9	10		V
Hysteresis		2.5	3	3.5	V

ELECTRICAL CHARACTERISTICS: Unless otherwise stated, all specifications are over the junction temperature range of -55°C to $+125^{\circ}\text{C}$ for the UC1848, -40°C to $+85^{\circ}\text{C}$ for the UC2848, and 0°C to $+70^{\circ}\text{C}$ for the UC3848. Test conditions are: $V_{CC} = 12\text{V}$, $C_T = 400\text{pF}$, $C_I = 100\text{pF}$, $I_{OFF} = 100\mu\text{A}$, $C_{DC} = 100\text{nF}$, $C_{vs} = 100\text{pF}$, and $I_{vs} = 400\mu\text{A}$, $T_A = T_J$.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
UV Comparator					
Turn-on Threshold		4.1	4.35	4.6	V
RHYSTERESIS	$V_{uv} = 4.2\text{V}$	77	90	103	$k\Omega$
Reference					
VREF	$T_A = 25^{\circ}\text{C}$	4.95	5	5.05	V
	$0 < I_o < 10\text{mA}$, $12 < V_{CC} < 20$	4.93		5.07	V
Line Regulation	$12 < V_{cc} < 20\text{V}$		4	15	mV
Load Regulation	$0 < I_o < 10\text{mA}$		3	15	mV
Short Circuit Current	$V_{REF} = 0\text{V}$	30	50	70	mA
Output Stage					
Rise & Fall Time (Note 1)	$C_I = 1\text{nF}$		20	45	ns
Output Low Saturation	$I_o = 20\text{mA}$		0.25	0.4	V
	$I_o = 200\text{mA}$		1.2	2.2	V
Output High Saturation	$I_o = -200\text{mA}$		2.0	3.0	V
UVLO Output Low Saturation	$I_o = 20\text{mA}$		0.8	1.2	V
Icc					
I _{START}	$V_{CC} = 12\text{V}$		0.2	0.4	mA
I _{CC} (pre-start)	$V_{CC} = 15\text{V}$, $V(\text{UV}) = 0$		0.5	1	mA
I _{CC} (run)			22	26	mA

Note 1: Ensured by design.

APPLICATION INFORMATION

Under Voltage Lockout

The Under Voltage Lockout block diagram is shown in Fig 1. The VCC comparator monitors chip supply voltage. Hysteretic thresholds are set at 13V and 10V to facilitate off-line applications. If the VCC comparator is low, I_{CC} is low (<500μA) and the output is low.

The UV comparator monitors input line voltage (V_{IN}). A pair of resistors divides the input line to UV. Hysteretic input line thresholds are programmed by Rv1 and Rv2. The thresholds are

$$V_{IN(\text{on})} = 4.35\text{V} \cdot (1 + Rv1/Rv2')$$

$$V_{IN(\text{off})} = 4.35\text{V} \cdot (1 + Rv1/Rv2) \text{ where } Rv2' = Rv2 \parallel 90k.$$

The resulting hysteresis is

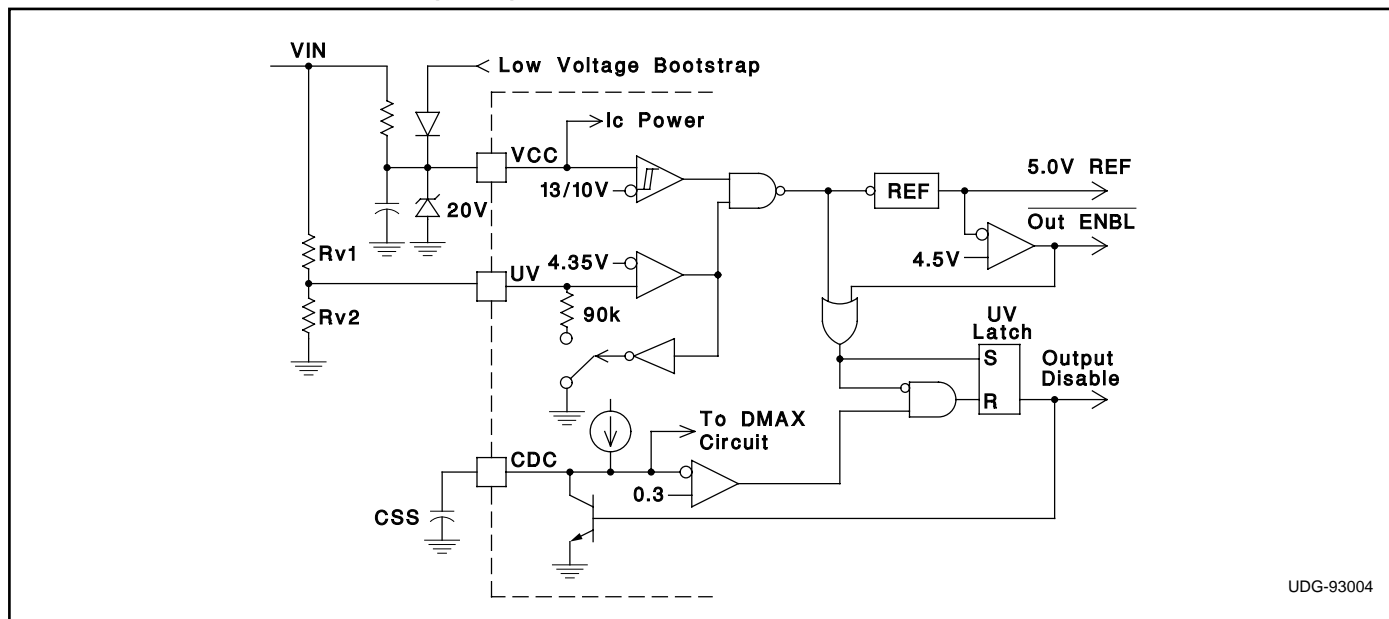
$$V_{IN(\text{hys})} = 4.35\text{V} \cdot Rv1 / 90k.$$

When the UV comparator is low, I_{CC} is low (500μA) and the output is low.

When both the UV and VCC comparators are high, the internal bias circuitry for the rest of the chip is activated. The CDC pin (see discussion on Maximum Duty Cycle Control and Soft Start) and the Output are held low until VREF exceeds the 4.5V threshold of the VREF comparator. When VREF is good, control of the output driver is transferred to the PWM circuitry and CDC is allowed to charge.

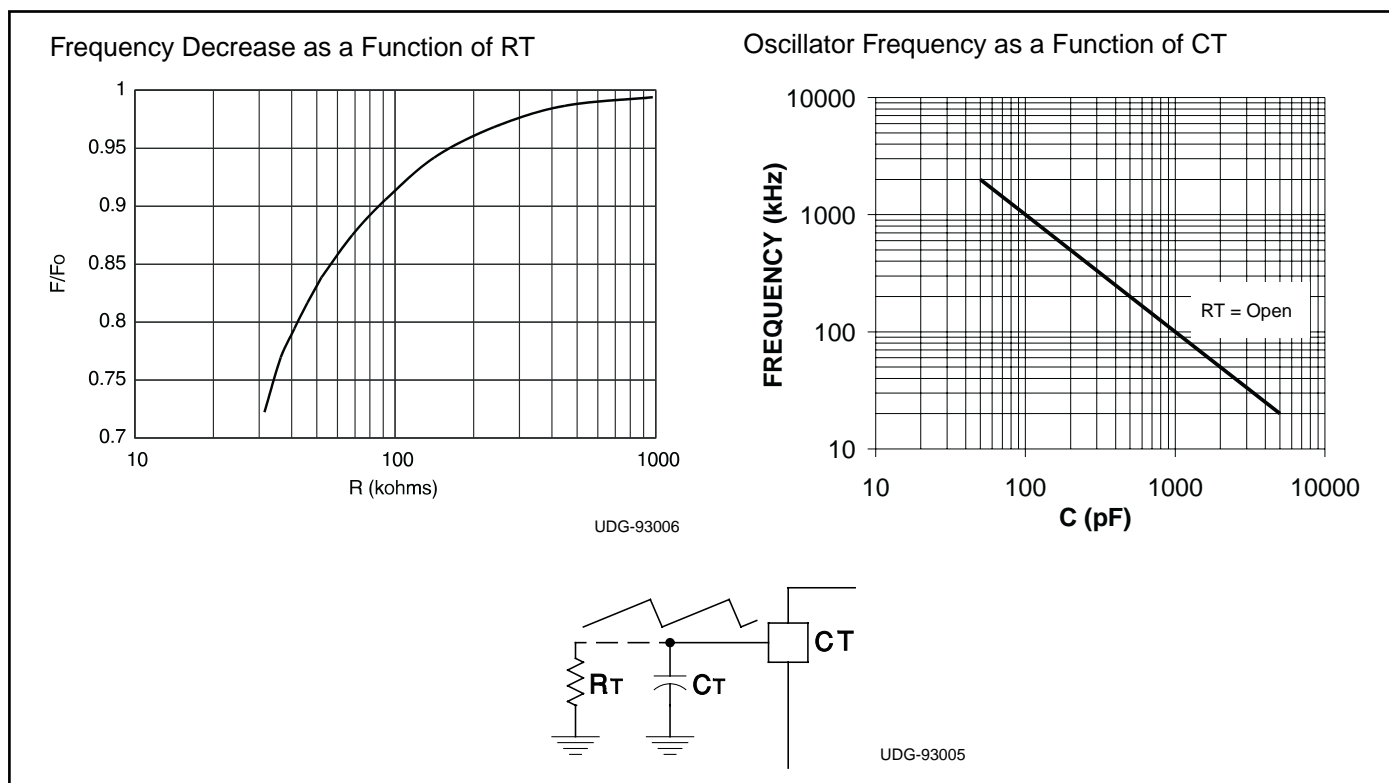
If any of the three UVLO comparators go low, the UVLO latch is set, the output is held low, and CDC is discharged. This state will be maintained until all three comparators are high and the CDC pin is fully discharged.

APPLICATION INFORMATION (cont.)



UDG-93004

Figure 1: Under voltage lockout.



UDG-93006

UDG-93005

Figure 2: Oscillator frequency.

APPLICATION INFORMATION (cont.)

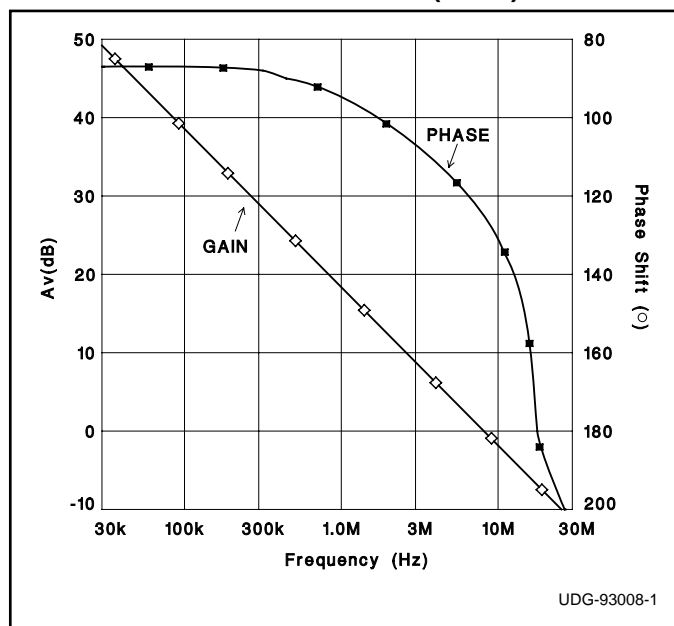


Figure 3: Error amplifier gain and phase response over frequency.

Oscillator

A capacitor from the CT pin to GND programs oscillator frequency, as shown in Fig. 2. Frequency is determined by:

$$F = 1 / (10k \cdot CT)$$

The sawtooth wave shape is generated by a charging current of 200 A and a discharge current of 1800 A. The discharge time of the sawtooth is guaranteed dead time for the output driver. If the maximum duty cycle control is defeated by connecting DMAX to VREF, the maximum duty cycle is limited by the oscillator to 90%. If an adjustment is required, an additional trim resistor RT from CT to Ground can be used to adjust the oscillator frequency. RT should not be less than 40k . This will allow up to a 22% decrease in frequency.

Inductor Current Waveform Synthesizer

Average current mode control is a very useful technique to control the value of any current within a switching converter. Input current, output inductor current, switch current, diode current or almost any other current can be controlled. In order to implement average current mode control, the value of the current must be explicitly known at all times. To control output inductor current (IL) in a buck derived isolated converter, switch current provides inductor current information, but only during the on time

of the switch. During the off time, switch current drops abruptly to zero, but the inductor current actually diminishes with a slope $dIL/dt = -V_O/L$. This down slope must be synthesized in some manner on the primary side to provide the entire inductor current waveform for the control circuit.

The patented current waveform synthesizer (Fig. 4) consists of a unidirectional voltage follower which forces the voltage on capacitor CI to follow the on time switch current waveform. A programmable discharge current synthesizes the off time portion of the waveform. ION is the input to the follower. The discharge current is programmed at IOFF.

The follower has a one volt offset, so that zero current corresponds to one volt at CI. The best utilization of the UC3848 is to translate maximum average inductor current to a 4V signal level. Given N and Ns (the turns ratio of the power and current sense transformers), proper scaling of IL to V(CI) requires a sense resistor Rs as calculated from:

$$R_s = 4V \cdot N_s \cdot N / I_L(\max)$$

Restated, the maximum average inductor current will be limited to:

$$I_L(\max) = 4V \cdot N_s \cdot N / R_s$$

IOFF and CI need to be chosen so that the ratio of $dV(CI)/dt$ to dIL/dt is the same during switch off time as on time. Recommended nominal off current is 100 A. This requires

$$CI = (100 \text{ A} \cdot N \cdot N_s \cdot L) / (R_s \cdot V_O(\text{nom}))$$

where L is the output inductor value and $V_O(\text{nom})$ is the converter regulated output voltage.

There are several methods to program IOFF. If accurate average current control is required during short circuit operation, IOFF must track output voltage. The method shown in Fig. 4 derives a voltage proportional to $V_{IN} \cdot D$ (Duty Cycle). (In a buck converter, output voltage is proportional to $V_{IN} \cdot D$.) A resistively loaded diode connection to the bootstrap winding yields a square wave whose amplitude is proportional to V_{IN} and is duty cycle modulated by the control circuit. Averaging this waveform with a filter generates a primary side replica of secondary regulated V_O . A single pole filter is shown, but in practice a two or three pole filter provides better transient response. Filtered voltage is converted by ROFF to a current to the IOFF pin to control CI down slope.

APPLICATION INFORMATION (cont.)

If the system is not sensitive to short circuit requirements, Figure 5 shows the simplest method of downslope generation: a single resistor ($R_{OFF} = 40k$) from I_{OFF} to V_{REF} . The discharge current is then $100\mu A$. The disadvantage to this approach is that the synthesizer continues to generate a down slope when the switch is off even during short circuit conditions. Actual inductor down slope is closer to zero during a short circuit. The penalty is that the average current is understated by an amount approximately equal to the nominal inductor ripple current. Output short circuit is therefore higher than the designed maximum output current.

A third method of generating I_{OFF} is to add a second winding to the output inductor core (Fig. 6). When the power switch is off and inductor current flows in the free wheeling diode, the voltage across the inductor is equal to the output voltage plus the diode drop. This voltage is then transformed by the second winding to the primary side of the converter. The advantages to this approach are its inherent accuracy and bandwidth. Winding the second coil on the output inductor core while maintaining the required isolation makes this a more costly solution. In the example, $R_{OFF} = V_O / 100\mu A$. The $4 \bullet R_{OFF}$ resistor is added to compensate the one volt input level of the I_{OFF} pin. Without this compensation, a minor current foldback behavior will be observed.

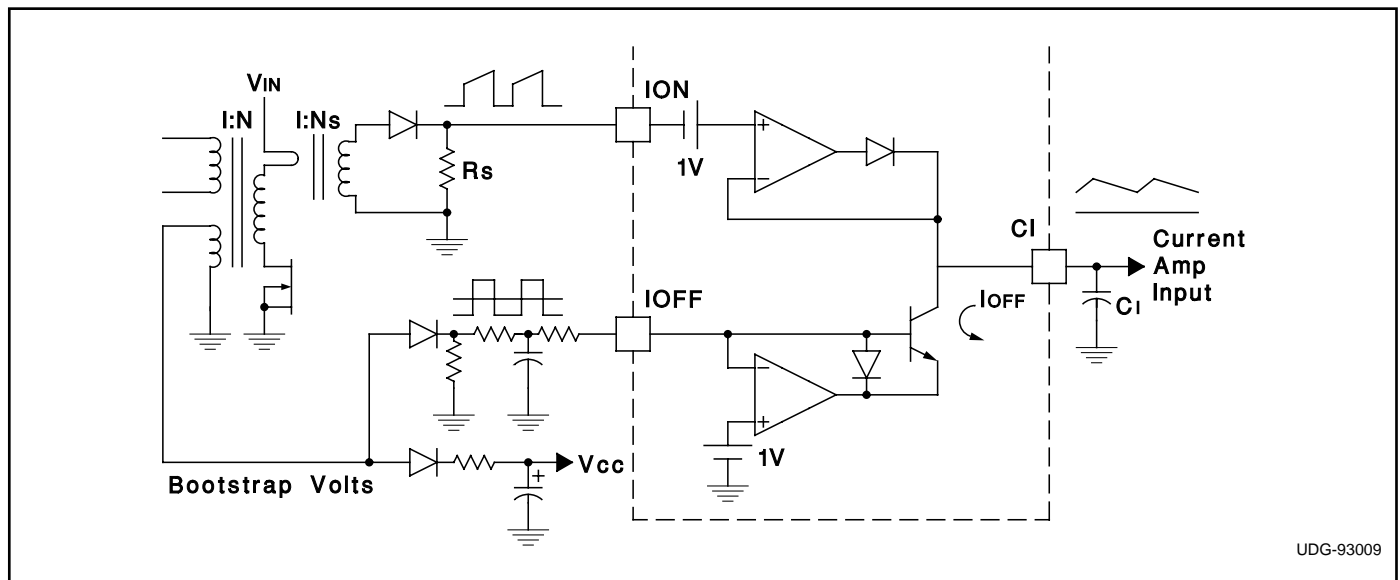


Figure 4: Inductor current waveform synthesizer.

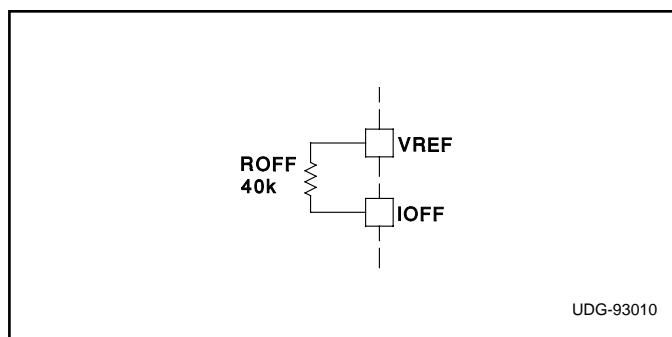


Figure 5: Fixed I_{OFF} .

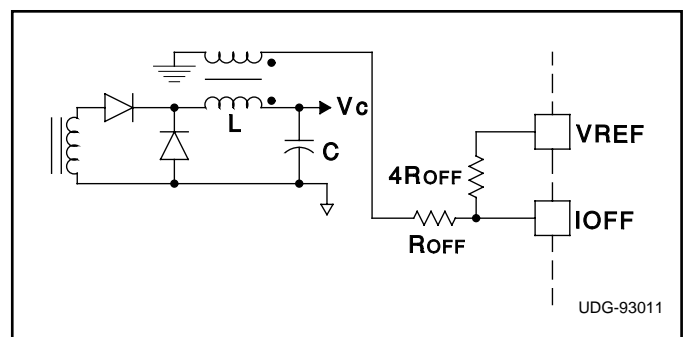


Figure 6: Second inductor winding generation of I_{OFF} .

APPLICATION INFORMATION (cont.)

Maximum Volt-Second Circuit

A maximum volt-second product can be programmed by a resistor (R_{vs}) from V_S to V_{IN} and a capacitor (C_{vs}) from V_S to ground (Figure 7). V_S is discharged while the switch is off. When the output turns on, V_S is allowed to charge. Since the threshold of the V_S comparator is much less than V_{IN} , the charging profile at V_s will be essentially linear. If V_S crosses the 4.0V threshold before the PWM turns the output off, the V_S comparator will turn the output off for the remainder of the cycle. The maximum volt-second product is

$$V_{IN} \cdot T_{ON(max)} = 4.0V \cdot R_{vs} \cdot C_{vs}.$$

Maximum Duty Cycle And Soft Start

A patented technique is used to accurately program maximum duty cycle. Programming is accomplished by a divider from V_{REF} to D_{MAX} (Fig. 7). The value programmed is:

$$D(max) = R_{d1} / (R_{d1} + R_{d2}).$$

For proper operation, the integrating capacitor, C_{DC} , should be larger than $C_{DC(min)} > T(osc) / 80k$, where $T(osc)$ is the oscillator period. C_{DC} also sets the soft start time constant, so values of C_{DC} larger than minimum may be desired. The soft start time constant is approximately:

$$T(ss) = 20k \cdot C_{DC}.$$

Ground Planes

The output driver on the UC3848 is capable of 2A peak currents. Careful layout is essential for correct operation of the chip. A ground plane must be employed (Fig. 8). A unique section of the ground plane must be designated for high di/dt currents associated with the output stage. This point is the power ground to which the PGND pin is connected. Power ground can be separated from the rest of the ground plane and connected at a single point, although this is not strictly necessary if the high di/dt paths are well understood and accounted for. V_{CC} should be bypassed directly to power ground with a good high frequency capacitor. The sources of the power MOSFET should connect to power ground as should the return connection for input power to the system and the bulk input capacitor. The output should be clamped with a high current Schottky diode to both V_{CC} and PGND. Nothing else should be connected to power ground.

V_{REF} should be bypassed directly to the signal portion of the ground plane with a good high frequency capacitor. Low esr/esl ceramic 1 F capacitors are recommended for both V_{CC} and V_{REF} . The capacitors from C_T , C_{DC} , and C_I should likewise be connected to the signal ground plane.

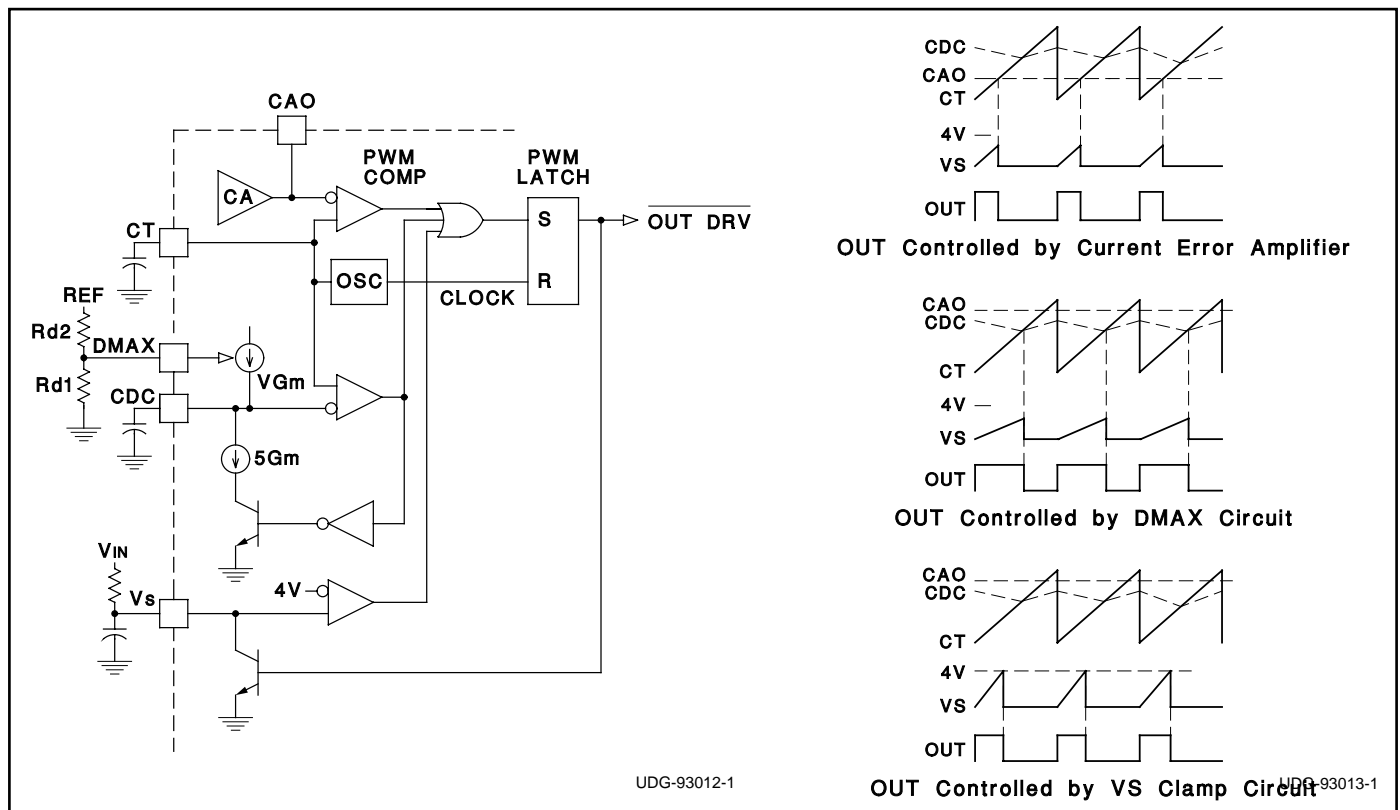
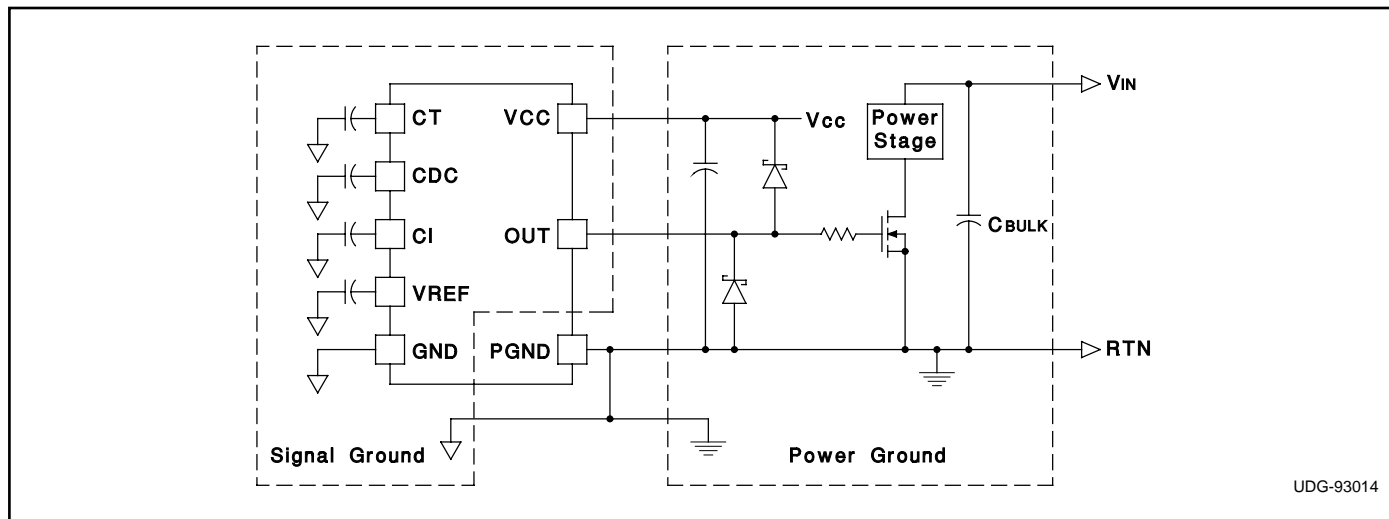
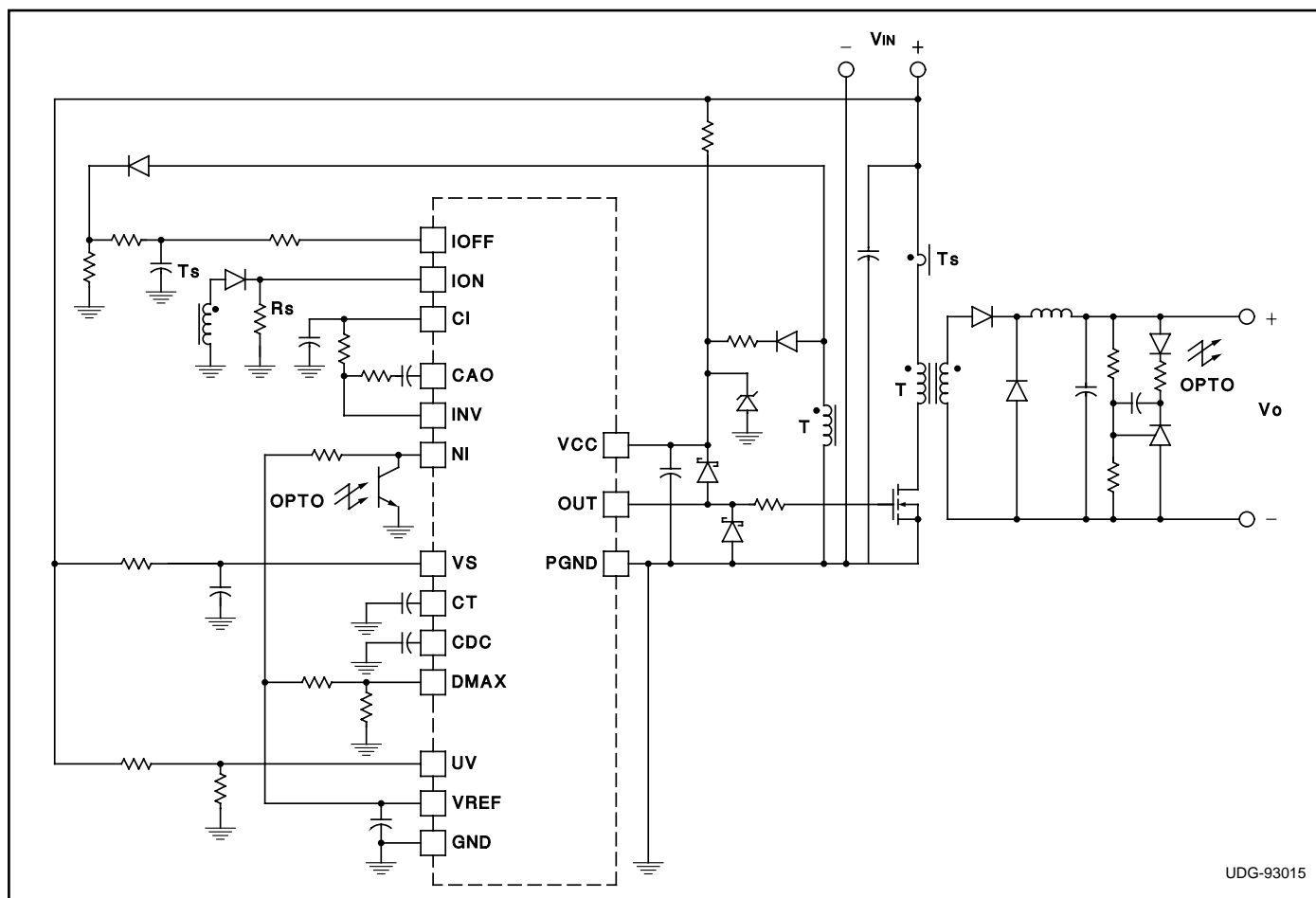


Figure 7: Duty cycle control.



UDG-93014

Figure 8: Ground plane considerations.



UDG-93015

Figure 9: Typical application - an average current-mode isolated forward converter.

PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp ⁽³⁾
UC1848J	OBSOLETE	CDIP	J	16		TBD	Call TI	Call TI
UC2848DW	ACTIVE	SOIC	DW	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
UC2848DWG4	ACTIVE	SOIC	DW	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
UC2848J	OBSOLETE	CDIP	J	16		TBD	Call TI	Call TI
UC3848DW	ACTIVE	SOIC	DW	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
UC3848DWG4	ACTIVE	SOIC	DW	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
UC3848DWTR	ACTIVE	SOIC	DW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
UC3848DWTRG4	ACTIVE	SOIC	DW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
UC3848N	ACTIVE	PDIP	N	16	25	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type
UC3848NG4	ACTIVE	PDIP	N	16	25	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

Important Information and Disclaimer:The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION



QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
UC3848DWTR	SOIC	DW	16	2000	330.0	16.4	10.85	10.8	2.7	12.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS

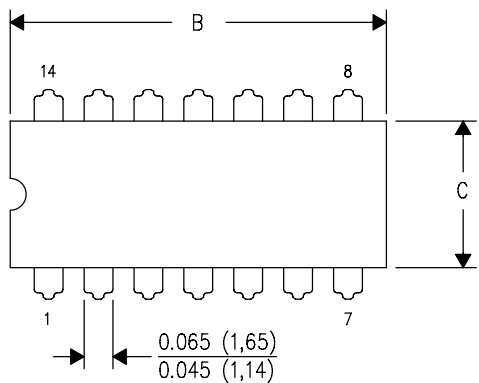


*All dimensions are nominal

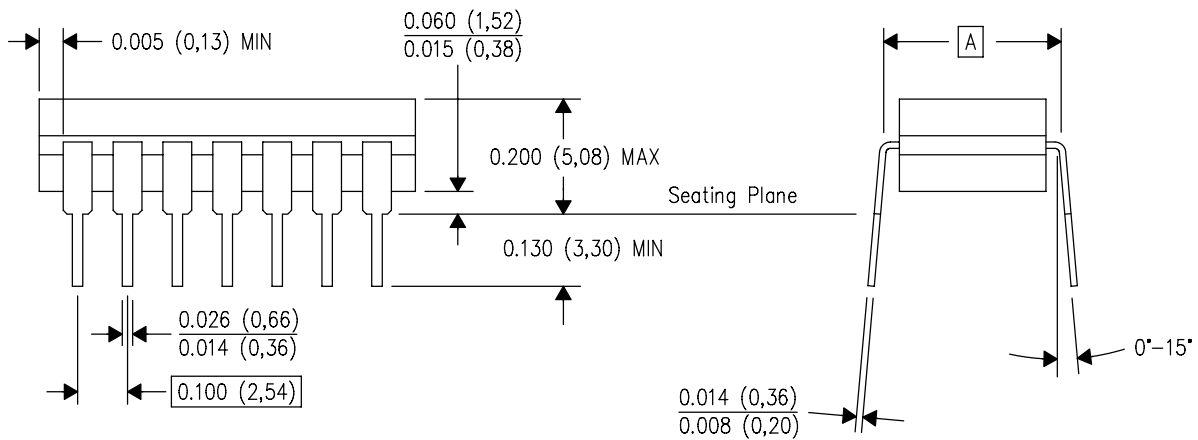
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
UC3848DWTR	SOIC	DW	16	2000	346.0	346.0	33.0

J (R-GDIP-T**)
14 LEADS SHOWN

CERAMIC DUAL IN-LINE PACKAGE



DIM \ PINS **	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)

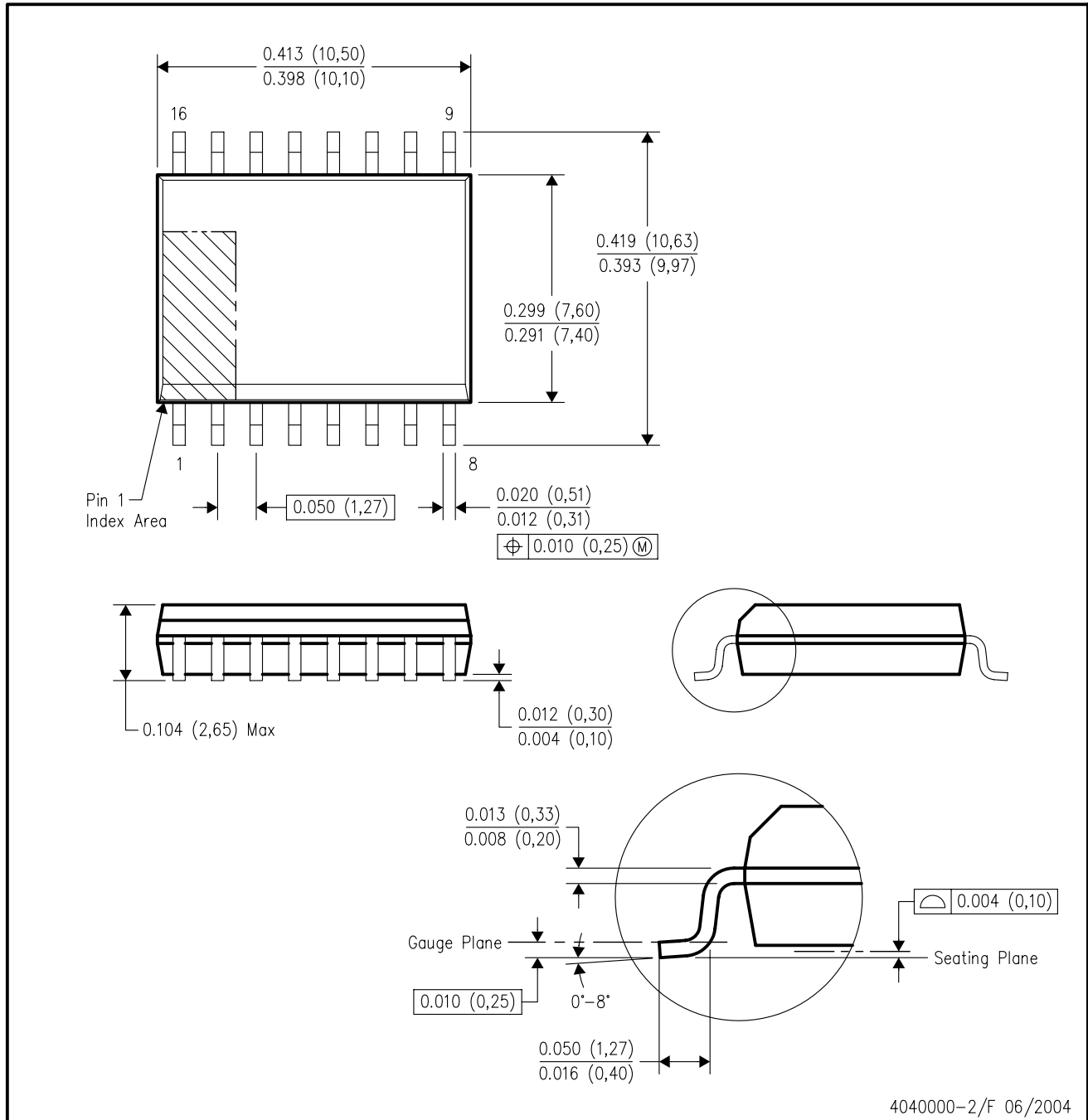


4040083/F 03/03

- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. This package is hermetically sealed with a ceramic lid using glass frit.
 - D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
 - E. Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

DW (R-PDSO-G16)

PLASTIC SMALL-OUTLINE PACKAGE



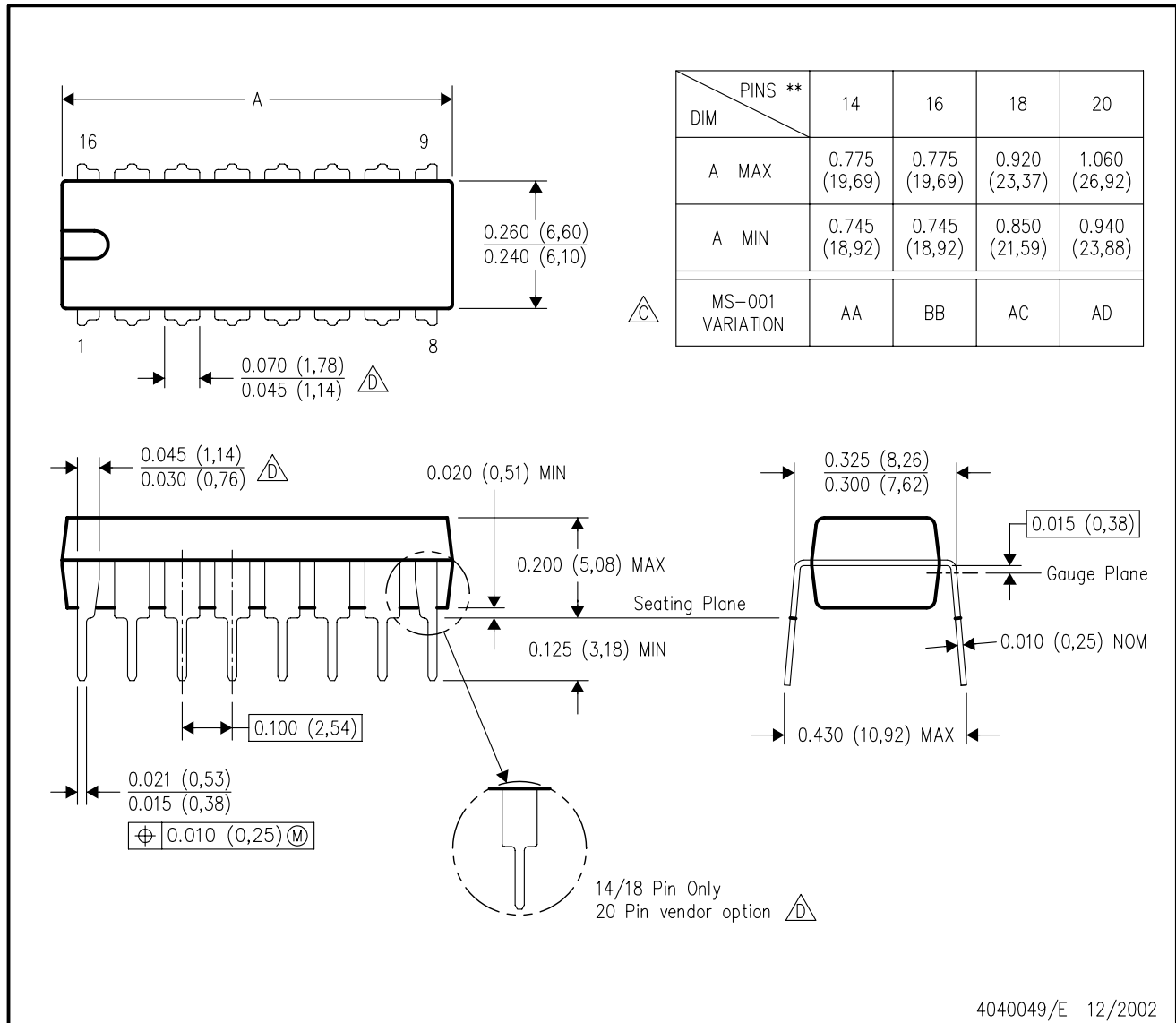
4040000-2/F 06/2004

- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
 - D. Falls within JEDEC MS-013 variation AA.

N (R-PDIP-T**)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
 - The 20 pin end lead shoulder width is a vendor option, either half or full width.

IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, modifications, enhancements, improvements, and other changes to its products and services at any time and to discontinue any product or service without notice. Customers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All products are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its hardware products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by government requirements, testing of all parameters of each product is not necessarily performed.

TI assumes no liability for applications assistance or customer product design. Customers are responsible for their products and applications using TI components. To minimize the risks associated with customer products and applications, customers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any TI patent right, copyright, mask work right, or other TI intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information published by TI regarding third-party products or services does not constitute a license from TI to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of TI information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. Reproduction of this information with alteration is an unfair and deceptive business practice. TI is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

Resale of TI products or services with statements different from or beyond the parameters stated by TI for that product or service voids all express and any implied warranties for the associated TI product or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

TI products are not authorized for use in safety-critical applications (such as life support) where a failure of the TI product would reasonably be expected to cause severe personal injury or death, unless officers of the parties have executed an agreement specifically governing such use. Buyers represent that they have all necessary expertise in the safety and regulatory ramifications of their applications, and acknowledge and agree that they are solely responsible for all legal, regulatory and safety-related requirements concerning their products and any use of TI products in such safety-critical applications, notwithstanding any applications-related information or support that may be provided by TI. Further, Buyers must fully indemnify TI and its representatives against any damages arising out of the use of TI products in such safety-critical applications.

TI products are neither designed nor intended for use in military/aerospace applications or environments unless the TI products are specifically designated by TI as military-grade or "enhanced plastic." Only products designated by TI as military-grade meet military specifications. Buyers acknowledge and agree that any such use of TI products which TI has not designated as military-grade is solely at the Buyer's risk, and that they are solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI products are neither designed nor intended for use in automotive applications or environments unless the specific TI products are designated by TI as compliant with ISO/TS 16949 requirements. Buyers acknowledge and agree that, if they use any non-designated products in automotive applications, TI will not be responsible for any failure to meet such requirements.

Following are URLs where you can obtain information on other Texas Instruments products and application solutions:

Products

Amplifiers	amplifier.ti.com
Data Converters	dataconverter.ti.com
DSP	dsp.ti.com
Clocks and Timers	www.ti.com/clocks
Interface	interface.ti.com
Logic	logic.ti.com
Power Mgmt	power.ti.com
Microcontrollers	microcontroller.ti.com
RFID	www.ti-rfid.com
RF/IF and ZigBee® Solutions	www.ti.com/lprf

Applications

Audio	www.ti.com/audio
Automotive	www.ti.com/automotive
Broadband	www.ti.com/broadband
Digital Control	www.ti.com/digitalcontrol
Medical	www.ti.com/medical
Military	www.ti.com/military
Optical Networking	www.ti.com/opticalnetwork
Security	www.ti.com/security
Telephony	www.ti.com/telephony
Video & Imaging	www.ti.com/video
Wireless	www.ti.com/wireless

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
Copyright © 2008, Texas Instruments Incorporated

www.BDTIC.com/TI