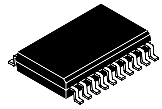


SLUS157O – DECEMBER 1999 – REVISED APRIL 2010

BiCMOS ADVANCED PHASE-SHIFT PWM CONTROLLER

FEATURES

- **Programmable Output Turn-on Delay**
- **Adaptive Delay Set**
- **Bidirectional Oscillator Synchronization**
- **Voltage-Mode, Peak Current-Mode, or Average Current-Mode Control**
- **Programmable Softstart/Softstop and Chip Disable via a Single Pin**
- **0% to 100% Duty-Cycle Control**
- **7-MHz Error Amplifier**
- **Operation to 1 MHz**
- **Typical 5-mA Operating Current at 500 kHz**
- **Very Low 150-μA Current During UVLO**

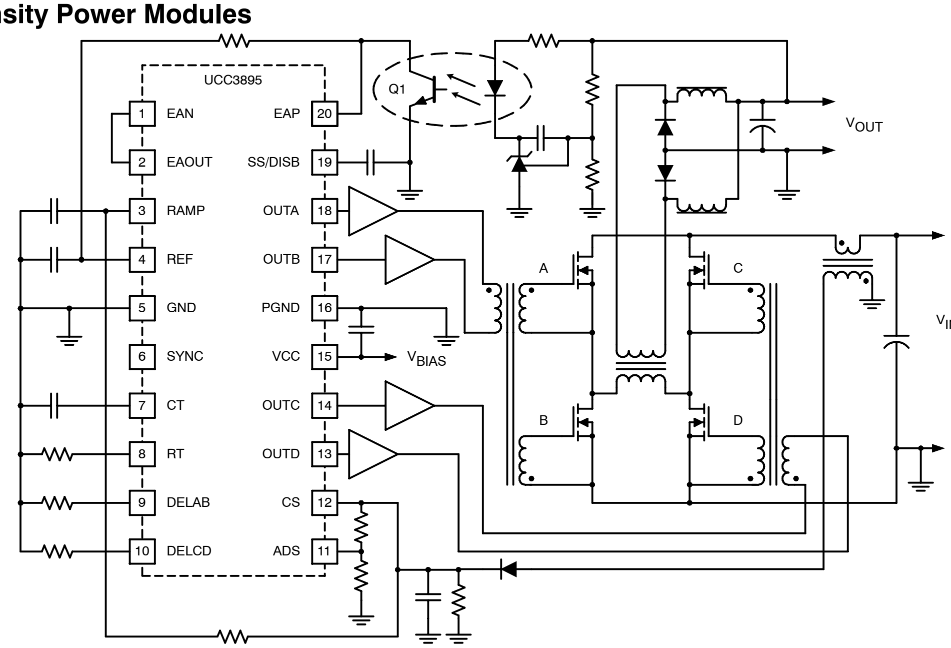
APPLICATIONS

- **Phase-Shifted Full-Bridge Converters**
- **Off-Line, Telecom, Datacom and Servers**
- **Distributed Power Architecture**
- **High-Density Power Modules**

DESCRIPTION

The UCC3895 is a phase-shift PWM controller that implements control of a full-bridge power stage by phase shifting the switching of one half-bridge with respect to the other. It allows constant frequency pulse-width modulation in conjunction with resonant zero-voltage switching to provide high efficiency at high frequencies. The part can be used either as a voltage-mode or current-mode controller.

While the UCC3895 maintains the functionality of the UC3875/6/7/8 family and UC3879, it improves on that controller family with additional features such as enhanced control logic, adaptive delay set, and shutdown capability. Since it is built using the BCDMOS process, it operates with dramatically less supply current than it's bipolar counterparts. The UCC3895 can operate with a maximum clock frequency of 1 MHz.



UDG–03123

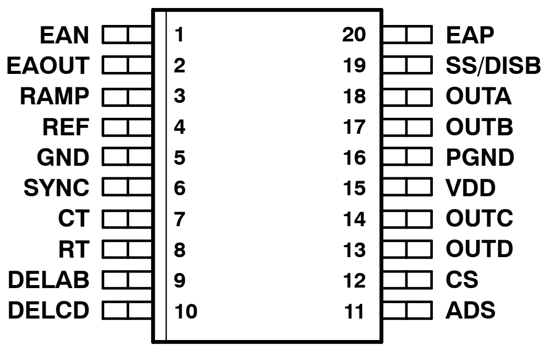
Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

ORDERING INFORMATION

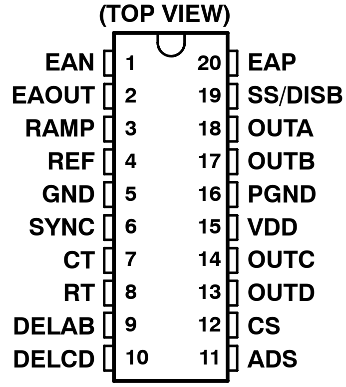
T_A	PACKAGED DEVICES					
	SOIC-20(DW)[(1)]	PDIP-20(N)	TSSOP-20(PW) (1)	PLCC-20(Q)[(1)]	CLCC-20(L)	CDIP-20(J)
-55°C to 125°C					UCC1895L	UCC1895J
-40°C to 85°C	UCC2895DW	UCC2895N	UCC2895PW	UCC2895Q		
0°C to 70°C	UCC3895DW	UCC3895N	UCC3895PW	UCC3895Q		

(1) The DW, PW and Q packages are available taped and reeled. Add TR suffix to device type (e.g. UCC2895DWTR) to order quantities of 2000 devices per reel for DW.

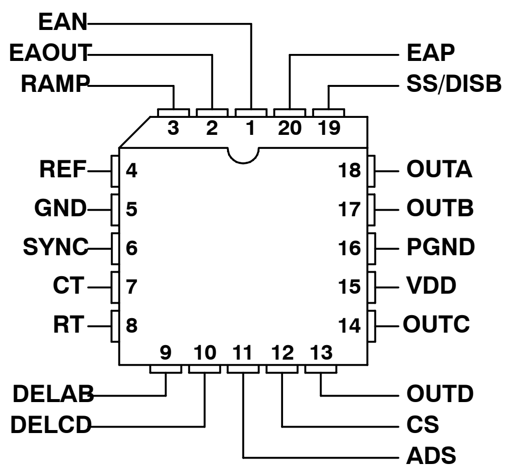
PW and DW PACKAGE
(TOP VIEW)



N and J PACKAGE
(TOP VIEW)



Q and L PACKAGE
(TOP VIEW)



PART	T_{JA}	T_{JC}	UNIT
UCC2895DW	90	25	°C/W
UCC2895N	80	35	
UCC2895PW	125	14	
UCC2895Q	75	34	
UCC1895J	85	28	
UCC1895L	80	20	

ABSOLUTE MAXIMUM RATINGS

All voltage values are with respect to the network ground terminal unless otherwise noted. (2)

		UCCx895N	UNIT
Supply voltage	(I_{DD} < 10 mA)	17	V
Supply current		30	mA
Reference current		15	
Output crrent		100	
Analog inputs	EAP, EAN, EAOUT, RAMP, SYNC, ADS, CS, SS/DISB	−0.3 V to REF+0.3 V	V
Drive outputs	OUTA, OUTB, OUTC, OUTD	−0.3 V to VCC + 0.3 V	
Power dissipation at T_A = 25°C	DW−20 package	650	mW
	N−20 package	1	W
Storage temperature range, T_{stg}		−65 to 150	°C
Junction temperature range, T_J		−55 to 150	
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds		300	

(2) Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under ”recommended operating conditions” is not implied. Exposure to Absolute Maximum Rated conditions for extended periods may affect device reliability

RECOMMENDED OPERATING CONDITIONS(3)

	MIN	TYP	MAX	UNIT
Supply voltage, V_{DD}	10		16.5	V
Supply voltage bypass capacitor, V_{DD}(1)		10 x C_{REF}		µF
Reference bypass capacitor, C_{REF}(2) (UCC1895)	0.1		1.0	
Reference bypass capacitor, C_{REF}(2) (UCC2895, UCC3895)	0.1		4.7	
Timing capacitor, C_T (for 500 kHz switching frequency)		220		pF
Timing resistor, R_T (for 500 kHz switching frequency)		82		kΩ
Delay resistor R_{DEL_AB}, R_{DEL_CD}	2.5		40	
Operating junction temperature, T_J(4)	−55		125	°C

(1) The V_{DD} capacitor should be a low ESR, ESL ceramic capacitor located directly across the VDD and PGND pins. A larger bulk capacitor should belocated as physically close as possible to the V_{DD} pins.
(2) The V_{REF} capacitor should be a low ESR, ESL ceramic capacitor located directly across the REF and GND pins. If a larger capacitor is desired for the V_{REF} then it should be located near the V_{REF} cap and connected to the V_{REF} pin with a resistor of 51 Ω or greater. The bulk capacitor on V_{DD} must be a factor of 10 greater than the total V_{REF} capacitance.
(3) It is recommended that there be a single point grounded between GND and PGND directly under the device. There should be a seperate ground plane associated with the GND pin and all components associated with pins 1 through 12 plus 19 and 20 be located over this ground plane. Any connections associated with these pins to ground should be connected to this ground plane.
(4) It is not recommended that the device operate under conditions beyond those specified in this table for extended periods of time.

ELECTRICAL CHARACTERISTICS

V_{DD} = 12 V, R_T = 82 kΩ, C_T = 220 pF, R_{DELAB} = 10 kΩ, R_{DELCD} = 10 kΩ, C_{REF} = 0.1 µF, C_{VDD} = 0.1 µF and no load on the outputs, T_A = T_J. T_A = 0°C to 70°C for UCC3895x, T_A = −40°C to 85°C for UCC2895x and TA = −55°C to 125°C for the UCC1895x. (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNITS
UVLO (UNDERVOLTAGE LOCKOUT)						
$UVLO_{(on)}$	Start-up voltage threshold		10.2	11	11.8	
$UVLO_{(off)}$	Minimum operating voltage after start-up		8.2	9	9.8	V
$UVLO_{(hys)}$	Hysteresis		1.0	2.0	3.0	
SUPPLY						
I_{START}	Start-up current	VDD = 8 V		150	250	µA
I_{DD}	Operating current			5	6	mA
V_{DD_CLAMP}	V_{DD} clamp voltage	IDD = 10 mA	16.5	17.5	18.5	V
VOLTAGE REFERENCE						
V_{REF}	Output voltage	T_J = 25°C	4.94	5.00	5.06	V
		10 V < VDD < V_{DD_CLAMP}, 0 mA < IREF < 5 mA, temperature	4.85	5	5.15	
I_{SC}	Short circuit current	REF = 0 V, T_J = 25°C	10	20		mA
ERROR AMPLIFIER						
	Common-mode input voltage range		−0.1		3.6	V
V_{IO}	Offset voltage		−7		7	mV
I_{BIAS}	Input bias current (EAP, EAN)		−1		1	µA
$EAOUT\_{VOH}$	High-level output voltage	EAP−EAN = 500 mV, I_{EAOUT} = −0.5 mA	4.0	4.5	5.0	V
$EAOUT\_{VOL}$	Low-level output voltage	EAP−EAN = −500 mV, I_{EAOUT} = 0.5 mA	0	0.2	0.4	
I_{SOURCE}	Error amplifier output source current	EAP−EAN = 500 mV, EAOUT = 2.5 V	1.0	1.5		mA
I_{SINK}	Error amplifier output sink current	EAP−EAN = −500 mV, EAOUT = 2.5 V	2.5	4.5		
A_{VOL}	Open-loop dc gain		75	85		dB
GBW	Unity gain bandwidth(1)		5.0	7.0		MHz
	Slew rate(1)	1 V < EAN < 0 V, EAP = 500 mV 0.5 V < EAOUT < 3.0 V	1.5	2.2		V/µs
	No-load comparator turn-off threshold		0.45	0.50	0.55	
	No-load comparator turn-on threshold		0.55	0.60	0.69	V
	No-load comparator hysteresis		0.035	0.10	0.165	
OSCILLATOR						
f_{OSC}	Frequency	T_J = 25°C	473	500	527	kHz
	Frequency total variation(1)	Over line, temperature		2.5%	5%	
V_{IH_SYNC}	SYNC input threshold, SYNC		2.05	2.10	2.40	
V_{OH_SYNC}	High-level output voltage, SYNC	I_{SYNC} = −400 µA, V_{CT} = 2.6 V	4.1	4.5	5.0	V
V_{OL_SYNC}	Low-level output voltage, SYNC	I_{SYNC} = 100 µA, V_{CT} = 0.0 V	0.0	0.5	1.0	
	Sync output pulse width	$LOAD_{SYNC}$ = 3.9 kΩ and 30 pF in parallel		85	135	ns
V_{RT}	Timing resistor voltage		2.9	3	3.1	
$V_{CT(peak)}$	Timing capacitor peak voltage		2.25	2.35	2.55	V
$V_{CT(valley)}$	Timing capacitor valley voltage		0.0	0.2	0.4	

(1) Ensured by design. Not production tested.

ELECTRICAL CHARACTERISTICS V_{DD} = 12 V, R_T = 82 kΩ, C_T = 220 pF, R_{DELAB} = 10 kΩ, R_{DELCD} = 10 kΩ, C_{REF} = 0.1 µF, C_{VDD} = 0.1 µF and no load on the outputs, $T_A = T_J$. T_A = 0°C to 70°C for UCC3895x, T_A = –40°C to 85°C for UCC2895x and TA = –55°C to 125°C for the UCC1895x. (unless otherwise noted)

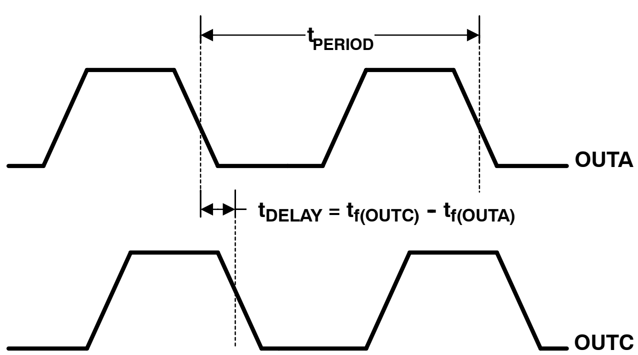
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNITS
CURRENT SENSE						
$I_{CS(bias)}$	Current sense bias current	0 V < CS < 2.5 V, 0 V ADS < 2.5 V	–4.5		20	µA
	Peak current threshold		1.90	2.00	2.10	V
	Overcurrent threshold		2.4	2.5	2.6	V
	Current sense to output delay	0V ≤ CS ≤ 2.3 V, DELAB=DELCD=REF		75	110	ns
SOFT-START/SHUTDOWN						
I_{SOURCE}	Softstart source current	SS/DISB = 3.0 V, CS = 1.9 V	–40	–35	–30	µA
I_{SINK}	Softstart sink current	SS/DISB = 3.0 V, CS = 2.6 V	325	350	375	µA
	Softstart/disable comparator threshold		0.44	0.50	0.56	V
ADAPTIVE DELAY SET (ADS)						
	DELAB/DELCD output voltage	ADS = CS = 0 V	0.45	0.50	0.55	V
		ADS = 0 V, CS = 2.0 V	1.9	2.0	2.1	V
t_{DELAY}	Output delay(1)(3)	ADS = CS = 0 V	450	560	620	ns
	ADS bias current	0 V < ADS < 2.5 V, 0 V < CS < 2.5 V	–20		20	µA
OUTPUT						
V_{OH}	High–level output voltage (all outputs)	I_{OUT} = –10 mA, VDD to output		250	400	mV
V_{OL}	Low-level output voltage (all outputs)	I_{OUT} = 10 mA		150	250	mV
t_R	Rise time(1)	C_{LOAD} = 100 pF		20	35	ns
t_F	Fall time(1)	C_{LOAD} = 100 pF		20	35	ns

(1) Ensured by design. Not production tested.
(2) Minimum phase shift is defined as:

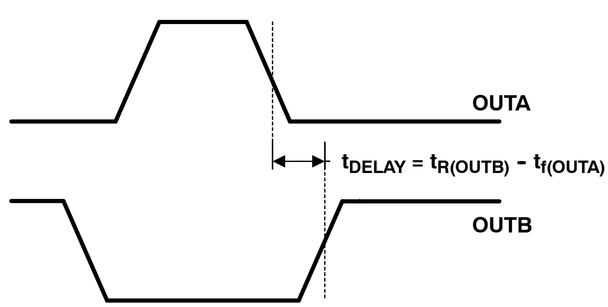
$$\Phi = 180 \times \frac{t_{f\,(OUTC)} - t_{f\,(OUTA)}}{t_{PERIOD}} \quad \text{or} \quad \Phi = 180 \times \frac{t_{f\,(OUTC)} - t_{f\,(OUTB)}}{t_{PERIOD}} \quad \text{where}$$

$t_{f(OUTA)}$ = falling edge of OUTA signal, $t_{f(OUTB)}$ = falling edge of OUTB signal
$t_{f(OUTC)}$ = falling edge of OUTC signal, $t_{f(OUTD)}$ = falling edge of OUTD signal
t_{PERIOD} = period of OUTA or OUTB signal

(3) Output delay is measured between OUTA/OUTB or OUTC/OUTD. Output delay is defined as shown below where:
$t_{f(OUTA)}$ = falling edge of OUTA signal, $t_{r(OUTB)}$ = rising edge of OUTB signal



Same applies to OUTB and OUTD



Same applies to OUTC and OUTD

ELECTRICAL CHARACTERISTICS

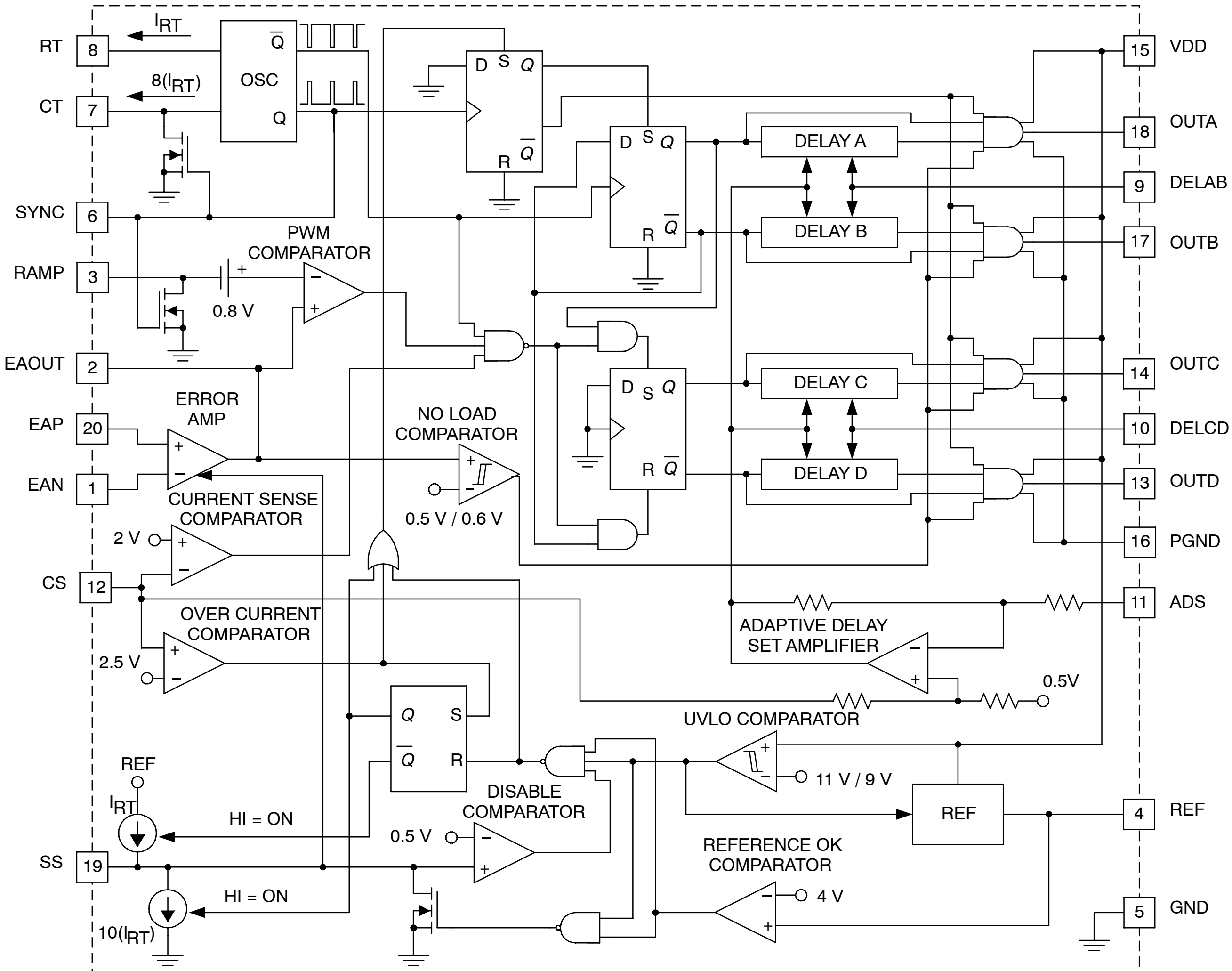
V_{DD} = 12 V, R_T = 82 kΩ, C_T = 220 pF, R_{DELAB} = 10 kΩ, R_{DELCD} = 10 kΩ, C_{REF} = 0.1 μF, C_{VDD} = 0.1 μF and no load on the outputs, T_A = T_J. T_A = 0°C to 70°C for UCC3895x, T_A = –40°C to 85°C for UCC2895x and TA = 55°C to 125°C for the UCC1895x. (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNITS
PWM COMPARATOR							
	EAOUT to RAMP input offset voltage	RAMP = 0 V,	DELAB=DELCD=REF	0.72	0.85	1.05	V
	Minimum phase shift[(2)] (OUTA to OUTC, OUTB to OUTD)	RAMP = 0 V	EAOUT = 650 mV	.0%	.85%	1.4%	
t_{DELAY}	Delay[(3)] (RAMP to OUTC, RAMP to OUTD)	0 V < RAMP < 2.5 V, DELAB=DELCD=REF	EAOUT = 1.2 V,		70	120	ns
$I_{R(bias)}$	RAMP bias current	RAMP < 5 V,	CT = 2.2 V	–5		5	μA
$I_{R(sink)}$	RAMP sink current	RAMP = 5 V,	CT = 2.6 V	12	19		mA

TERMINAL FUNCTIONS

TERMINAL NAME	NO.	I/O	DESCRIPTION
ADS	11	I	Adaptive delay set. Sets the ratio between the maximum and minimum programmed output delay dead time.
CS	12	I	Current sense input for cycle-by-cycle current limiting and for over-current comparator.
CT	7	I	Oscillator timing capacitor for programming the switching frequency. The UCC3895’s oscillator charges CT via a programmed current.
DELAB	9	I	Delay programming between complementary outputs. DELAB programs the dead time between switching of output A and output B.
DELCD	10	I	Delay programming between complementary outputs. DELCD programs the dead time between switching of output C and output D.
EAOUT	2	I/O	Error amplifier output.
EAP	20	I	Non-inverting input to the error amplifier. Keep below 3.6 volts for proper operation.
EAN	1	I	Inverting input to the error amplifier. Keep below 3.6 volts for proper operation.
GND	5	–	Chip ground for all circuits except the output stages.
OUTA	18	O	The four outputs are 100-mA complementary MOS drivers, and are optimized to drive FET driver circuits such as UCC27424 or gate drive transformers.
OUTB	17	O	
OUTC	14	O	
OUTD	13	O	
PGND	16	–	Output stage ground.
RAMP	3	I	Inverting input of the PWM comparator.
REF	4	O	5 V, ±1.2%, 5 mA voltage reference. For best performance, bypass with a 0.1-μF low ESR, low ESL capacitor to ground. Do not use more than 4.7 μF of total capacitance on this pin.
RT	8	I	Oscillator timing resistor for programming the switching frequency.
SS/DISB	19	I	Soft-start/disable. This pin combines the two independent functions.
SYNC	6	I/O	Oscillator synchronization. This pin is bidirectional.
VDD	15	I	Power supply input pin. VDD must be bypassed with a minimum of a 1.0-μF low ESR, low ESL capacitor to ground. The addition of a 10–μF low ESR, low ESL between VDD and PGND is recommended.

BLOCK DIAGRAM



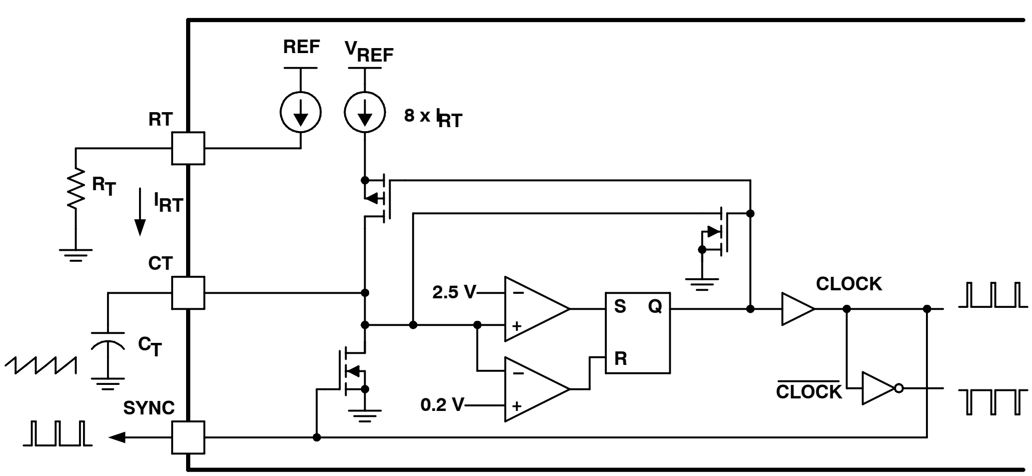


Figure 1. Oscillator Block Diagram

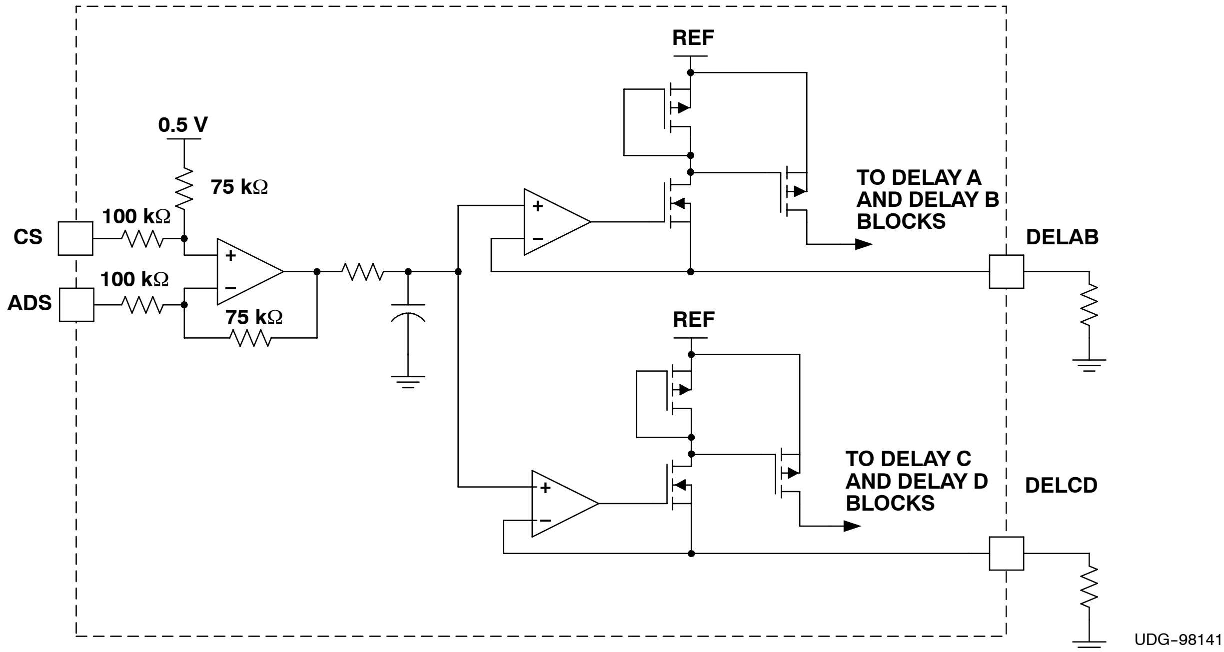


Figure 2. Adaptive Delay Set Block Diagram

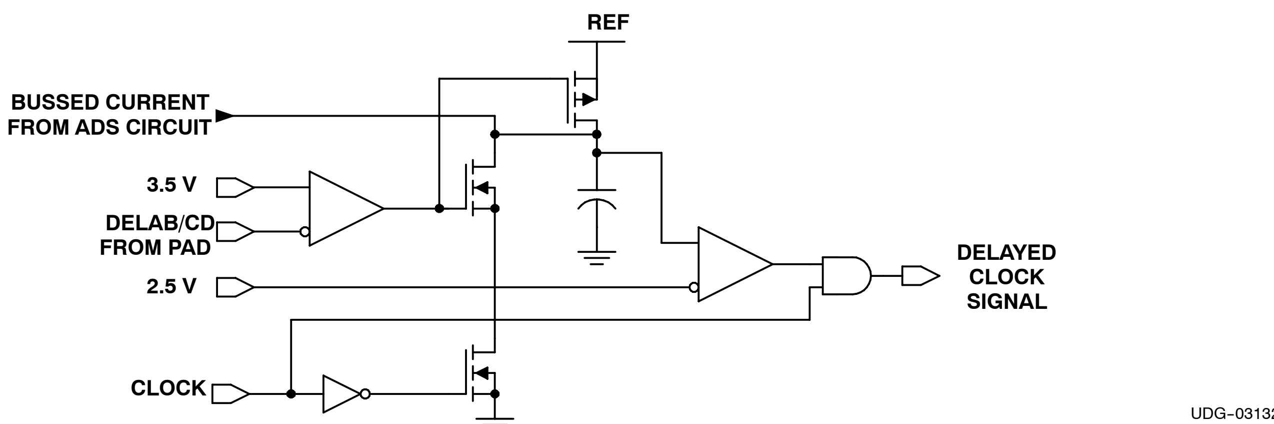


Figure 3. Delay Block Diagram (One Delay Block Per Outlet)

DETAILED PIN DESCRIPTION

Adaptive Delay Set (ADS)

This function sets the ratio between the maximum and minimum programmed output-delay dead time. When the ADS pin is directly connected to the CS pin, no delay modulation occurs. The maximum delay modulation occurs when ADS is grounded. In this case, delay time is four times longer when CS = 0 than when CS = 2.0 V (the peak-current threshold), ADS changes the output voltage on the delay pins DELAB and DELCD by the following formula:

$$V_{DEL} = \left[0.75 \times \left(V_{CS} - V_{ADS}\right)\right] + 0.5\ V \tag{1}$$

where V_{CS} and V_{ADS} are in volts. ADS must be limited to between 0 V and 2.5 V and must be less than or equal to CS. DELAB and DELCD are clamped to a minimum of 0.5 V.

Current Sense (CS)

The inverting input of the current-sense comparator and the non-inverting input of the overcurrent comparator and the ADS amplifier. The current sense signal is used for cycle-by-cycle current limiting in peak current mode control, and for overcurrent protection in all cases with a secondary threshold for output shutdown. An output disable initiated by an overcurrent fault also results in a restart cycle, called *soft stop*, with full soft start.

Oscillator Timing Capacitor (CT)

The UCC3895's oscillator charges CT via a programmed current. The waveform on C_T is a sawtooth, with a peak voltage of 2.35 V. The approximate oscillator period is calculated by the following formula:

$$t_{OSC} = \frac{5 \times R_T \times C_T}{48} + 120\ ns \tag{2}$$

where C_T is in Farads, and R_T is in Ohms and t_{OSC} is in seconds. C_T can range from 100 pF to 880 pF.

NOTE: A large C_T and a small R_T combination results in extended fall times on the C_T waveform. The increased fall time increases the SYNC pulse width, hence limiting the maximum phase shift between OUTA, OUTB and OUTC, OUTD outputs, which limits the maximum duty cycle of the converter. (Refer to Figure 1)

Delay Programming Between Complementary Outputs (DELAB, DELCD)

DELAB programs the dead time between switching of OUTA and OUTB, and DELCD programs the dead time between OUTC and OUTD. This delay is introduced between complementary outputs in the same leg of the external bridge. The UCC2895N allows the user to select the delay, in which the resonant switching of the external power stages takes place. Separate delays are provided for the two half-bridges to accommodate differences in resonant-capacitor charging currents. The delay in each stage is set according to the following formula:

$$t_{DELAY} = \frac{(25 \times 10^{-12}) \times R_{DEL}}{V_{DEL}} + 25\ ns \tag{3}$$

where V_{DEL} (V), and R_{DEL} is in (Ω) and t_{DELAY} is in seconds. DELAB and DELCD can source about 1 mA maximum. Choose the delay resistors so that this maximum is not exceeded. Programmable output delay is defeated by tying DELAB and/or DELCD to REF. For an optimum performance keep stray capacitance on these pins at less than 10 pF.

DETAILED PIN DESCRIPTION (continued)

Error Amplifier (EAOUT), (EAP), (EAN)

EAOUT connected internally to the non-inverting input of the PWM comparator and the no-load comparator. EAOUT is internally clamped to the soft-start voltage. The no-load comparator shuts down the output stages when EAOUT falls below 500 mV, and allows the outputs to turn on again when EAOUT rises above 600 mV.

EAP is the non–inverting and the EAN is the inverting input to the error amplifier.

Output MOSFET Drivers (OUTA, OUTB, OUTC, OUTD)

The 4 outputs are 100-mA complementary MOS drivers, and are optimized to drive MOSFET driver circuits. OUTA and OUTB are fully complementary, (assuming no programming delay). They operate near 50% duty cycle and one-half the oscillator frequency. OUTA and OUTB are intended to drive one half-bridge circuit in an external power stage. OUTC and OUTD drive the other half-bridge and have the same characteristics as OUTA and OUTB. OUTC is phase shifted with respect to OUTA, and OUTD is phase shifted with respect to OUTB.

NOTE: Changing the phase relationship of OUTC and OUTD with respect to OUTA and OUTB requires other than the nominal 50% duty ratio on OUTC and OUTD during those transients.

Power Ground (PGND)

To keep output switching noise from critical analog circuits, the UCC3895 has two different ground connections. PGND is the ground connection for the high-current output stages. Both GND and PGND must be electrically tied together. Also, since PGND carries high current, board traces must be low impedance.

Inverting Input of the PWM Comparator (RAMP)

This pin receives either the C_T waveform in voltage and average current-mode controls, or the current signal (plus slope compensation) in peak current-mode control.

Voltage Reference (REF)

The 5 V, ± 1.2% reference supplies power to internal circuitry, and can also supply up to 5 mA to external loads. The reference is shut down during undervoltage lockout but is operational during all other disable modes. For best performance, bypass with a 0.1-μF, low-ESR, low-ESL capacitor to GND. Do not use more than 1.0 μF of total capacitance on this pin. To ensure the stability of the internal reference.

Oscillator Timing Resistor (RT)

The oscillator in the UCC3895 operates by charging an external timing capacitor, C_T, with a fixed current programmed by R_T. R_T current is calculated as follows:

$$I_{RT}\ (A) = \frac{3.0\ V}{R_T\ (\Omega)} \tag{4}$$

R_T can range from 40 kΩ to 120 kΩ. Soft-start charging and discharging currents are also programmed by I_{RT} (Refer to Figure 1).

Analog Ground (GND)

This pin is the chip ground for all internal circuits except the output stages.

DETAILED PIN DESCRIPTION (continued)

Soft-Start/Disable (SS/DISB)

This pin combines two independent functions.

Disable Mode: A rapid shutdown of the chip is accomplished by externally forcing SS/DISB below 0.5 V, externally forcing REF below 4 V, or if VDD drops below the undervoltage lockout threshold. In the case of REF being pulled below 4 V or an undervoltage condition, SS/DISB is actively pulled to ground via an internal MOSFET switch.

If an overcurrent fault is sensed (CS = 2.5 V), a *soft-stop* is initiated. In this mode, SS/DISB sinks a constant current of (10 × I_{RT}). The soft-stop continues until SS/DISB falls below 0.5 V. When any of these faults are detected, all outputs are forced to ground immediately.

NOTE: If SS/DISB is forced below 0.5 V, the pin starts to source current equal to I_{RT}. The only time the part switches into low I_{DD} current mode, though, is when the part is in undervoltage lockout.

Soft-start Mode: After a fault or disable condition has passed, VDD is above the start threshold, and/or SS/DISB falls below 0.5 V during a soft-stop, SS/DISB switches to a soft-start mode. The pin then sources current, equal to I_{RT}. A user-selected resistor/capacitor combination on SS/DISB determines the soft start time constant.

NOTE: SS/DISB actively clamps the EAOUT pin voltage to approximately the SS/DISB pin voltage during both soft-start, soft-stop, and disable conditions.

Oscillator Synchronization (SYNC)

This pin is bidirectional (refer to Figure 1). When used as an output, SYNC can be used as a clock, which is the same as the device's internal clock. When used as an input, SYNC overrides the chip's internal oscillator and act as it's clock signal. This bidirectional feature allows synchronization of multiple power supplies. Also, the SYNC signal internally discharge the C_T capacitor and any filter capacitors that are present on the RAMP pin. The internal SYNC circuitry is level sensitive, with an input-low threshold of 1.9 V, and an input-high threshold of 2.1 V. A resistor as small as 3.9 kΩ may be tied between SYNC and GND to reduce the sync pulse width.

Chip Supply (VDD)

This is the input pin to the chip. VDD must be bypassed with a minimum of 1.0 µF low ESR, low ESL capacitor to ground. The addition of a 10-µF low ESR, low ESL between VDD and PGND is recommended.

APPLICATION INFORMATION

Programming DELAB, DELCD and the Adaptive Delay Set

The UCC2895N allows the user to set the delay between switch commands within each leg of the full-bridge power circuit according to equations:

$$t_{DELAY} = \frac{(25 \times 10^{-12}) \times R_{DEL}}{V_{DEL}} + 25\text{ ns} \quad (5)$$

From this equation VDEL is determined in conjunction with the desire to use (or not) the adaptive delay set feature from the following formula:

$$V_{DEL} = \left[0.75 \times \left(V_{CS} - V_{ADS}\right)\right] + 0.5\text{ V} \quad (6)$$

The following diagram illustrates the resistors needed to program the delay periods and the adaptive delay set function.

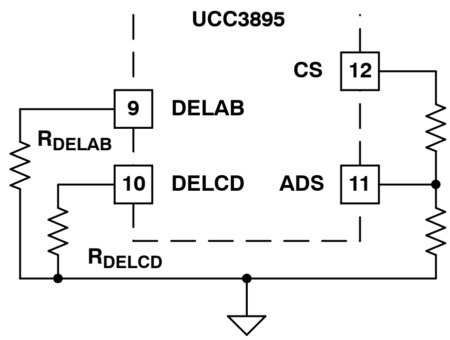


Figure 4. Programming Adaptive Delay Set

The adaptive delay set feature (ADS) allows the user to vary the delay times between switch commands within each of the converter's two legs. The delay-time modulation is implemented by connecting ADS (pin 11) to CS, GND, or a resistive divider from CS through ADS to GND to set V_{ADS} as shown in Figure 4. From equation (6) for V_{DEL}, if ADS is tied to GND then V_{DEL} rises in direct proportion to V_{CS}, causing a decrease in t_{DELAY} as the load increases. In this condition, the maximum value of V_{DEL} is 2 V.

If ADS is connected to a resistive divider between CS and GND, the term (V_{CS}–V_{ADS}) becomes smaller, reducing the level of V_{DEL}. This decreases the amount of delay modulation. In the limit of ADS tied to CS, V_{DEL} = 0.5 V and no delay modulation occurs. Figure 5 graphically shows the delay time vs. load for varying adaptive delay set feature voltages (V_{ADS}).

In the case of maximum delay modulation (ADS=GND), when the circuit goes from light load to heavy load, the variation of V_{DEL} is from 0.5 V to 2 V. This causes the delay times to vary by a 4:1 ratio as the load is changed.

The ability to program an adaptive delay is a desirable feature because the optimum delay time is a function of the current flowing in the primary winding of the transformer, and can change by a factor of 10:1 or more as circuit loading changes. Reference[5] describes the many interrelated factors for choosing the optimum delay times for the most efficient power conversion, and illustrates an external circuit to enable adaptive delay set using the UC3879. Implementing this adaptive feature is simplified in the UCC3895 controller, giving the user the ability to tailor the delay times to suit a particular application with a minimum of external parts.

APPLICATION INFORMATION

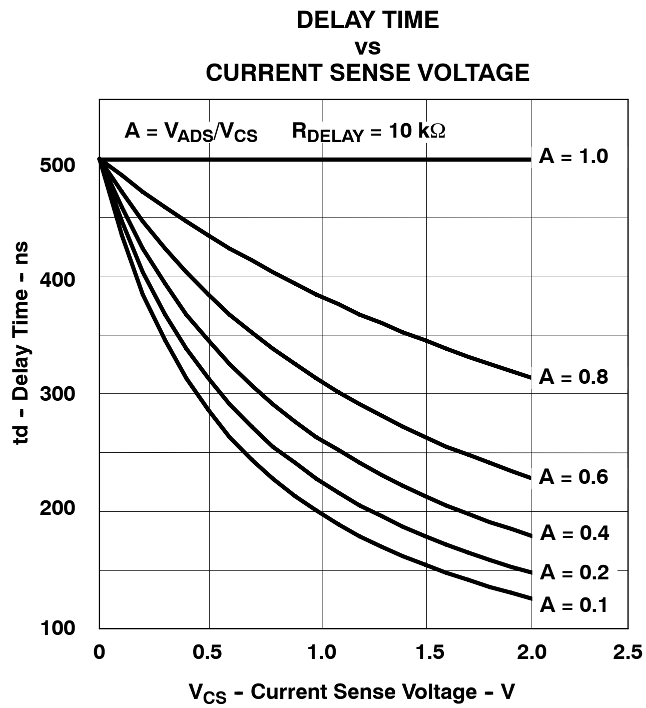


Figure 5. Delay Time Under Varying ADS Voltages

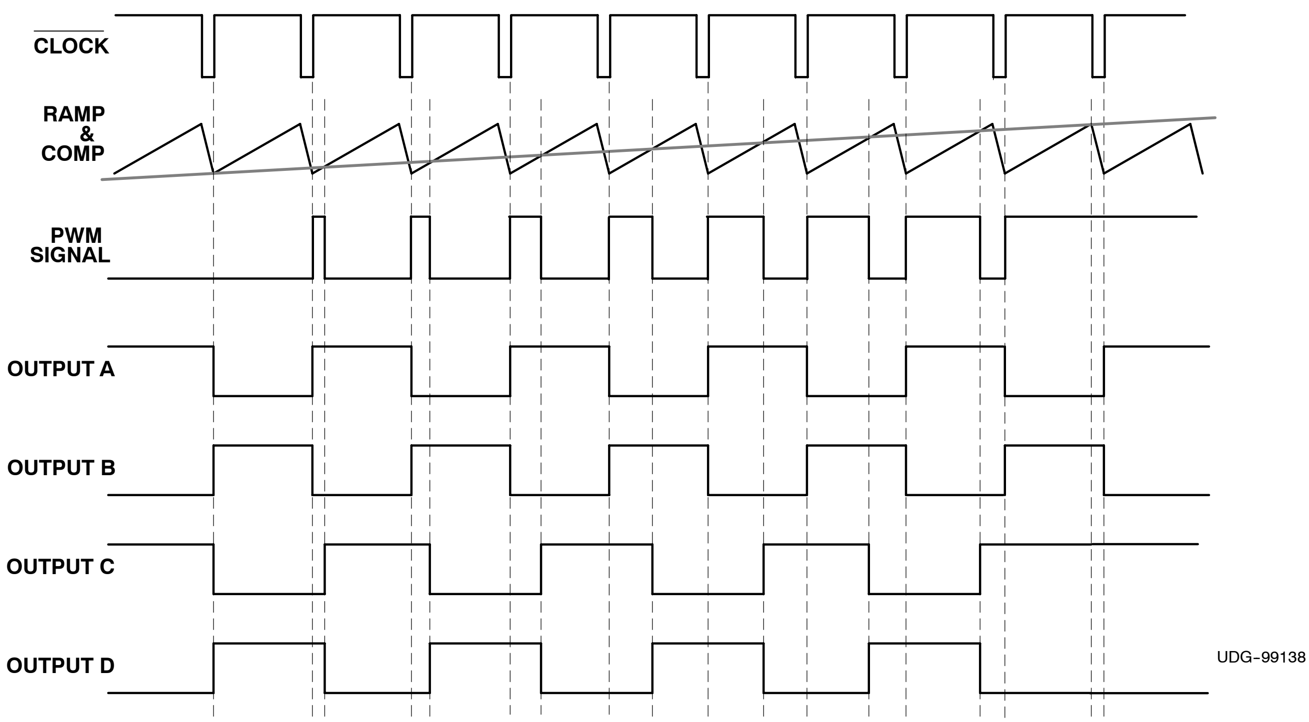


Figure 6. UCC3895 Timing Diagram (No Output Delay Shown, COMP to RAMP offset not included)

TYPICAL CHARACTERISTICS

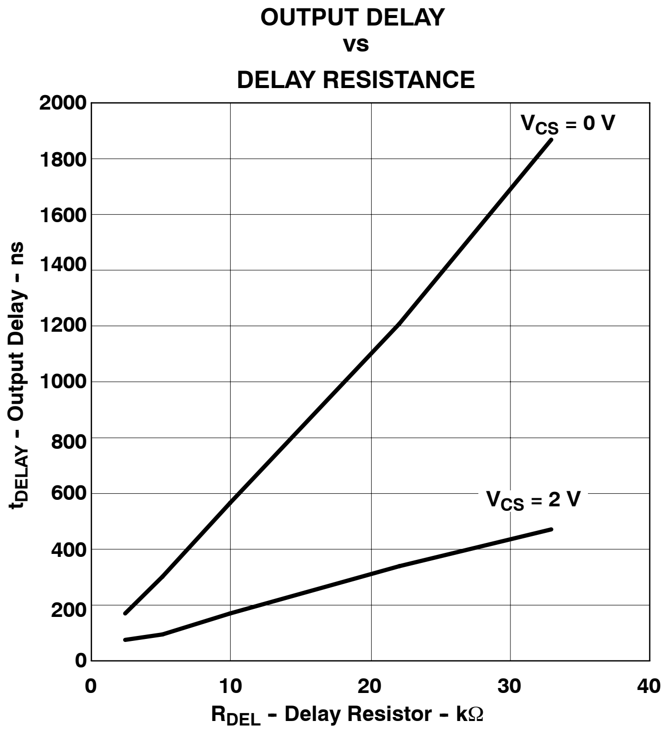


Figure 7

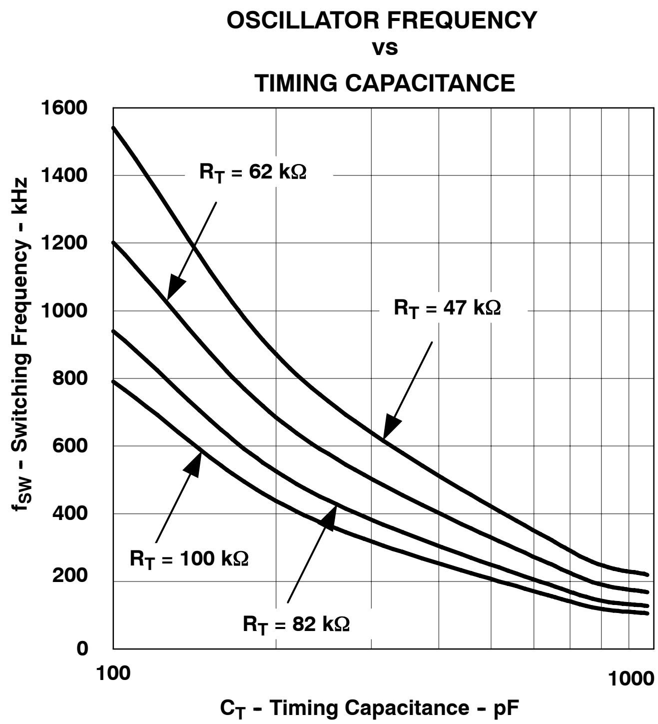


Figure 8

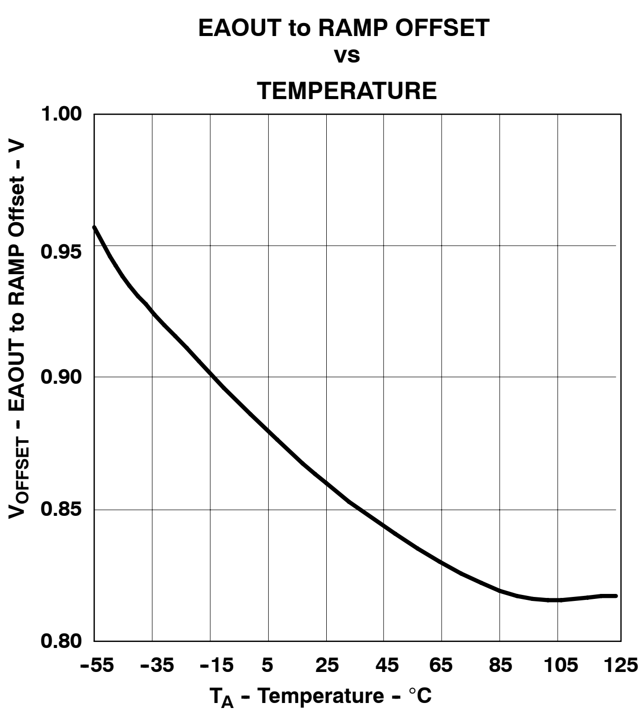


Figure 9

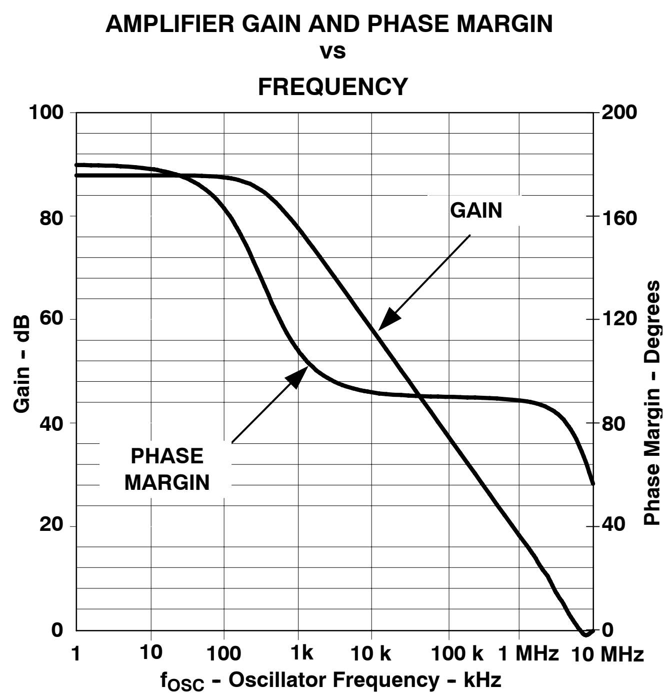


Figure 10

TYPICAL CHARACTERISTICS

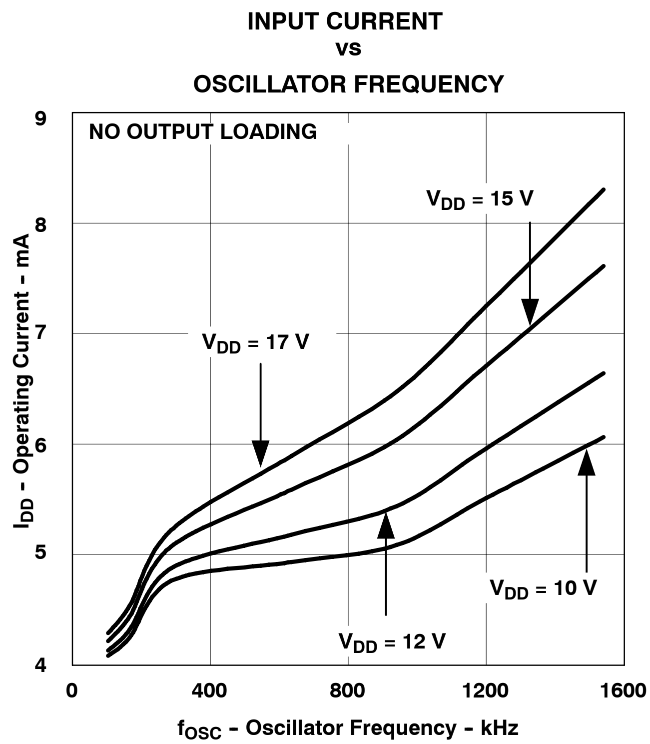


Figure 11

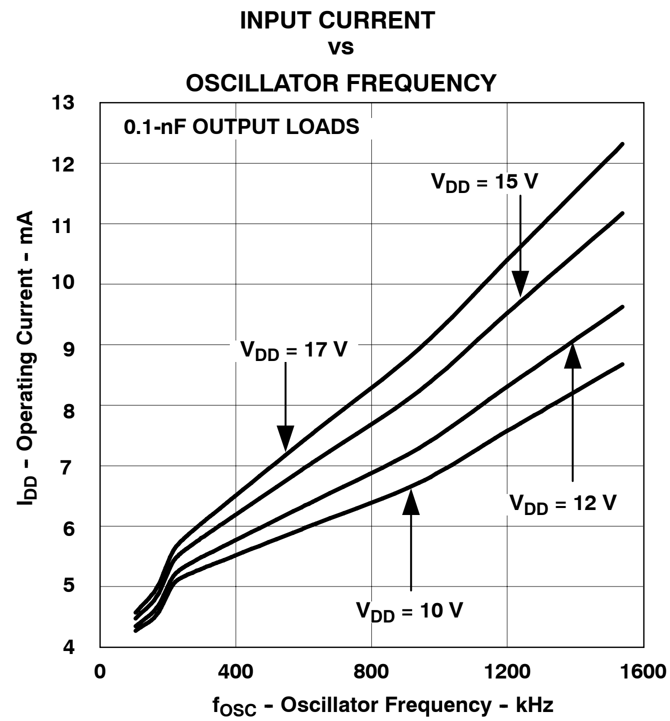


Figure 12

REFERENCES

1. M. Dennis, *A Comparison Between the BiCMOS UCC3895 Phase Shift Controller and the UC3875* Application Note (SLUA246).
2. L. Balogh, *The Current-Doubler Rectifier: An Alternative Rectification Technique for Push-Pull and Bridge Converters* Application Note (SLUA121).
3. W. Andreycak, *Phase Shifted, Zero Voltage Transition Design Considerations*, Application Note (SLUA107).
4. L. Balogh, *The New UC3879 Phase Shifted PWM Controller Simplifies the Design of Zero Voltage Transition Full-Bridge Converters*, Application Note (SLUA122).
5. L. Balogh, *Design Review: 100 W, 400 kHz, dc-to-dc Converter with Current Doubler Synchronous Rectification Achieves 92% Efficiency*, Unitrode Power Supply Design Seminar Manual, SEM-1100, 1996, Topic 2.
6. UC3875 Phase Shift Resonant Controller, Datasheet, (SLUS229).
7. UC3879 Phase Shift Resonant Controller, Datasheet, (SLUS230).
8. UCC3895EVM-1, “Configuring the UCC3895 for direct Control Driven Synchronous Rectification, (Texas Instrument’s Literature Number SLUU109A)
9. UCC3895, CD Output Asymetrical Duty Cycle Operation, (Texas Instrument’s Literature Number SLUA275)
10. Texas Instrument’s Literature Number SLUA323
11. Synchronous Rectifiers of a Current Doubler, (Texas Instrument’s Literature Number SLUA287)

REVISION HISTORY

1. Page 6, changed REF pin description from “Do not use more than 1.0 μF of total capacitance on this pin.” to “Do not use more than 4.7 μF of total capacitance on this pin.”
2. Page 2, added thermal information table.

PACKAGING INFORMATION

Orderable Device	Status [1]	Package Type	Package Drawing	Pins	Package Qty	Eco Plan [2]	Lead/Ball Finish	MSL Peak Temp [3]
UCC1895J	ACTIVE	CDIP	J	20	1	TBD	A42	N / A for Pkg Type
UCC1895L	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type
UCC2895DW	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
UCC2895DWG4	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
UCC2895DWTR	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
UCC2895DWTRG4	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
UCC2895N	ACTIVE	PDIP	N	20	20	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type
UCC2895NG4	ACTIVE	PDIP	N	20	20	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type
UCC2895PW	ACTIVE	TSSOP	PW	20	70	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
UCC2895PWG4	ACTIVE	TSSOP	PW	20	70	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
UCC2895PWTR	ACTIVE	TSSOP	PW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
UCC2895PWTRG4	ACTIVE	TSSOP	PW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
UCC2895Q	ACTIVE	PLCC	FN	20	46	Green (RoHS & no Sb/Br)	CU SN	Level-2-260C-1 YEAR
UCC2895QG3	ACTIVE	PLCC	FN	20	46	Green (RoHS & no Sb/Br)	CU SN	Level-2-260C-1 YEAR
UCC3895DW	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
UCC3895DWG4	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
UCC3895DWTR	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
UCC3895DWTRG4	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
UCC3895N	ACTIVE	PDIP	N	20	20	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type
UCC3895NG4	ACTIVE	PDIP	N	20	20	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type
UCC3895PW	ACTIVE	TSSOP	PW	20	70	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
UCC3895PWG4	ACTIVE	TSSOP	PW	20	70	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
UCC3895PWTR	ACTIVE	TSSOP	PW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
UCC3895PWTRG4	ACTIVE	TSSOP	PW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
UCC3895Q	ACTIVE	PLCC	FN	20	46	Green (RoHS & no Sb/Br)	CU SN	Level-2-260C-1 YEAR
UCC3895QG3	ACTIVE	PLCC	FN	20	46	Green (RoHS &	CU SN	Level-2-260C-1 YEAR

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)
						no Sb/Br)		

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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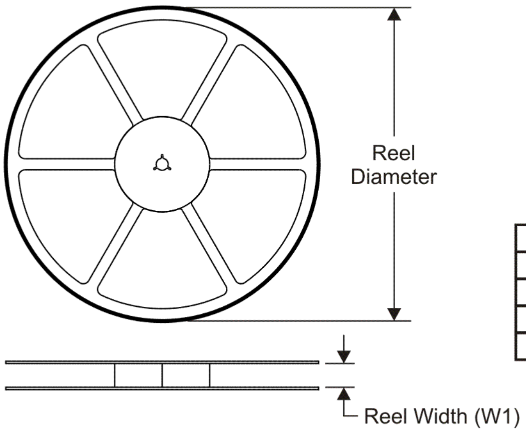
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF UCC1895, UCC2895, UCC3895 :
- Automotive: UCC2895-Q1
- Enhanced Product: UCC2895-EP

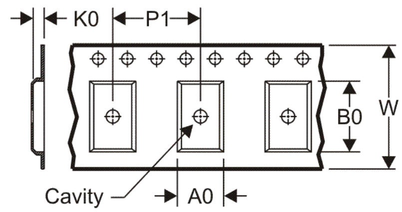
NOTE: Qualified Version Definitions:
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects
- Enhanced Product - Supports Defense, Aerospace and Medical Applications

TAPE AND REEL INFORMATION

REEL DIMENSIONS

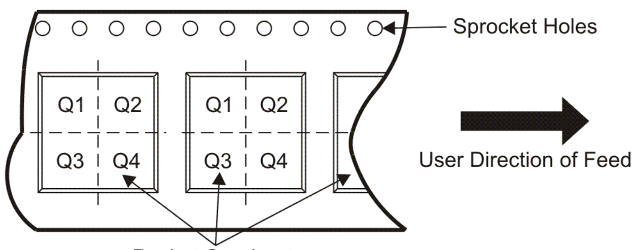


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

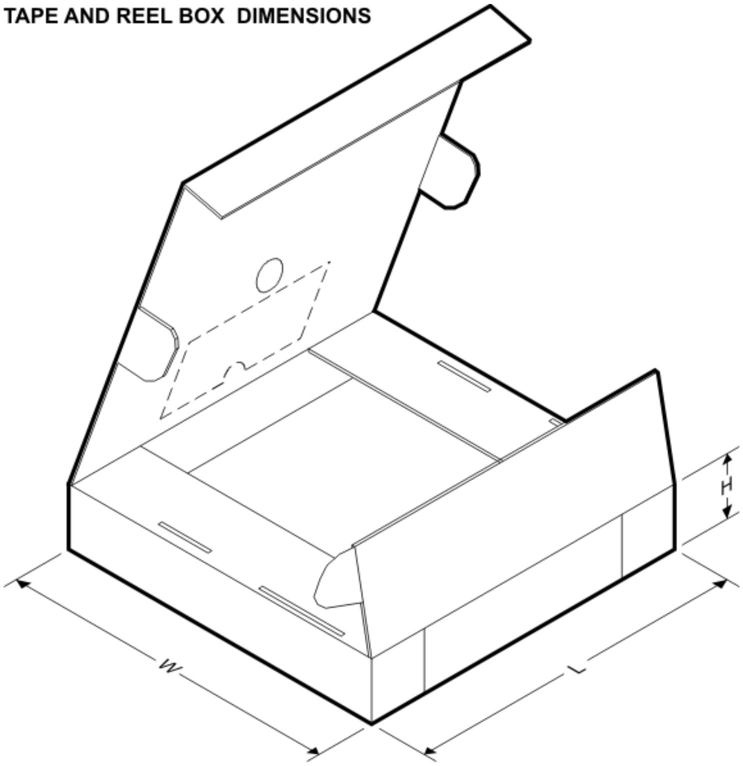
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
UCC2895DWTR	SOIC	DW	20	2000	330.0	24.4	10.8	13.0	2.7	12.0	24.0	Q1
UCC2895PWTR	TSSOP	PW	20	2000	330.0	16.4	6.95	7.1	1.6	8.0	16.0	Q1
UCC3895DWTR	SOIC	DW	20	2000	330.0	24.4	10.8	13.0	2.7	12.0	24.0	Q1
UCC3895PWTR	TSSOP	PW	20	2000	330.0	16.4	6.95	7.1	1.6	8.0	16.0	Q1

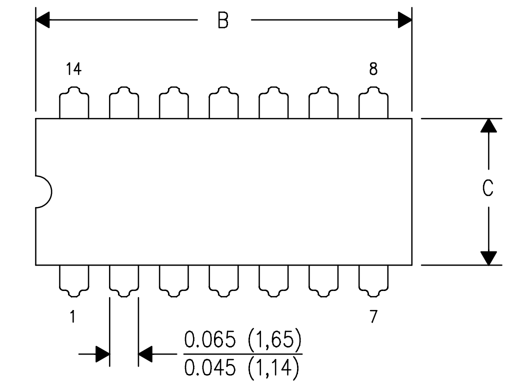
TAPE AND REEL BOX DIMENSIONS



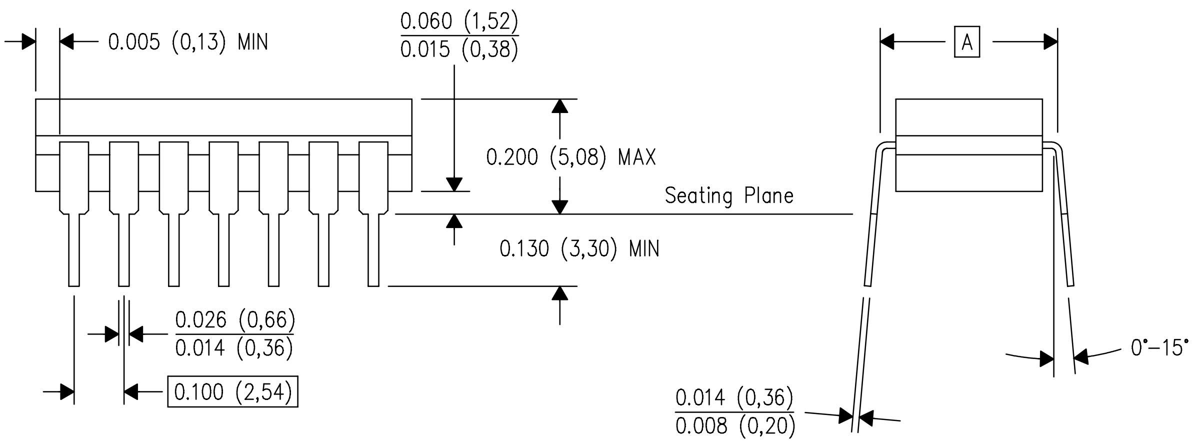
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
UCC2895DWTR	SOIC	DW	20	2000	346.0	346.0	41.0
UCC2895PWTR	TSSOP	PW	20	2000	346.0	346.0	33.0
UCC3895DWTR	SOIC	DW	20	2000	346.0	346.0	41.0
UCC3895PWTR	TSSOP	PW	20	2000	346.0	346.0	33.0

14 LEADS SHOWN



PINS ** / DIM	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)

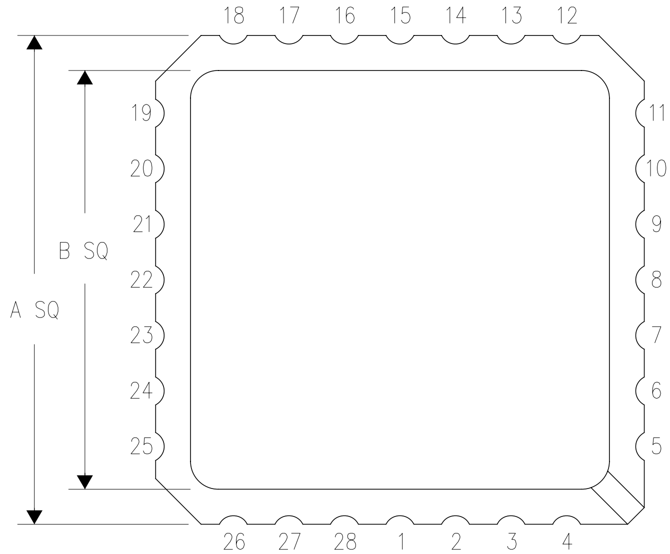


4040083/F 03/03

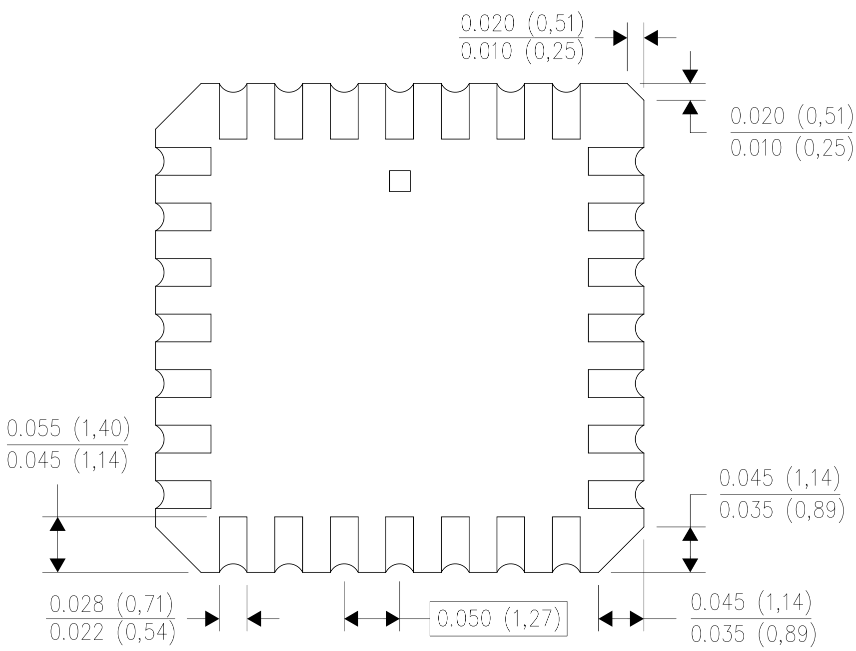
NOTES:
- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. This package is hermetically sealed with a ceramic lid using glass frit.
- D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
- E. Falls within MIL STD 1835 GDIP1–T14, GDIP1–T16, GDIP1–T18 and GDIP1–T20.

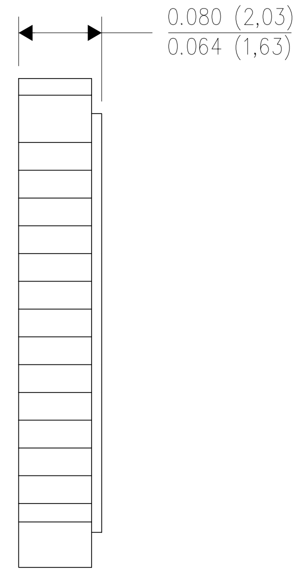
FK (S–CQCC–N**) LEADLESS CERAMIC CHIP CARRIER

28 TERMINAL SHOWN



NO. OF TERMINALS **	A		B	
	MIN	MAX	MIN	MAX
20	0.342 (8,69)	0.358 (9,09)	0.307 (7,80)	0.358 (9,09)
28	0.442 (11,23)	0.458 (11,63)	0.406 (10,31)	0.458 (11,63)
44	0.640 (16,26)	0.660 (16,76)	0.495 (12,58)	0.560 (14,22)
52	0.740 (18,78)	0.761 (19,32)	0.495 (12,58)	0.560 (14,22)
68	0.938 (23,83)	0.962 (24,43)	0.850 (21,6)	0.858 (21,8)
84	1.141 (28,99)	1.165 (29,59)	1.047 (26,6)	1.063 (27,0)

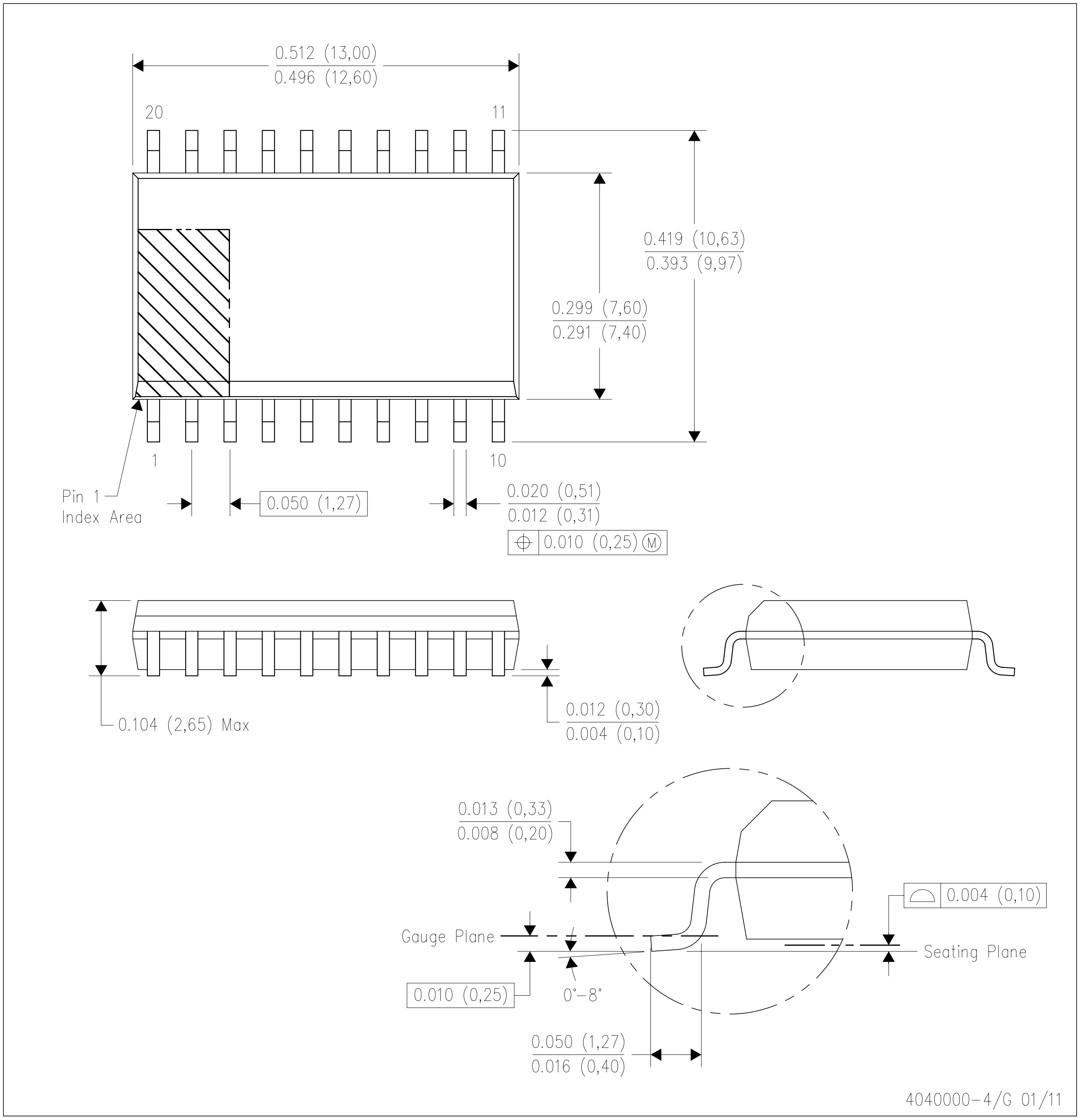




4040140/D 01/11

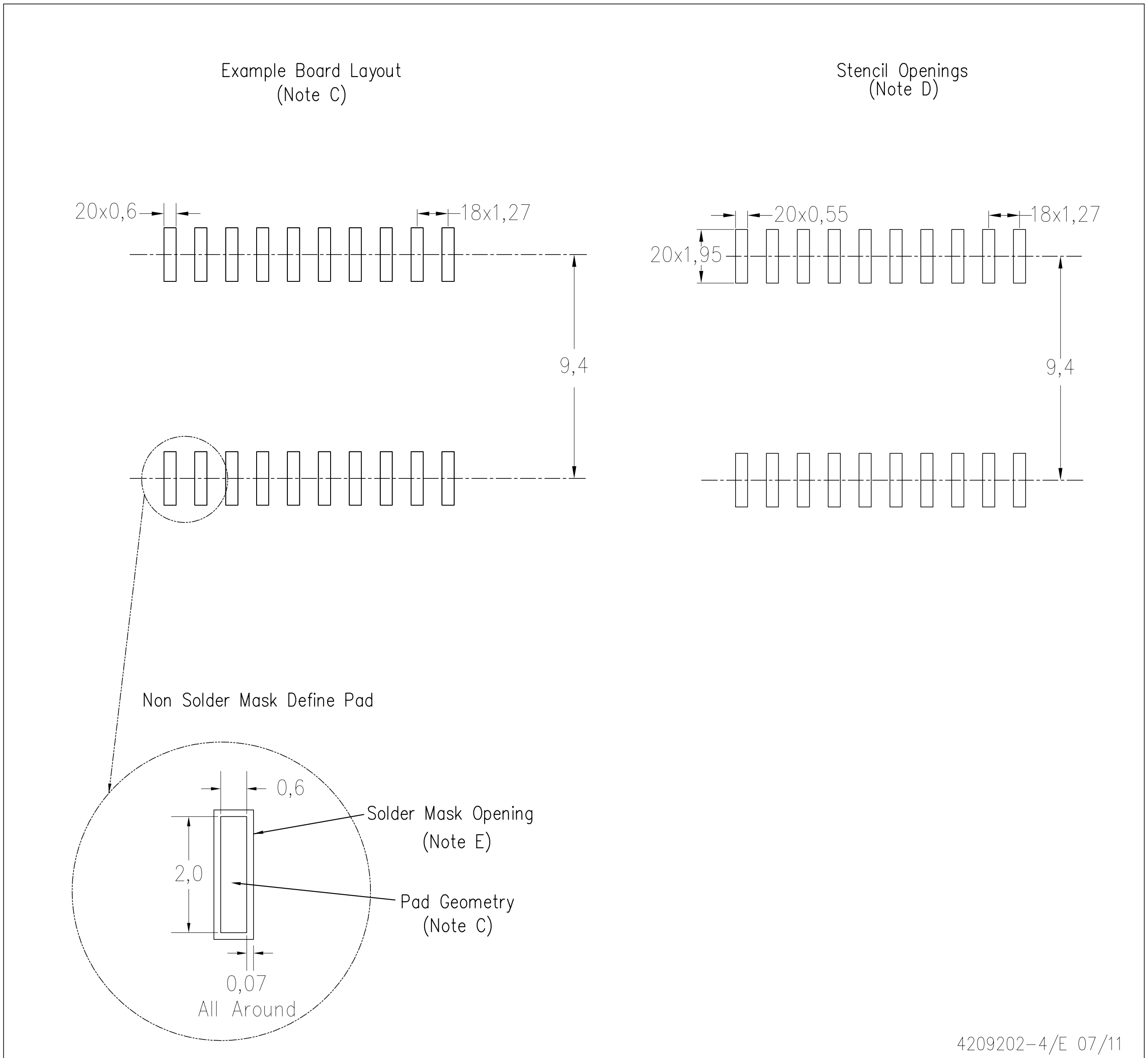
NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package can be hermetically sealed with a metal lid.
D. Falls within JEDEC MS–004

DW (R–PDSO–G20) PLASTIC SMALL OUTLINE



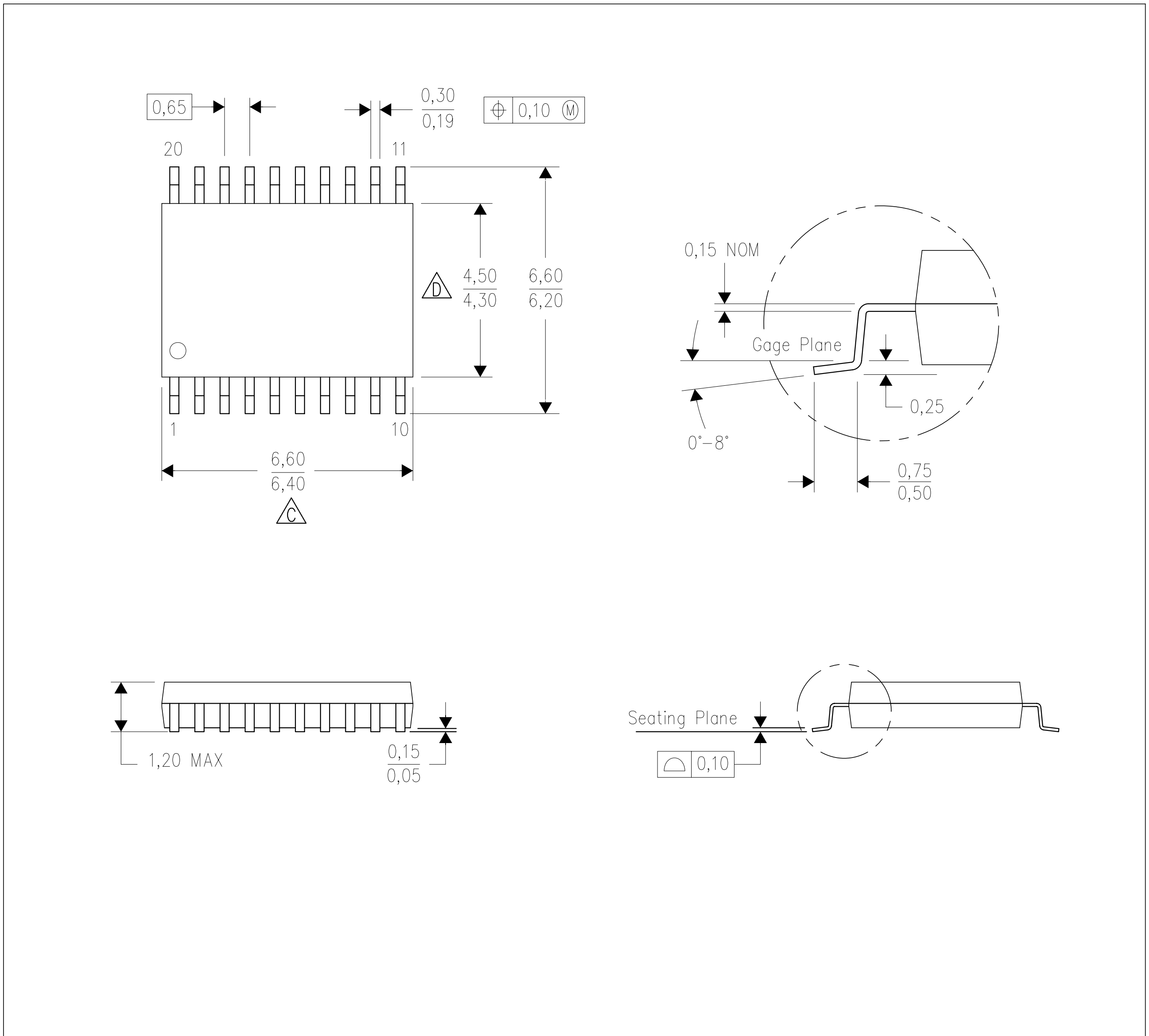
NOTES: A. All linear dimensions are in inches (millimeters). Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
D. Falls within JEDEC MS–013 variation AC.

DW (R–PDSO–G20) PLASTIC SMALL OUTLINE



NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Refer to IPC7351 for alternate board design.
- D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525
- E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

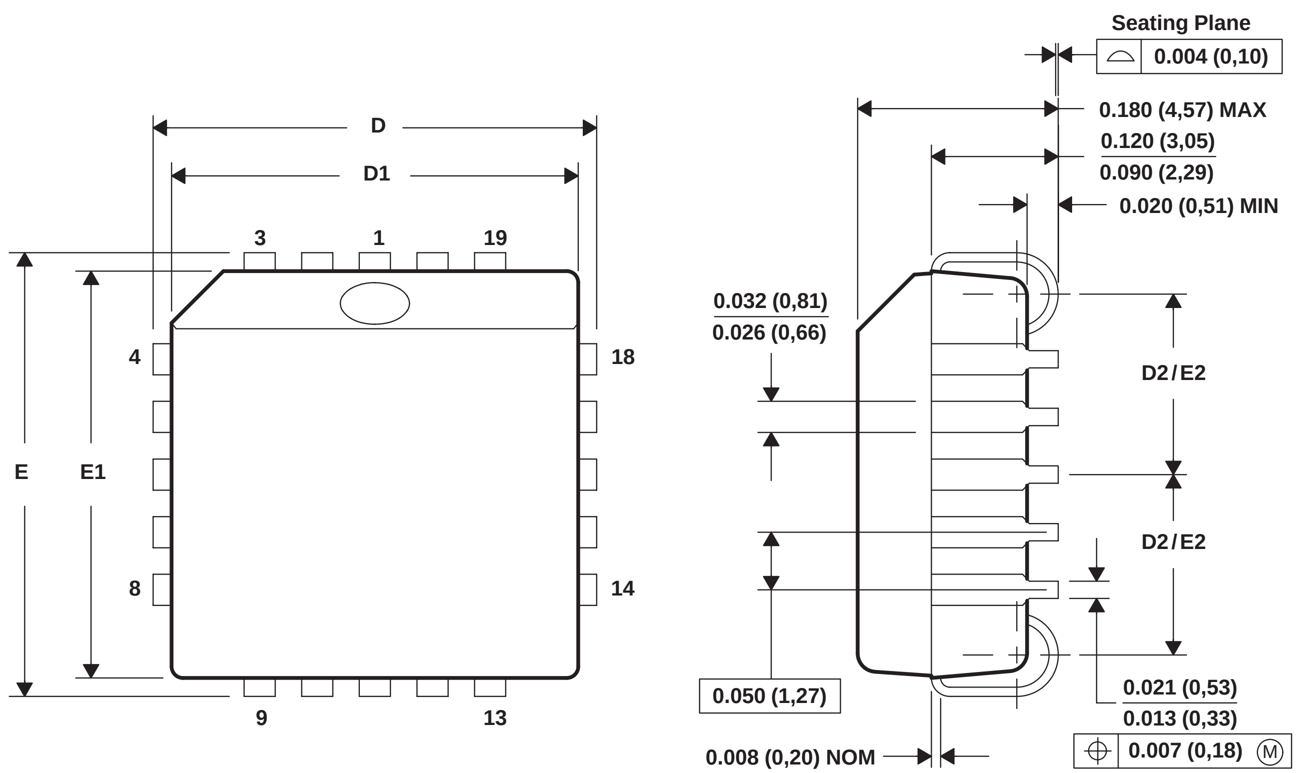
PW (R–PDSO–G20) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
E. Falls within JEDEC MO–153

FN (S-PQCC-J)** **PLASTIC J-LEADED CHIP CARRIER**

20 PIN SHOWN



NO. OF PINS **	D / E		D1 / E1		D2 / E2	
	MIN	MAX	MIN	MAX	MIN	MAX
20	0.385 (9,78)	0.395 (10,03)	0.350 (8,89)	0.356 (9,04)	0.141 (3,58)	0.169 (4,29)
28	0.485 (12,32)	0.495 (12,57)	0.450 (11,43)	0.456 (11,58)	0.191 (4,85)	0.219 (5,56)
44	0.685 (17,40)	0.695 (17,65)	0.650 (16,51)	0.656 (16,66)	0.291 (7,39)	0.319 (8,10)
52	0.785 (19,94)	0.795 (20,19)	0.750 (19,05)	0.756 (19,20)	0.341 (8,66)	0.369 (9,37)
68	0.985 (25,02)	0.995 (25,27)	0.950 (24,13)	0.958 (24,33)	0.441 (11,20)	0.469 (11,91)
84	1.185 (30,10)	1.195 (30,35)	1.150 (29,21)	1.158 (29,41)	0.541 (13,74)	0.569 (14,45)

4040005 / B 03/95

NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS-018