8-Pin High-Performance Resonant Mode Controller

FEATURES

- **Variable Switching Frequency Control**
- **Programmable Minimum Switching Frequency With 4% Accuracy (3% accuracy at temperature range: -20°C to 105°C)**
- **Programmable Maximum Switching Frequency**
- **Programmable Dead Time for Best Efficiency**
- **Programmable Soft-Start Time**
- **Easy ON/OFF Control**
- **Over-Current Protection**
- **Over-Temperature Protection**
- **Bias Voltage UVLO and OVP**
- **Integrated Gate Driver With 0.4-A Source and 0.8-A Sink Capability**
- **Operating Temperature Range: –40°C to 125°C**
- **SOIC 8-Pin Package**

APPLICATIONS

- **100-W to 1-kW Power Supplies**
- **LCD, Plasma and DLP TVs**
- **Adaptors, Computing and ATX Power Supplies**
- **Home Audio Systems**
- **Electronic Lighting Ballasts**

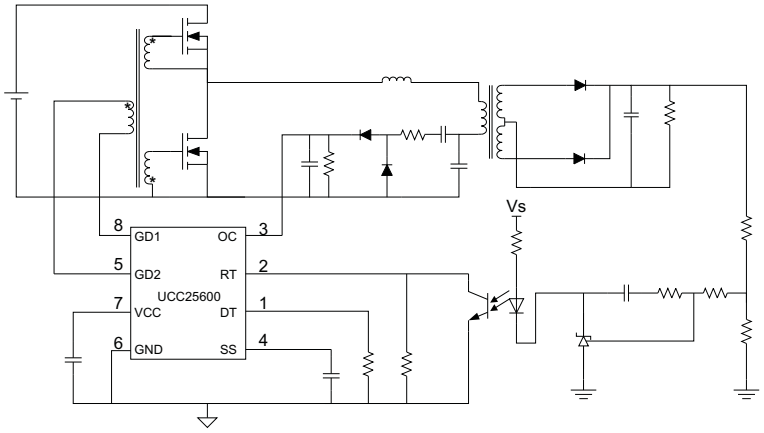
DESCRIPTION

The UCC25600 high performance resonant mode controller is designed for dc-to-dc applications utilizing resonant topologies, especially the LLC half bridge resonant converter. This highly integrated controller implements frequency modulation control and complete system functions in only an 8-pin package. Switching to the UCC25600 will greatly simplify the system design, layout and improve time to market, all at a price point lower than competitive 16-pin device offerings.

The internal oscillator supports the switching frequencies from 30 kHz to 350 kHz. This high accuracy oscillator realizes the minimum switching frequency limiting with 4% tolerance, allowing the designer to avoid "over design" of the power stage and, thus, further reducing overall system cost. The programmable dead time enables zero-voltage switching with minimum magnetizing current. This will maximize system efficiency across a variety of applications. The programmable soft-start timer maximizes design flexibility demanded by the varied requirements of end equipments utilizing a half bridge topology. By incorporating 0.4-A source and 0.8-A sink driving capability, a low cost, reliable gate driver transformer is a real option.

The UCC25600 delivers complete system protection functions including over current, UVLO, bias supply OVP and over temperature protection.

TYPICAL APPLICATION DIAGRAM



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ORDERING INFORMATION

PART NUMBER	PACKAGE	OPERATING TEMPERATURE
UCC25600D	8-Pin SOIC	-40°C to 125°C

ABSOLUTE MAXIMUM RATINGS(1)(2)(3)(4)

over operating free-air temperature range (unless otherwise noted)

PARAMETER	LIMIT	UNIT
Supply voltage, VCC	22	V
Voltage, GD1, GD2	-0.5 to VCC + 0.5	
Gate drive current – continuous, GD1, GD2	+/- 25	mA
Current, RT	-5	
Current, DT	-0.7	
Operating junction temperature, T_J	−40 to 125	°C
Storage temperature, T_{STG}	−65 to 150	
Lead temperature (10 seconds)	260	

(1) These are stress limits. Stress beyond these limits may cause permanent damage to the device. Functional operation of the device at these or any conditions beyond those indicated under RECOMMENDED OPERATING CONDITIONS is not implied. Exposure to absolute maximum rated conditions for extended periods of time may affect device reliability.
(2) All voltages are with respect to GND.
(3) All currents are positive into the terminal, negative out of the terminal.
(4) In normal use, terminals GD1 and GD2 are connected to an external gate driver and are internally limited in output current.

ELECTROSTATIC DISCHARGE (ESD) PROTECTION

PARAMETER	RATING	UNIT
Human Body Model (HBM)	2,000	V
Charged Device Model (CDM)	500	

DISSIPATION RATINGS

PACKAGE	THERMAL IMPEDANCE, JUNCTION-TO-AMBIENT	T_A = 25°C POWER RATING	T_A = 85°C POWER RATING
8-Pin SOIC	150°C/watt (1)(2)	667 mW (1)	267 mW (1)

(1) Thermal resistance is a strong function of board construction and layout. Air flow will reduce thermal resistance. This number is only a general guide.
(2) Thermal resistance calculated with a low-K methodology.

RECOMMENDED OPERATING CONDITIONS

over operating free-air temperature range (unless otherwise noted)

PARAMETER	MINIMUM	MAXIMUM	UNIT
VCC input voltage from a low-impedance source	11.5	18.0	V
RT resistance	1	8.666	kΩ
DT resistance	3.3	39	
SS capacitor	0.01	1	µF

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ELECTRICAL CHARACTERISTICS

over operating free-air temperature range, −40°C < T_A < 125°C, T_J = T_A, VCC = 12 V, GND = 0 V, R_{RT} = 4.7 kΩ, R_{DT} = 16.9 kΩ, C_{VCC} = 1 µF, (unless otherwise noted)

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Bias Supply (VCC)						
	VCC current, disabled	SS = 0 V		1	1.5	mA
	VCC current, enabled	SS = 5 V, C_{GD1} = C_{GD2} = 1 nF	2.5	5	7.5	
	VCC current, UVLO	VCC = 9 V		100	400	µA
V_{UVLO}	UVLO turn-on threshold	Measured at VCC rising	9.9	10.5	11.1	V
	UVLO turn-off threshold	Measured at VCC falling	8.9	9.5	10.1	
	UVLO hysteresis	Measured at VCC	0.7	1	1.3	
V_{OVP}	OVP turn-off threshold	Measured at VCC rising	18	20	22	
	OVP turn-on threshold	Measured at VCC falling	16	18	20	
	OVP hysteresis	Measured at VCC	1.5	2	2.5	
Dead Time (DT)						
T_{DT}	Dead time	R_{DT} = 16.9 kΩ	390	420	450	ns
Oscillator						
$F_{SW(min)}$	Minimum switching frequency at GD1, GD2	-40°C to 125°C	40.04	41.70	43.36	kHz
		-20°C to 105°C	40.45	41.70	42.95	
K_{ICO}	Switching frequency gain/I (RT)	R_{RT} = 4.7 kΩ, I_{RT} = 0 to 1 mA	60	80	100	Hz/µA
	GD1, GD2 on time mismatching		-50		50	ns
F_{SW_BM}	Switching frequency starting burst mode	SS = 5 V	300	350	400	kHz
	Switching frequency to come out of burst mode	SS = 5 V	280	330	380	
$F_{SW(start)}$	Switching frequency at soft start	-40°C to 125°C	122	142.5	162	
		-20°C to 105°C	125	142.5	160	
External Disable/Soft Start						
	Enable threshold	Measure at SS rising	1.1	1.2	1.3	V
	Disable threshold	Measured at SS falling	0.85	1	1.1	
	Disable hysteresis	Measured at SS	0.15		0.35	
	Disable prop. delay	Measured between SS (falling) and GD2 (falling)	250	500	750	ns
I_{SS}	Source current on ISS pin	V_{SS} = 0.5 V	-225	-175	-125	µA
	Source current on ISS pin	V_{SS} = 1.35 V	-5.5	-5	-4.5	

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ELECTRICAL CHARACTERISTICS (continued)

over operating free-air temperature range, −40°C < T_A < 125°C, T_J = T_A, VCC = 12 V, GND = 0 V, R_{RT} = 4.7 kΩ, R_{DT} = 16.9 kΩ, C_{VCC} = 1 µF, (unless otherwise noted)

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Peak Current Limit						
$V_{OC1(off)}$	Level 1 over current threshold – V_{OC} rising		0.9	1	1.1	V
$V_{OC2(off)}$	Level 2 over current latch threshold – V_{OC} rising		1.8	2.0	2.2	
$V_{OC1(on)}$	Level 1 over current threshold – V_{OC} falling		0.5	0.6	0.7	
T_{d_OC}	Propagation delay		60	200	500	ns
I_{OC}	OC bias current	V_{OC} = 0.8 V	-200		200	nA
Gate Drive						
	GD1, GD2 output voltage high	I_{GD1}, I_{GD2} = −20 mA	9		11	V
	GD1, GD2 on resistance high	I_{GD1}, I_{GD2} = −20 mA		12	30	Ω
	GD1, GD2 output voltage low	I_{GD1}, I_{GD2} = 20 mA		0.08	0.2	V
	GD1, GD2 on resistance low	I_{GD1}, I_{GD2} = 20 mA		4	10	Ω
	Rise time GDx	1 V to 9 V, C_{LOAD} = 1 nF		18	35	ns
	Fall time GDx	9 V to 1 V, C_{LOAD} = 1 nF		12	25	
	GD1, GD2 output voltage during UVLO	VCC = 6 V, I_{GD1}, I_{GD2} = 1.2 mA	0.5		1.75	V
Thermal Shutdown						
	Thermal shutdown threshold			160		°C
	Thermal shutdown recovery threshold			140		

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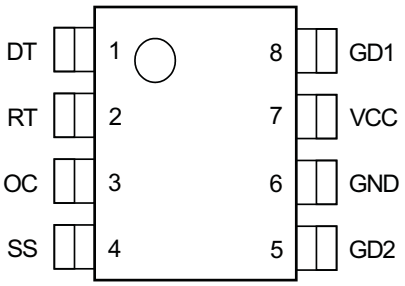
DEVICE INFORMATION

8-Pin SOIC, Top View



TERMINAL FUNCTIONS

TERMINAL			DESCRIPTION
NAME	NO.	I/O	
DT	1	I	This pin sets the dead time of high-side and low-side switch driving signals. Connect a resistor to ground. With internal 2.25-V voltage reference, the current flowing through the resistor sets the dead time. To prevent shoot through when this pin is accidentally short to ground, the minimum dead time is set to 120 ns. Any dead time setting less than 120 ns will automatically have 120-ns dead time.
RT	2	I	The current flowing out of this pin sets the frequency of the gate driver signals. Connect the opto-coupler collector to this pin to control the switching frequency for regulation purpose. Parallel a resistor to ground to set the minimum current flowing out of the pin and set the minimum switching frequency. To set the maximum switching frequency limiting, simply series a resistor with the opto-coupler transistor. This resistor sets the maximum current flowing out of the pin and limits the maximum switching frequency.
OC	3	I	Over-current protection pin. When the voltage on this pin is above 1 V, gate driver signals are actively pulled low. After the voltage falls below 0.6 V, the gate driver signal recovers with soft start. When OC pin voltage is above 2 V, the device is latched off. Bringing VCC below UVLO level resets the overcurrent latch off.
SS	4	I	Soft-start pin. This pin sets the soft-start time of the system. Connect a capacitor to ground. Pulling this pin below 1 V will disable the device to allow easy ON/OFF control. The soft-start function is enabled after all fault conditions, including bias supply OV, UVLO, over-current protection and over-temperature protection.
GD1	8	O	High-side and low-side switch gate driver. Connect gate driver transformer primary side to these two pins to drive the half bridge.
GD2	5	O	
GND	6	-	Ground.
VCC	7	-	Bias Supply. Connect this pin to a power supply less than 20 V. Parallel a 1-µF capacitor to ground to filter out noise.

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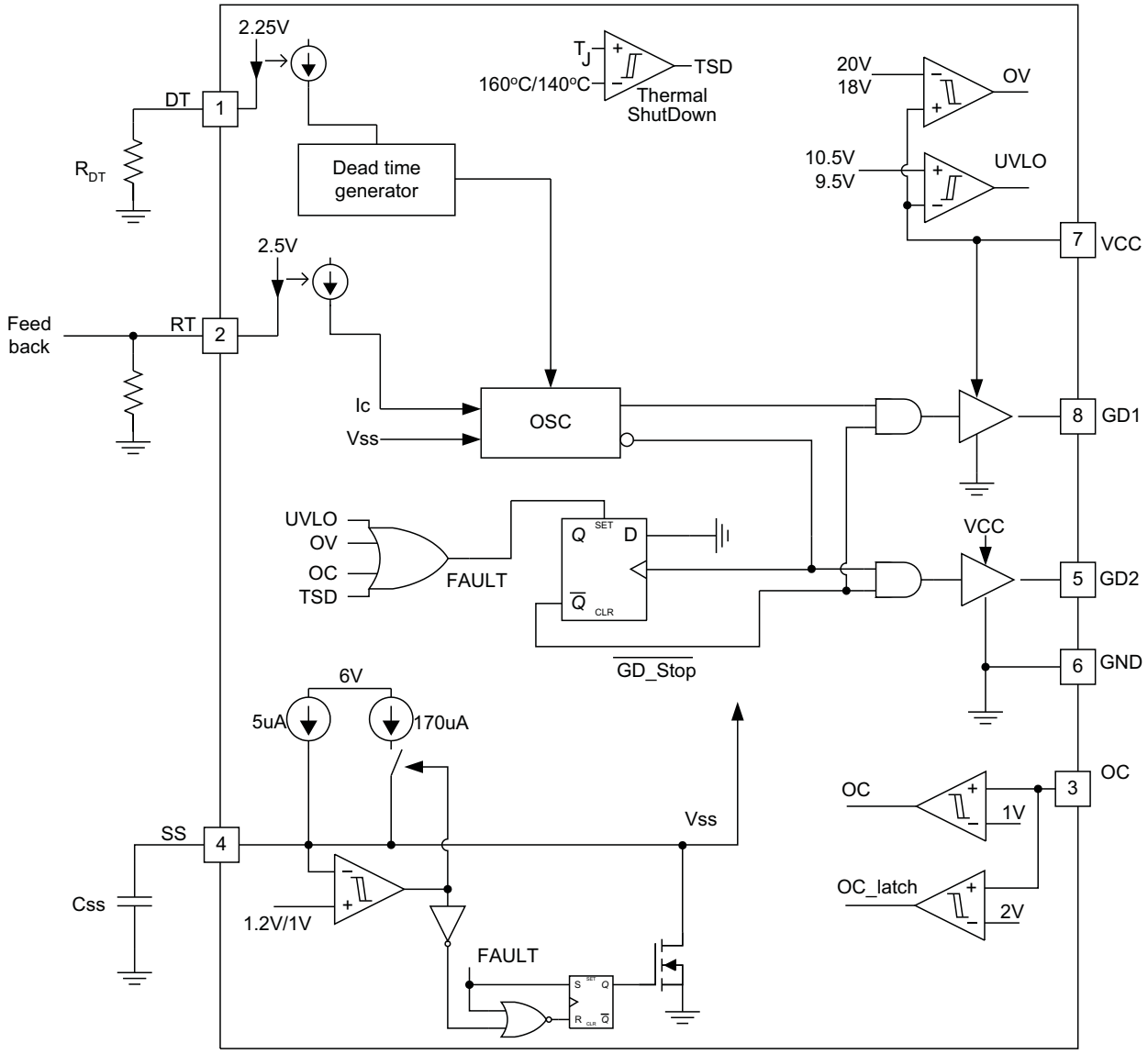
Block Diagram



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TYPICAL CHARACTERISTICS

At V_{CC} = 12 V, R_{RT} = 4.7 kΩ, R_{DT} = 16.9 kΩ, V_{SS} = 5 V, V_{OC} = 0 V; all voltages are with respect to GND, T_J = T_A = 25°C, unless otherwise noted.

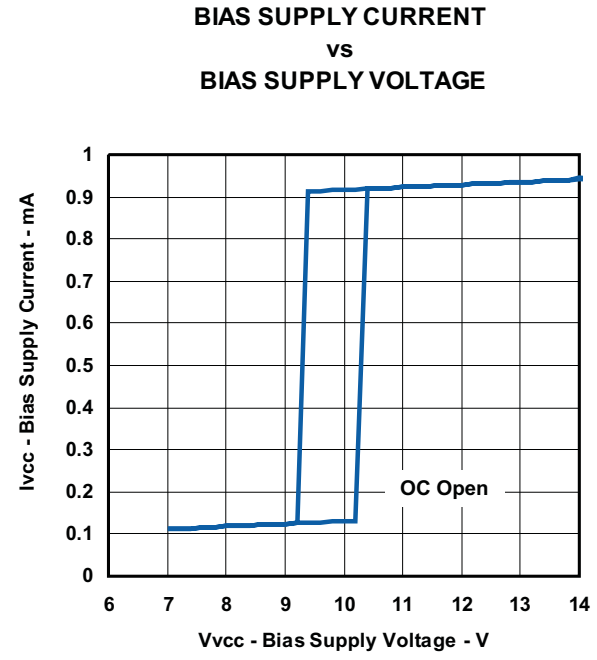

Figure 1.

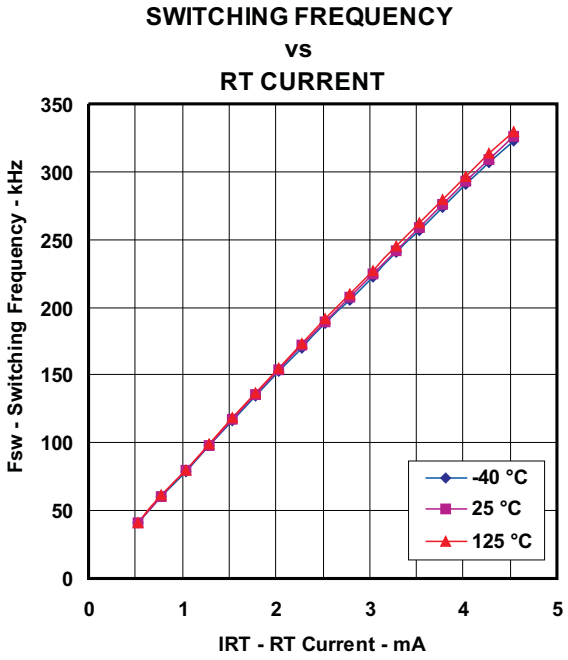

Figure 2.

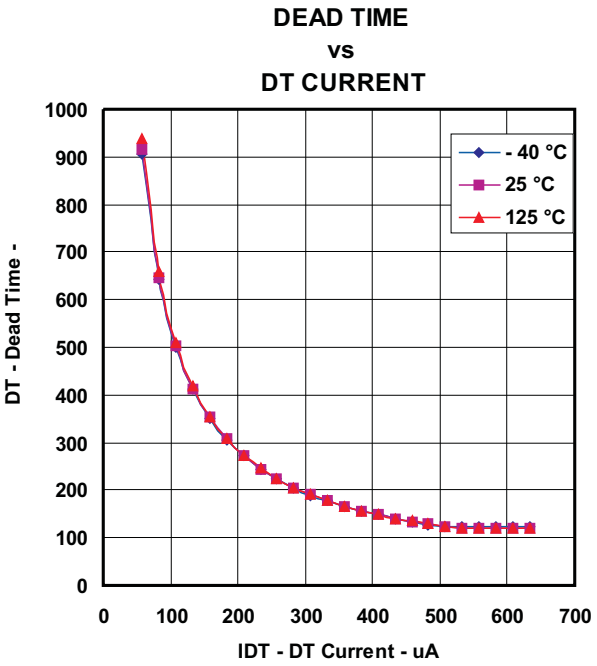

Figure 3.

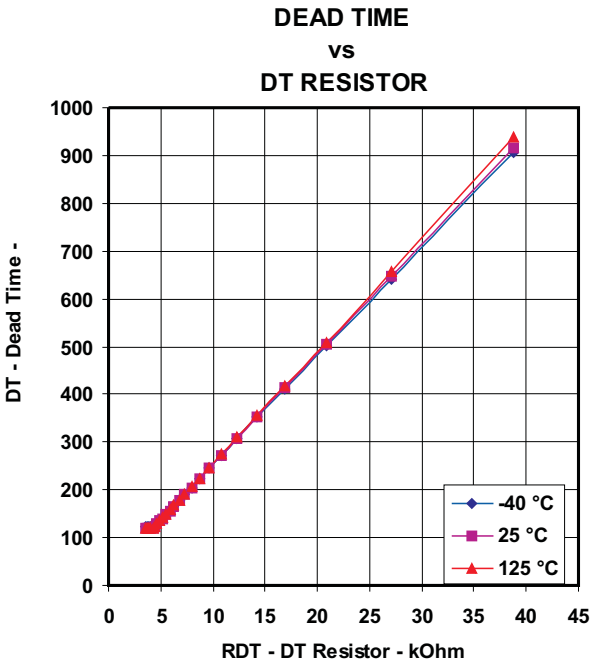

Figure 4.

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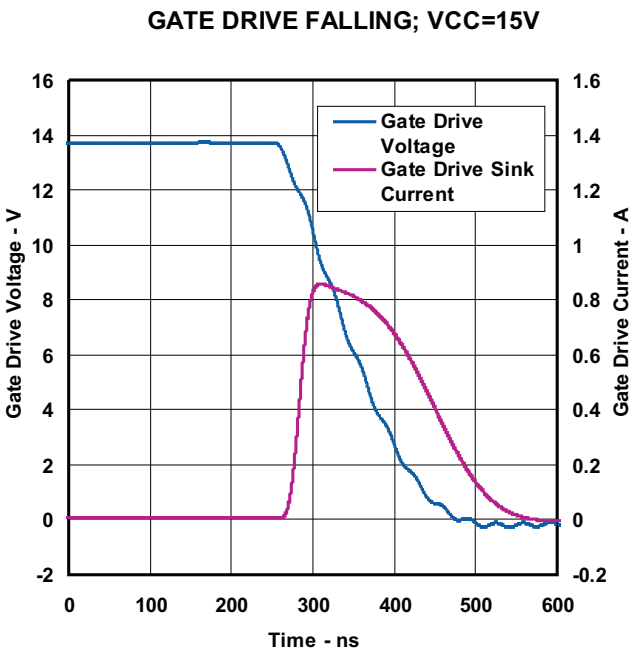
TYPICAL CHARACTERISTICS (continued)



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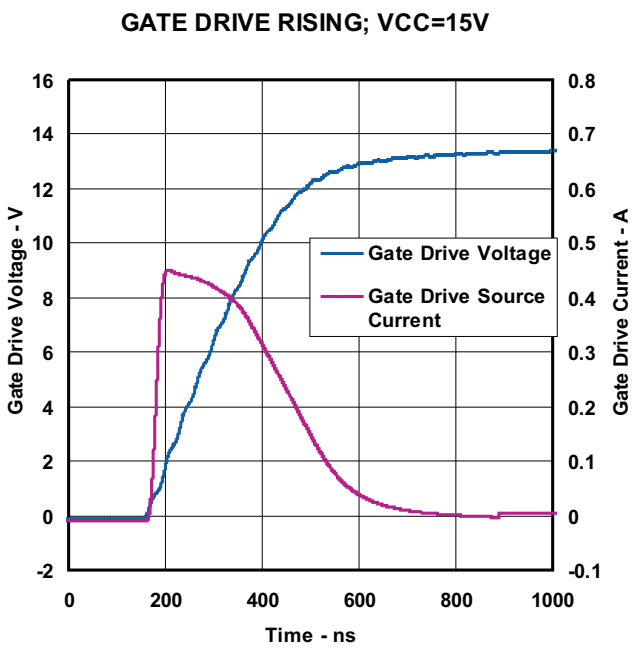

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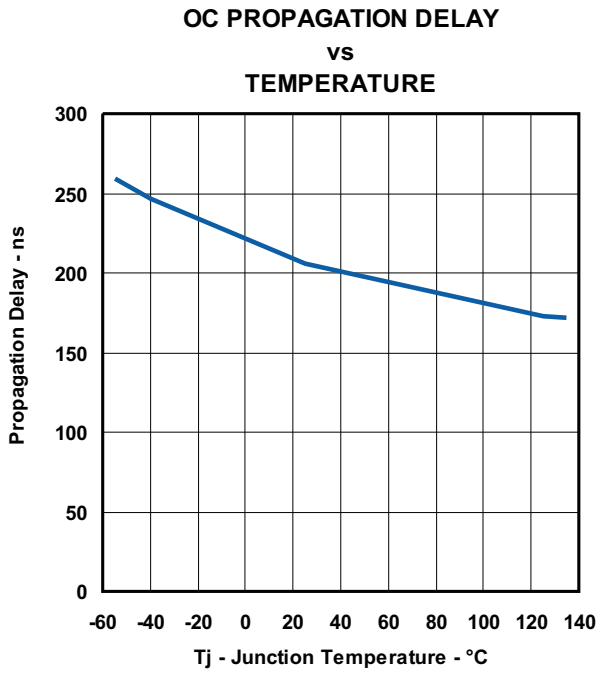

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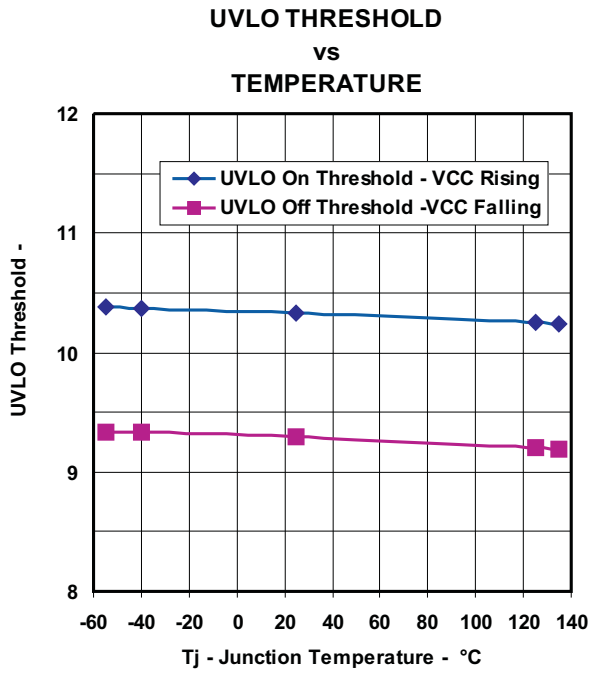

Figure 8.

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TYPICAL CHARACTERISTICS (continued)

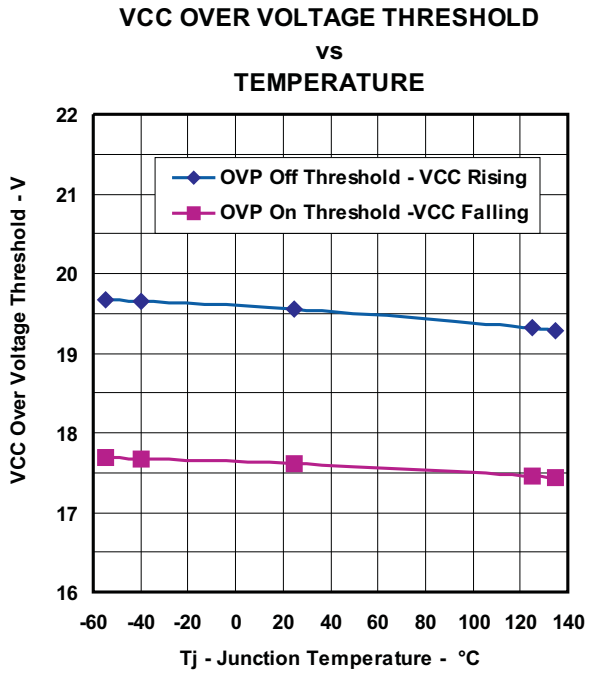

Figure 9.

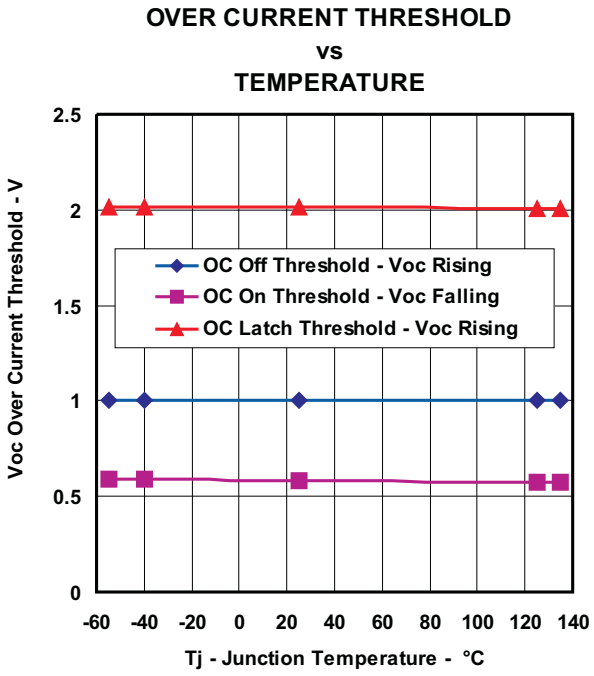

Figure 10.

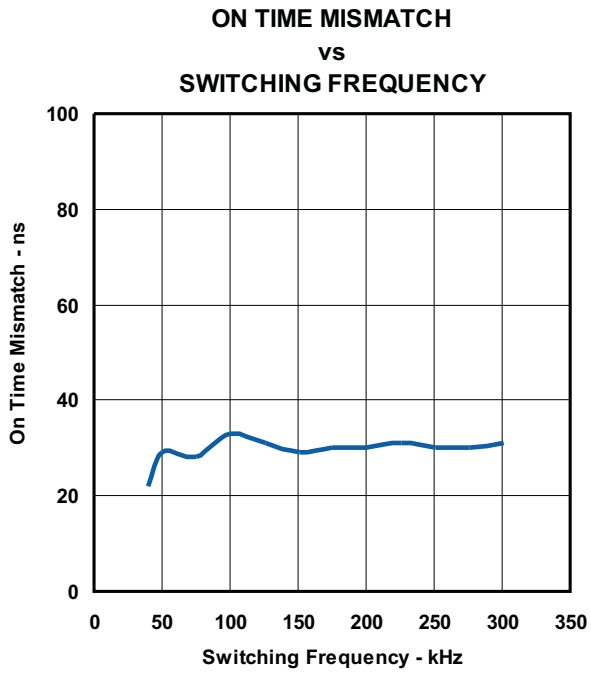

Figure 11.

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APPLICATION INFORMATION

Principal of Operation

The soft-switching capability, high efficiency and long holdup time make the LLC resonant converter attractive for many applications, such as digital TV, ac/dc adapters and computer power supplies. Figure 12 shows the schematic of the LLC resonant converter.

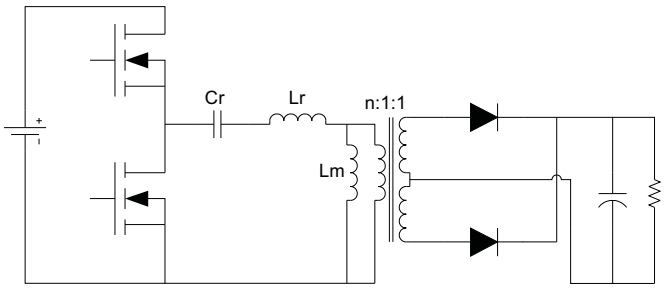

Figure 12. LLC Resonant Converter

The LLC resonant converter is based on the Series Resonant Converter (SRC). By utilizing the transformer magnetizing inductor, zero-voltage switching can be achieved over a wide range of input voltage and load. As a result of multiple resonances, zero-voltage switching can be maintained even when the switching frequency is higher or lower than resonant frequency. This simplifies the converter design to avoid the zero-current switching region, which can lead to system damage. The converter achieves the best efficiency when operated close to its resonant frequency at a nominal input voltage. As the switching frequency is lowered the voltage gain is significantly increased. This allows the converter to maintain regulation when the input voltage falls low. These features make the converter ideally suited to operate from the output of a high-voltage boost PFC pre-regulator, allowing it to hold up through brief periods of ac line-voltage dropout.

Due to the nature of resonant converter, all the voltages and currents on the resonant components are approximately sinusoidal. The gain characteristic of LLC resonant converter is analyzed based on the First Harmonic Approximation (FHA), which means all the voltages and currents are treated as sinusoidal shape with the frequency same as switching frequency.

According to the operation principle of the converter, the LLC resonant converter can be draw as the equivalent circuit as shown in Figure 13.

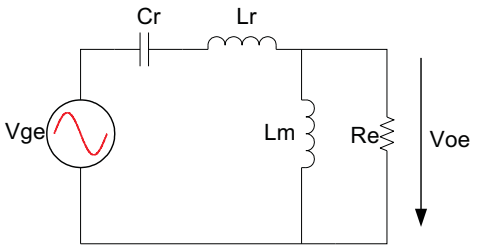

Figure 13. LLC Resonant Converter Equivalent Circuit

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In this equivalent circuit, the V_{ge} and V_{oe} are the fundamental harmonics of the voltage generated by the half bridge and the voltage on the transformer primary side, respectively. These voltages can be calculated through Fourier analysis. The load resistor R_e is the equivalent resistor of the load, and it can be calculated as:

$$R_e = \frac{8}{\pi^2} n^2 R \tag{1}$$

Based on this equivalent circuit, the converter gain at different switching frequencies can be calculated as:

$$\frac{V_o}{V_{DC}/2} = \left| \frac{\frac{j\omega L_m R_e}{j\omega L_m + R_e}}{\frac{j\omega L_m R_e}{j\omega L_m + R_e} + \frac{1}{j\omega C_r} + j\omega L_r} \right| \tag{2}$$

In this equation $V_{DC}/2$ is the equivalent input voltage due to the half bridge structure.

Table 1. Circuit Definition Calculations

NORMALIZED GAIN	RESONANT FREQUENCY	QUALITY FACTOR	NORMALIZED FREQUENCY	INDUCTOR RATIO
$M = \frac{V_o}{V_{DC}/2}$	$f_0 = \frac{1}{2\pi\sqrt{L_r C_r}}$	$Q_e = \frac{\sqrt{L_r / C_r}}{R_e}$	$f_n = \frac{f}{f_0}$	$L_n = \frac{L_m}{L_r}$

Following the definitions in Table 1, the converter gain at different switching frequencies can be written as:

$$M = \left| \frac{L_n f_n^2}{L_n f_n^2 + (f_n - 1)(f_n + 1 + j f_n L_n Q_e)} \right| \tag{3}$$

Because of the FHA, this gain equation is an approximation. When the switching frequency moves away from the resonant frequency, the error becomes larger. However, this equation can be used as the design tool. The final results need to be verified by the time based simulation or hardware test.

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From Equation 3, when switching frequency is equal to resonant frequency, f_n = 1 and converter voltage gain is equal to 1. Converter gain at different loads and inductor ratio conditions are shown in Figure 14 through Figure 17.

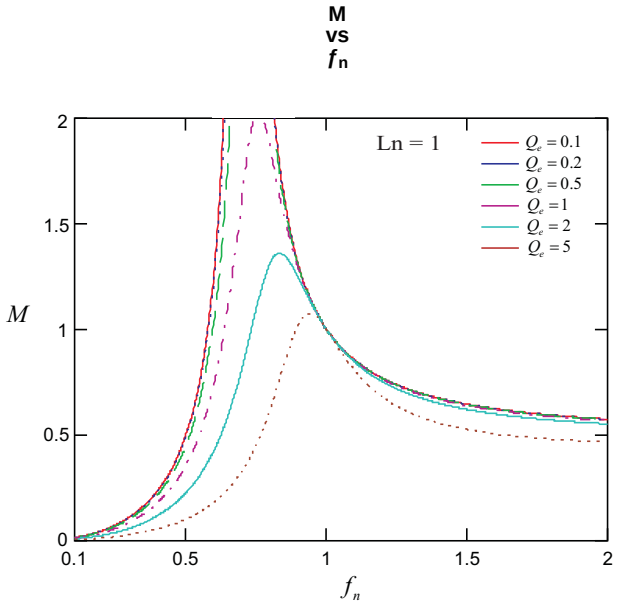

Figure 14.

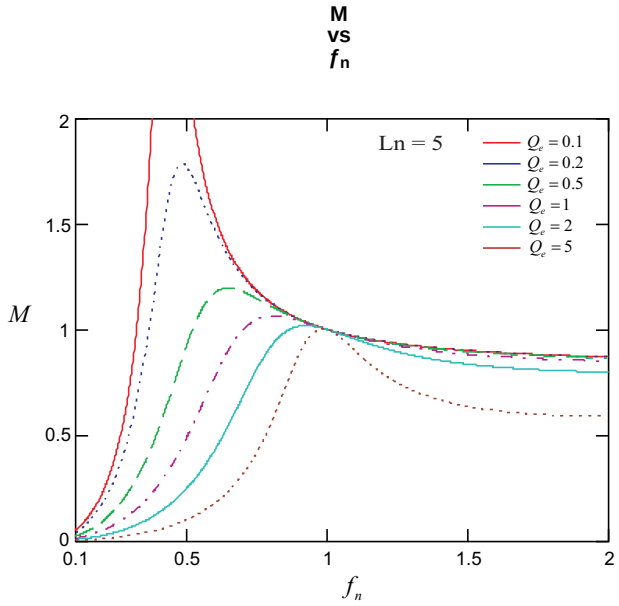

Figure 15.

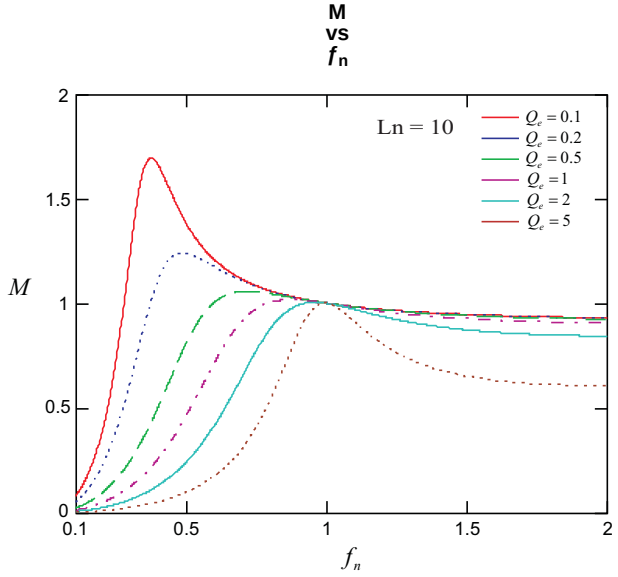

Figure 16.

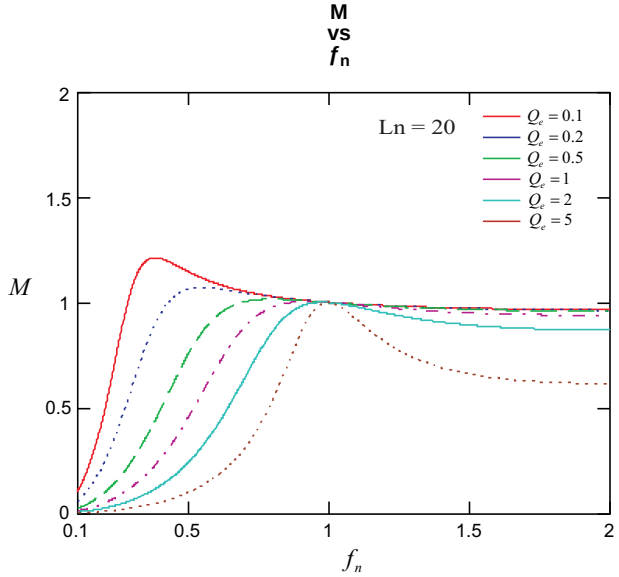

Figure 17.

Based on its theory of operation the LLC resonant converter is controlled through Pulse Frequency Modulation (PFM). The output voltage is regulated by adjusting the switching frequency according to the input and output conditions. Optimal efficiency is achieved at the nominal input voltage by setting the switching frequency close to the resonant frequency. When the input voltage droops low the switching frequency is decreased to boost the gain and maintain regulation.

The UCC25600 resonant half-bridge controller uses variable switching frequency control to adjust the resonant tank impedance and regulate output voltage. This 8-pin package device integrates the critical functions for optimizing the system performance while greatly simplifying the design and layout.

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Adjustable Dead Time

Resonant half-bridge converter relies on the resonant tank current at MOSFETs turn-off to achieve soft switching and reduce switching loss. Higher turn-off current provides more energy to discharge the junction capacitor, while it generates more turn-off loss. Smaller turn-off current reduces turn-off loss, but it requires longer time to discharge MOSFETs junction capacitors and achieve soft switching. By choosing an appropriate dead time, turn-off current is minimized while still maintaining zero-voltage switching, and best system performance is realized.

In UCC25600, dead time can be adjusted through a single resistor from DT pin to ground. With internal 2.25-V voltage reference, the current flow through the resistor sets the dead time.

$$t_d = 20ns + R_{dt} \times 24ns / k\Omega \tag{4}$$

To prevent shoot through when DT pin accidentally connects to ground, a minimum 120-ns dead time is inserted into the two gate driver outputs. Any dead-time setting less than 120-ns, will be limited to 120-ns.

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Oscillator

With variable switching frequency control, UCC25600 relies on the internal oscillator to vary the switching frequency. The oscillator is controlled by the current flowing out of RT pin. Except during soft start, the relationship between the gate signal frequency and the current flowing out of RT pin can be represented as:

$$f_S = \frac{1}{2}\frac{1}{\frac{6ns \times 1A}{I_{RT}} + 150ns} \approx I_{RT} \times 83Hz / \mu A \tag{5}$$

Since the switching frequency is proportional to the current, by limiting the maximum and minimum current flowing out of RT pin, the minimum and maximum switching frequency of the converter could be easily limited. As shown in Figure 18, putting a resistor from RT pin to ground limits the minimum current and putting a resistor in series with the opto-coupler limits the maximum current.

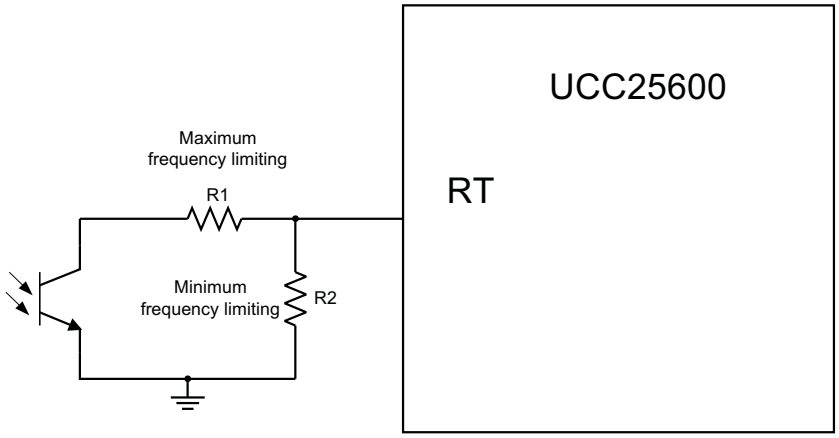

Figure 18. Maximum and Minimum Frequency Setting for UCC25600

The frequency limiting resistor can be calculated based on following equations.

$$I_{f\,max} = \frac{6ns}{\frac{1}{2f_{max}} - 150ns} \tag{6}$$

$$I_{f\,min} = \frac{6ns}{\frac{1}{2f_{min}} - 150ns} \tag{7}$$

$$I_{f\,max} = 2.5V\left(\frac{1}{R_1} + \frac{1}{R_2}\right) \tag{8}$$

$$I_{f\,min} = \frac{2.5V}{R_2} \tag{9}$$

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Soft Start

During start up and fault recovery conditions, soft start is always implemented to prevent excessive resonant tank current and ensure Zero-Voltage Switching (ZVS). During soft start, the switching frequency is increased. The soft-start time can be programmed by placing a capacitor from SS pin to ground.

The soft-start pin also serves as an ON/OFF control pin of the device. By actively pulling the SS pin below 1 V, the device is disabled. When the pull down is removed, SS pin voltage is increased because of internal charging current. Once SS pin becomes above 1.2 V, the device starts to generated gate-driver signal and enters soft-start mode. The time sequence of soft start is shown in Figure 19.

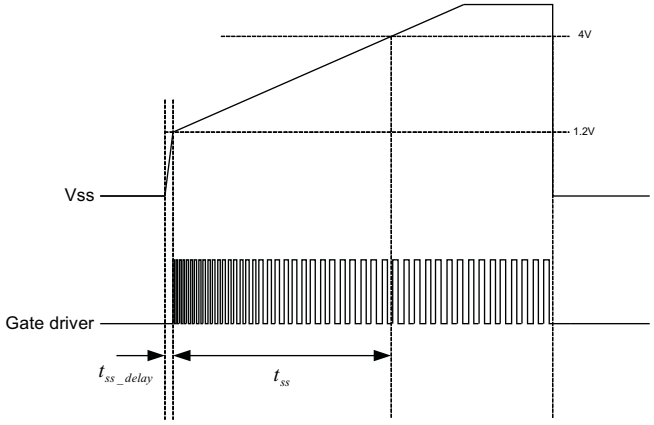

Figure 19. Soft-Start Sequence

To prevent a long delay between the ON command and apperance of a gate driver signal, the SS pin current is set as two different levels. When SS pin voltage is below 1.2 V, its output current is 175 μA. This high current could charge the soft-start pin capacitor to 1.2 V in a short period of time, and reduces the time delay. This time delay can be calculated using following equation:

$$t_{SS\_delay} = \frac{1.2V}{175\mu A} C_{SS} \tag{10}$$

The switching frequency during soft start is determined by both the current flowing out of the RT pin and the voltage on SS pin. The switching frequency can be calculated based on the following equation:

$$f_S = \frac{1}{2} \frac{1}{\frac{6ns \times 1A}{I_{RT} + \left(1.81mA - \frac{V_{SS}}{2.2k\Omega}\right)} + 150ns} \tag{11}$$

After SS pin voltage reaches 4 V, soft-start period is finished and switching frequency becomes the same as demanded by the RT pin current. The time used to charge SS pin from 1.2 V to 4 V is defined as soft-start time and can be calculated as:

$$t_{SS} = \frac{2.8V}{5\mu A} C_{SS} \tag{12}$$

To ensure reliable operation, the gate drivers restart with GD2 turning high. This prevents uncertainty during system start up.

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Burst-Mode Operation

During light load condition, the resonant converter tends to increase its switching frequency and maintain the output voltage regulation. However, due to ringing caused by transformer parasitic capacitor and the rectification-diode-junction capacitors, the energy could be directly transferred to the load through these capacitors. When this power becomes more than the load requires, output voltage become higher than the regulation level. In this case, further increasing the switching frequency will not help the situation because energy transfer to the load is not through the power stage itself.

To prevent output over voltage during this condition, the UCC25600 includes the burst-mode operation function. When the control loop demands switching frequency higher than 350 kHz, the gate driver is disabled and the power stage stops switching. When the output voltage drops, the control loop begins to demand switching frequency less than 330 kHz, the gate driver recovers and the power stage begins to deliver power again. This allows output voltage to be regulated.

This burst mode can be easily disabled by limiting the maximum switching frequency to less than 350 kHz. In this way, the control loop will never demand a switching frequency higher than 350kHz and burst mode operation will not occur.

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Over-Current Protection

To prevent power stage failure under excessive load current condition, the UCC25600 includes an over-current protection function. With a dedicated OC pin, the power stage is shut down when OC pin voltage is above 1 V. Once the OC pin voltage becomes lower than 0.6 V, the gate driver recovers with soft start. To enhance system safety, the UCC25600 latches up the whole system when OC pin becomes above 2 V. Bring VCC below UVLO level to reset the device.

The current can be indirectly sensed through the voltage across resonant capacitor by using the sensing network shown in Figure 20.

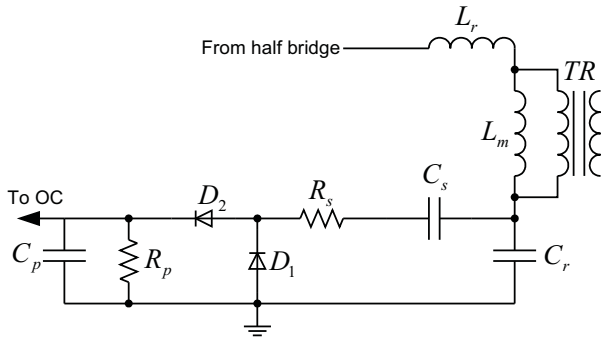

Figure 20. Current Sensing for LLC Resonant Converter

The general concept of this sensing method is that, ac voltage across the resonant capacitor is proportional to load current.

According to the FHA model, peak voltage of the ac component on the resonant capacitor can be calculated as:

$$V_{Cr\_pk} = \frac{4}{\pi} n V_o \left| \frac{j f_n L_n Q_e + 1}{f_n^{\,2} L_n} \right| \tag{13}$$

Therefore, the resonant capacitor voltage reaches its maximum value at the minimum switching frequency and maximum load. According to this equation, the current sensing network components can be calculated. Due to the nature of FHA, the final circuit parameters need to be verified through actual hardware test.

Calculated Current Sensing Network Components

NAME	FUNCTION	DESIGN EQUATION
R_S	Transfer ac voltage across resonant capacitor into current source	$R_s = \frac{V_{Cr\_pk}(max)^2}{2P_{Rs}(max)}$
C_S	Blocking dc voltage on resonant capacitor	$C_s = \frac{10}{R_s f_{\min}}$
R_P	Load resistor of the current source	$R_p = \frac{R_s}{V_{Cr\_pk}(max)}\pi$
C_P	Filter capacitor	$C_p = \frac{10}{R_p f_{\min}}$

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Gate Driver

Half-bridge resonant converter is controlled by the nearly 50% duty cycle variable frequency square wave voltage. This allows the half bridge to be easily driven by the gate-driver transformer. Compared with a half-bridge driver device, a gate-driver transformer provides a simple and reliable solution, which:

- Eliminate the need for gate driver power supply
- Enable simplified layout
- Preventing shoot through due to the transformer coupling
- No latch up

The UCC25600 integrates two-gate drivers with 0.4-A source and 0.8-A sink capability to directly drive the gate driver transformer.

For LLC resonant converter, it is critical for the gate-driver signal to be precisely symmetrical. Otherwise, the resonant tank operation will be asymmetrical. The load current distribution will be unbalanced for the output rectifiers, which in turn requires over design of the power stages and thermal management.

In UCC25600, the gate-driver outputs are precisely trimmed to have less than 50 ns mismatch. Although the gate-driver signal is quite symmetrical, it is still recommended to insert the dc blocking capacitor in the gate-driver transformer primary side to prevent transformer saturation during fast transients.

VCC

Connect a regulated bias supply to VCC pin. When VCC becomes above 10.5 V the device is enabled and after all fault conditions are cleared the gate driver starts with soft start. When VCC drops below 9.5 V, the device enters UVLO protection mode and both gate drivers are actively pulled low. When VCC rises above 20 V the device enters VCC over-voltage protection mode and the device is disabled with both gate drivers actively pulled low. VCC over-voltage protection will recover with soft start when VCC voltage returns below 18 V.

Over-Temperature Protection

UCC25600 continuously senses its junction temperature. When its junction temperature rises above 160°C the device will enter over-temperature protection mode with both gate drivers actively pulled low. When junction temperature drops below 140°C, gate driver restarts with soft start.

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)
UCC25600D	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
UCC25600DR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
UCC25600DRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
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Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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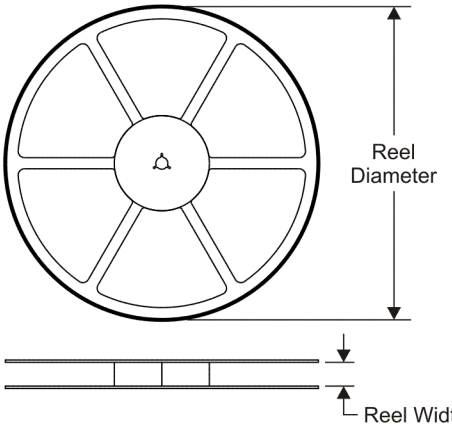
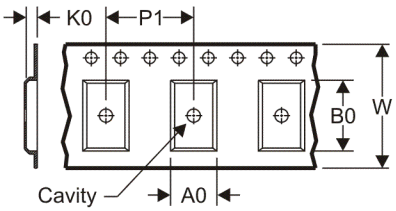
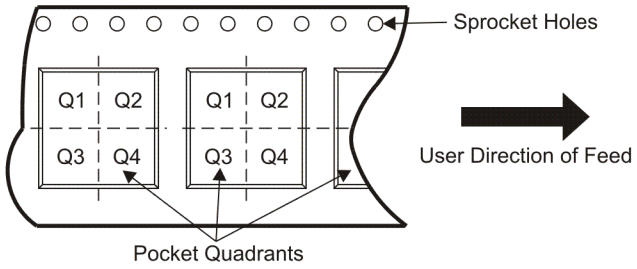


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
UCC25600DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

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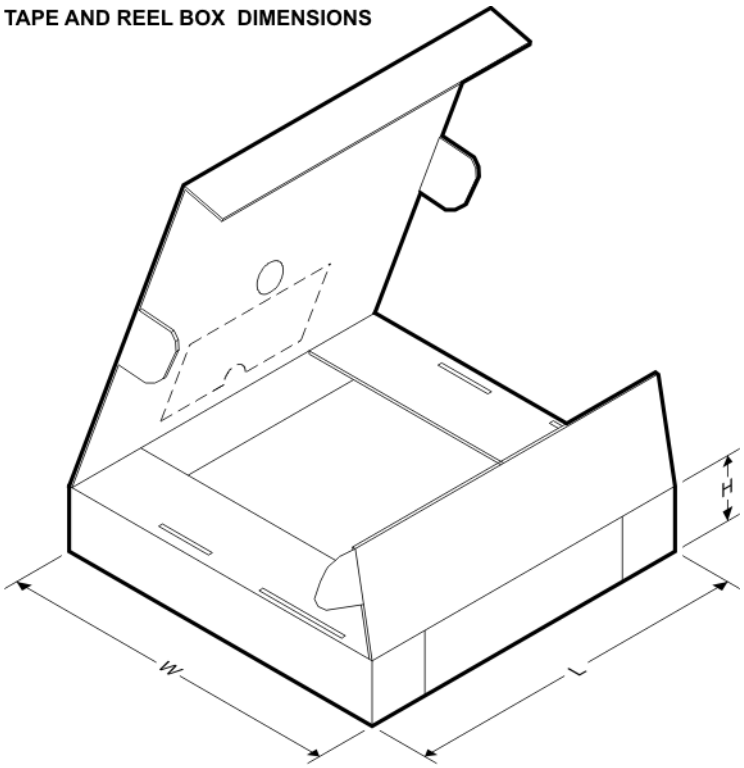
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
UCC25600DR	SOIC	D	8	2500	340.5	338.1	20.6

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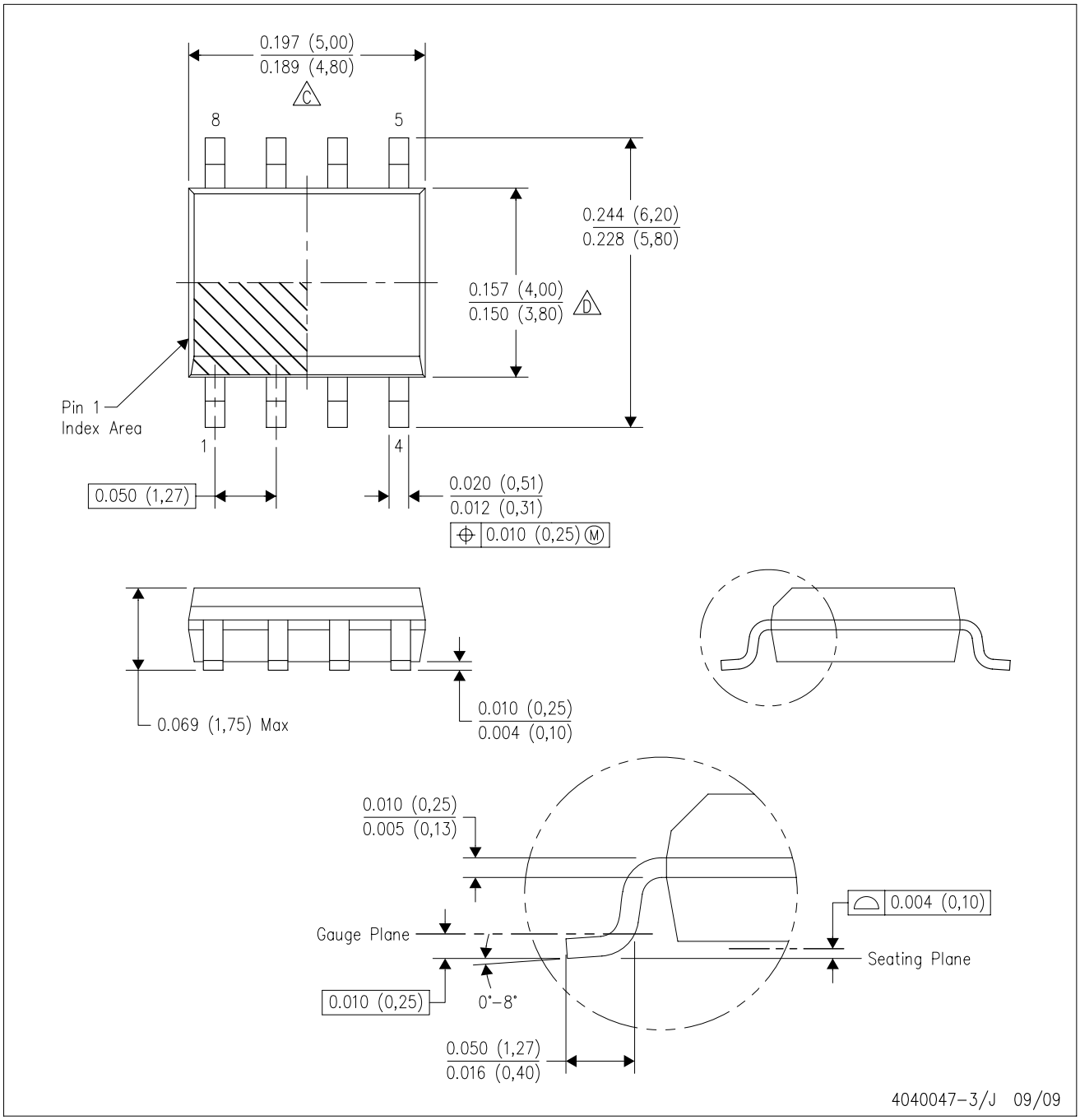
D (R–PDSO–G8) PLASTIC SMALL–OUTLINE PACKAGE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 (0,15) per end.
D. Body width does not include interlead flash. Interlead flash shall not exceed .017 (0,43) per side.
E. Reference JEDEC MS–012 variation AA.

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