SLUS829D – AUGUST 2008 – REVISED JULY 2009

ADVANCED CURRENT-MODE ACTIVE CLAMP PWM CONTROLLER

FEATURES

- **Low Output Jitter**
- **“Soft Stop” shut down of MAIN and AUX**
- **110-V Input Startup Function**
- **Ideal for Active Clamp/Reset Forward, Flyback and Synchronous Rectifier Uses**
- **Provides Complementary Auxiliary Driver with Programmable Deadtime (Turn-On Delay) between AUX and MAIN Switches**
- **Peak Current-Mode Control with 0.5-V Cycle-by-Cycle Current Limiting**
- **TrueDrive™ 2-A Sink, 2-A Source Outputs**
- **Trimmed Internal Bandgap Reference for Accurate Line UV and Line OV Threshold**
- **Programmable Slope Compensation**
- **High-Performance 1.0-MHz Synchronizable Oscillator with Internal Timing Capacitor**
- **Precise Programmable Maximum Duty Cycle**
- **PB-Free Lead Finish Package**

APPLICATIONS

- **High-Efficiency DC/DC Power Supplies**
- **Server Power, 48-V Telecom, Datacom, and 42-V Automotive Applications**

DESCRIPTION

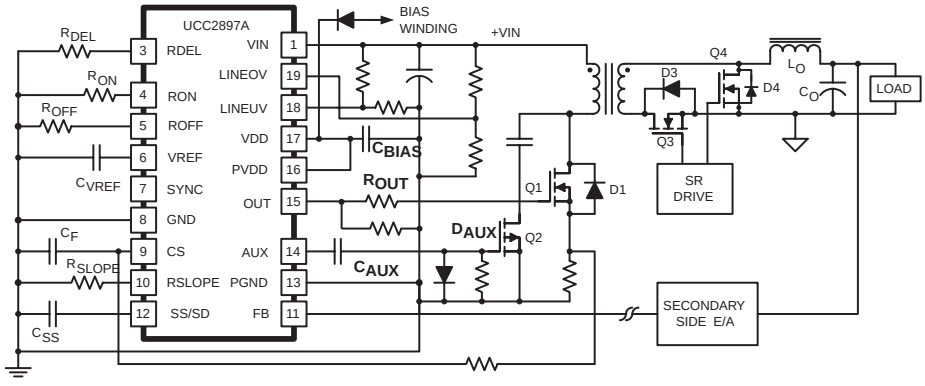
The UCC2897A PWM controller simplifies implementation of the various active clamp/reset and synchronous rectifier switching power topologies.

The UCC2897A is a peak current-mode, fixed-frequency, high-performance pulse width modulator. It includes the logic and the drive capability for the P-channel auxiliary switch along with a simple method of programming the critical delays for proper active clamp operation.

Features include an internal programmable slope compensation circuit, precise D_{MAX} limit, and a synchronizable oscillator with an internal timing capacitor. An accurate line monitoring function also programs the converter’s ON and OFF transitions with regard to the bulk input voltage, VIN.

The UCC2897A adds a second level hiccup mode current sense threshold, bi-directional synchronization and input overvoltage protection functionalities. The UCC2897A is offered in 20-pin TSSOP (PW) and 20-pin QFN (RGP) package.

TYPICAL APPLICATION DIAGRAM



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range unless otherwise noted(1)

			UNIT
Line input voltage, V_{IN}		120	V
Supply voltage, V_{DD}	(I_{DD} < 10 mA)	16.5	V
Analog inputs	FB, CS, SYNC, LINEOV, LINEUV	−0.3 to (V_{REF} + 0.3)	V
Output source current (peak), I_{O_SOURCE}	OUT, AUX	2.5	A
Output sink current (peak), I_{O_SINK}		−2.5	
Operating junction temperature range, T_J		−55 to 150	°C
Storage temperature, T_{stg}		−65 to 150	
ESD rating	Human body model, (HBM)	2000	V
	Charged device model (CDM)	500	
Lead temperature, T_{sol}, 1,6 mm (1/16 inch) from case for 10 seconds		300	°C

(2) Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability. All voltages are with respect to GND. Currents are positive into and negative out of, the specified terminal.

RECOMMENDED OPERATING CONDITIONS

	MIN	NOM	MAX	UNIT
Line input voltage, V_{IN}	18		110	V
Supply voltage, V_{DD}	8.5	12.0	16.0	V
Supply bypass capacitance, VDD (2)	1			µF
Timing resistance, R_{ON} = R_{OFF} (for 250-kHz operation)		75		kΩ
Operating junction temperature, T_J	−40		125	°C
Reference bypass capacitance, C_{REF}	0.1			µF

(2) Supply bypass capacitance should be greater than VREF capacitance by at least 10 times.

ORDERING INFORMATION

						PART NUMBERS†	
T_A	APPLICATION	AUX OUTPUT POLARITY	CYCLE-BY-CYCLE CS THRESHOLD	HICCUP MODE CS THRESHOLD	110-V HV JFET START-UP CIRCUIT	TSSOP−20 (PW)‡	QFN−20 (RGP)‡
−40°C to 125°C	DC/DC	P-Channel	0.5 V	0.75 V	Yes	UCC2897APW	UCC2897ARGP

† The PW package is available taped and reeled. Add R suffix to device type (e.g. UCC2897APWR) to order quantities of 2,000 devices per reel. Bulk quantities are 70 units per tube. The RGP package is available in two options of tape and reel. The RGPT is orderable in small reels of 250 (e.g. UCC2897ARGPT); the RGPR contains 3000 pieces per reel (e.g. UCC2897ARGPR).

‡ The TSSOP-20 (PW) and QFN−20 (RGP) package uses Pb-free lead finish of Pd-Ni-Au which is compatible with MSL level 1 at 255°C to 260°C peak reflow temperature and compatible with either lead free or Sn/Pb soldering operations.

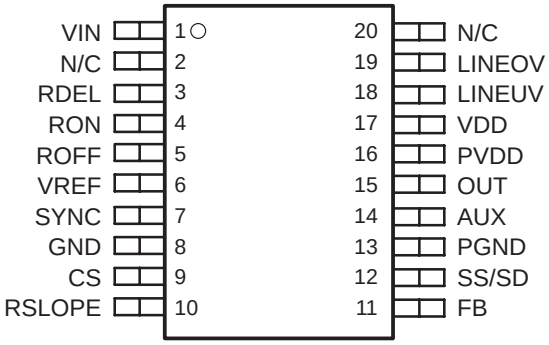
THERMAL RESISTANCE INFORMATION

PACKAGE	THERMAL RESISTANCE(1)		UNITS
TSSOP−20 (PW)	θjc	36.6 to 35.0	°C/W
	θja	108.4 to 147.0	
QFN−20 (RGP)	θjc	TBD	°C/W
	θja	TBD	

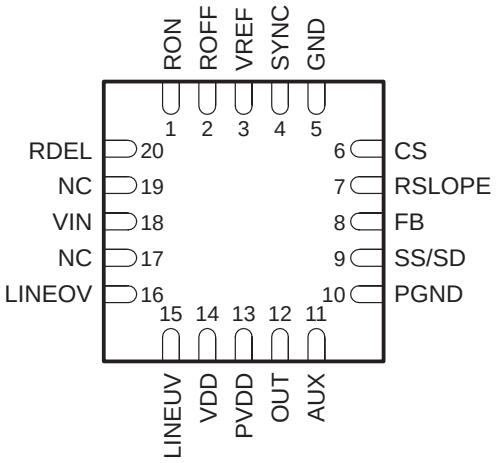
(1) Thermal resistance is measured in accordance with JEDEC JESD 51 test conditions and is useful for thermal performance comparison of different packages. Performance in any specific use is a function of board layout, board construction, air flow and other parameters.

PIN ASSIGNMENTS

PW PACKAGE (TOP VIEW)



QFN PACKAGE (BOTTOM VIEW)



ELECTRICAL CHARACTERISTICS

V_{DD} = 12 V(1), 1-µF capacitor from VDD to GND, 0.01-µF capacitor from VREF to GND, R_{ON} = R_{OFF} = 75 kΩ, R_{DEL} = 10 kΩ, R_{SLOPE} = 50 kΩ, −40 °C ≤ T_A = T_J ≤ 125°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
OVERALL						
$I_{STARTUP}$	Start-up current	V_{DD} < V_{UVLO}		300	500	µA
I_{DD}	Operating supply current(1)(2)	V_{FB} = 0 V, V_{CS} = 0 V, Outputs not switching		2	3	mA
HIGH-VOLTAGE BIAS SECTION						
I_{DD-ST}	VDD startup current	Current available from VDD during start-up, T_A = −40°C to 85°C, VIN = 36 V, (3)	4	11		mA
I_{VIN}	JFET leakage current	VIN = 120 V; VDD = 14 V			75	µA
UNDERVOLTAGE LOCKOUT						
UVLO	Start threshold voltage		12.2	12.7	13.2	V
	Minimum operating voltage after start		7.6	8.0	8.4	
	Hysteresis		4.4	4.7	5.0	
LINE MONITOR						
V_{LINEUV}	Line UV voltage threshold		1.243	1.268	1.294	V
$I_{LINEUVHYS}$	Line UV hysteresis current		−11.5	−13.0	−14.5	µA
V_{LINEOV}	Line OV voltage threshold		1.243	1.268	1.294	V
$I_{LINEOVHYS}$	Line OV hysteresis current		−11.5	−13.0	−14.5	µA
SOFT-START						
I_{SSC}	SS charge current	R_{ON} = 75 kΩ (4)	−10.5	−14.5	−18.5	µA
I_{SSD}	SS discharge current	R_{ON} = 75 kΩ (4)	10.5	14.5	18.5	
$V_{SS/SD}$	Discharge/shutdown threshold voltage		0.4	0.5	0.6	V
VOLTAGE REFERENCE						
V_{REF}	Reference voltage	T_J = 25°C	4.85	5.00	5.15	V
V_{REF}	Reference voltage	0 A < I_{REF} < 5 mA, over temperature	4.75	5.00	5.25	
I_{SC}	Short circuit current	REF = 0 V, T_J = 25°C	−20	−11	−8	mA
INTERNAL SLOPE COMPENSATION						
m	Slope	FB = High	-10%	$\frac{R_{CS}}{R_{SLOPE}}$	+10%	
OSCILLATOR						
f_{OSC}	Oscillator frequency	T_J = 25°C	237	250	265	kHz
		−40°C < T_J < 125°C; 8.5V < VDD < 14.5V	225		270	
V_{P_P}	Oscillator amplitude (peak-to-peak)			2		V

(1) Set VDD above the start threshold before setting at 12 V.
(2) Does not include current of the external oscillator network.
(3) The power supply starts with I_{DD-ST} load on VDD, part will start up with no load up to 125°C. For more information see the Detailed Pin Description section for VIN and VDD.
(4) I_{SSC} and $I_{SS/SD}$ are directly proportional to I_{RON}. See equation 7.

ELECTRICAL CHARACTERISTICS

V_{DD} = 12 V(1), 1-µF capacitor from VDD to GND, 0.01-µF capacitor from VREF to GND, R_{ON} = R_{OFF} = 75 kΩ, R_{DEL} = 10 kΩ, R_{SLOPE} = 50 kΩ, −40 °C ≤ T_A = T_J ≤ 125°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SYNCHRONIZATION						
	SYNC input high voltage		3.0			V
	SYNC input low voltage				1.6	V
	SYNC pull down output current			600		µA
	SYNC pull up output current			−600		µA
	SYNC output pulse width			150		ns
t_{DEL}	SYNC-to-output delay			50		ns
PWM						
D_{MAX}	Maximum duty cycle		66%	70%	74%	
	Minimum duty cycle				0%	
	PWM offset	CS = 0 V	0.43	0.50	0.61	V
CURRENT SENSE						
V_{LVL}	Current sense level shift voltage		0.40	0.50	0.60	V
$V_{ERR(max)}$	Maximum voltage error (clamped)			5.0		
V_{CS}	Current sense threshold cycle−by−cycle		0.43	0.48	0.53	
OUTPUT (OUT AND AUX)						
t_R	Rise time	C_{LOAD} = 2 nF		19	28	ns
t_F	Fall time	C_{LOAD} = 2 nF		14	23	
t_{DEL1}	Delay time (AUX to OUT)	C_{LOAD} = 2 nF, R_{DEL} = 10 kΩ		110		
t_{DEL2}	Delay time (OUT to AUX)	C_{LOAD} = 2 nF, R_{DEL} = 10 kΩ		115		
$I_{OUT(src)}$	Output source current			−2		A
$I_{OUT(sink)}$	Output sink current			2		
$V_{OUT(low)}$	Low-level output voltage	I_{OUT} = 150 mA		0.4		V
$V_{OUT(high)}$	High-level output voltage	I_{OUT} = −150 mA		11.1		

(1) Set VDD above the start threshold before setting at 12 V.
(2) Maximum pulse width needs to be less than D_{MAX}, which is a function of R_{ON} and R_{OFF}. For more information on D_{MAX}, see detailed pin description for R_{OFF}.

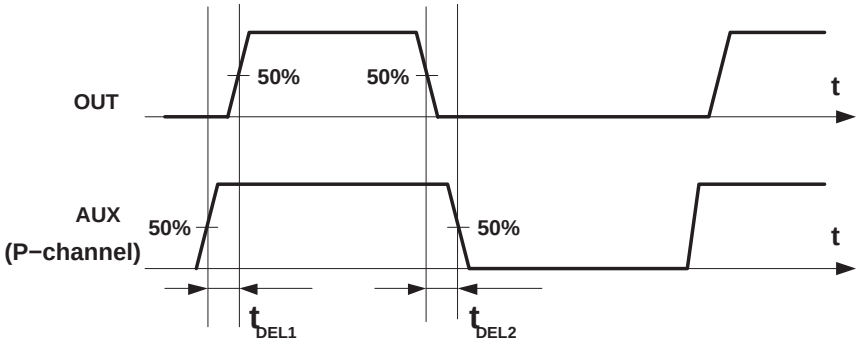
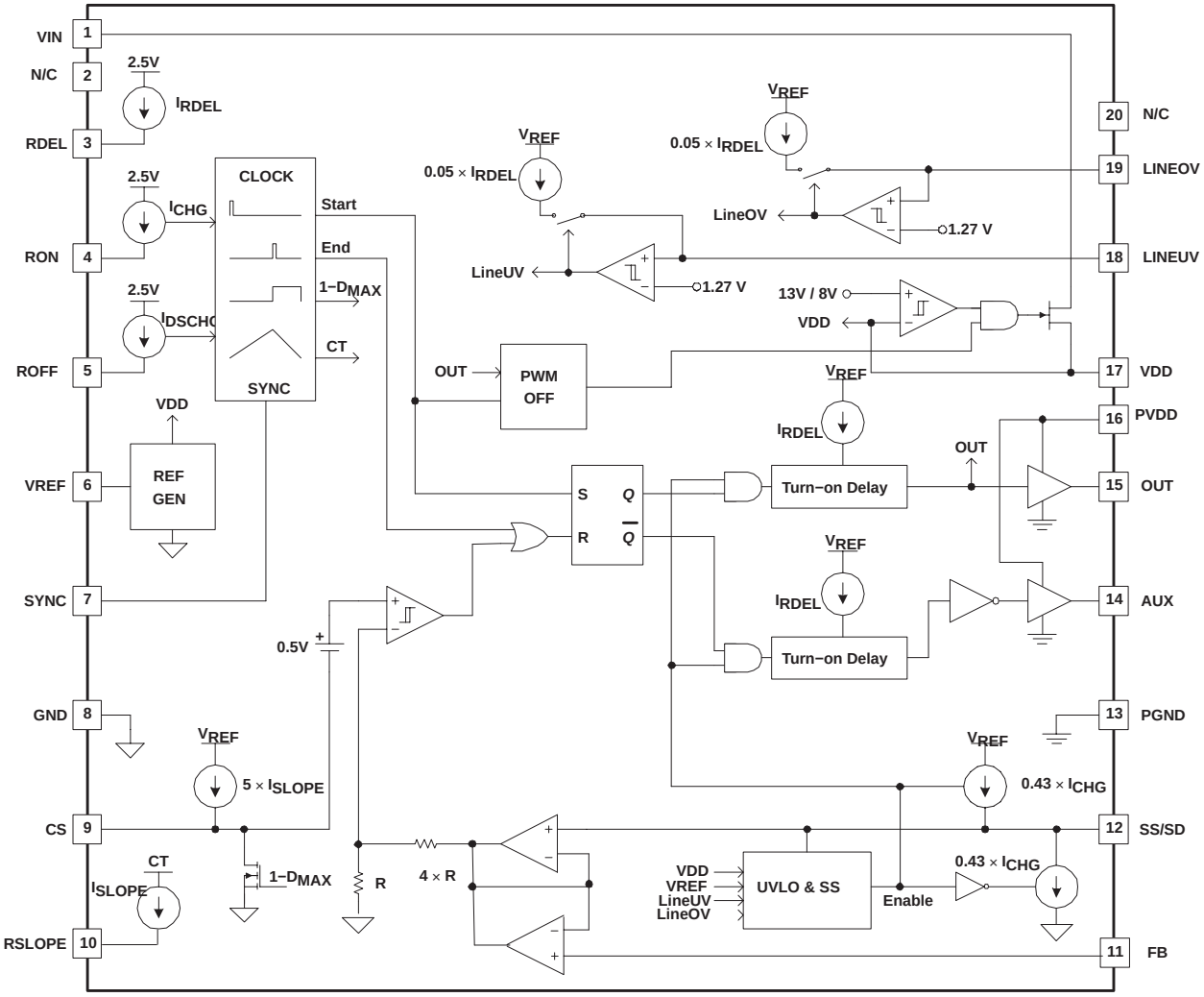


Figure 1. Output Timing Diagram

FUNCTIONAL BLOCK DIAGRAM



Note: Pin numbers shown are for PW (TSSOP−20) package.

TERMINAL FUNCTIONS

TERMINAL			I/O	DESCRIPTION
NAME	UCC2897A TSSOP−20 (PW)	UCC2897A QFN−20 (RGP)		
AUX	14	11	O	This output drives the auxiliary clamp MOSFET which is turned on when the main PWM switching device is turned off. The AUX pin can directly drive the auxiliary switch with 2-A source turn-on current and 2-A sink turn-off current.
CS	9	6	I	This pin is used to sense the peak current utilized for current mode control and for current limiting functions. The peak signal which can be applied to this pin before pulse−by−pulse current limiting activates is approximately 0.5 V.
FB	11	8	I	This pin is used to bring the error signal from an external optocoupler or error amplifier into the PWM control circuitry. Often, there is a resistor tied from FB to VREF, and an optocoupler is used to pull the control pin closer to GND to reduce the pulse width of the OUT output driving the main power switch of the converter.
GND	8	5	−	This pin serves as the fundamental analog ground for the PWM control circuitry. This pin should be connected to PGND directly at the device.
LINEOV	19	16	I	This is an input pin of voltage comparator with programmable hysteresis and 1.27−V threshold, providing LINE overvoltage or other functions.
LINEUV	18	15	I	This pin provides a means to accurately enable/disable the power converter stage by monitoring the bulk input voltage or another parameter. When the circuit initially starts (or restarts from a disabled condition), a rising input on LINEUV enables the outputs when the threshold of 1.27 V is crossed. After the circuit is enabled, then a falling LINEUV signal disables the outputs when the same threshold is reached. The hysteresis between the two levels is programmed using an internal current source.
OUT	15	12	O	This output pin drives the main PWM switching element MOSFET in an active clamp controller. It can directly drive an N−channel device with 2−A source turn−on current and 2−A sink turn−off current. Recommend connecting a 10−kΩ resistor from this pin to PGND pin.
PGND	13	10	−	The PGND should serve as the current return for the high−current output drivers OUT and AUX. Ideally, the current path from the outputs to the switching devices, and back would be as short as possible, and enclose a minimal loop area.
PVDD	16	13	I	This is the supply pin for the power devices. It is separated internally from the VDD pin.
RSLOPE	10	7	I	A resistor connected from this pin to GND programs an internal current source that sets the slope compensation ramp for the current mode control circuitry.
RTDEL	3	20	I	A resistor from this pin to GND programs the turn−on delay of the two gate drive outputs to accommodate the resonant transitions of the active clamp power converter.
ROFF	5	2	I	A resistor connected from this pin to GND programs an internal current source that discharges the internal timing capacitor.
RON	4	1	I	A resistor connected from this pin to GND programs an internal current source that charges the internal timing capacitor.
SS/SD	12	9	I	A capacitor from SS/SD to ground is charged by an internal current source of I_{RON} to program the soft−start interval for the controller. During a fault condition this capacitor is discharged by a current source equal to I_{RON}.
SYNC	7	4	I	The SYNC pin serves as a bidirectional synchronization input for the internal oscillator. The synchronization function is implemented such that the user programmable maximum duty cycle (set by RON and ROFF) remains accurate during synchronized operation. Thiis pin should be left open if not used. Its external capacitance should be minimized. No capacitors should be connected to this pin.
VDD	17	14	I	This is the power supply for the device. There should be a 1.0−µF capacitor directly from VDD to PGND. The capacitor value should be minimum 10 times bigger than that on VREF. PGND and GND should be connected externally and directly from PGND pin to GND pin.
VIN	1	18	I	This pin is connected to the input power rail directly. Inside the device, a high−voltage start−up device is utilized to provide the start−up current for the controller until a bootstrap type bias rail becomes available.
VREF	6	3	O	This is the 5−V reference voltage that can be utilized for an external load of up to 5 mA. Since this reference provides the supply rail for internal logic, it should be bypassed to AGND as close as possible to the device. The VREF bias profile may not be monotonic before VDD reaches 5 V.

DETAILED PIN DESCRIPTIONS

RDEL

This pin is internally connected to an approximately 2.5-V DC source. A resistor (R_{DEL}) to GND sets the turn-on delay for both gate drive signals of the UCC2987A controller. The delay time is identical for both switching transitions, between OUT is turning off and AUX is turning on as well as when AUX is turning off and OUT is turning on. The delay time is defined as:

$$t_{DEL1} = t_{DEL2} = 11.1 \times 10^{-12} \times R_{DEL} + 15 \times 10^{-9} \text{ seconds} \quad (1)$$

For proper selection of the delay time refer to the various references describing the design of active clamp power converters.

RON

This pin is internally connected to an approximately 2.5-V DC source. A resistor (R_{ON}) to GND (pin 6) sets the charge current of the internal timing capacitor. The RON pin, in conjunction with the ROFF pin (pin 3) are used to set the operating frequency and maximum operating duty cycle.

ROFF

This pin is internally connected to an approximately 2.5-V DC source. A resistor (R_{OFF}) to GND (pin 6) sets the discharge current of the internal timing capacitor. The RON and ROFF pins are used to set the switching period (T_{SW}) and maximum operating duty cycle (D_{MAX}) according to the following equations:

$$t_{ON} = 36.1 \times 10^{-12} \times R_{ON} \times \left(\frac{S}{\Omega}\right) - t_{DEL}(s) \text{ seconds} \quad (2)$$

$$t_{OFF} = 15 \times 10^{-12} \times R_{OFF} \times \left(\frac{S}{\Omega}\right) + t_{DEL}(s) + 170 \times 10^{-9} \times (s) \text{ seconds} \quad (3)$$

$$T_{SW} = t_{ON} + t_{OFF} \quad (4)$$

$$D_{MAX} = \frac{t_{ON}}{t_{ON} + t_{OFF}} \quad (5)$$

DETAILED PIN DESCRIPTIONS (continued)

VREF

The controller's internal, 5-V bias rail is connected to this pin. The internal bias regulator requires a high quality ceramic bypass capacitor (C_{VREF}) to GND for noise filtering and to provide compensation to the regulator circuitry. The recommended C_{VREF} value is 0.22-µF and X7R capacitors are recommended. The minimum bypass capacitor value is 0.022-µF limited by stability considerations of the bias regulator, while the maximum is approximately 22-µF. The capacitance on VREF and VDD should be in a minimum ratio of 1:10.

The VREF pin is internally current limited and can supply approximately 5-mA to external circuits. The 5-V bias is only available when the undervoltage lock out (UVLO) circuit enables the operation of UCC2897A controller. The VREF bias profile may not be monotonic before VDD reaches 5.0 V.

For the detailed functional description of the undervoltage lock out (UVLO) circuit refer to the *Functional Description* section of this datasheet.

SYNC

This pin is a bi-directional synchonization terminal. This pin should be left open if not used.

This pin provides an input for an external clock signal which can be used to synchronize the internal oscillator of the UCC2897A controller. The synchronizing frequency must be higher than the free running frequency of the onboard oscillator $\left(T_{SYNC} < T_{SW}\right)$. The acceptable minimum pulse width of the synchronization signal is approximately 50 ns (positive logic), and it should remain shorter than $\left(1 - D_{MAX}\right) \times T_{SYNC}$ where D_{MAX} is set by R_{ON} and R_{OFF}. If the pulse width of the synchronization signal stays within these limits, the maximum operating duty ratio remains valid as defined by the ratio of R_{ON} and R_{OFF}, and D_{MAX} is the same in free running and in synchronized modes of operation. If the pulse width of the synchronization signal would exceed the $\left(1 - D_{MAX}\right) \times T_{SYNC}$ limit, the maximum operating duty cycle is defined by the synchronization pulse width.

In the stand-alone mode, the sync pin is driven by the internal oscillator which provides output pulses. The pulse width from SYNC output does not vary with the duty cycle. That signal can be use to synchronize other PWM controllers or circuits needing a constant frequency time base.

External capacitance should be minimized on this pin layout. There should be no capacitors connected between this pin and GND or PGND. For more information on synchronization of the UCC2897A refer to the *Functional Description* section of this datasheet.

GND

This pin provides a reference potential for all small signal control and programming circuitry inside the UCC2897A. Ground layout is critical for correct operation. High current surges from the MOSFET drivers conduct through PVDD, OUT, AUX, and PGND. To localize these surges, PVDD must be bypassed directly to PGND. PGND current must be electrically, capacitively, and inductively isolated from GND with only one short trace connecting PGND to GND, located to best minimize noise into GND.

DETAILED PIN DESCRIPTIONS (continued)

CS

This is a direct input to the PWM and current limit comparators of the UCC2897A controller. The CS pin should never be connected directly across the current sense resistor (R_{CS}) of the power converter. A small, customary R−C filter between the current sense resistor and the CS pin is necessary to accommodate the proper operation of the onboard slope compensation circuit and in order to protect the internal discharge transistor connected to the CS pin (R_F, C_F).

Slope compensation is achieved across R_F by a linearly increasing current flowing out of the CS pin. The slope compensation current is only present during the on-time of the gate drive signal of the main power switch (OUT) of the converter. The internal pull-down transistor of the CS pin is activated during the discharge time of the timing capacitor. This time interval is $\left(1 - D_{MAX}\right) \times T_{SW}$ long and represents the guaranteed off time of the main power switch.

RSLOPE

A resistor (R_{SLOPE}) connected between this pin and GND (pin 6) sets the amplitude of the slope compensation current. During the on time of the main gate drive output (OUT) the voltage across R_{SLOPE} is a representation of the internal timing capacitor waveform. As the timing capacitor is being charged, the voltage across R_{SLOPE} also increases, generating a linearly increasing current waveform. The current provided at the CS pin for slope compensation is proportional to this current flowing through R_{SLOPE}.

Due to the high speed, AC voltage waveform present at the RSLOPE pin, the parasitic capacitance and inductance of the external circuit components connected to the RSLOPE pin should be carefully minimized.

For more information on how to program the internal slope compensation refer to the *Setup Guide* section of this datasheet.

FB

FB and SS/SD interact. The one with the lower voltage value takes control on the duty cycle, refer to SS/SD description. This pin is an input for the control voltage of the pulse width modulator of the UCC2897A. The control voltage is generated by an external error amplifier by comparing the converters output voltage to a voltage reference and employing the compensation for the voltage regulation loop. Usually, the error amplifier is located on the secondary side of the isolated power converter and its output voltage is sent across the isolation boundary by an opto coupler. Thus, the FB pin is usually driven by the opto coupler. An external pull-up resistor to the VREF pin (pin 4) is also needed for proper operation as part of the feedback circuitry.

The control voltage is internally buffered and connected to the PWM comparator through a voltage divider to make it compatible to the signal level of the current sense circuit. The useful voltage range of the FB pin is between approximately 2.5 V and 4.5 V. Control voltages below the 2.5-V threshold result in zero duty cycle (pulse skipping) while voltages above 4.5 V result in full duty cycle (D_{MAX}) operation.

DETAILED PIN DESCRIPTIONS (continued)

SS/SD

A capacitor (C_{SS}) connected between this pin and GND (pin 6) programs the soft start time of the power converter. The soft-start capacitor is charged by a precise, internal DC current source which is programmed by the R_{ON} resistor connected to pin 2. The soft-start current is defined as:

$$I_{SS} = 0.43 \times I_{RON} = 0.43 \times \frac{V_{REF}}{2} \times \frac{1}{R_{ON}} \quad (6)$$

This DC current charges C_{SS} from 0 V to approximately 5 V. Internal to the UCC2897A, the soft−start capacitor voltage is buffered and ORed with the control voltage present at the FB pin (pin 9). The lower of the two voltages manipulates the controller's PWM engine through the voltage divider described with regards to the FB pin. Accordingly, the useful control range on the SS pin is similar to the control range of the FB pin and it is between 2.5 V and 4.5 V approximately. During line undervoltage protection, the PWM follows this pin capacitor discharge to achieve soft stop funtion.

PGND

This pin serves as a dedicated connection to all high-current circuits inside the UCC2897A. The high-current portion of the controller consists of the two high-current gate drivers, and the various bias connections except VREF (pin 4). The PGND (pin 11) and GND (pin 6) pins are not connected internally, a low-impedance, external connection between the two ground pins is also required. It is recommended to form a separate ground plane for the low current setup components (R_{DEL}, R_{ON}, R_{OFF}, C_{VREF}, C_F, R_{SLOPE}, C_{SS} and the emitter of the opto-coupler in the feedback circuit). This separate ground plane (GND) should have a single connection to the rest of the ground of the power converter (PGND) and this connection should be between pin 6 and pin 11 of the controller.

AUX

This is a high-current gate drive output for the auxiliary switch to implement the active clamp operation for the power stage. The auxiliary output (AUX) of the UCC2897A drives a P-channel device as the clamp switch therefore it requires an active low operation (the switch is ON when the output is low).

OUT

This high-current output drives an external N-channel MOSFET. The UCC2897A controller uses an active high drive signal for the main switch of the converter.

Due to the high speed and high-drive current capability of these outputs (AUX, OUT) the parasitic inductance of the external circuit components connected to these pins should be carefully minimized. A potential way of avoiding unnecessary parasitic inductances in the gate drive circuit is to place the controller in close proximity to the MOSFETs and by ensuring that the outputs (AUX, OUT) and the gates of the MOSFET devices are connected by wide, overlapping traces. It is recommend connecting a 10−kΩ resistor from this pin to PGND pin to reduce possible parasitic effect from layout.

DETAILED PIN DESCRIPTIONS (continued)

VDD

The VDD rail is the primary bias for the internal, high-current gate drivers, the internal 5-V bias regulator and for parts of the undervoltage lockout circuit. To reduce switching noise on the bias rail, a good quality ceramic capacitor (C_{HF}) must be placed very closely between the VDD pin and PGND (pin 11) to provide adequate filtering. The recommended C_{HF} value is 1-µF for most applications but its value might be affected by the properties of the external MOSFET transistors used in the power stage.

In addition to the low-impedance, high-frequency filtering, the controller's bias rail requires a larger value energy storage capacitor (C_{BIAS}) connected parallel to C_{HF}. The energy storage capacitor must provide the hold up time to operate the UCC2897A (including gate drive power requirements) during start up. In steady state operation the controller must be powered from a bootstrap winding off the power transformer or by an auxiliary bias supply. In case of an independent auxiliary bias supply, the energy storage is provided by the output capacitance of the bias supply. The capacitor values are also determined by the capacitor values connected to VREF. The capacitance on VREF and VDD should be in a minimum ratio of 1:10.

LINEUV

This input monitors the incoming power source to provide an accurate undervoltage lockout function with user programmable hysteresis for the power supply controlled by the UCC2897A. The unique property of the UCC2897A is to use only one pin to implement these functions without sacrificing on performance. The input voltage of the power supply is scaled to the precise 1.27-V threshold of the undervoltage lockout comparator by an external resistor divider (R_{IN1}, R_{IN2} in Figure 7). Once the line monitor's input threshold is exceeded, an internal current source gets connected to the LINEUV pin. The current generator is programmed by the R_{DEL} resistor connected to pin 1 of the controller. The actual current level is given as:

$$I_{HYST} = \frac{V_{REF}}{2} \times \frac{1}{R_{DEL}} \times 0.05 \quad (7)$$

As this current flows through R_{IN2} of the input divider, the undervoltage lockout hysteresis is a function of I_{HYST} and R_{IN2} allowing accurate programming of the hysteresis of the line monitoring circuit. When LINEUV is detected, PWM follows VSS capacitor discharge and soft stop function is provided. The soft−start capacitor starts discharging when the soft−start capacitor voltage reaches 2.5 V. Both OUT and AUX stop switcing while soft−start capacitor continues discharging until its voltage reaches 0.5 V when the soft start is resumed on the assumption of all other soft start conditions are met.

For more information on how to program the line monitoring function refer to the *Setup Guide* of this datasheet.

DETAILED PIN DESCRIPTIONS (continued)

VIN

The UCC2897A controller is equipped with a high voltage, N-channel JFET start up device to initiate operation from the input power source of the converter in applications where the input voltage does not exceed the 110-V maximum rating of the start up transistor. In these applications, the VIN pin can be connected directly to the positive terminal of the input power source. The internal JFET start up transistor provides charge current for the energy storage capacitor (C_{BIAS}) connected across the VDD (pin 14) and PGND (pin 11) terminals. Note that the start up device is turned off immediately when the voltage on the VDD pin exceeds approximately 12.7 V, the controller's undervoltage lockout threshold for turn-on. The JFET is also disabled at all times when the high-current gate drivers are switching to protect against excessive power dissipation and current through the device. For dependable startup, VDD must not be loaded by more than 4 mA.

For more information on biasing the UCC2897A, refer to the *Setup Guide* and *Additional Application Information* Sections of this datasheet.

LINEOV

This input monitors the incoming power source to provide an accurate overvoltage protection with user programmable hysteresis for the power supply controlled by the controller. The circuit implementation of the overvoltage protection function is identical to the technique used for monitoring the input power rail for undervoltage lockout. This allows implementing an accurate threshold and hysteresis using only one pin. The input voltage of the power supply is scaled to the precise 1.27-V threshold of the overvoltage protection comparator by an external resistor divider (R_{IN3}, R_{IN4} in Figure 7). Once the line monitor's input threshold is exceeded, an internal current source gets connected to the LINEOV pin. The current generator is programmed by the R_{DEL} resistor connected to pin 1 of the controller. The actual current level is given as:

$$I_{HYST} = \frac{V_{REF}}{2} \times \frac{1}{R_{DEL}} \times 0.05 \quad (8)$$

As this current flows through R_{IN4} of the input divider, the overvoltage protection hysteresis is a function of I_{HYST} and R_{IN4} allowing accurate programming of the hysteresis of the line monitoring circuit.

For more information on how to program the overvoltage protection, refer to the *Setup Guide* of this datasheet.

FUNCTIONAL DESCRIPTION

JFET Control and UVLO

The UCC2897A controller includes a high voltage JFET start up transistor. The steady state power consumption of the of the control circuit which also includes the gate drive power loss of the two power switches of an active clamp converter exceeds the current and thermal capabilities of the device. Thus the JFET should only be used for initial start up of the control circuitry and to provide keep-alive power during stand-by mode when the gate drive outputs are not switching. Accordingly, the start-up device is managed by its own control algorithm implemented on board the UCC2897A. The following timing diagram illustrates the operation of the JFET start up device.

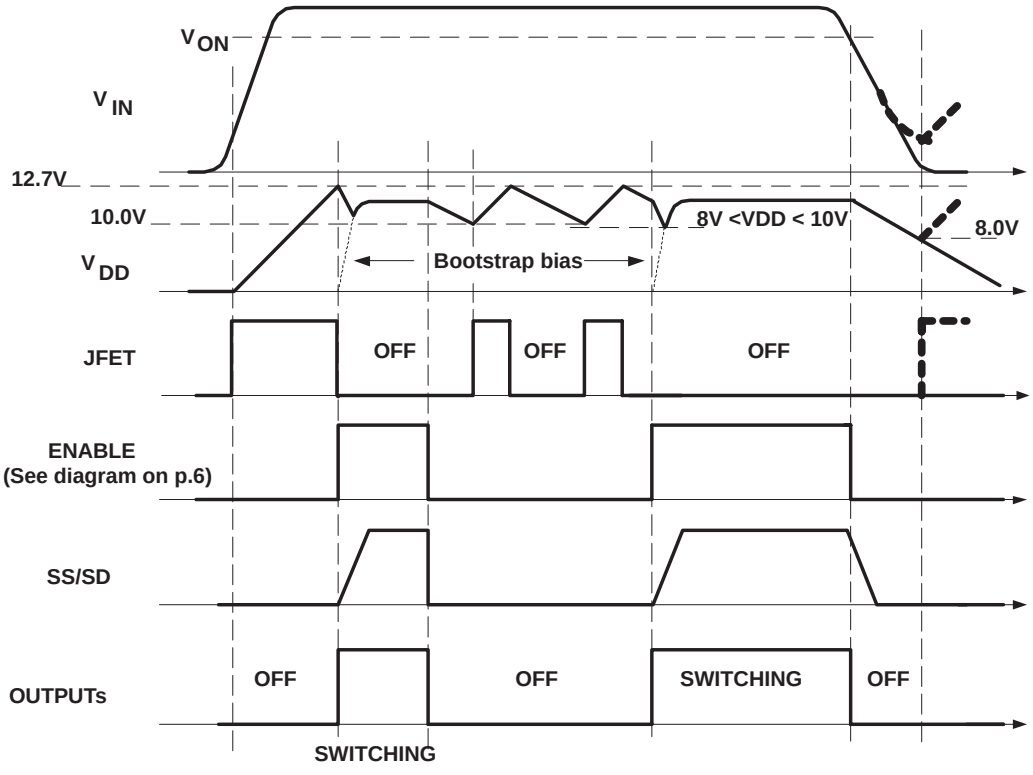


Figure 2. JFET Control Startup and Shutdown

Note: Values are typical in the drawing.

During initial power up the JFET is on and charges the C_{BIAS} and C_{HF} capacitors connected to the VDD pin. The VDD pin is monitored by the controller's undervoltage lockout circuit to ensure proper biasing before the operation is enabled. When the VDD voltage reaches approximately 12.7 V (UVLO turn-on threshold) the UVLO circuit enables the rest of the controller. At that time, the JFET is turned off and 5 V appears on the VREF terminal. Switching waveforms might not appear at the gate drive outputs unless all other conditions of proper operation are met. These conditions are:

- the voltage on the CS pin is below the current limit threshold
- the control voltage is above the zero duty cycle boundary (V_{FB} > 2.5 V)
- the input voltage is in the valid operating range (V_{VON}<V_{VIN}<V_{VOFF}) i.e. the line under or overvoltage protections are not activated.

FUNCTIONAL DESCRIPTION

As the controller starts operation it draws its bias power from the C_{BIAS} capacitor until the bootstrap winding takes over (refering to Figure 10 and Figure 11). During this time VDD voltage is falling rapidly as the JFET is already off but the bootstrap voltage is still not sufficient to power the control circuits. It is imperative to store enough energy in C_{BIAS} to prevent the bias voltage to dip below the turn off threshold of the UVLO circuit during the start up time interval. Otherwise the power supply goes through several cycles of retry attempts before steady state operation might be established.

During normal operation the bias voltage is determined by the bootstrap bias design. The UCC2897A can tolerate a wide range of bias voltages between the minimum operating voltage (UVLO turn-off threshold) and the maximum operating voltage as defined in the Recommended Operating Conditions.

In applications where the power supply must be able to go to stand by in response to an external command, the bias voltage of the controller must be kept alive to be able to react intelligently to the control signal. In stand by mode, switching action is suspended for an undefined period of time and the bootstrap power is unavailable to bias the controller. Without an alternate power source the bias voltage would collapse and the controller would initiate a re-start sequence. To avoid this situation, the on board JFET of the UCC2897A controller can keep the VDD bias alive as long as the gate drive outputs remain inactive. As shown in the timing diagram in Figure 2, the JFET is turned on when VDD = 10 V and charges the C_{BIAS} capacitor to approximately 12.7 V. At that time the JFET turns off and VDD gradually decreases to 10 V then the procedure is repeated. When the power supply is enabled again, the controller is fully biased and ready to initiate its soft start sequence. As soon as the gate drive pulses appear the JFET are turned off and bias must be provided by the bootstrap bias generator.

During power down the situation is different as switching action might continue until the VDD bias voltage drops below the controller's own UVLO turn-off threshold (approximately 8 V). At that time the UCC2897A shuts down completely turning off its 5 V bias rail and returning to start up state when the JFET device is turned on and the C_{BIAS} capacitor starts charging again. In case the converter's input voltage is re-established, the UCC2897A attempts to restart the converter.

Line Undervoltage Protection

As shown in Figure 3, when the input power source is removed the power supply is turned off by the line undervoltage protection because the bootstrap winding keeps the VDD bias up as long as switching takes place in the power stage. As the power supply's input voltage gradually decreases towards the line cut off voltage the converter's operating duty cycle must compensate for the lower input voltage. At minimum input voltage the duty cycle nears its maximum value (D_{MAX}). Under these conditions the voltage across the clamp capacitor approaches its highest value since the transformer must be reset in a relatively short time. The timing diagram in Figure 3 highlights that in the instance when the converter stops switching the clamp capacitor voltage might be at its maximum level. Since the clamp capacitor's only load is the power transformer, this high voltage could linger across the clamp capacitor for a long time when the converter is off. With this high voltage present across the clamp capacitor a soft start would be very dangerous, due to the narrow duty cycle of the main switch and the long on-time of the clamp switch. This could cause the power transformer to saturate during the next soft-start cycle.

FUNCTIONAL DESCRIPTION

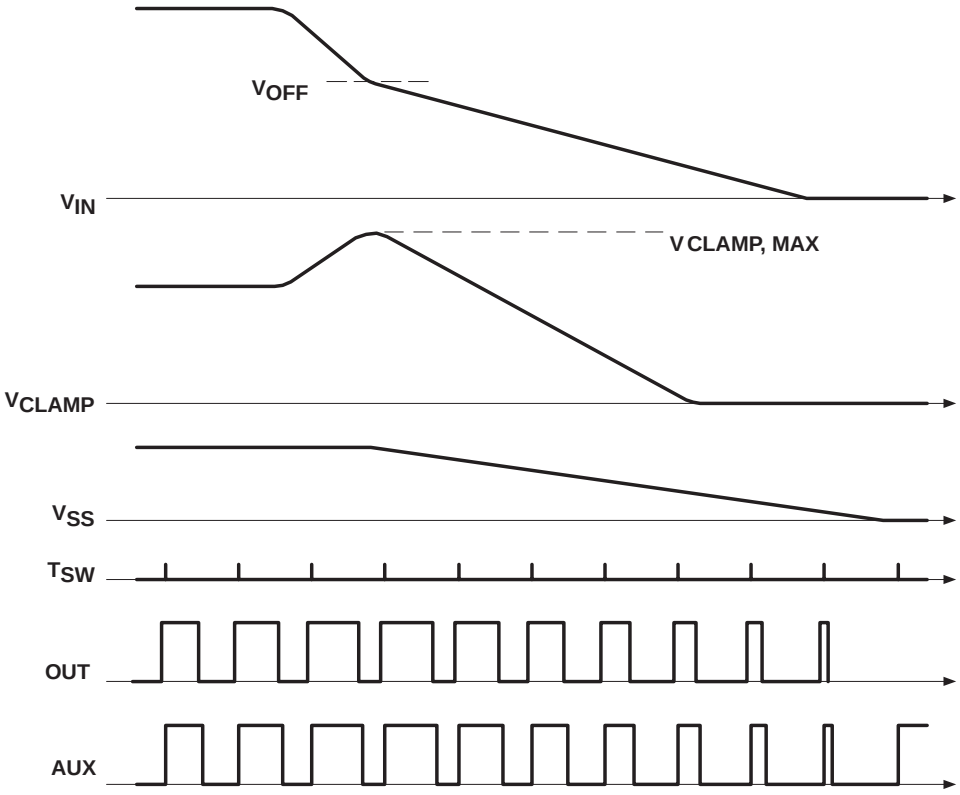


Figure 3. Line Undervoltage Shutdown Waveforms, P−Channel

To eliminate this potential hazard the UCC2897A controller safely discharge the clamp capacitor during power down. The OUT and the AUX output continues switching while the soft-start capacitor C_{SS} is being slowly discharged. Notice that the AUX pulse width gradually increases as the clamp voltage decreases never applying the high voltage across the transformer for extended period of time. From this, the function of soft stop is achieved.

Line Overvoltage Protection

When the line overvoltage protection is triggered in the UCC2897A controller, the gate drive signals are immediately disabled. At the same time, the slow discharge of C_{SS} is initiated. While the soft-start capacitor is discharging the gate drive signals remains disabled. Once V_{SS} = 0.5 V and the overvoltage disappears from the input of the power supply, operation resumes through a regular soft-start of the converter as it is demonstrated in Figure 4. The pulses of OUT and AUX stop if one of three conditions is met:

1. VDD reaches UVLO off,
2. VSS reaches below 2.5 V,
3. or FB voltage is below 2.5 V.

FUNCTIONAL DESCRIPTION

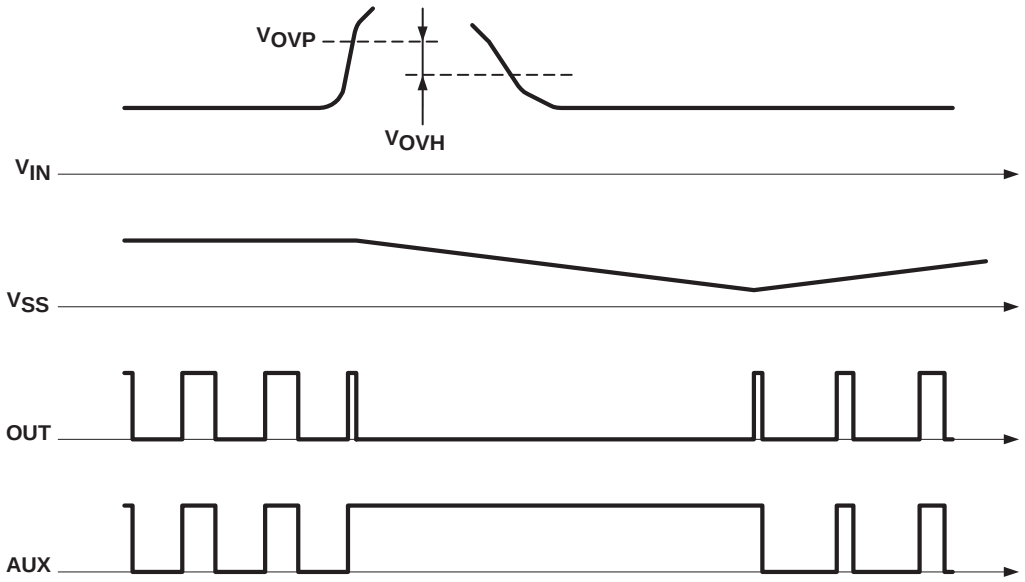


Figure 4. Line Overvoltage Sequence, P−Channel

Pulse Skipping

During output load current transients or light load conditions most PWM controllers needs to be able to skip some number of PWM pulses. In an active clamp topology where the clamp switch is driven complementarily to the main switch, this would apply the clamp voltage across the transformer continuously. Since operating conditions might require skipping several switching cycles on the main transistor, saturating the transformer is very likely if the AUX output stays on.

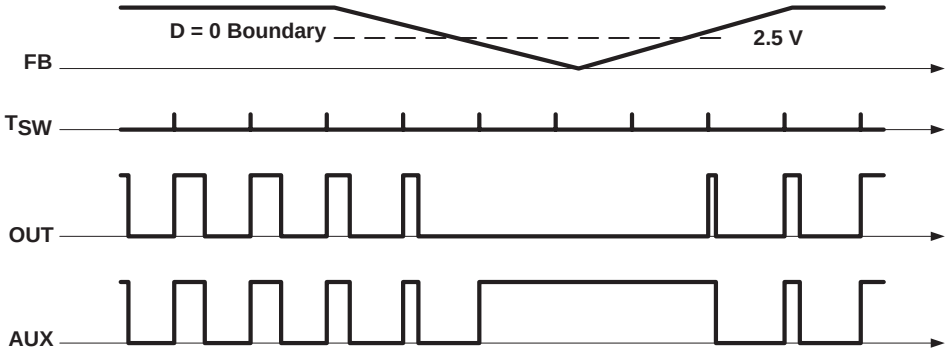


Figure 5. Pulse Skipping Operation, P−Channel

To overcome this problem, the UCC2897A family incorporates pulse skipping for both outputs in the controller. As can be seen above, when a pulse is skipped at the main output (OUT) because the feedback signal demands zero duty ratio, the corresponding output pulse on the AUX output is omitted as well. This operation allows to prevent reverse saturation of the power transformer and to preserve the clamp capacitor voltage level during pulse skipping operation.

FUNCTIONAL DESCRIPTION

Synchronization

The UCC2897A has a bi-directional synchronization pin. In the stand-alone operation the SYNC pin is driven by the internal oscillator of the UCC2897A which provides an approximately 5-V amplitude square wave output. This signal can be used to synchronize other PWM controllers or circuits needing a constant frequency time base. The synchronization output of the UCC2897A is generated when the internal timing capacitor reaches its peak value. Therefore, the synchronization waveform does not coincide with the turn on of the main gate driver output as it is usually implemented in PWM controllers.

The operation of the oscillator and relevant other waveforms in free running and synchronized mode are shown in Figure 6.

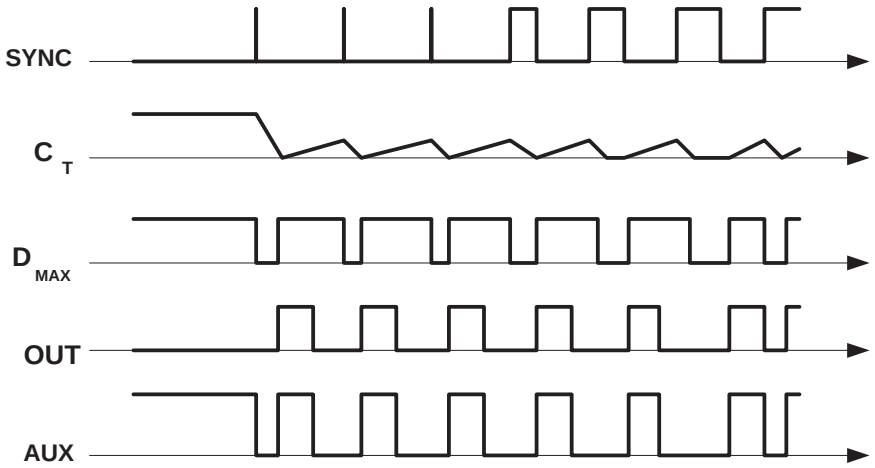


Figure 6. ASynchronization Waveform for SYNC Input, P−Channel

The most critical and unique feature of the oscillator is to limit the maximum operating duty cycle of the converter. It is achieved by accurately controlling the charge and discharge intervals of the on board timing capacitor. The maximum on-time of OUT pin, which is also the maximum duty cycle of the active clamp converter is limited by the charging interval of the timing capacitor. While the capacitor is being reset to its initial voltage level OUT is guaranteed to be off.

When synchronization is used, the rising edge of the signal terminates the charging period and initiate the discharge of the timing capacitor. Once the timing capacitor voltage reaches the predefined valley voltage, a new charge period starts automatically. This method of synchronization leaves the charge and discharge slopes of the timing waveform unaffected thus maintains the maximum duty cycle of the converter, independent of the mode of operation.

Although the synchronization circuit is level sensitive, the actual synchronization event occurs at the rising edge of the waveform. This allows the synchronizing pulse width to vary significantly but certain limitations must be observed. The minimum pulse width should be sufficient to guarantee reliable triggering of the internal oscillator circuitry, therefore it should be greater than approximately 50 nanoseconds. The other limiting factor is to keep it shorter than $\left(1 - D_{MAX}\right) \times T_{SYNC}$ where T_{SYNC} is the period of the synchronization frequency.

FUNCTIONAL DESCRIPTION

When a wider than $\left(1 - D_{MAX}\right) \times T_{SYNC}$ pulse is connected to the SYNC input, the oscillator is not able to maintain the maximum duty cycle, originally set by the timing resistor ratio (R_{ON}, R_{OFF}). Furthermore, the timing capacitor waveform has a flat portion as highlighted by the vertical marker in the timing diagram. During this flat portion of the waveform both outputs is off which state is not compatible with the operation of active clamp power converters. Therefore, this operating mode is not recommended .

Note that both outputs of the UCC2897A controller are off if the synchronization signal stays continuously high.

When two UCC2897A's are synchronized by tying their SYNC pins together, they will operate in−phase. It is possible to set different maximum duty cycle limits for the two UCC2897's and still synchronize them by a simple connection between their respective SYNC terminals.

APPLICATION INFORMATION: SETUP GUIDE

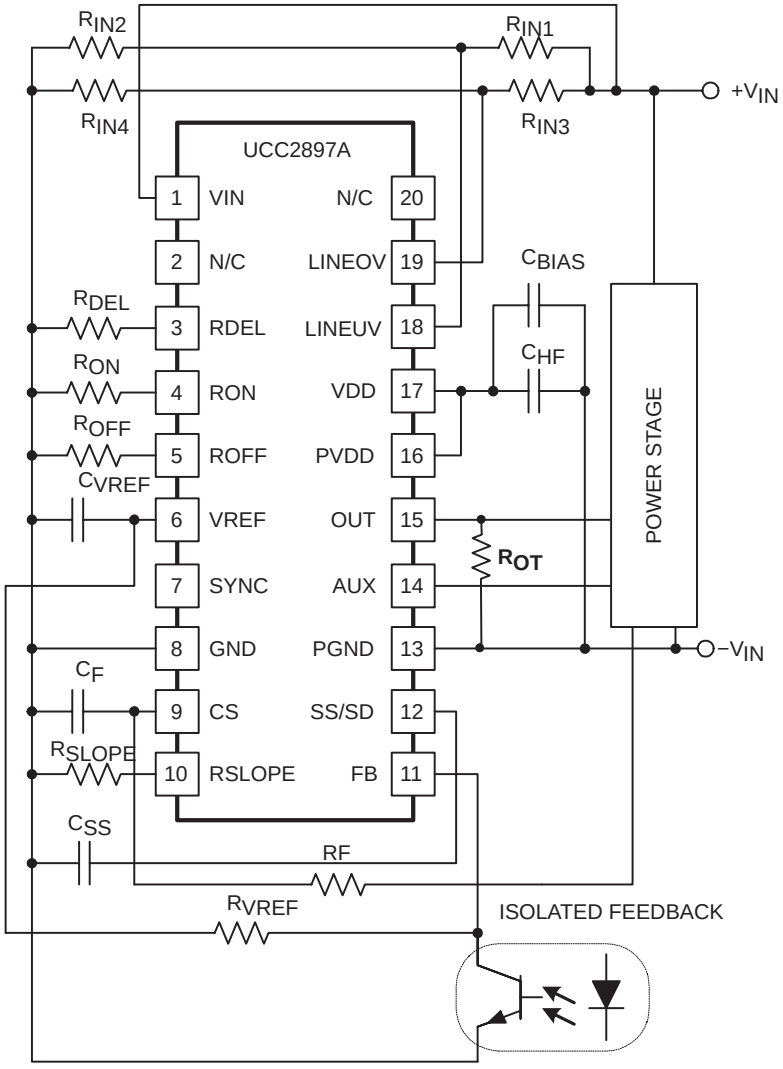


Figure 7. UCC2897A Typical Setup

APPLICATION INFORMATION: SETUP GUIDE

The UCC2897A family offers a highly integrated feature set and excellent accuracy to control an active clamp forward or active clamp flyback power converter. In order to take advantage of all the benefits integrated in these controllers, the following procedure can simplify the setup and avoid unnecessary iterations in the design procedure. Refer to Figure 7 setup diagrams for component names.

Before the controller design begins, the power stage design must be completed. From the power stage design the following operating parameters are needed to complete the setup procedure of the controller:

- Switching frequency (f_{SW})
- Maximum operating duty cycle (D_{MAX})
- Soft start duration (t_{SS})
- Gate drive power requirements of the external power MOSFETs ($Q_{G(main)}$, $Q_{G(aux)}$)
- Bias method and voltage for steady state operation (bootstrap or bias supply)
- Gate drive turn-on delay (t_{DEL})
- Turn−on input voltage threshold (V_{ON})
- Minimum operating input voltage (V_{OFF}) where $V_{IN\ (off)} < V_{IN(on)}$
- Maximum operating input voltage (V_{OVP})
- overvoltage protection hysteresis (V_{OVH})
- The down slope of the output inductor current waveform reflected across the primary side current sense resistor $\left(dV_L/dt\right)$

Step 1. Oscillator

The two timing elements of the oscillator can be calculated from f_{SW} and D_{MAX} by the following two equations:

$$R_{ON} = \frac{t_{ON}}{37.33 \times 10^{-12}} \times \left(\frac{\Omega}{s}\right) = \frac{D_{MAX}}{f_{SW} \times 37.33 \times 10^{-12}} \times \left(\frac{\Omega}{s}\right) \quad (9)$$

$$R_{OFF} = \frac{t_{OFF}}{16 \times 10^{-12}} \times \left(\frac{\Omega}{s}\right) = \frac{1 - D_{MAX}}{f_{SW} \times 16 \times 10^{-12}} \times \left(\frac{\Omega}{s}\right) \quad (10)$$

where D_{MAX} is a dimensionless number between 0 and 1.

Step 2. Soft Start

Once R_{ON} is defined, the charge current of the soft-start capacitor can be calculated as:

$$I_{SS} = 0.43 \times \frac{V_{REF}}{2} \times \frac{1}{R_{ON}} \quad (11)$$

During soft start, C_{SS} is being charged from 0 V to 5 V by the calculated I_{SS} current. The actual control range of the soft-start capacitor voltage is between 2.5 V and 4.5 V. Therefore, the soft-start capacitor value must be based on this narrower control range and the required start up time (t_{SS}) according to:

$$C_{SS} = \frac{I_{SS} \times t_{SS}}{4.5\ V - 2.5\ V} \quad (12)$$

APPLICATION INFORMATION: SETUP GUIDE

Note, that t_{SS} defines a time interval to reach the maximum current capability of the converter and not the time required to ramp the output voltage from 0 V to its nominal, regulated level. Using an open-loop start up scheme does not allow accurate control over the ramp up time of the output voltage. In addition to the I_{SS} and C_{SS} values, the time required to reach the nominal output voltage of the converter is a function of the maximum output current (current limit), the output capacitance of the converter and the actual load conditions. If it is critical to implement a tightly controlled ramp-up time at the output of the converter, the soft-start must be implemented using a closed loop technique. Closed loop soft-start can be implemented with the error amplifier of the voltage regulation loop when its voltage reference is ramped from 0 V to its final steady state value during the required t_{SS} start up time interval.

Step 3. VDD Bypass Requirements

First, the high-frequency filter capacitor is calculated based on the gate charge parameters of the external MOSFETs. Assuming that the basic switching frequency ripple should be kept below 0.1-V across C_{HF}, its value can be approximated as:

$$C_{HF} = \frac{Q_{G(main)} + Q_{G(aux)}}{0.1\ V} \tag{13}$$

The energy storage requirements are defined primarily by the start up time (t_{SS}) and turn-on (approximately 12.7 V) and turn-off (approximately 8 V) thresholds of the controller's undervoltage lockout circuit monitoring the VDD pin. In addition, the bias current consumption of the entire primary side control circuit ($I_{DD} + I_{EXT}$) must be known. This power consumption can be estimated as:

$$P_{BIAS} = \left[I_{DD} + I_{EXT} + \left(Q_{G(main)} + Q_{G(aux)} \times f_{SW}\right)\right] \times V_{DD} \tag{14}$$

During start up (t_{SS}) this power is provided by C_{BIAS} while its voltage must remain above the UVLO turn-off threshold. This relationship can be expressed as:

$$P_{BIAS} \times t_{SS} < \frac{1}{2} \times C_{BIAS} \times \left(12.7^2 - 8^2\right) \tag{15}$$

Rearranging the equation yields the minimum value for C_{BIAS}:

$$C_{BIAS} > \frac{2 \times P_{BIAS} \times t_{SS}}{\left(12.7^2 - 8^2\right)} \tag{16}$$

Equation 17 may yeild a big capacitance value that may not be feasible in some applications. In such cases, an additional energy storage circuit. A smaller footprint may be designed to ease the space demand. Refer to the Application Note for such a design.

Step 4. Delay Programming

From the power stage design, the required turn-on delay (t_{DEL}) of the gate drive signals is defined. The corresponding R_{DEL} resistor value to implement this delay is given by:

$$R_{DEL} = t_{DEL1} \times 0.91 \times 10^{11} \times \left(\frac{\Omega}{s}\right) \tag{17}$$

or

$$R_{DEL} = t_{DEL2} \times 0.91 \times 10^{11} \times \left(\frac{\Omega}{s}\right) \tag{18}$$

APPLICATION INFORMATION: SETUP GUIDE

Step 5. Input Voltage Monitoring

The input voltage monitoring functions is governed by the following two expressions of the voltage at the LINEUV pin:

$$V_{LINEUV} = V_{ON} \times \frac{R_{IN2}}{R_{IN1} + R_{IN2}} \text{ at turn on, and} \quad (19)$$

$$V_{LINEUV} = V_{OFF} \times \frac{R_{IN2}}{R_{IN1} + R_{IN2}} + I_{HYST} \times \frac{R_{IN1} \times R_{IN2}}{R_{IN1} + R_{IN2}} \text{ at turn off.} \quad (20)$$

Since V_{ON} and V_{OFF} are given by the power supply specification, V_{LINEUV} equals the 1.27-V threshold of the line monitor and I_{HYST} is already defined as:

$$I_{HYST} = \frac{V_{REF}}{2} \times \frac{1}{R_{DEL}} \times 0.05 \quad (21)$$

the two unknown, R_{IN1} and R_{IN2} are fully determined.

$$R_{IN1} = \frac{V_{ON} - V_{OFF}}{I_{HYST}} \quad (22)$$

$$R_{IN2} = \frac{1.27V}{V_{ON} - 1.27V} \times R_{IN1} \quad (23)$$

Step 6. Current Sense and Slope Compensation

The UCC2897A offers onboard, user programmable slope compensation. The programming of the right amount of slope compensation is accomplished by the appropriate selection of two external resistors, R_F and R_{SLOPE}.

First, the current sense filter resistor value (R_F) must be calculated based on the desired filtering of the current sense signal. The filter consists of two components, C_F and R_F. The C_F filter capacitor is connected between the CS pin and the GND pin. While the value of C_F can be freely selected as the first step of the filter design, it should be minimized to avoid filtering the slope compensation current exiting the CS pin. The recommended range for the filter capacitance is between 50 pF and 270 pF. The value of the filter resistor can be calculated from the filter capacitance and the desired filter corner frequency f_F.

$$R_F = \frac{1}{2\pi \times f_F \times C_F} \quad (24)$$

After R_F is defined R_{SLOPE} can be calculated. The amount of slope compensation is defined by the stability requirements of the inner peak current loop of the control algorithm and is measured by the number m. When the slope of the applied compensation ramp equals the down slope of the output inductor current waveform reflected across the primary side current sense resistor $\left(dV_L/dt\right)$, *m* equals 1. The minimum value of *m* is 0.5 to prevent current loop instability. Best current mode performance can be achieved around *m*=1. The further increase of *m* moves the control closer to voltage mode control operation.

APPLICATION INFORMATION: SETUP GUIDE

In the UCC2897A controllers, slope compensation is implemented by sourcing a linearly increasing current at the CS pin. When this current passes through the current sense filter resistor (R_F), it is converted to a slope compensation ramp which can be characterized by its $\left(dV_S/dt\right)$. The $\left(dV_S/dt\right)$ of the slope compensation current is defined by R_{SLOPE} according to:

$$\frac{dI_S}{dt} = \frac{5 \times 2\ V}{t_{ON} \times R_{SLOPE}} \tag{25}$$

where

- 2V is the peak−to−peak ramp amplitude of the internal oscillator waveform
- 5 is the multiplication factor of the internal current mirror

The voltage equivalent of the compensation ramp $\left(dV_S/dt\right)$ can be easily obtained by multiplying with R_F. After introducing the application specific *m* and $\left(dV_L/dt\right)$ values, the equation can be rearranged for R_{SLOPE}:

$$R_{SLOPE} = \frac{5 \times 2\ V \times R_F}{t_{ON} \times m \times \left(\frac{dV_L}{dt}\right)} \tag{26}$$

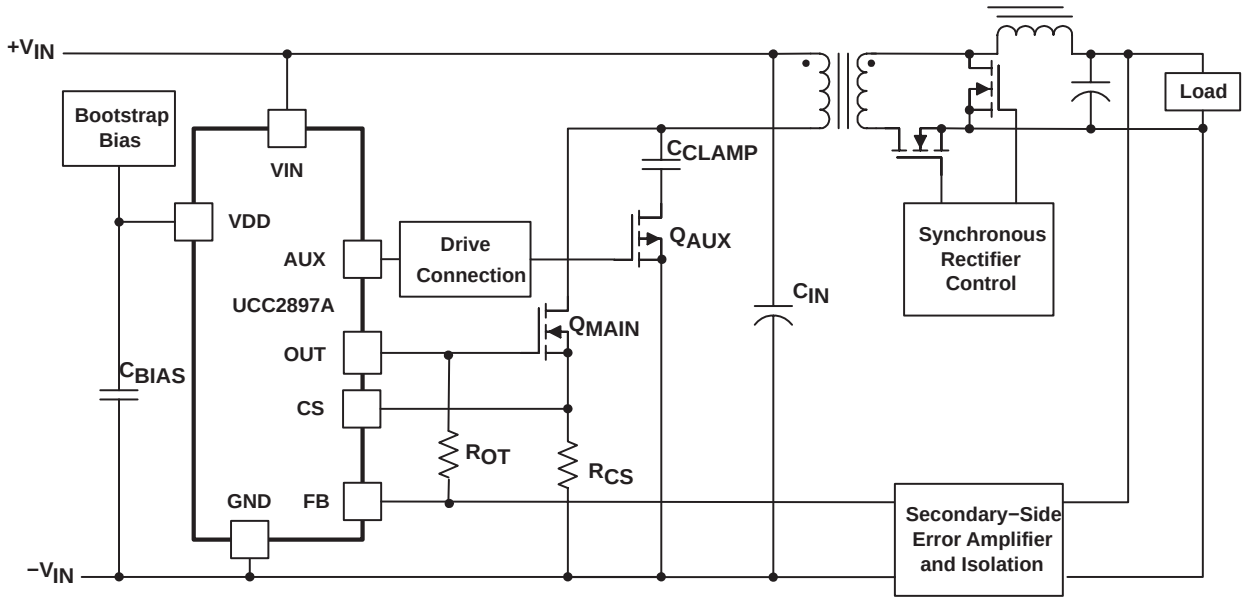


Figure 8. Active Clamp Forward Converter

ADDITIONAL APPLICATION INFORMATION

Gate Drive Connection

The low side P-channel gate drive circuit involves a level shifter using a capacitor and a diode which ensures that the gate drive amplitude of the auxiliary switch is independent of the actual duty cycle of the converter.

Detailed analysis and design examples of these and many similar gate drive solutions are given in reference [6].

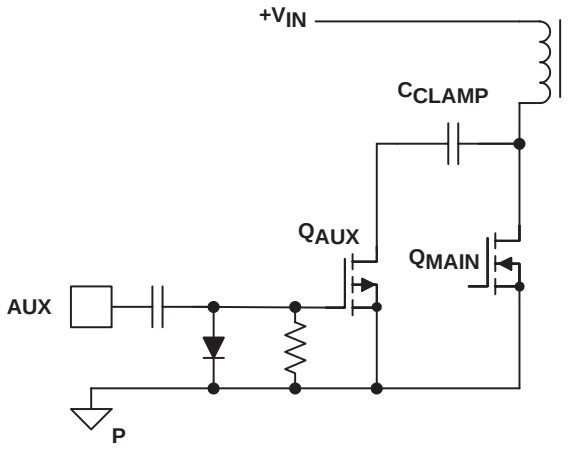


Figure 9. Low-Side P-Channel

Bootstrap Biasing

Many converters use a bootstrap circuit to generate its own bias power during steady state operation. The popularity of this solutions is justified by the simplicity and high efficiency of the circuit. Usually, bias power is derived from the main transformer by adding a dedicated, additional winding to the structure. Using a flyback converter as shown in Figure 10, a bootstrap winding provides a quasi-regulated bias voltage for the primary side control circuits. The voltage on the VDD pin is equal to the output voltage times the turns ratio between the output and the bootstrap windings in the transformer. Since the output is regulated, the bias rail is regulated as well.

ADDITIONAL APPLICATION INFORMATION

While the same arrangement can be used in a forward type converter, the bootstrap winding off the main power transformer would not be able to provide a quasi-regulated voltage. In the forward converter, the voltage across the bootstrap winding equals the input voltage times the turns ratio. Accordingly the bias voltage would vary with the input voltage and most likely would exceed the maximum operating voltage of the control circuits at high line. A linear regulator can be used to limit and regulate the bias voltage if the power dissipation is acceptable. Another possible solution for the forward converter is to generate the bias voltage from the output inductor as shown in Figure 11.

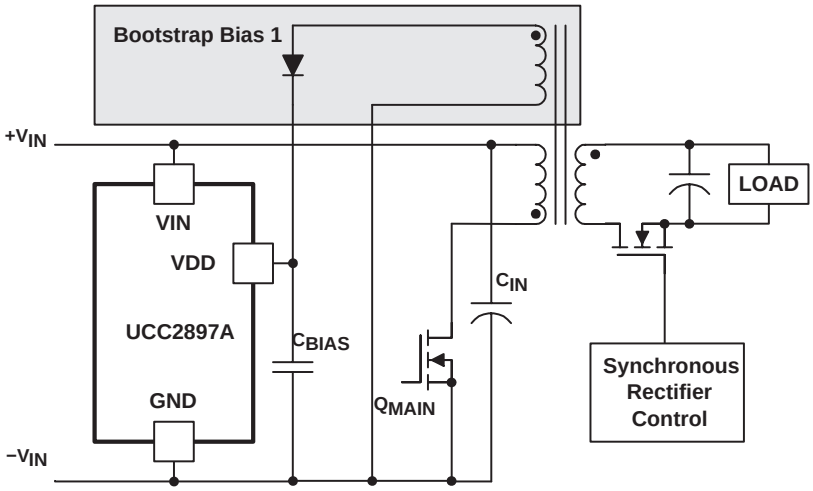


Figure 10. Bootstrap Bias 1, Flyback Example

This solution uses the regulated output voltage across the output inductor during the freewheeling period to generate a quasi-regulated bias for the control circuits.

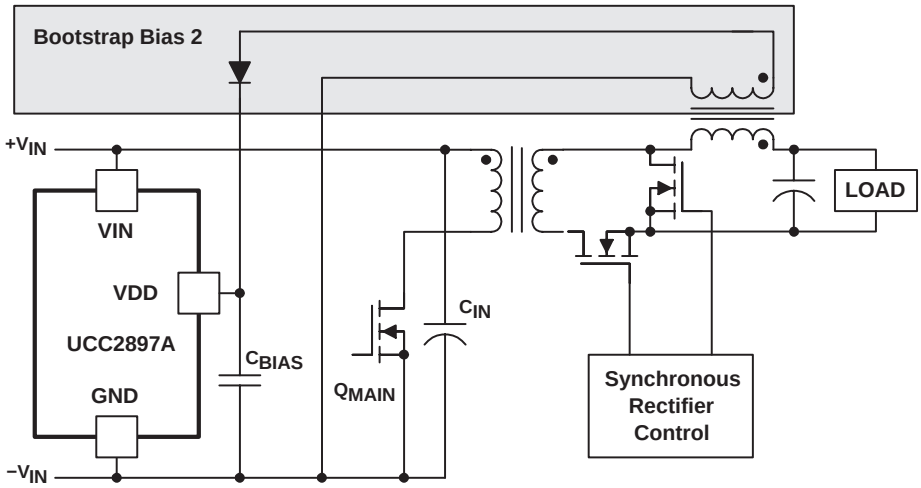


Figure 11. Bootstrap Bias 2, Forward Example

ADDITIONAL APPLICATION INFORMATION

This solution uses the regulated output voltage across the output inductor during the freewheeling period to generate a quasi-regulated bias for the control circuits.

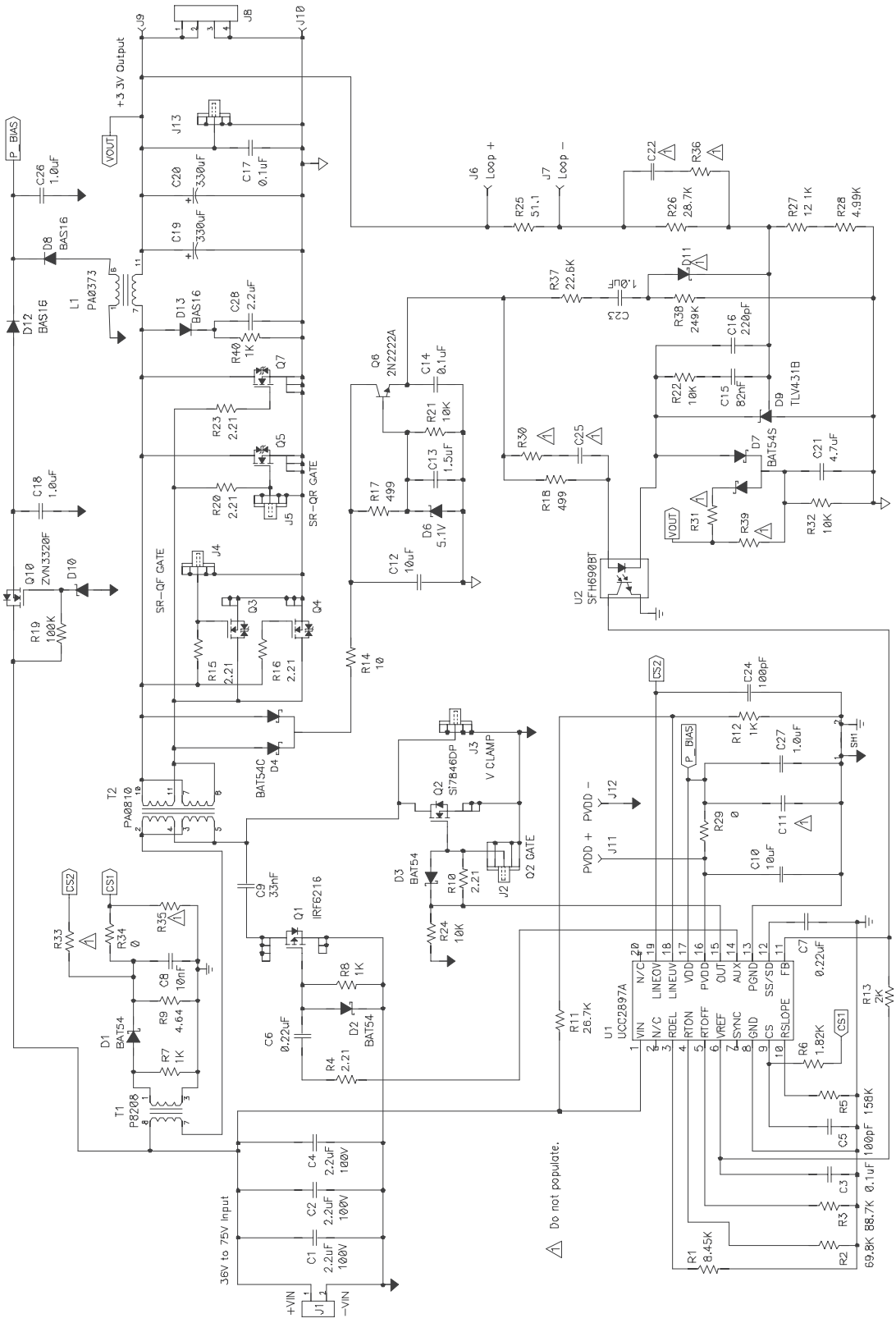
Both of the illustrated solution provides reliable bias power during normal operation. Note that in both cases, the bias voltages are proportional to the output voltage. This nature of the bootstrap bias supply causes the converter to operate in a hiccup mode under significant overload or under short-circuit conditions as the bootstrap winding is not able to hold the bias rail above the undervoltage lockout threshold of the controller.

Another biasing solution, based on the active circuit shown on the previous page with components Q10, C18, R19, D10 and D12. Such a circuit may be used in the applications where the allowed biasing capacitor size is limited to optimize the board spaceutilization.

References and Additional Development Tools

1. Evaluation Module: UCC2891EVM, 48-V to 3.3-V, 30-A Forward Converter with Active Clamp Reset.
2. User's Guide: Using the UCC2891EVM, 48-V to 3.3-V, 30-A Forward Converter with Active Clamp Reset, (SLUU178)
3. Application Note: Designing for High Efficiency with the UCC2891 Active Clamp PWM Controller, Steve Mappus (SLUA303)
4. Power Supply Design Seminar Topic: Design Considerations for Active Clamp and Reset Technique, D. Dalal, SEM1100−Topic3 (SLUP112)
5. Power Supply Design Seminar Topic: Active Clamp and Reset Technique Enhances Forward Converter Performance, B. Andreycak, SEM1000−Topic 3. (SLUP108)
6. Power Supply Design Seminar Topic: Design and Application Guide for High Speed MOSFET Gate Drive Circuits, L. Balogh, SEM1400−Topic 2 (SLUP169)
7. Datasheet: UCC3580, Single Ended Active-Clamp/Reset PWM Controller, (SLUS292)
8. Evaluation Module: UCC3580EVM, Flyback Converters, Active Clamp vs. Hard−Switched.
9. Reference Designs: Highly Efficient 100W Isolated Power Supply Reference Design Using UCC3580−1. Texas Instruments Hardware Reference Design Number PMP206.
10. Reference Designs: Active Clamp Forward Reference Design using UCC3580−1. Texas Instruments Hardware Reference Design Number PMP368

ADDITIONAL APPLICATION INFORMATION



TYPICAL CHARACTERISTICS

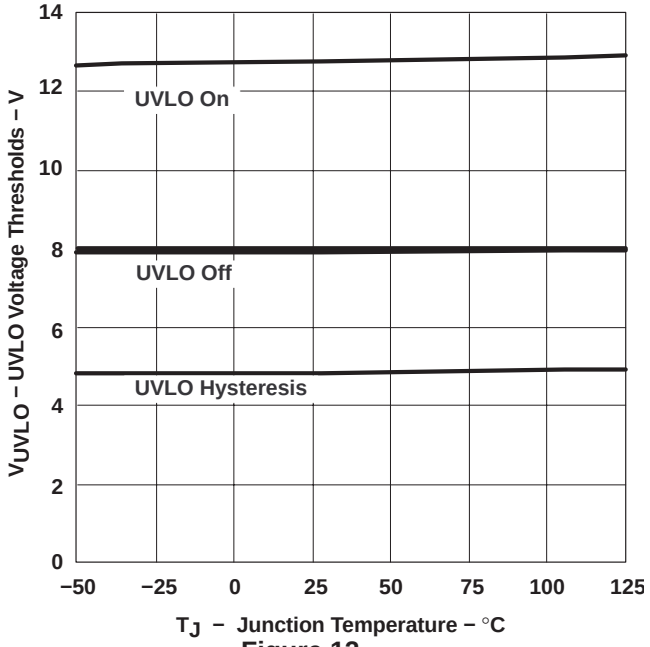


Figure 12

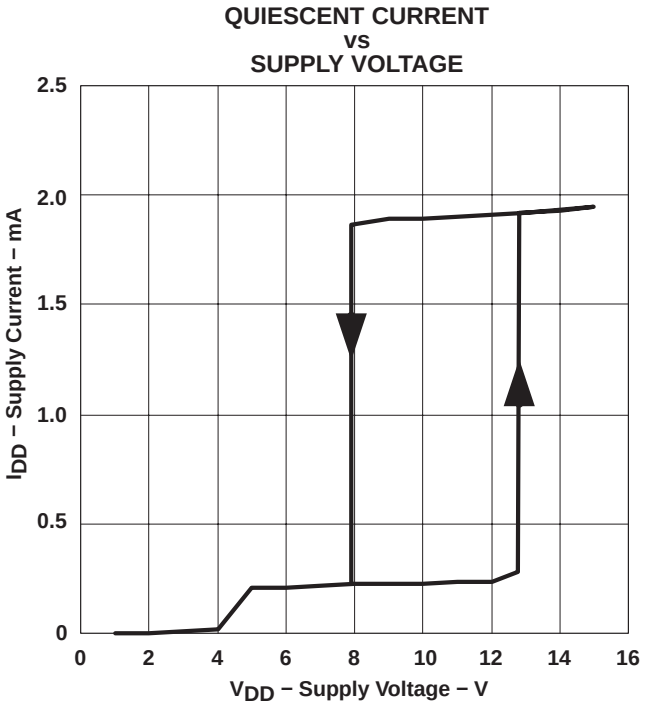


Figure 13

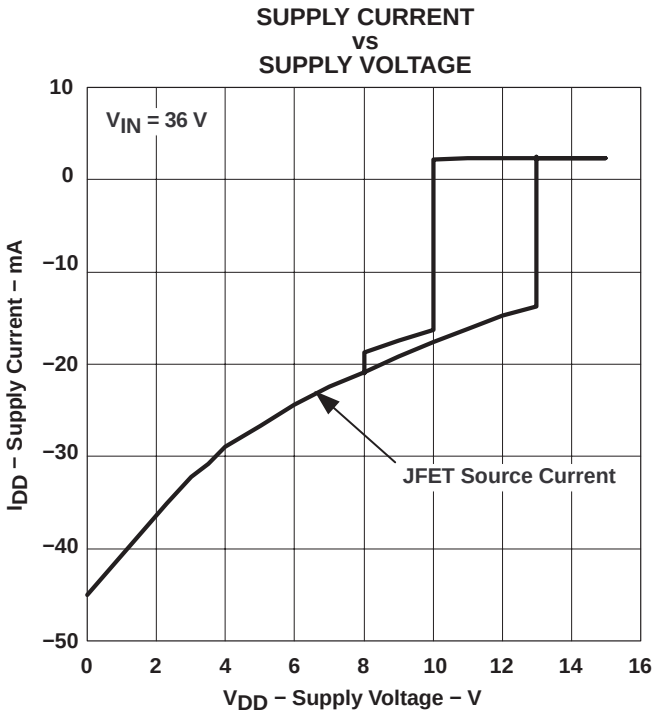


Figure 14

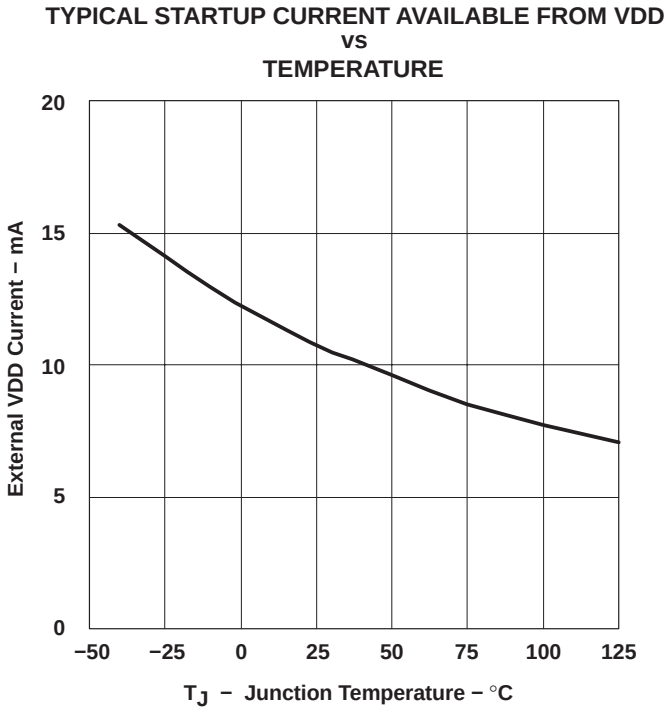


Figure 15

TYPICAL CHARACTERISTICS

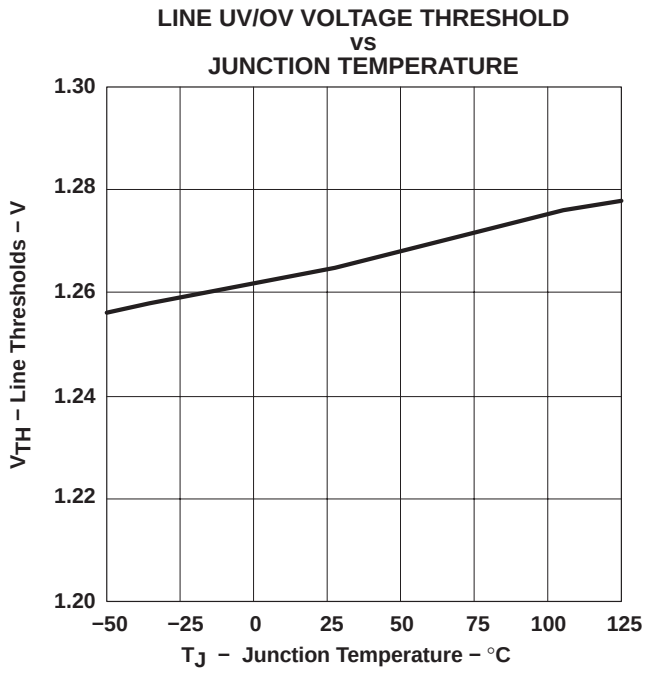


Figure 16

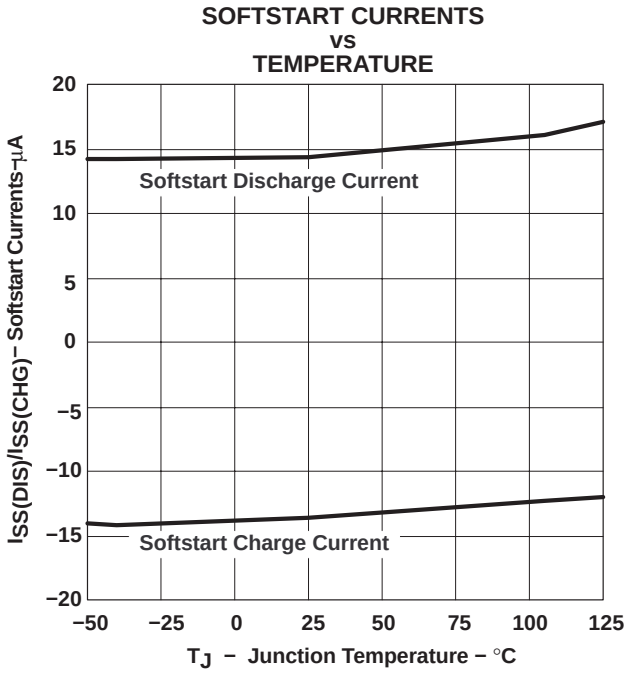


Figure 17

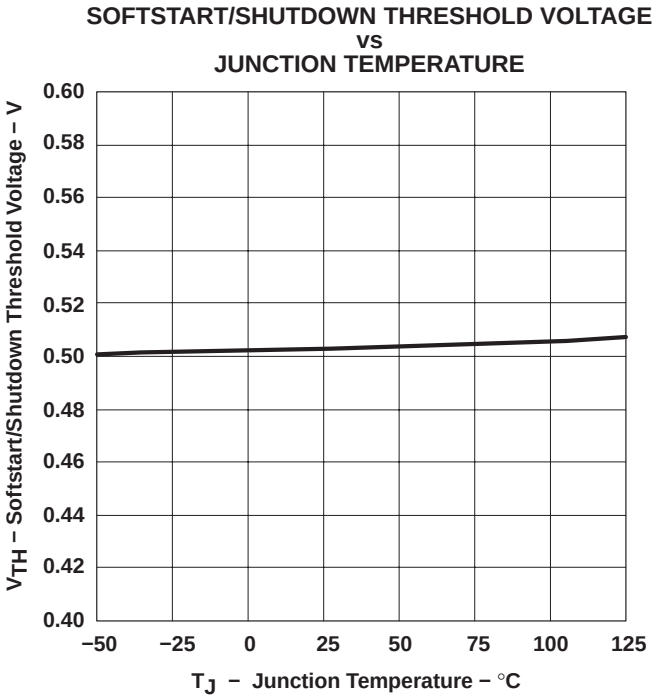


Figure 18

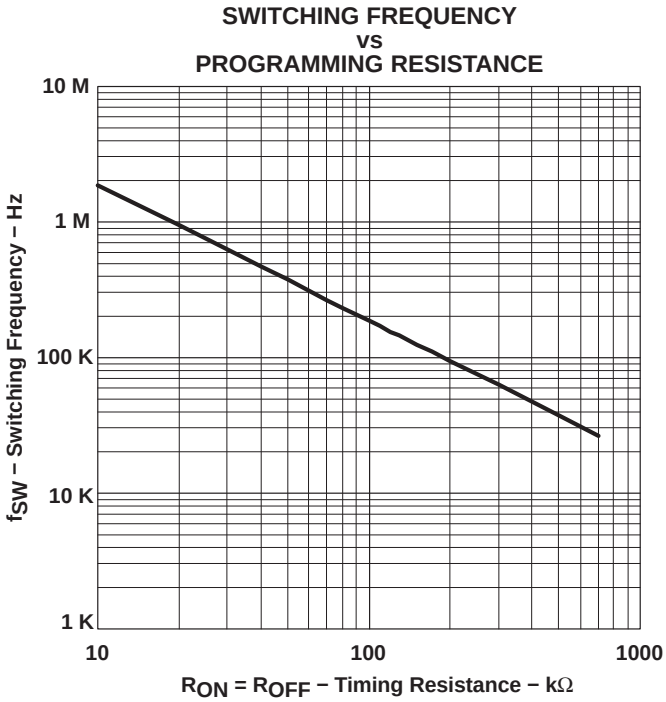


Figure 19

TYPICAL CHARACTERISTICS

OSCILLATOR FREQUENCY
vs
JUNCTION TEMPERATURE

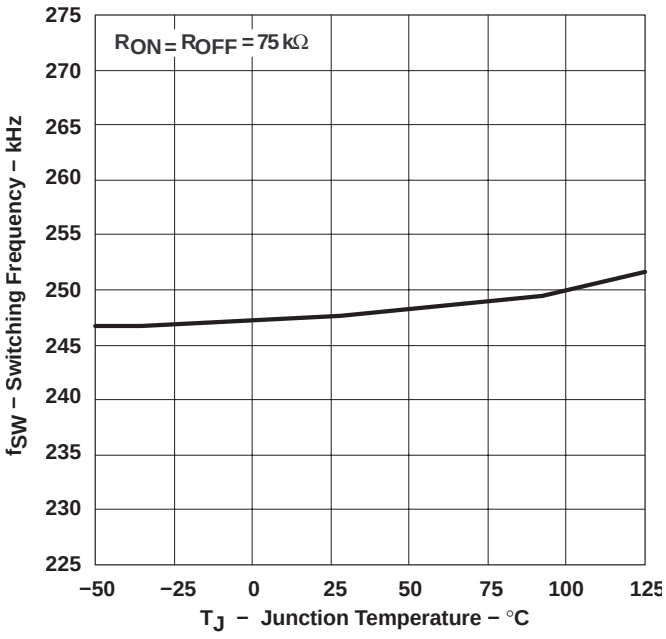


Figure 20

MAXIMUM DUTY CYCLE
vs
JUNCTION TEMPERATURE

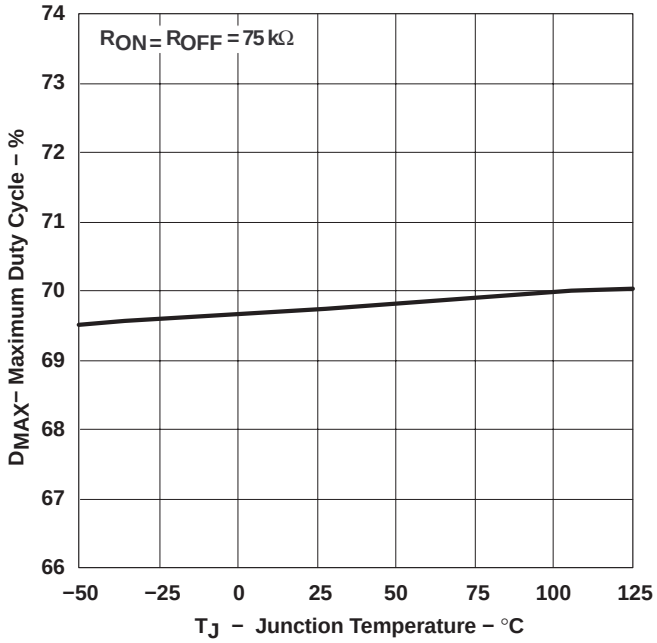


Figure 21

CURRENT SENSE THRESHOLD VOLTAGE
vs
JUNCTION TEMPERATURE

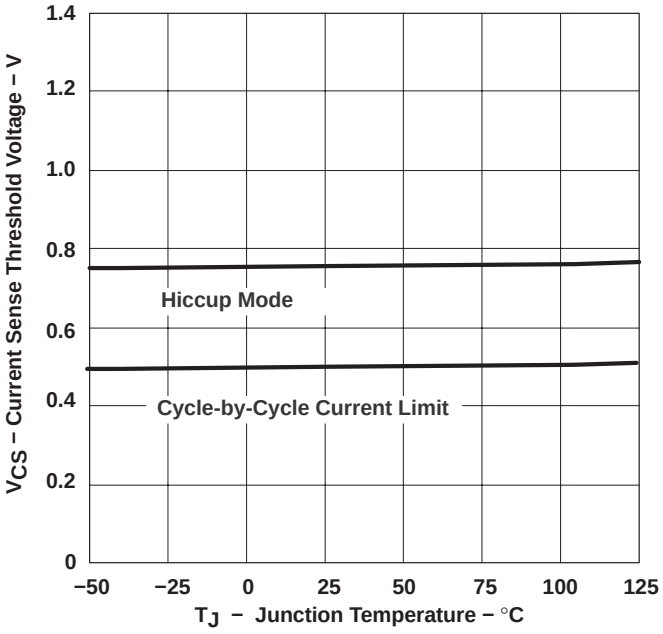


Figure 22

SYNCHRONIZATION THRESHOLD VOLTAGE
vs
JUNCTION TEMPERATURE

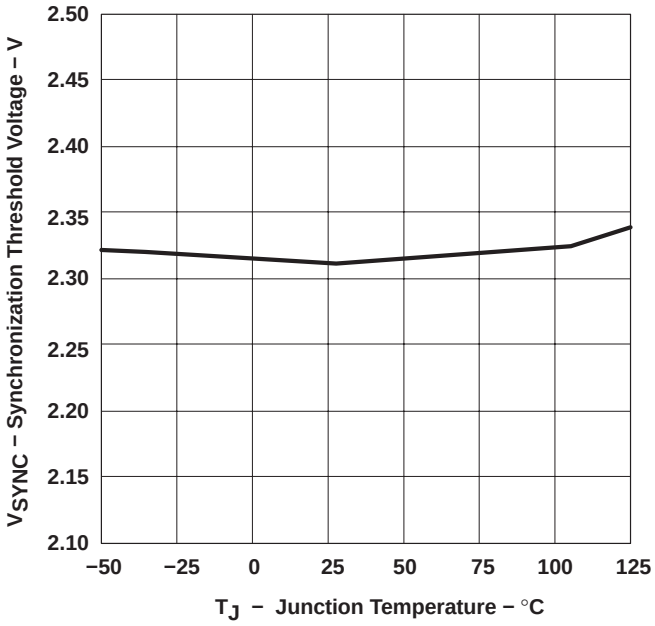


Figure 23

TYPICAL CHARACTERISTICS

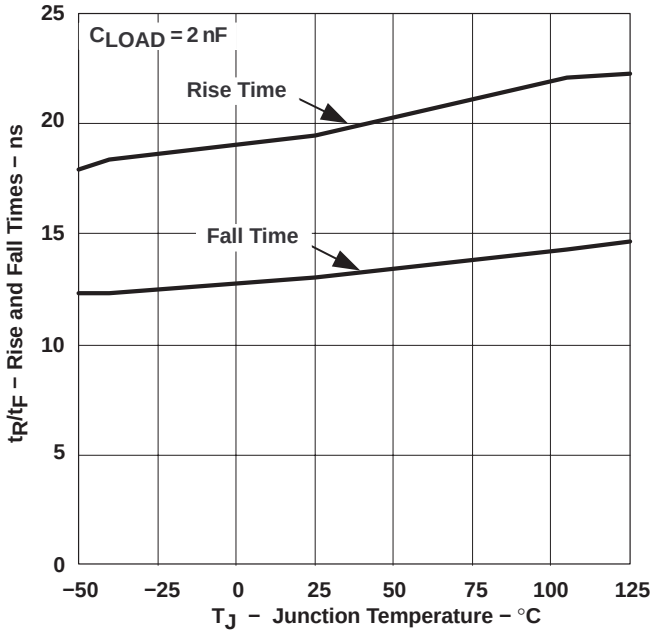


Figure 24

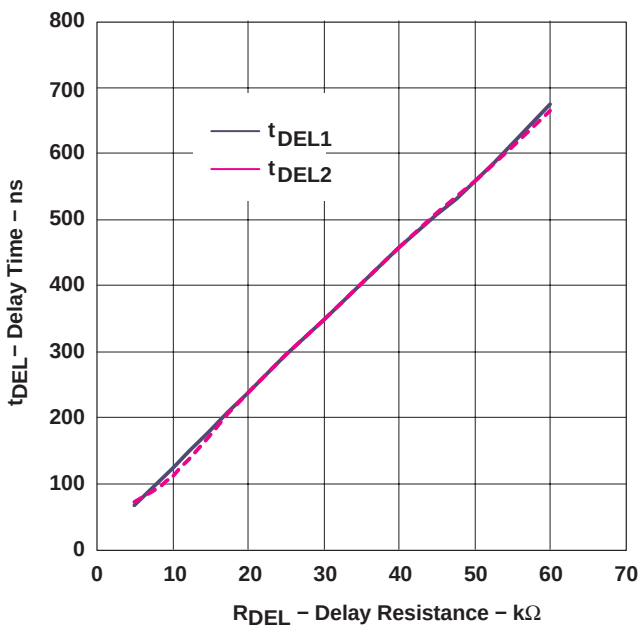


Figure 25

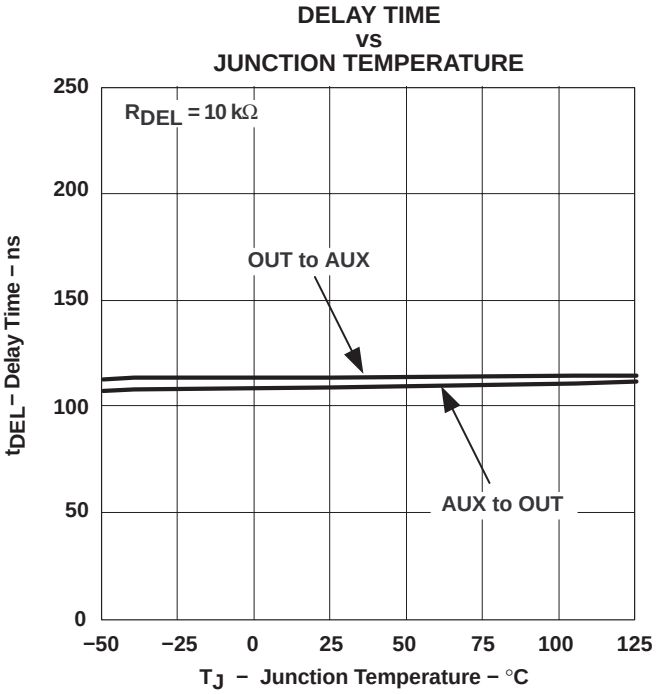


Figure 26

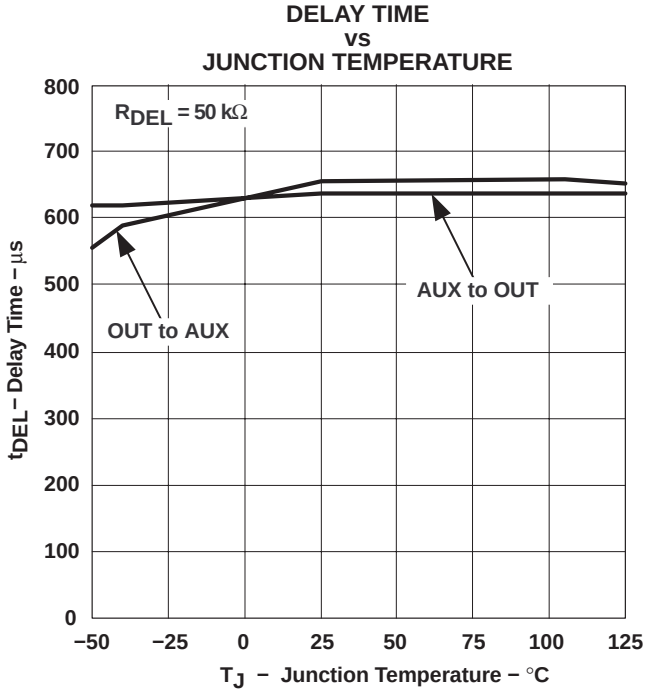


Figure 27

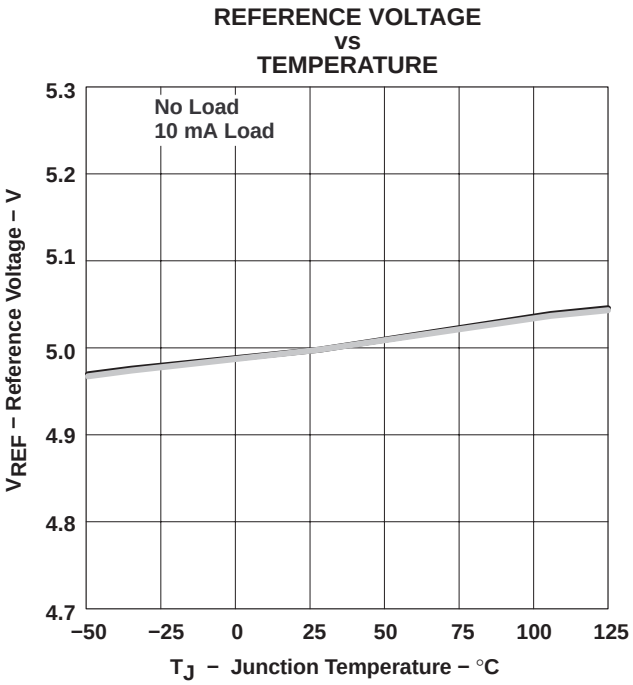


Figure 28

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)
UCC2897APW	ACTIVE	TSSOP	PW	20	70	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
UCC2897APWR	ACTIVE	TSSOP	PW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
UCC2897ARGPR	ACTIVE	QFN	RGP	20	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
UCC2897ARGPT	ACTIVE	QFN	RGP	20	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR

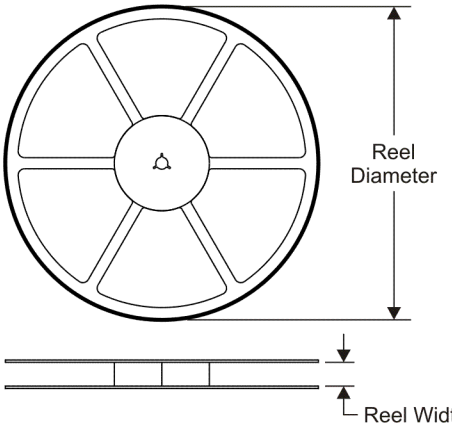
(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

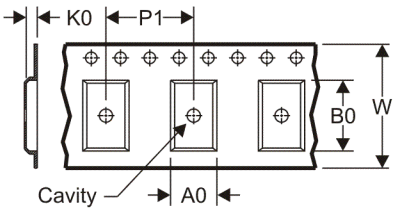
(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

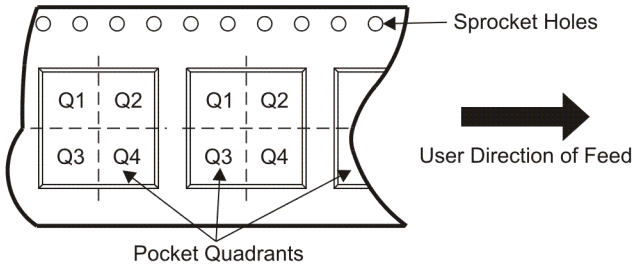


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

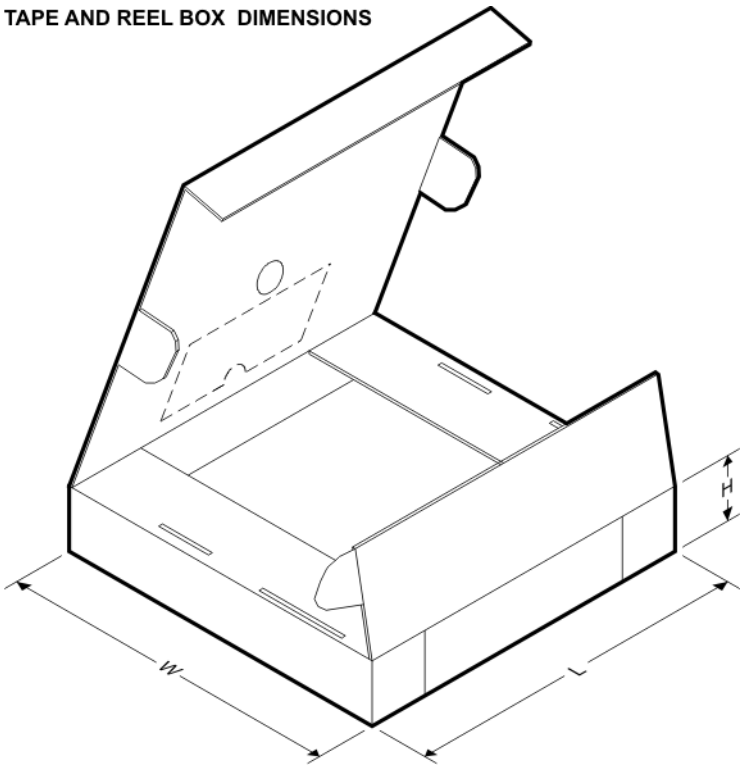
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
UCC2897APWR	TSSOP	PW	20	2000	330.0	16.4	6.95	7.1	1.6	8.0	16.0	Q1
UCC2897ARGPR	QFN	RGP	20	3000	330.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2
UCC2897ARGPT	QFN	RGP	20	250	180.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2

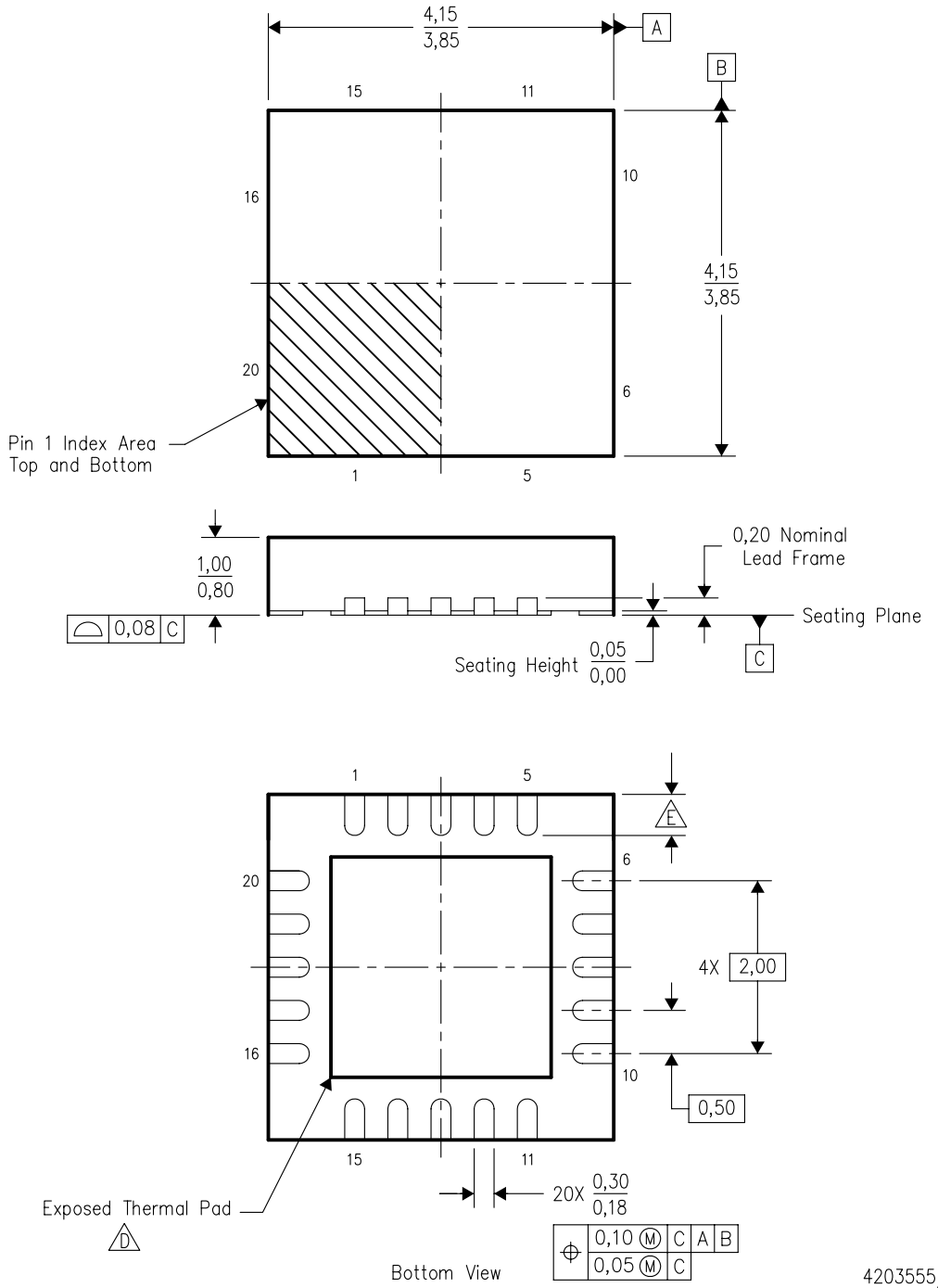
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
UCC2897APWR	TSSOP	PW	20	2000	346.0	346.0	33.0
UCC2897ARGPR	QFN	RGP	20	3000	346.0	346.0	29.0
UCC2897ARGPT	QFN	RGP	20	250	190.5	212.7	31.8

RGP (S–PQFP–N20) PLASTIC QUAD FLATPACK



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. QFN (Quad Flatpack No–Lead) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance. See the Product Data Sheet for details regarding the exposed thermal pad dimensions.
E. Check thermal pad mechanical drawing in the product datasheet for nominal lead length dimensions.

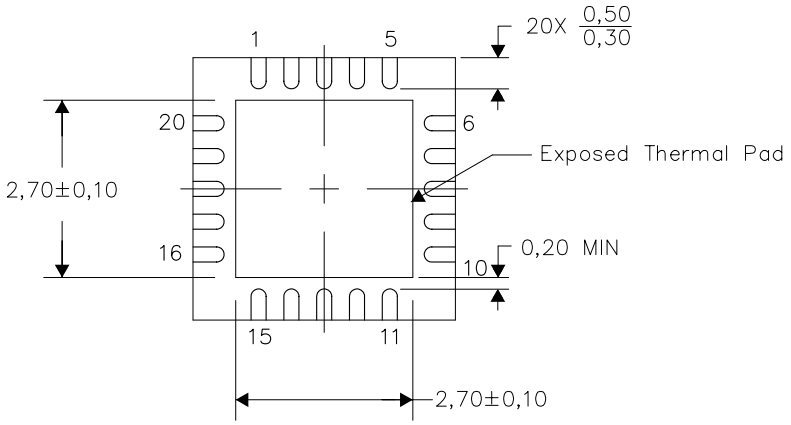
RGP (S–PVQFN–N20) PLASTIC QUAD FLATPACK NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.

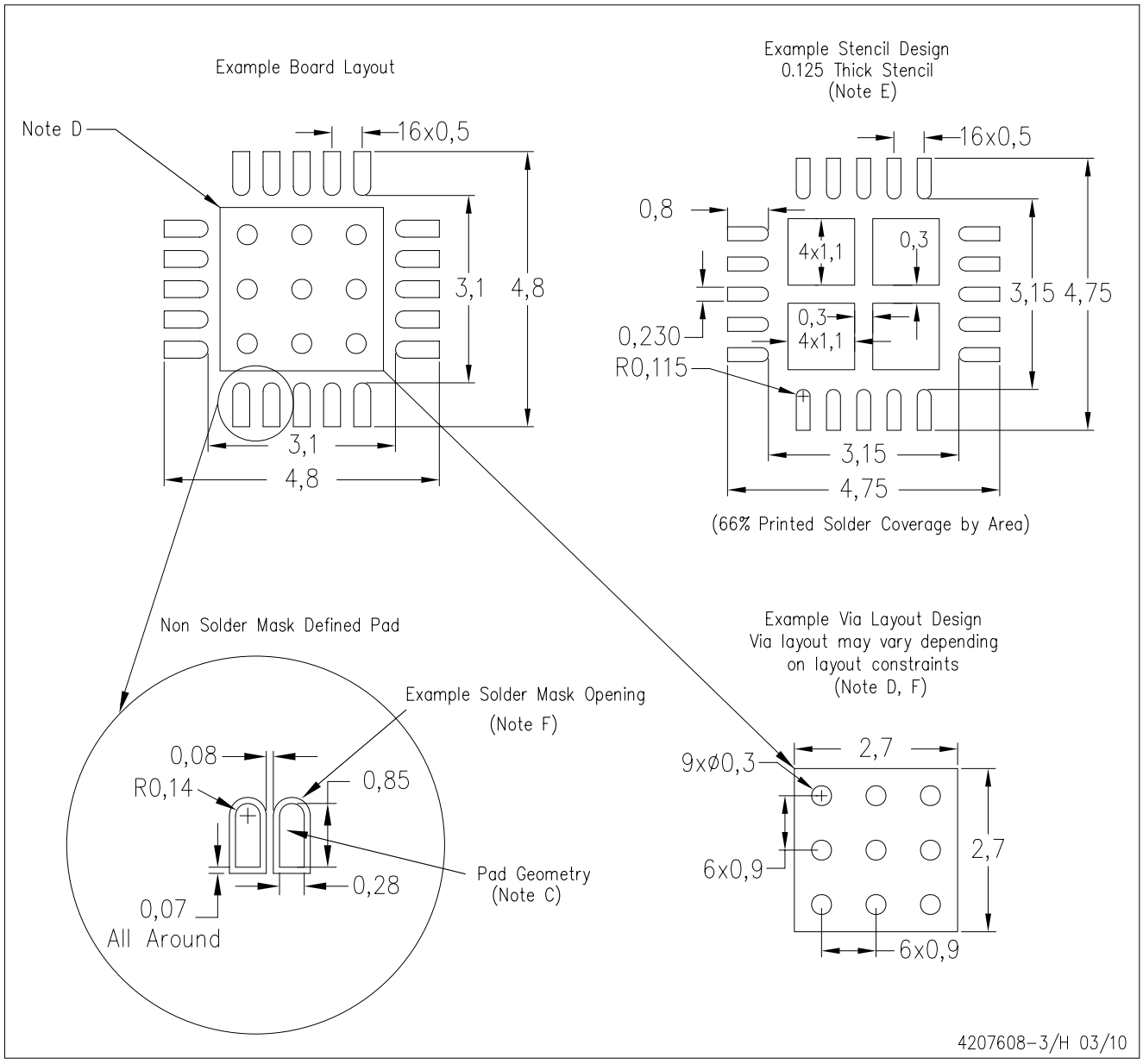


Bottom View

NOTE: All linear dimensions are in millimeters

Exposed Thermal Pad Dimensions

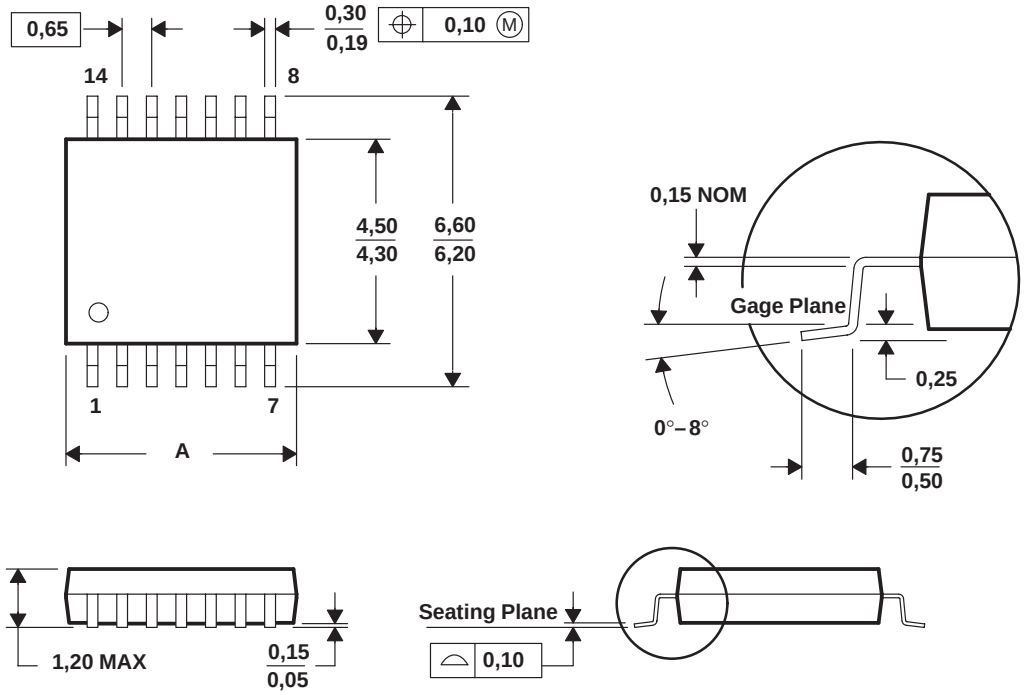
RGP (S–PVQFN–N20) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat–Pack Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http: //www.ti.com>.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
F. Customers should contact their board fabrication site for recommended solder mask tolerances and via tenting recommendations for vias placed in the thermal pad.

PW (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

14 PINS SHOWN



DIM \ PINS **	8	14	16	20	24	28
A MAX	3,10	5,10	5,10	6,60	7,90	9,80
A MIN	2,90	4,90	4,90	6,40	7,70	9,60

4040064/F 01/97

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
D. Falls within JEDEC MO-153

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