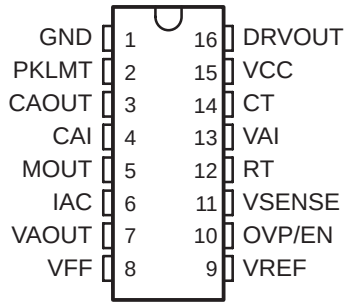
UCC2819, UCC3819
PROGRAMMABLE OUTPUT
POWER FACTOR PREREGULATOR

SLUS482B - APRIL 2001 – REVISED DECEMBER 2004

- Controls Boost Preregulator to Near-Unity Power Factor
- World Wide Line Operation
- Over-Voltage Protection
- Accurate Power Limiting
- Average Current Mode Control
- Improved Noise Immunity
- Improved Feed-Forward Line Regulation
- Leading Edge Modulation
- 150-μA Typical Start-Up Current
- Low-Power BiCMOS Operation
- 10.8-V to 17-V Operation
- Programmable Output Voltage (Tracking Boost Topology)

D, DW, N, and PW PACKAGES
(TOP VIEW)



description

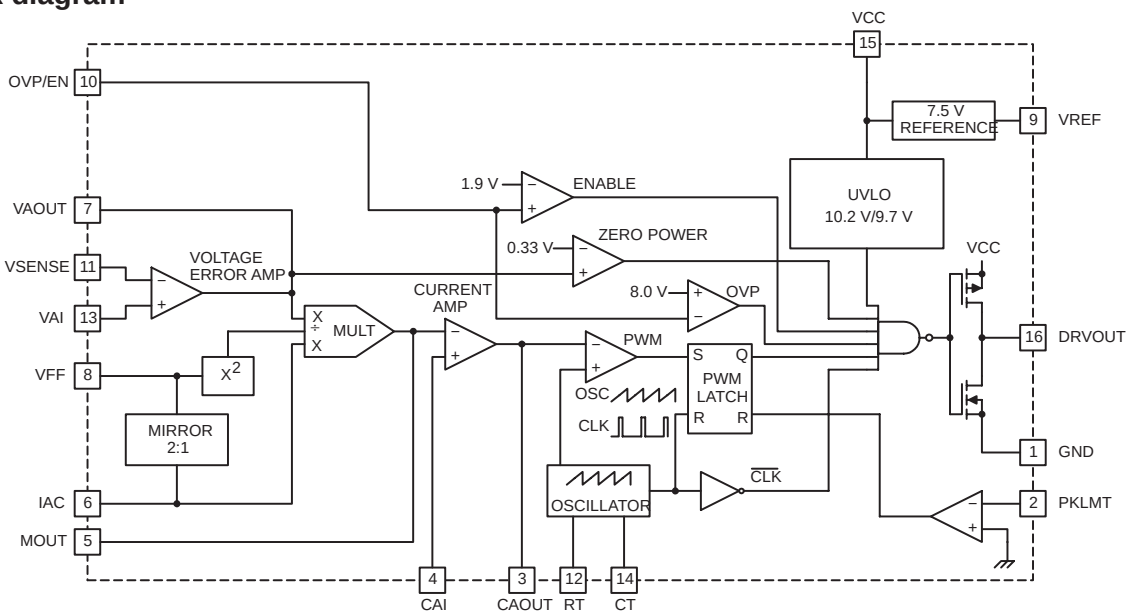
The UCC2819/UCC3819 provides all the functions necessary for active power factor corrected preregulators. The controller achieves near unity power factor by shaping the ac-input line current waveform to correspond to that of the ac-input line voltage. Average current mode control maintains stable, low distortion sinusoidal line current.

Designed in Texas Instrument's BiCMOS process, the UCC3819 offers new features such as lower start-up current, lower power dissipation, overvoltage protection, a shunt UVLO detect circuitry and a leading-edge modulation technique to reduce ripple current in the bulk capacitor.

The UCC3819 allows the output voltage to be programmed by bringing out the error amplifier noninverting input.

Available in the 16-pin D, DW, N, and PW packages.

block diagram



UDG-01009

absolute maximum ratings over operating free-air temperature (unless otherwise noted)†

Supply voltage, VCC . . . . . 18 V
Gate drive current, continuous . . . . . 0.2 A
Gate drive current . . . . . 1.2 A
Input voltage, CAI, MOUT . . . . . 8 V
Input voltage, PKLMT . . . . . 5 V
Input voltage, VSENSE, OVP/EN, VAI . . . . . 10 V
Input current, RT, IAC, PKLMT . . . . . 10 mA
Maximum negative voltage, DRVOUT, PKLMT, MOUT . . . . . −0.5 V
Power dissipation . . . . . 1 W

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under recommended operating conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

AVAILABLE OPTIONS

T_J	PACKAGE DEVICES			
	D PACKAGE	DW PACKAGE	N PACKAGE	PW PACKAGE
0°C to 70°C	UCC3819D	UCC3819DW	UCC3819N	UCC3819PW
−40°C to 85°C	UCC2819D	UCC2819DW	UCC2819N	UCC2819PW

† The D, DW, and PW packages are available taped and reeled. Add TR suffix to device type (e.g. UCC3819DTR) to order quantities of 2500 devices per reel.

electrical characteristics, T_A = 0°C to 70°C for the UCC3819, −40°C to 85°C for the UCC2819, VCC = 12 V, R_T = 22 kΩ, C_T = 270 pF, (unless otherwise noted)

supply current

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Supply current, off	VCC = (VCC turnon threshold −0.3 V)		150	300	µA
Supply current, on	VCC = 12 V, No load on DRVOUT	2	4	6	mA

UVLO

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
VCC turnon threshold		9.7	10.2	10.8	V
VCC turnoff threshold		9.4	9.7		V
UVLO hysteresis		0.3	0.5		V

voltage amplifier

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
VIO	VAOUT = 2.75 V, VCM = 3.75 V	−15		15	mV
VAI bias current	VAOUT = 2.75 V, VCM = 3.75 V		50	200	nA
V_{SENSE} bias current	VSENSE = VREF, VAOUT = 2.5 V		50	200	nA
CMRR	VCM = 1 V to 7.5 V	50	70		dB
Open loop gain	VAOUT = 2 V to 5 V	50	90		dB
High-level output voltage	I_L = −150 µA	5.3	5.5	5.6	V
Low-level output voltage	I_L = 150 µA	0	50	150	mV

electrical characteristics, T_A = 0°C to 70°C for the UCC3819, −40°C to 85°C for the UCC2819, VCC = 12 V, R_T = 22 kΩ, C_T = 270 pF, (unless otherwise noted)

over voltage protection and enable

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Over voltage reference		VREF +0.48	VREF +0.50	VREF +0.52	V
Hysteresis		300	500	600	mV
Enable threshold		1.7	1.9	2.1	V
Enable hysteresis		0.1	0.2	0.3	V

current amplifier

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Input offset voltage	V_{CM} = 0 V, V_{CAOUT} = 3 V	−3.5	0	2.5	mV
Input bias current	V_{CM} = 0 V, V_{CAOUT} = 3 V		−50	−100	nA
Input offset current	V_{CM} = 0 V, V_{CAOUT} = 3 V		25	100	nA
Open loop gain	V_{CM} = 0 V, V_{CAOUT} = 2 V to 5 V	90			dB
Common-mode rejection ratio	V_{CM} = 0 V to 1.5 V, V_{CAOUT} = 3 V	60	80		dB
High-level output voltage	I_L = −120 µA	5.6	6.5	6.8	V
Low-level output voltage	I_L = 1 mA	0.1	0.2	0.5	V
Gain bandwidth product	See Note 1		2.5		MHz

voltage reference

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Input voltage, (UCC3819)	T_A = 0°C to 70°C	7.387	7.5	7.613	V
Input voltage, (UCC2819)	T_A = −40°C to 85°C	7.369	7.5	7.631	V
Load regulation	I_{REF} = 1 mA to 2 mA	0		10	mV
Line regulation	VCC = 10.8 V to 15 V, See Note 2	0		10	mV
Short-circuit current	V_{REF} = 0 V	−20	−25	−50	mA

oscillator

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Initial accuracy	T_A = 25°C	85	100	115	kHz
Voltage stability	VCC = 10.8 V to 15 V	−1		1	%
Total variation	Line, temp, See Note 1	80		120	kHz
Ramp peak voltage		4.5	5	5.5	V
Ramp amplitude voltage (peak to peak)		3.5	4	4.5	V

NOTES: 1. Ensured by design, Not production tested.
2. Reference variation for V_{CC} < 10.8 V is shown in Figure 2.

electrical characteristics, T_A = 0°C to 70°C for the UCC3819, −40°C to 85°C for the UCC2819, VCC = 12 V, R_T = 22 kΩ, C_T = 270 pF, (unless otherwise noted)

peak current limit

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
PKLMT reference voltage		−15		15	mV
PKLMT propagation delay		150	350	500	ns

multiplier

PARAMETER	TEST CONDITIONS			MIN	TYP	MAX	UNITS
I_{MOUT}, high line, low power output current, (0°C to 85°C)	I_{AC} = 500 µA,	V_{FF} = 4.7 V,	VAOUT = 1.25 V	0	−6	−20	µA
I_{MOUT}, high line, low power output current, (−40°C to 85°C)	I_{AC} = 500 µA,	V_{FF} = 4.7 V,	VAOUT = 1.25 V	0		−23	µA
I_{MOUT}, high line, high power output current	I_{AC} = 500 µA,	V_{FF} = 4.7 V,	VAOUT = 5 V	−70	−90	−105	µA
I_{MOUT}, low line, low power output current	I_{AC} = 150 µA,	V_{FF} = 1.4 V,	VAOUT = 1.25 V	−10	−19	−50	µA
I_{MOUT}, low line, high power output current	I_{AC} = 150 µA,	V_{FF} = 1.4 V,	VAOUT = 5 V	−268	−300	−346	µA
I_{MOUT}, IAC limited	I_{AC} = 150 µA,	V_{FF} = 1.3 V,	VAOUT = 5 V	−250	−300	−400	µA
Gain constant (K)	I_{AC} = 300 µA,	V_{FF} = 3 V,	VAOUT = 2.5 V	0.5	1	1.5	1/V
I_{MOUT}, zero current	I_{AC} = 150 µA,	V_{FF} = 1.4 V,	VAOUT = 0.25 V		0	−2	µA
	I_{AC} = 500 µA,	V_{FF} = 4.7 V,	VAOUT = 0.25 V		0	−2	µA
I_{MOUT}, zero current, (0°C to 85°C)	I_{AC} = 500 µA,	V_{FF} = 4.7 V,	VAOUT = 0.5 V		0	−3	µA
I_{MOUT}, zero current, (−40°C to 85°C)	I_{AC} = 500 µA,	V_{FF} = 4.7 V,	VAOUT = 0.5 V		0	−3.5	µA
Power limit (I_{MOUT} x V_{FF})	I_{AC} = 150 µA,	V_{FF} = 1.4 V,	VAOUT = 5 V	−375	−420	−485	µW

feed-forward

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
VFF output current	I_{AC} = 300 µA	−140	−150	−160	µA

gate driver

PARAMETER	TEST CONDITIONS			MIN	TYP	MAX	UNITS
Pullup resistance	I_O = –100 mA to −200 mA				5	12	Ω
Pulldown resistance	I_O = 100 mA				2	10	Ω
Output rise time	C_L = 1 nF,	R_L = 10 Ω,	V_{DRVOUT} = 0.7 V to 9 V		25	50	ns
Output fall time	C_L = 1 nF,	R_L = 10 Ω,	V_{DRVOUT} = 9 V to 0.7 V		10	50	ns
Maximum duty cycle				93	95	100	%
Minimum controlled duty cycle	At 100 kHz					2	%

zero power

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Zero power comparator threshold	Measured on VAOUT	0.20	0.33	0.50	V

pin descriptions

CAI: (current amplifier noninverting input) Place a resistor between this pin and the GND side of current-sense resistor. This input and the inverting input (MOUT) remain functional down to and below GND.

CAOUT: (current amplifier output) This is the output of a wide bandwidth operational amplifier that senses line current and commands the PFC pulse-width modulator (PWM) to force the correct duty cycle. Compensation components are placed between CAOUT and MOUT.

CT: (oscillator timing capacitor) A capacitor from CT to GND sets the PWM oscillator frequency according to:

$$f \approx \left(\frac{0.6}{RT \times CT}\right)$$

The lead from the oscillator timing capacitor to GND should be as short and direct as possible.

DRVOUT: (gate drive) The output drive for the boost switch is a totem-pole MOSFET gate driver on DRVOUT. Use a series gate resistor to prevent interaction between the gate impedance and the output driver that might cause the DRVOUT to overshoot excessively. See characteristic curve (Figure 13) to determine minimum required gate resister value. Some overshoot of the DRVOUT output is always expected when driving a capacitive load.

GND: (ground) All voltages measured with respect to ground. VCC and REF should be bypassed directly to GND with a 0.1-µF or larger ceramic capacitor.

IAC: (current proportional to input voltage) This input to the analog multiplier is a current proportional to instantaneous line voltage. The multiplier is tailored for very low distortion from this current input (I_{IAC}) to multiplier output. The recommended maximum I_{IAC} is 500 µA.

MOUT: (multiplier output and current amplifier inverting input) The output of the analog multiplier and the inverting input of the current amplifier are connected together at MOUT. As the multiplier output is a current, this is a high-impedance input so the amplifier can be configured as a differential amplifier. This configuration improves noise immunity and allows for the leading-edge modulation operation. The multiplier output current is limited to $\left(2 \times I_{IAC}\right)$. The multiplier output current is given by the equation:

$$I_{MOUT} = \frac{I_{IAC} \times (V_{VAOUT} - 1)}{V_{VFF}^{2} \times K}$$

where $K = \frac{1}{V}$ is the multiplier gain constant.

OVP/EN: (over-voltage/enable) A window comparator input that disables the output driver if the boost output voltage is a programmed level above the nominal or disables both the PFC output driver and resets SS if pulled below 1.9 V (typ).

PKLMT: (PFC peak current limit) The threshold for peak limit is 0 V. Use a resistor divider from the negative side of the current sense resistor to VREF to level shift this signal to a voltage level defined by the value of the sense resistor and the peak current limit. Peak current limit is reached when PKLMT voltage falls below 0 V.

RT: (oscillator charging current) A resistor from RT to GND is used to program oscillator charging current. A resistor between 10 kΩ and 100 kΩ is recommended. Nominal voltage on this pin is 3 V.

pin descriptions (continued)

VAI: (voltage amplifier non-inverting input) This input can be tied to the VREF or any other voltage reference (≤7.5 V) to set the boost regulator output voltage.

VAOUT: (voltage amplifier output) This is the output of the operational amplifier that regulates output voltage. The voltage amplifier output is internally limited to approximately 5.5 V to prevent overshoot.

VCC: (positive supply voltage) Connect to a stable source of at least 20 mA between 10 V and 17 V for normal operation. Bypass VCC directly to GND to absorb supply current spikes required to charge external MOSFET gate capacitances. To prevent inadequate gate drive signals, the output devices are inhibited unless V_{VCC} exceeds the upper under-voltage lockout voltage threshold and remains above the lower threshold.

VFF: (feed-forward voltage) The RMS voltage signal generated at this pin by mirroring 1/2 of the I_{IAC} into a single pole external filter. At low line, the VFF roll should be 14 V.

VSENSE: (voltage amplifier inverting input) This is normally connected to a compensation network and to the boost converter output through a divider network.

VREF: (voltage reference output) VREF is the output of an accurate 7.5-V voltage reference. This output is capable of delivering 20 mA to peripheral circuitry and is internally short-circuit current limited. VREF is disabled and remains at 0 V when V_{VCC} is below the UVLO threshold. Bypass VREF to GND with a 0.1-µF or larger ceramic capacitor for best stability. Please refer to Figures 8 and 9 for VREF line and load regulation characteristics.

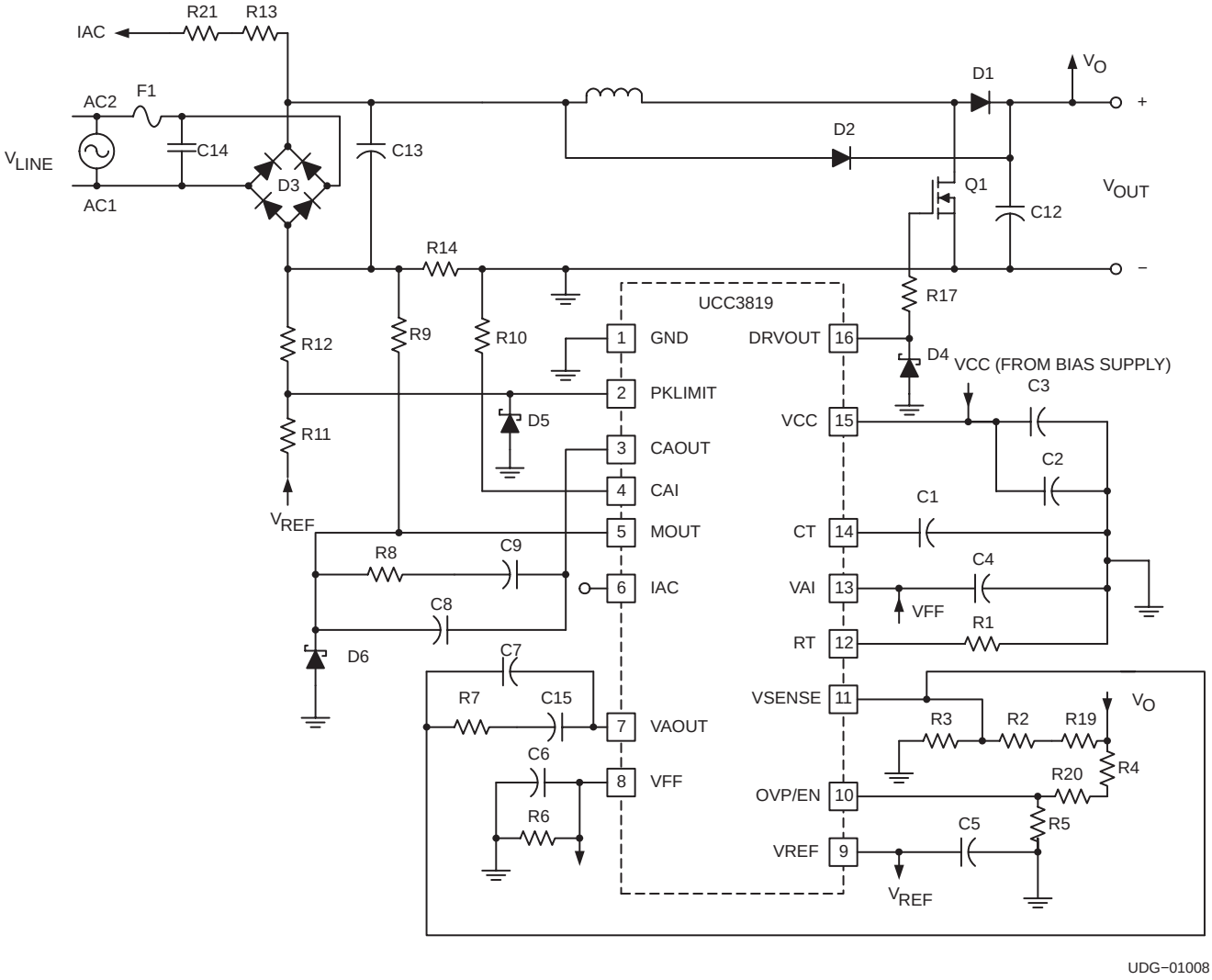
APPLICATION INFORMATION

The UCC3819 is based on the UCC3818 PFC preregulator. For a more detailed application information for this part, please refer to the UCC3818 datasheet product folder.

The main difference between the UCC3818 and the UCC3819 is that the non-inverting input of the voltage error amplifier is made available to the user through an external pin (VAI) in the UCC3819. The SS pin and function were eliminated to accommodate this change.

The benefit of VAI pin is that it can be used to dynamically change the PFC output voltage based on the line voltage (RMS) level or other conditions. Figure 1 shows one suggested implementation of the tracking boost PFC converter as this approach is sometimes referred to. The VAI pin is tied to the VFF pin and hence output voltage scales up with the line voltage. The benefit of this approach is that at lower line voltages the output voltage is lower and that leads to smaller boost inductor value, lower MOSFET conduction losses and reduced component stresses. In order for this feature to work, the downstream converter has to operate over a wider input range.

APPLICATION INFORMATION



UDG–01008

Figure 1. Suggested Implementation of UCC3819 in a Tracking Boost PFC Preregulator

APPLICATION INFORMATION

REFERENCE VOLTAGE
vs
SUPPLY VOLTAGE

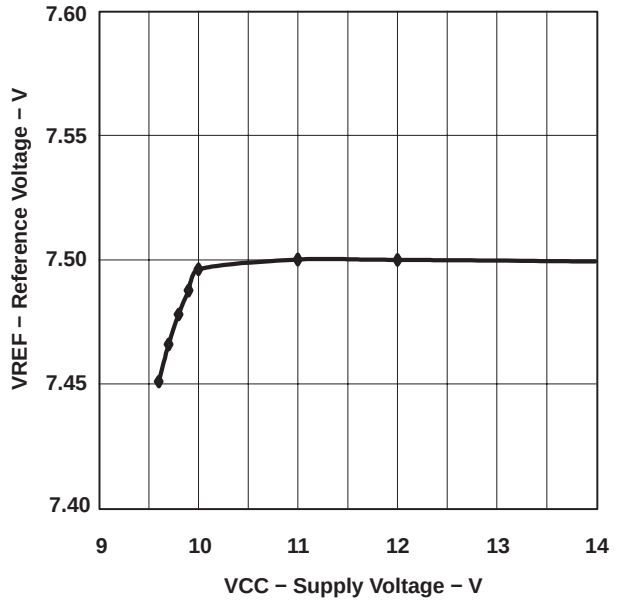


Figure 2

REFERENCE VOLTAGE
vs
REFERENCE CURRENT

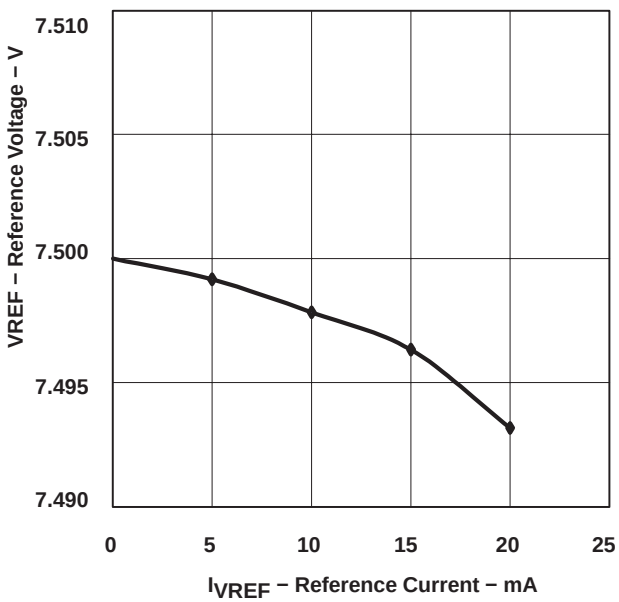


Figure 3

MULTIPLIER OUTPUT CURRENT
vs
VOLTAGE ERROR AMPLIFIER OUTPUT

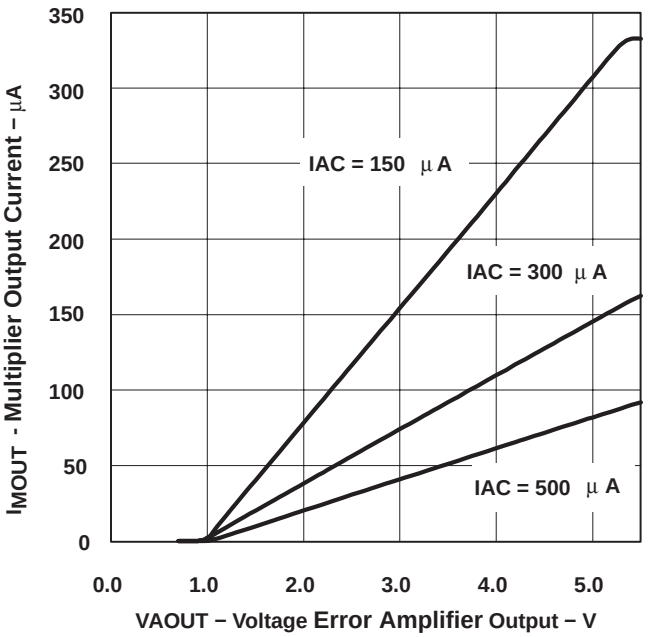


Figure 4

MULTIPLIER GAIN
vs
VOLTAGE ERROR AMPLIFIER OUTPUT

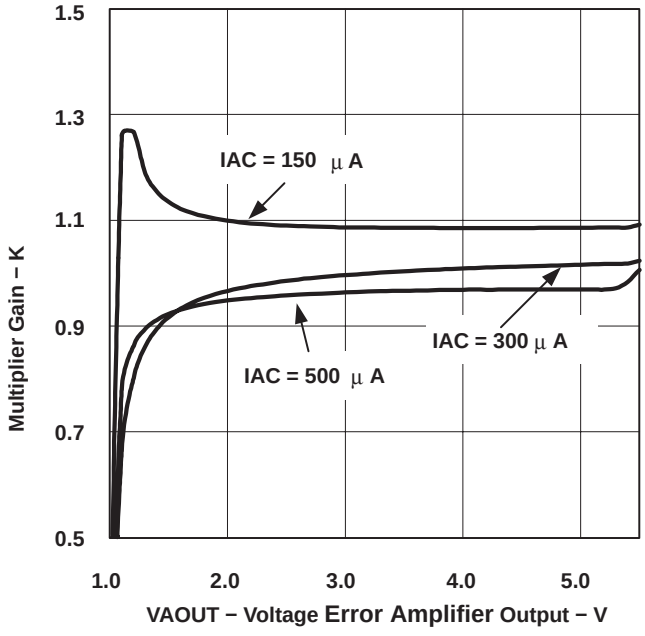


Figure 5

APPLICATION INFORMATION

MULTIPLIER CONSTANT POWER PERFORMANCE

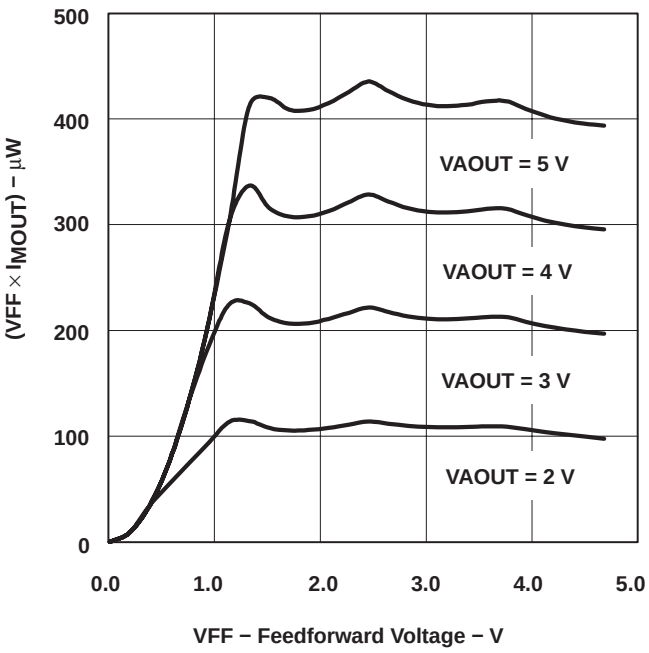


Figure 6

RECOMMENDED MINIMUM GATE RESISTANCE
vs
SUPPLY VOLTAGE

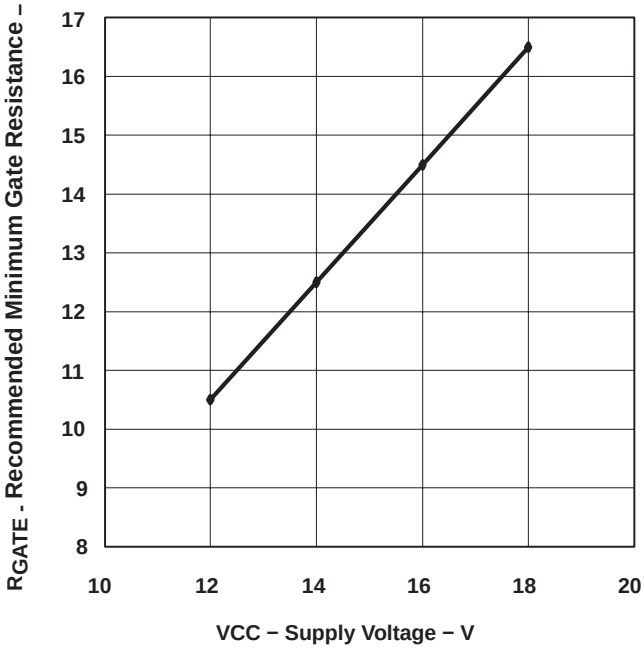


Figure 7

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)
UCC2819D	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
UCC2819DG4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
UCC2819DTR	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
UCC2819DTRG4	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
UCC2819N	ACTIVE	PDIP	N	16	25	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type
UCC2819NG4	ACTIVE	PDIP	N	16	25	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type
UCC3819N	ACTIVE	PDIP	N	16	25	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type
UCC3819NG4	ACTIVE	PDIP	N	16	25	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type

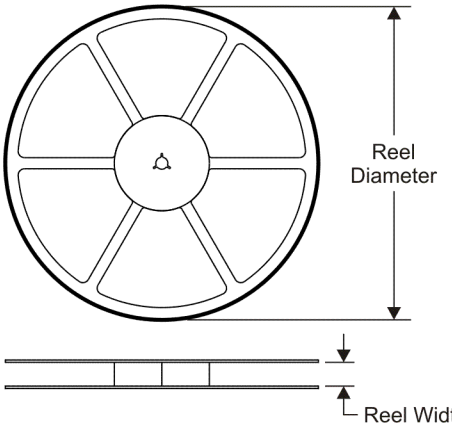
(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

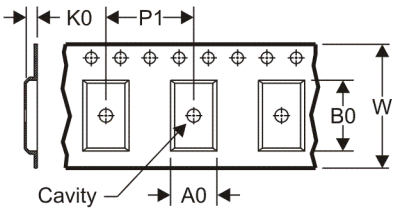
(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

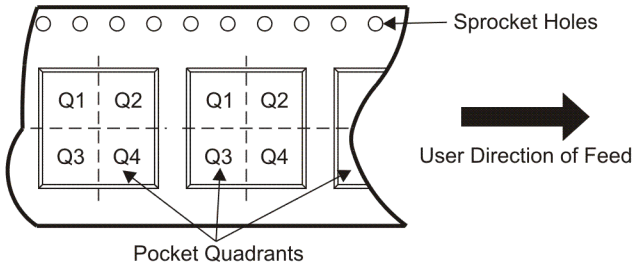


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

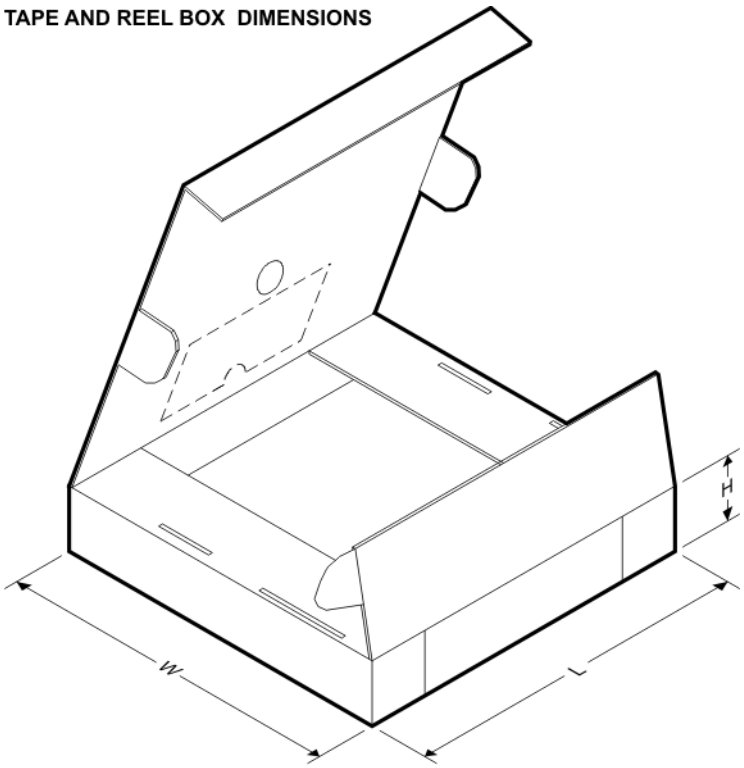
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
UCC2819DTR	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1

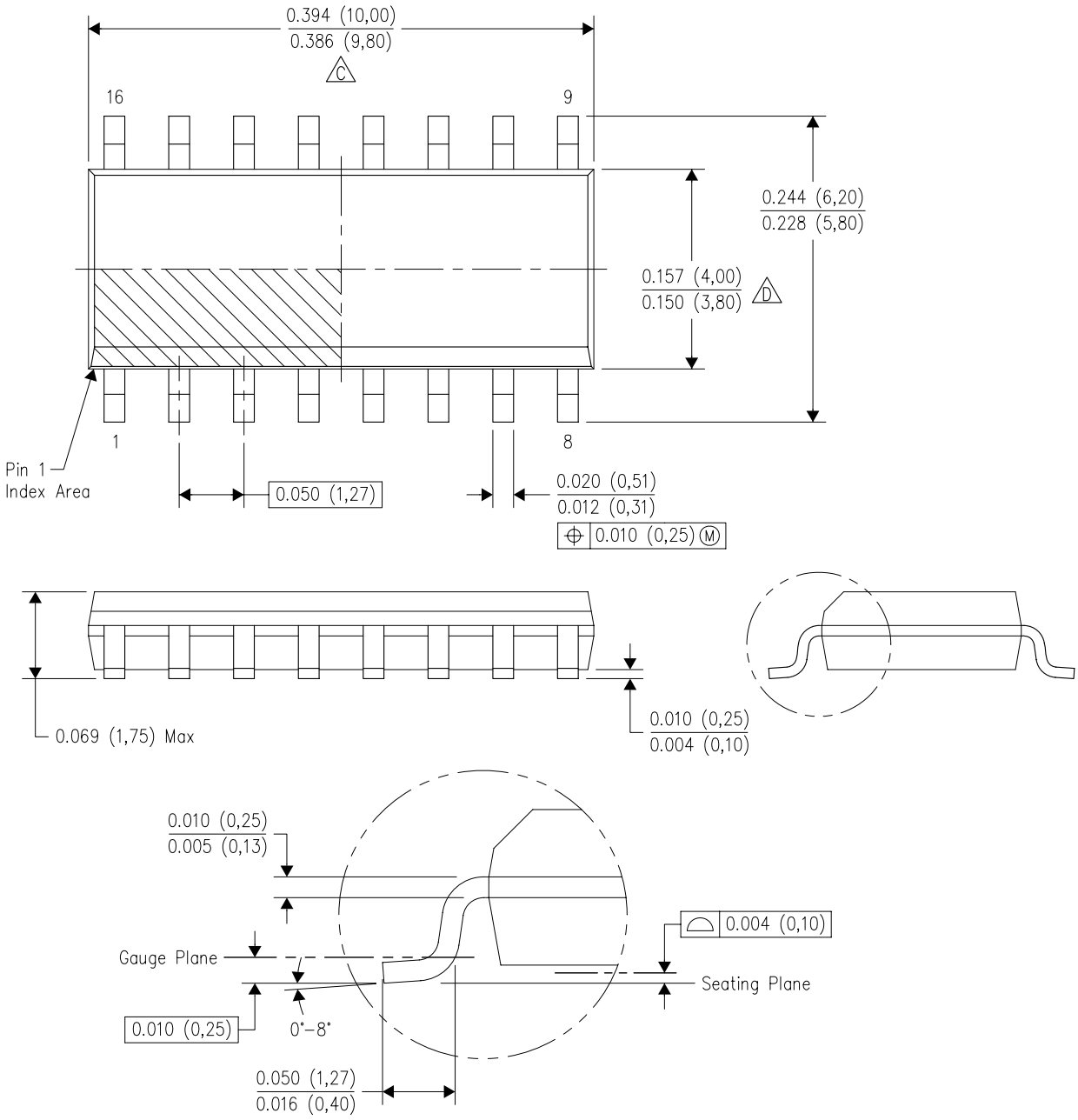
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

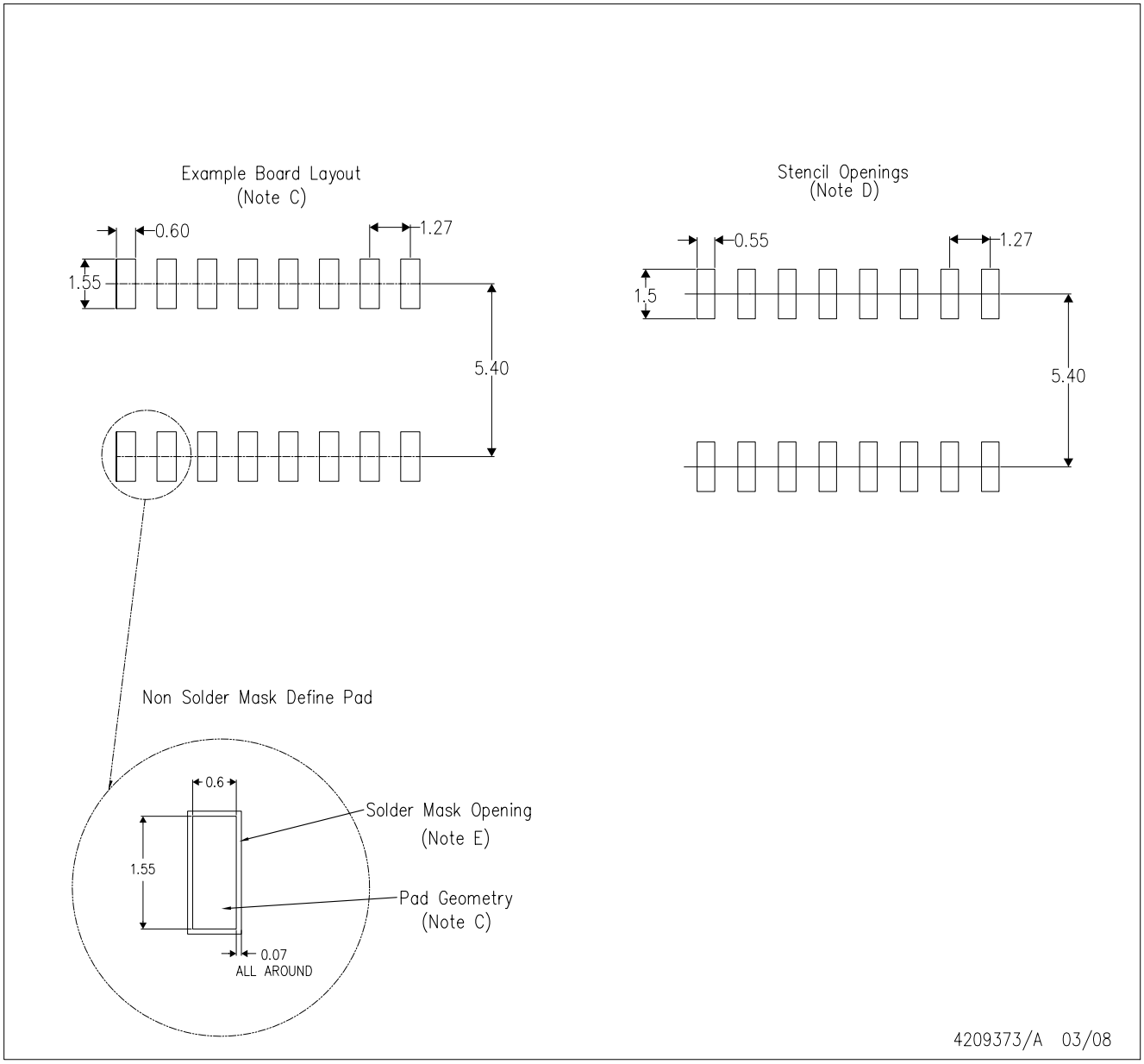
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
UCC2819DTR	SOIC	D	16	2500	333.2	345.9	28.6

D (R–PDSO–G16) PLASTIC SMALL–OUTLINE PACKAGE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 (0,15) per end.
D. Body width does not include interlead flash. Interlead flash shall not exceed .017 (0,43) per side.
E. Reference JEDEC MS–012 variation AC.

D(R–PDSO–G16)

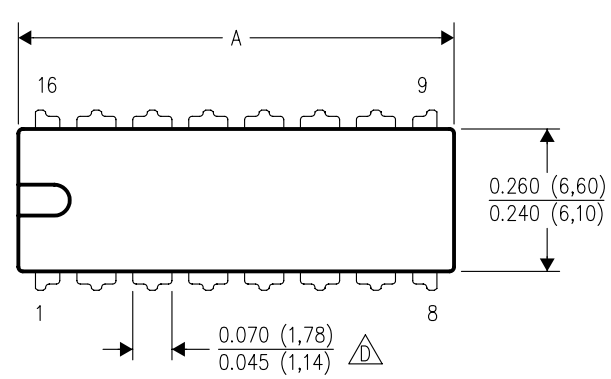


NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Refer to IPC7351 for alternate board design.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

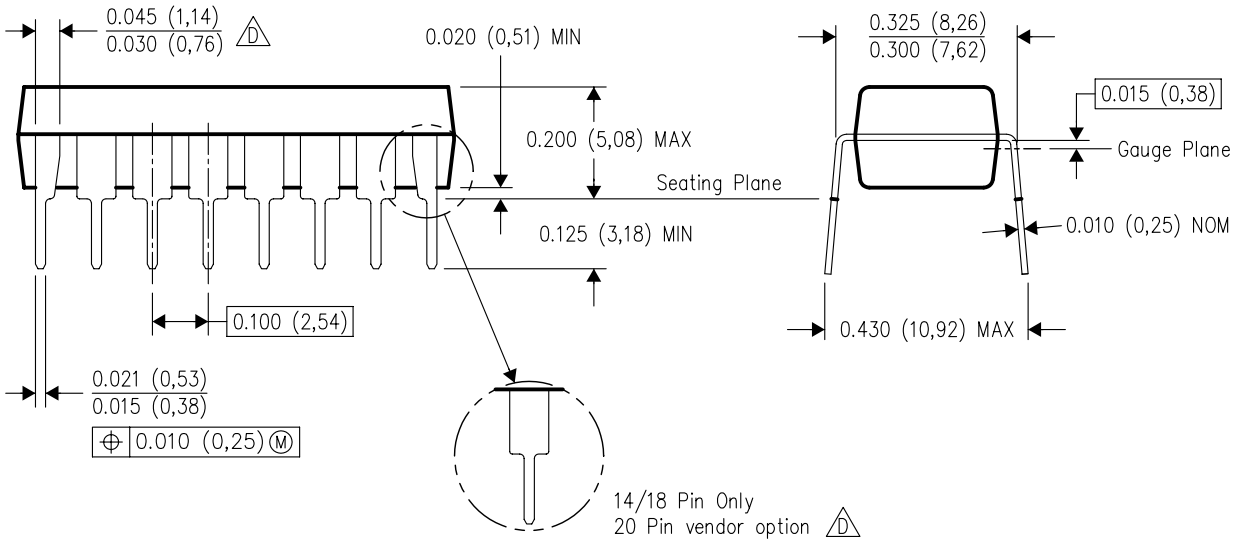
N (R–PDIP–T**)

PLASTIC DUAL–IN–LINE PACKAGE

16 PINS SHOWN



DIM \ PINS **	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS–001 VARIATION (C)	AA	BB	AC	AD



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NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001, except 18 and 20 pin minimum body length (Dim A).
D. The 20 pin end lead shoulder width is a vendor option, either half or full width.

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