9-LINE 3 TO 5 VOLT LOW CAPACITANCE SCSI ACTIVE TERMINATOR

FEATURES

- Complies with SCSI, SCSI–2 and SPI–2 Single Ended Standards
- 2.7-V to 5.25-V Operation
- 1.8-pF Channel Capacitance during Disconnect
- 0.5-μA Supply Current in Disconnect Mode
- 110-Ω/2.5-kΩ Programmable Termination
- Completely Meets SCSI Hot Plugging
- –400-mA Sourcing Current for Termination
- +400-mA Sinking Current for Active Negation Drivers
- Trimmed Termination Current to 4%
- Trimmed Impedance to 7%
- Current Limit and Thermal Shutdown Protection

DESCRIPTION

The UCC5614 provides 9 lines of active termination for a small computer system's interface (SCSI) parallel bus. The SCSI standard recommends active termination at both ends of the cable segment.

The UCC5614 is ideal for high performance 3.3-V SCSI systems. The key features contributing to such low operating voltage are the 0.1-V drop-out regulator and the 2.7-V reference. During disconnect the supply current is typically only 0.5 μA, which makes the device attractive for battery powered systems.

The UCC5614 is designed with an ultra low channel capacitance of 1.8 pF, which eliminates effects on signal i   cted terminators at interim points on the bus.

BLOCK DIAGRAM

www.BDTIC.com/TI

1
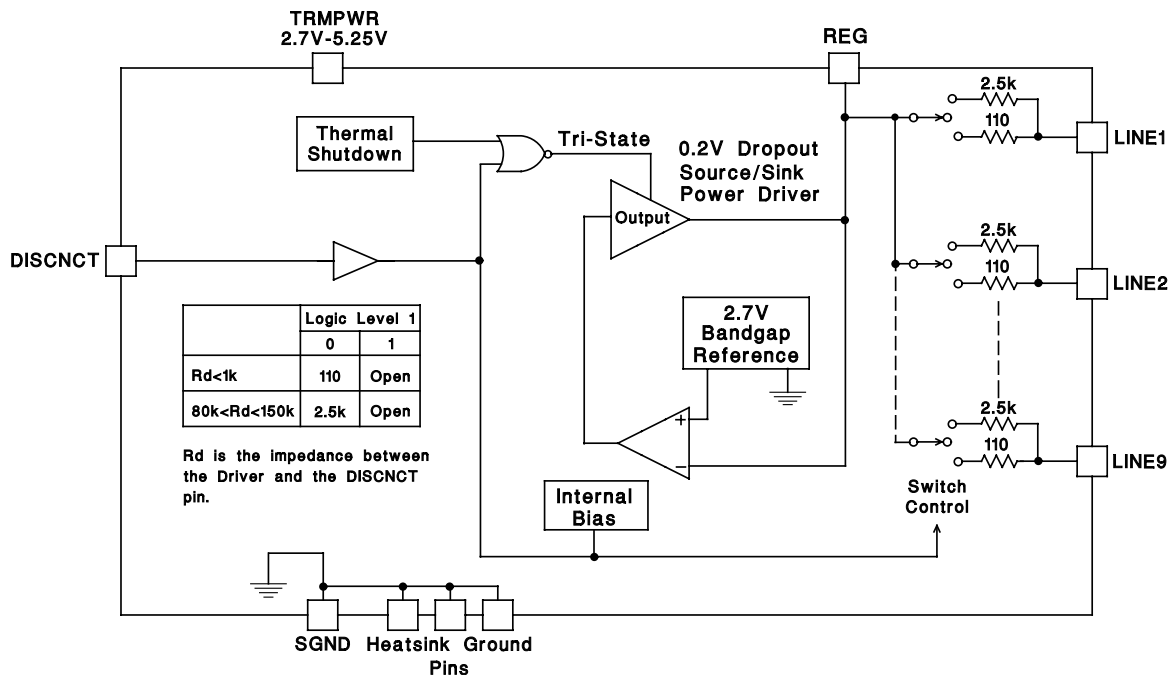
UCC5614

DESCRIPTION (CONTINUED)

The UCC5614 can be programmed for either a 110-Ω or 2.5-kΩ termination. The 110-Ω termination is used for standard SCSI bus lengths and the 2.5-kΩ termination is typically used in short bus applications. When driving the TTL compatible DISCNCT pin directly, the 110-Ω termination is connected when the DISCNCT pin is driven low, and disconnected when driven high. When the DISCNCT pin is driven through an impedance between 80 kΩ and 150 kΩ, the terminator is in short bus mode. The 2.5-kΩ termination is connected when the DISCNCT pin is driven low and disconnected when driven high.

The power amplifier output stage allows the UCC5614 to source full termination current and sink active negation current when all termination lines are actively negated.

The UCC5614 is pin for pin compatible with Unitrode's other 9-line SCSI terminators, allowing lower capacitance and lower voltage upgrades to existing systems. The UCC5614, as with all Unitrode terminators, is completely hot pluggable and appears as high impedance at the terminating channels with VTRMPWR = 0 V or open.

Internal circuit trimming is utilized, first to trim the 110-Ω termination impedance to a 7% tolerance, and then most importantly, to trim the output current to a 4% tolerance, as close to the max SCSI specification as possible, which maximizes noise margin in fast SCSI operation.

Other features include thermal shutdown and current limit.

This device is offered in low thermal resistance versions of the industry standard 16-pin narrow body SOIC, 16-pin N and 24-pin TSSOP.
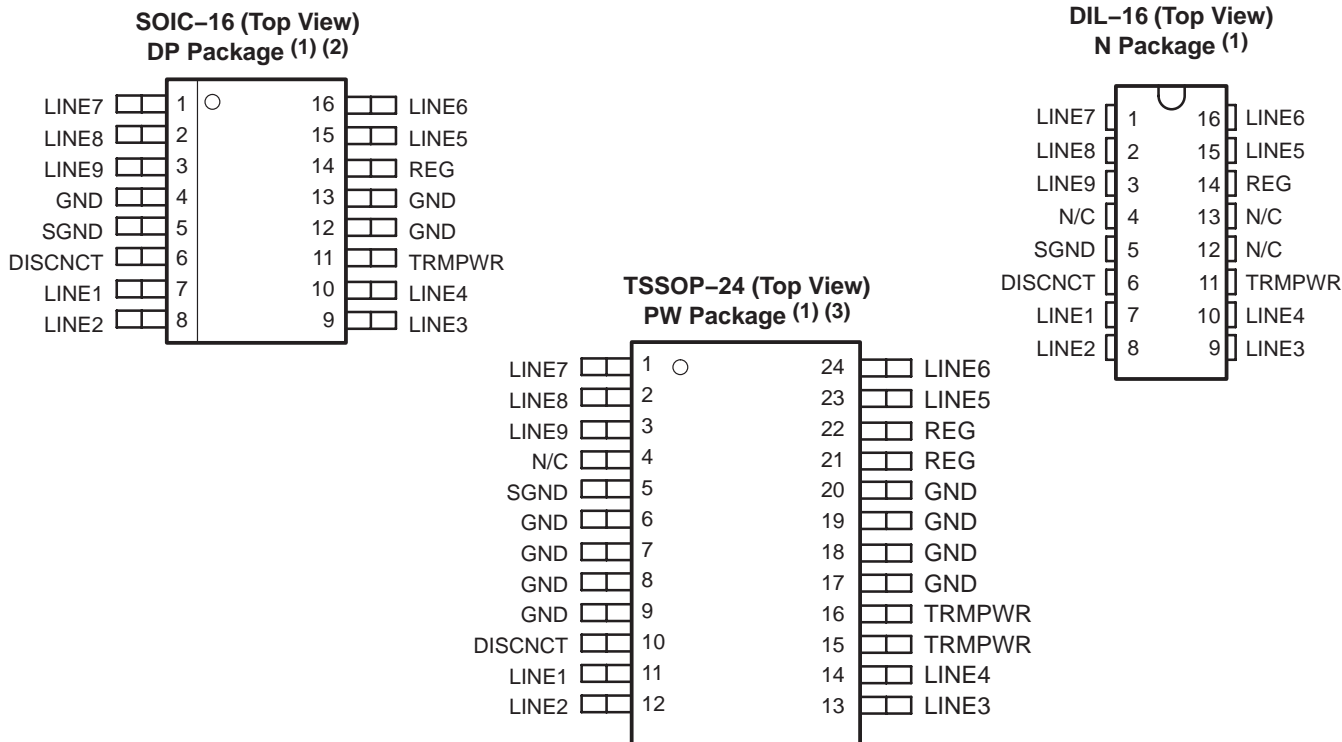
ORDERING INFORMATION

T_A	PACKAGED DEVICE		
	SOIC-16 (DP)†	DIL-16 (N)	TSSOP-24 (PW)‡
0°C to 70°C	UCC5614DP	UCC5614N	UCC5614PW

† The DP package is available taped and reeled in quanities of 2,500. Add TR suffix to device type (e.g. UCC5614DPTR) to order quantities of 2,500 devices per reel.

‡ The PW package is available taped and reeled in quanities of 2,000. Add TR suffix to device type (e.g. UCC5614PWTR) to order quantities of 2,000 devices per reel.

CONNECTION DIAGRAMS

SOIC–16 (Top View)
DP Package (1) (2)

LINE7	1	16	LINE6
LINE8	2	15	LINE5
LINE9	3	14	REG
GND	4	13	GND
SGND	5	12	GND
DISCNCT	6	11	TRMPWR
LINE1	7	10	LINE4
LINE2	8	9	LINE3

DIL–16 (Top View)
N Package (1)

LINE7	1	16	LINE6
LINE8	2	15	LINE5
LINE9	3	14	REG
N/C	4	13	N/C
SGND	5	12	N/C
DISCNCT	6	11	TRMPWR
LINE1	7	10	LINE4
LINE2	8	9	LINE3

TSSOP–24 (Top View)
PW Package (1) (3)

LINE7	1	24	LINE6
LINE8	2	23	LINE5
LINE9	3	22	REG
N/C	4	21	REG
SGND	5	20	GND
GND	6	19	GND
GND	7	18	GND
GND	8	17	GND
GND	9	16	TRMPWR
DISCNCT	10	15	TRMPWR
LINE1	11	14	LINE4
LINE2	12	13	LINE3

NOTES: (1). Drawings are not to scale.
(2). DP package pin 5 serves as ground and pins 4,12 and 13 serve as heatsink ground.
(3). PW package pin 5 serves as ground and pins 6,7,8,9,17,18,19 and 20 serve as heatsink ground.

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range unless otherwise noted†‡

	UCC5629	UNIT
TRMPWR voltage	6	V
Input voltage	0 to 7	V
Regulator output current	2	W
Storage temperature, T_{stg}	–65 to 150	°C
Operating junction temperature, T_J	–55 to 150	°C
Lead temperature (soldering, 10 sec.)	300	°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability. All voltages are with respect to GND. Currents are positive into and negative out of, the specified terminal.

‡ Currents are positive into, negative out of the specified terminal. Consult Packaging Section of Databook for thermal limitations and considerations of packages. All voltages are referenced to GND.

RECOMMENDED OPERATING CONDITIONS

	MIN	NOM	MAX	UNIT
TRMPWR voltage	2.7		5.25	V
Temperature ranges	0		70	°C
Signal line voltage	0		5	V
DISCNCT input voltage	0		TRMPWR	V

UCC5614

ELECTRICAL CHARACTERISTICS

T_A = 0°C to 70°C, TRMPWR = 3.3 V, DISCNCT = 0 V, $R_{DISCNCT}$ = 0 Ω, T_A = T_J, (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Supply Current Section					
Termpwr supply current	All termination lines = Open		1	2	mA
	All termination lines = 0.2 V		210	218	
Power down mode	DISCNCT = Trmpwr		0.5	5	µA
Output Section (110 Ω – Terminator Lines)					
Terminator impedance		102.3	110	117.7	Ohms
Output high voltage	(Note 1)	2.5	2.7	3.0	V
Max output current	VLINE = 0.2 V TJ = 25°C	−22.1	−23	−24	mA
	VLINE = 0.2 V	−21	−23	−24	
	VLINE = 0.2 , TRMPWR = 3 V, TJ = 25°C (Note 1)	−20.2	−23	−24	
	VLINE = 0.2 V, TRMPWR = 3 V (Note 1)	−19	−23	−24	
	VLINE = 0.5 V			−22.4	
Output leakage	DISCNCT = 2.4 V, TRMPWR = 0 V to 5.25 V		10	400	nA
Output capacitance	DISCNCT = 2.4 V (Note 2) (DP Package)		1.8	2.5	pF
Output Section (2.5 kΩ – Terminator Lines) (RDISCNCT = 80 kΩ)					
Terminator impedance		2	2.5	3	kΩ
Output high voltage	TRMPWR = 3 V (Note 1)	2.5	2.7	3.0	V
Max output current	VLINE = 0.2 V	−0.7	−1	−1.4	mA
	VLINE = 0.2 V, TRMPWR = 3 V (Note 1)	−0.6	−1	−1.5	
Output leakage	DISCNCT = 2.4 V, TRMPWR = 0 to 5.25 V		10	400	nA
Output capacitance	DISCNCT = 2.4 V (Note 2) (DP Package)		1.8	2.5	pF
Regulator Section					
Regulator output voltage	5.25 V > TRMPWR > 3 V	2.5	2.7	3.0	V
Drop out voltage	All Termination Lines = 0.2 V		0.1	0.2	
Short circuit current	VREG = 0 V	−200	−400	−800	mA
Sinking current capability	VREG = 3 V	200	400	800	
Thermal shutdown	(Note 2)		170		°C
Thermal shutdown hysteresis	(Note 2)		10		
Disconnect Section					
Disconnect threshold	RDISCNCT = 0 & 80 kΩ	0.8	1.5	2.0	V
Input current	DISCNCT = 0 V		30	50	mA

NOTES: 1. Measuring each termination line while other eight are low (0.2 V).
2. Ensured by design. Not production tested.

Terminal Functions

TERMINAL		I/O	DESCRIPTION
NAME	NO.		
DISCNCT	7	I	Taking this pin high causes the 9 channels to become high impedance and the chip to go into low power mode. In short laptop buses an 80-kΩ to 150-kΩ resister to ground terminates the bus at 2.5 kΩ. Less than 110 Ω to ground enables the terminator.
GND	9		Ground reference for the device
LINE1 TO LINE9	4	I	110-Ω termination channels
REG	9	o	Output of the internal 2.7-V regulator
TRMPWR	4	I	Power for the device

APPLICATION INFORMATION
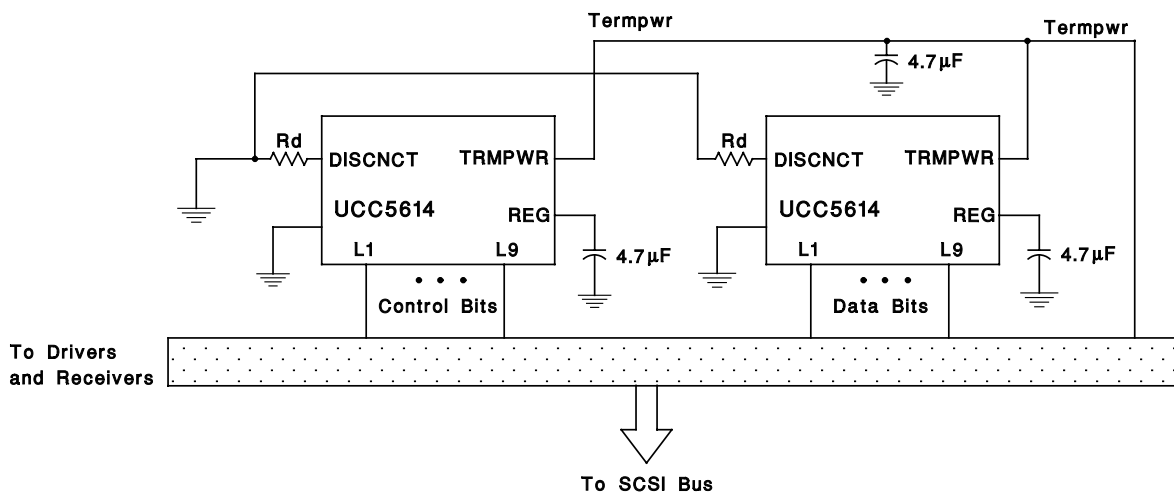
Figure 1. Typical SCSI Bus Configuration Utilizing two UCC5614 Devices
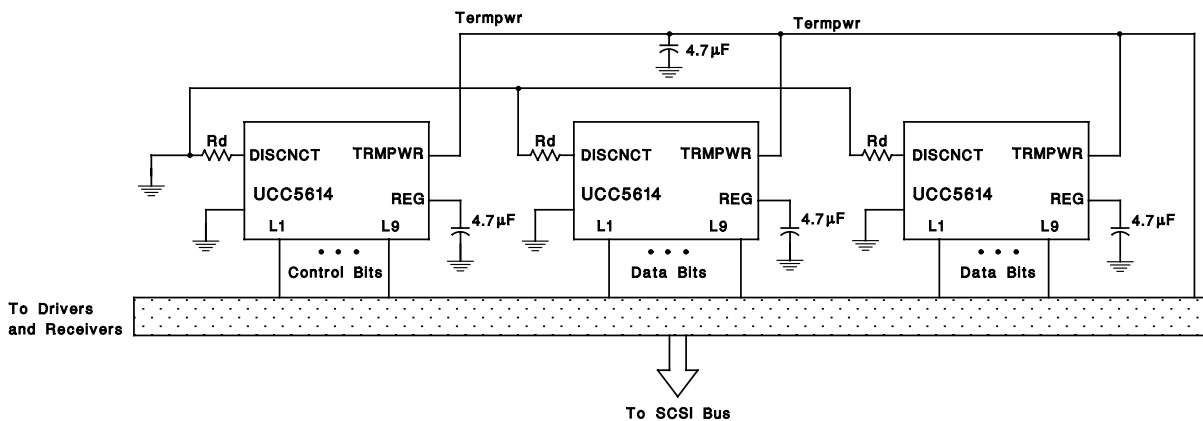
Figure 2. Typical Wide SCSI Bus Configuration Utilizing three UCC5614 Devices

---

TEXAS
INSTRUMENTS
www.ti.com

www.BDTIC.com/TI

5

PACKAGE OPTION ADDENDUM

PACKAGING INFORMATION

Orderable Device	Status [1]	Package Type	Package Drawing	Pins	Package Qty	Eco Plan [2]	Lead/Ball Finish	MSL Peak Temp [3]
UCC5614DP	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
UCC5614DPG4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
UCC5614DPTR	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
UCC5614DPTRG4	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
UCC5614PWP	ACTIVE	TSSOP	PW	24	60	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
UCC5614PWPG4	ACTIVE	TSSOP	PW	24	60	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
UCC5614PWPTR	ACTIVE	TSSOP	PW	24	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
UCC5614PWPTRG4	ACTIVE	TSSOP	PW	24	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
UCC5614Z	OBSOLETE		UTR	16		TBD	Call TI	Call TI

[1] The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

[2] Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

[3] MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

TAPE DIMENSIONS

Reel Diameter

Reel Width (W1)

K0 ← P1 →

B0 | W

Cavity — A0

A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

Sprocket Holes

Q1	Q2		Q1	Q2
Q3	Q4		Q3	Q4

User Direction of Feed

Pocket Quadrants

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
UCC5614DPTR	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
UCC5614PWPTR	TSSOP	PW	24	2000	330.0	16.4	6.95	8.3	1.6	8.0	16.0	Q1

www.BDTIC.com/TI

TAPE AND REEL BOX DIMENSIONS

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
UCC5614DPTR	SOIC	D	16	2500	346.0	346.0	33.0
UCC5614PWPTR	TSSOP	PW	24	2000	346.0	346.0	33.0

D (R−PDSO−G16)   PLASTIC SMALL OUTLINE

0.394 (10,00)
0.386 (9,80)
⚠C

16   9

0.244 (6,20)
0.228 (5,80)

0.157 (4,00)
0.150 (3,80) ⚠D

Pin 1
Index Area

1   8

0.050 (1,27)

0.020 (0,51)
0.012 (0,31)

⊕ 0.010 (0,25) Ⓜ

0.069 (1,75) Max

0.010 (0,25)
0.004 (0,10)

0.010 (0,25)
0.005 (0,13)

0.004 (0,10)

Gauge Plane

Seating Plane

0.010 (0,25)   0°–8°

0.050 (1,27)
0.016 (0,40)

4040047-6/M   06/11
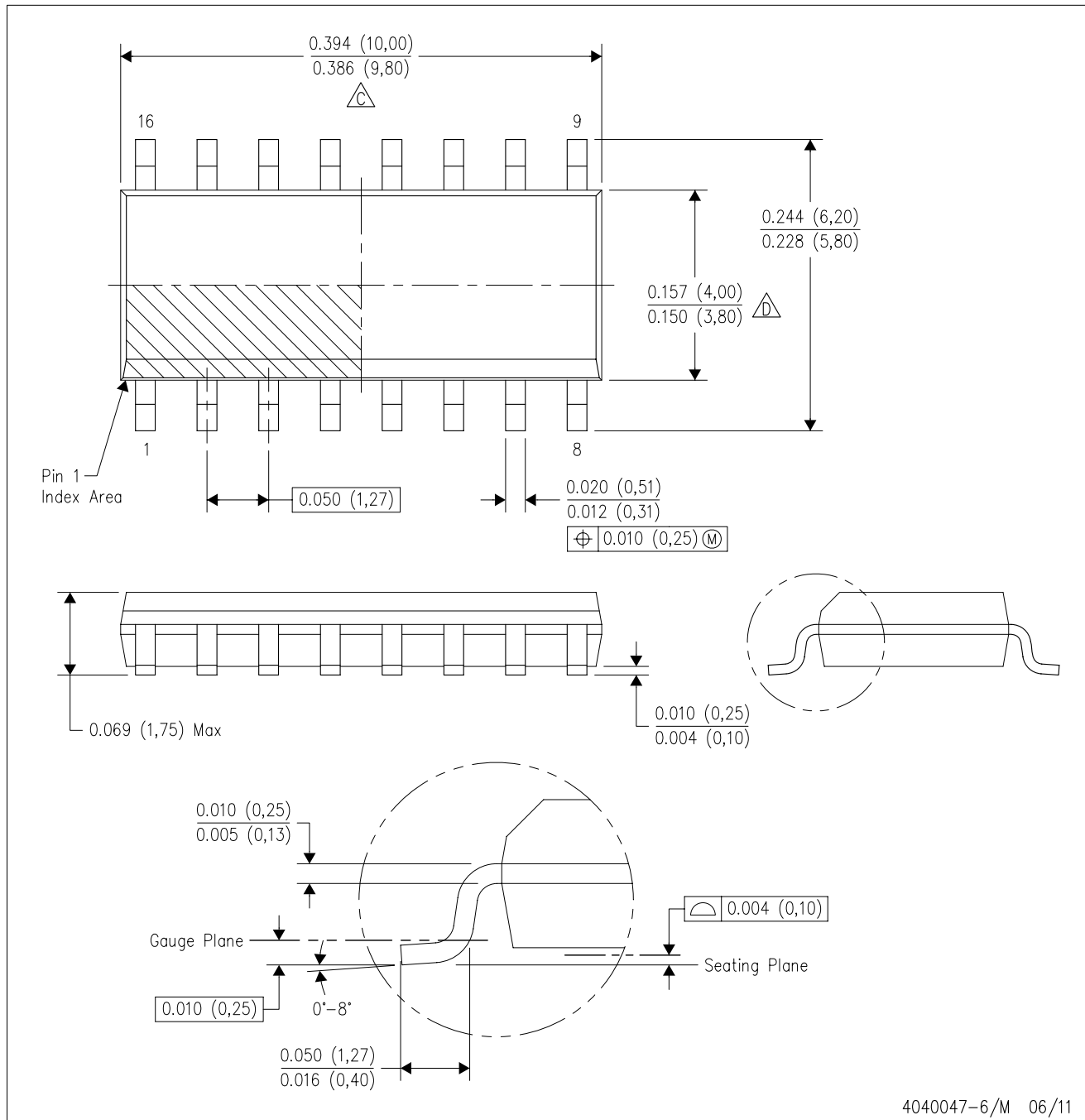
NOTES: A.   All linear dimensions are in inches (millimeters).
          B.   This drawing is subject to change without notice.
       ⚠C.   Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall
               not exceed 0.006 (0,15) each side.
       ⚠D.   Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
          E.   Reference JEDEC MS−012 variation AC.
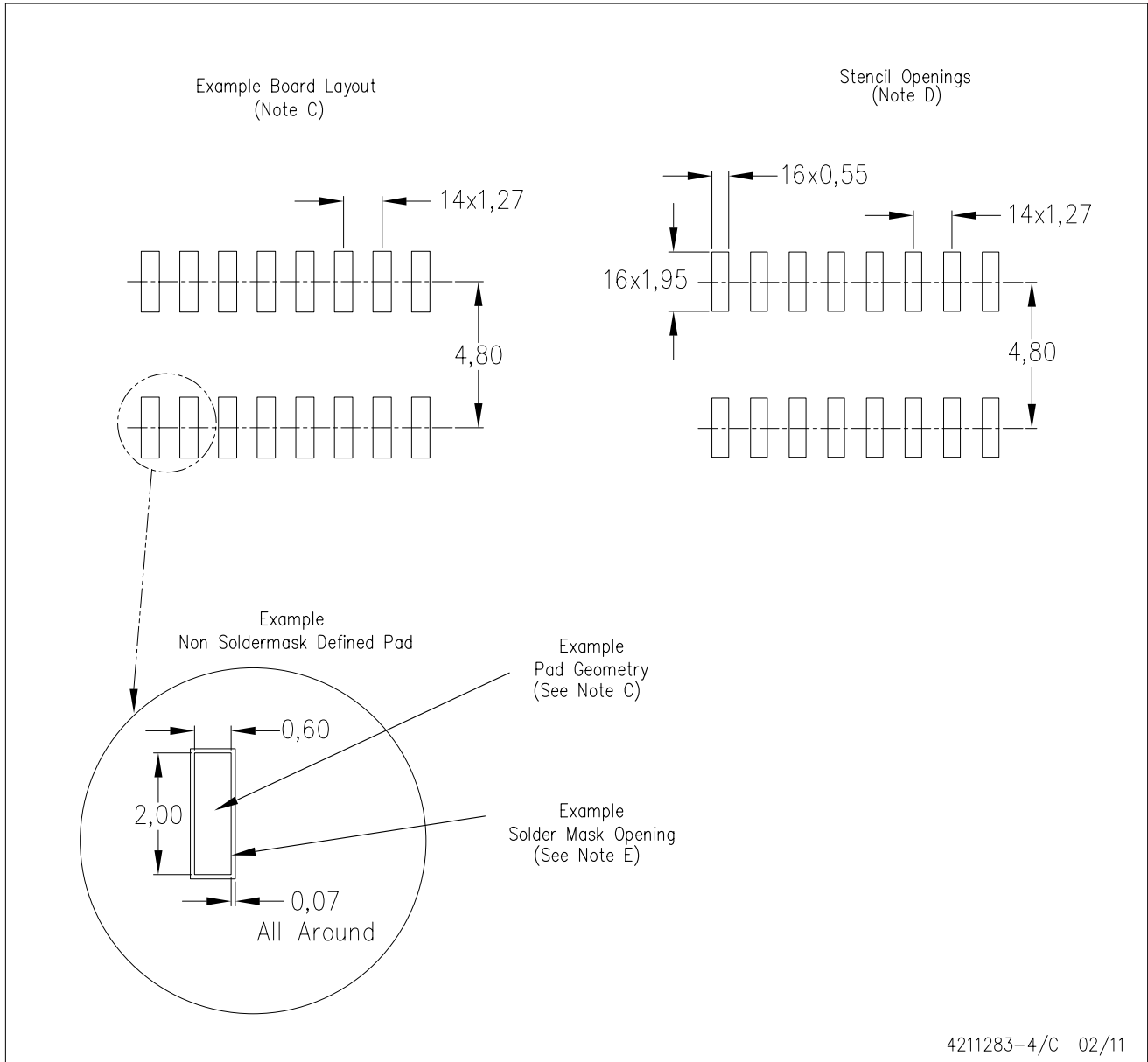
TEXAS
INSTRUMENTS
www.ti.com

D (R−PDSO−G16)   PLASTIC SMALL OUTLINE

Example Board Layout
(Note C)

14x1,27

4,80

Stencil Openings
(Note D)

16x0,55

16x1,95

14x1,27

4,80

Example
Non Soldermask Defined Pad

Example
Pad Geometry
(See Note C)

0,60

2,00

Example
Solder Mask Opening
(See Note E)

0,07

All Around

4211283−4/C 02/11

NOTES: A. All linear dimensions are in millimeters.
         B. This drawing is subject to change without notice.
         C. Publication IPC−7351 is recommended for alternate designs.
         D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should
             contact their board assembly site for stencil design recommendations. Refer to IPC−7525 for other stencil recommendations.
         E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

PW (R−PDSO−G24)   PLASTIC SMALL OUTLINE

0,65

$\dfrac{0,30}{0,19}$

⊕ | 0,10 Ⓜ

24   13

D | $\dfrac{4,50}{4,30}$ $\dfrac{6,60}{6,20}$

1   12

$\dfrac{7,90}{7,70}$

C

0,15 NOM

Gage Plane

0,25

0°−8°

$\dfrac{0,75}{0,50}$

1,20 MAX

$\dfrac{0,15}{0,05}$

Seating Plane

⌒ | 0,10
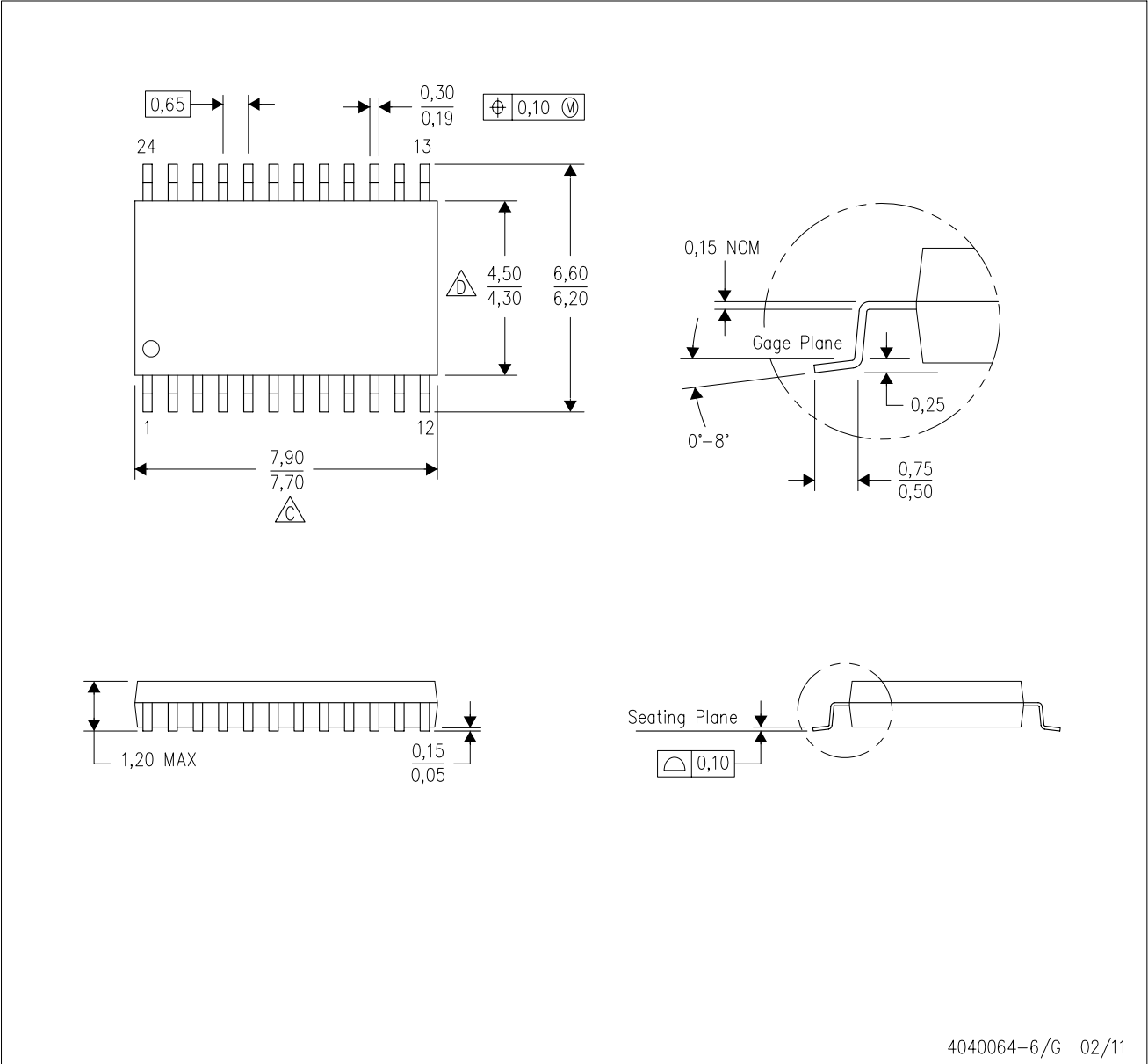
4040064−6/G 02/11

NOTES: A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M−1994.
  B. This drawing is subject to change without notice.
  C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
  D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
  E. Falls within JEDEC MO−153

PW (R-PDSO-G24)   PLASTIC SMALL OUTLINE
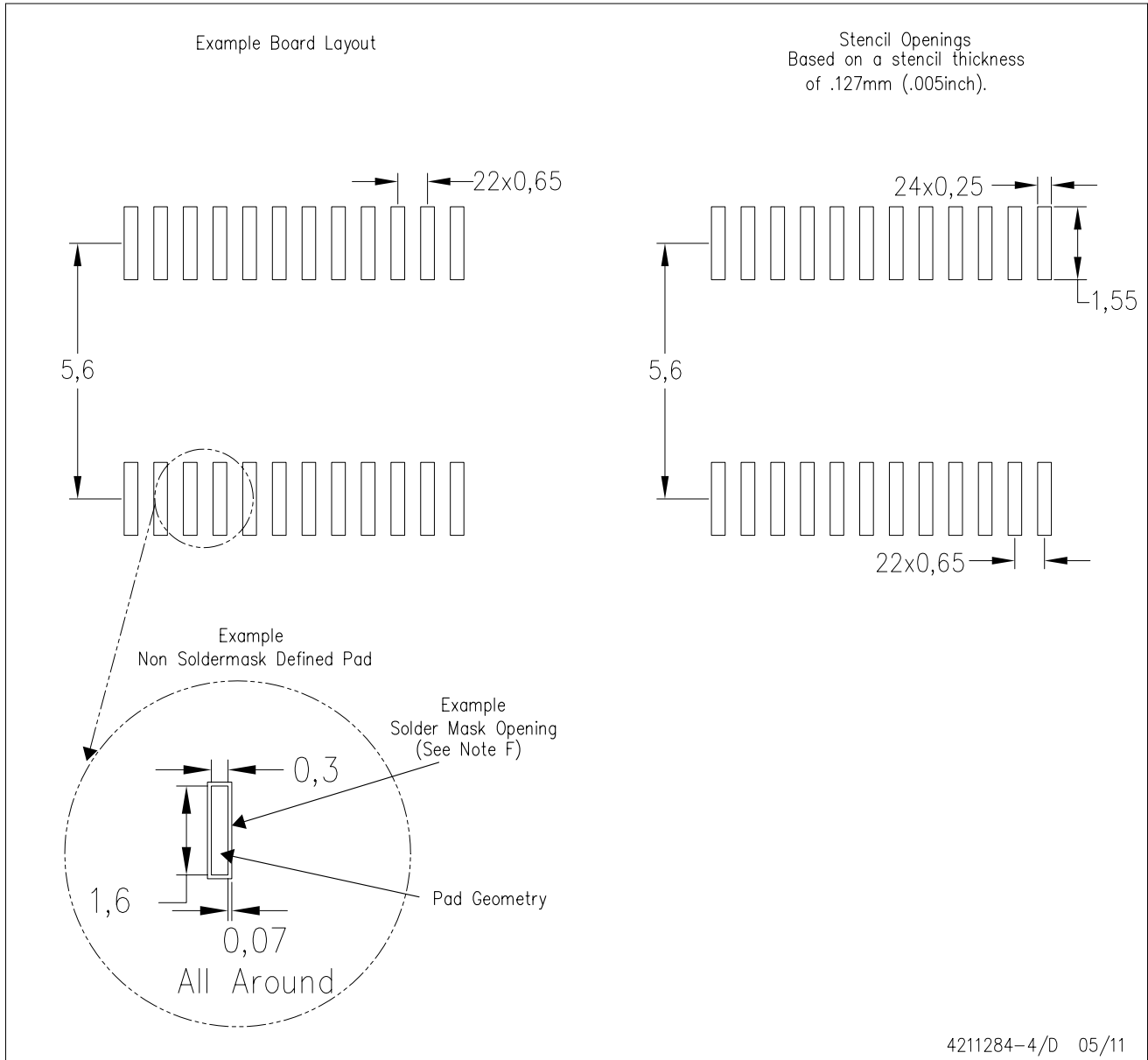
Example Board Layout

Stencil Openings
Based on a stencil thickness
of .127mm (.005inch).

22x0,65

24x0,25

1,55

5,6

5,6

22x0,65

Example
Non Soldermask Defined Pad

Example
Solder Mask Opening
(See Note F)

0,3

1,6

Pad Geometry

0,07

All Around

4211284-4/D 05/11

NOTES: A.   All linear dimensions are in millimeters.
         B.   This drawing is subject to change without notice.
         C.   Publication IPC-7351 is recommended for alternate design.
         D.   Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should
              contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
         E.   Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

www.BDTIC.com/TI