8-CHANNEL POWER SUPPLY SEQUENCER AND MONITOR WITH ERROR LOGGING

FEATURES

- **Single Supply Voltage: 3.3V**
- **Low Power Consumption: 3mA Nominal Supply Current**
- **Sequences and Monitors Eight Voltage Rails**
- **Rail Voltages Sampled With 3.2-mV Resolution**
- **Internal or External Voltage Reference**
- **Four Configurable Digital Outputs for Power-On Reset and Other Functions**
- **Configurable Digital Output Polarity**
- **Flexible Rail Sequencing Based On Timeline (ms), Parent Rail Regulation Window, Or Parent Rail Achieving Defined Threshold**
- **Independent Under- and Overvoltage Thresholds Per Rail**
- **Configurable Regulation Expiration Times Per Rail**
- **Flexible Alarm Processing: Ignore, Log Only, Retry n Times, Retry Continuously, Sequence, Parent Rail Can Shutdown Child Rails**
- **Alarm Conditions Logged With Timestamp: Under- and Overvoltage Glitch, Sustained Under- and Overvoltage, Rail Did Not Start**
- **On-chip Flash for Storing User Data**
- **Error Logging to Flash for System Failure Analysis**
- **I²C™ Interface for Configuration and Monitoring**
- **Microsoft™ Windows™ GUI for Configuration and Monitoring**

APPLICATIONS

- **Telecommunications Switches**
- **Servers**
- **Networking Equipment**
- **Test Equipment**
- **Industrial**
- **Any System Requiring Sequencing of Multiple Voltage Rails**

DESCRIPTION

The UCD9081 power-supply sequencer controls the enable sequence of up to eight independent voltage rails and provides four general-purpose digital outputs (GPO). The device operates from a 3.3-V supply, provides 3.2-mV resolution of voltage rails, and requires no external memory or clock. The UCD9081 monitors the voltage rails independently and has a high degree of rail sequence and alarm response options. The sequencing of rails can be based on timed events or on timed events in conjunction with other rails achieving regulation or a voltage threshold. In addition, each rail is monitored for undervoltage and overvoltage glitches and thresholds. Each rail the UCD9081 monitors can be configured to shut down a user-defined set of other rails and GPOs, and alarm conditions are monitored on a per-rail basis.

Figure 1 shows the UCD9081 power-supply sequencer in a typical application.

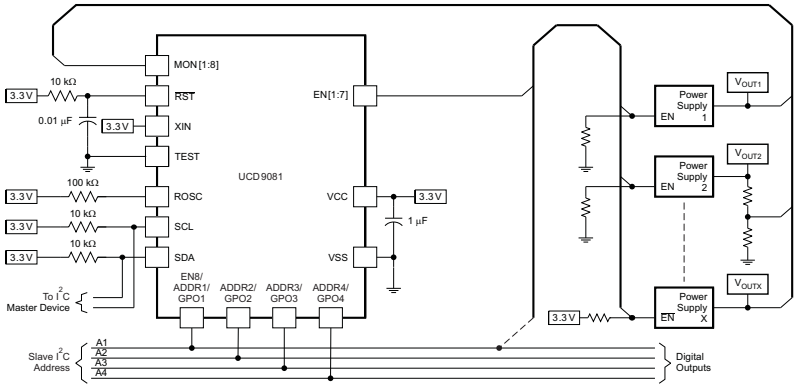

Figure 1. Typical Application Diagram

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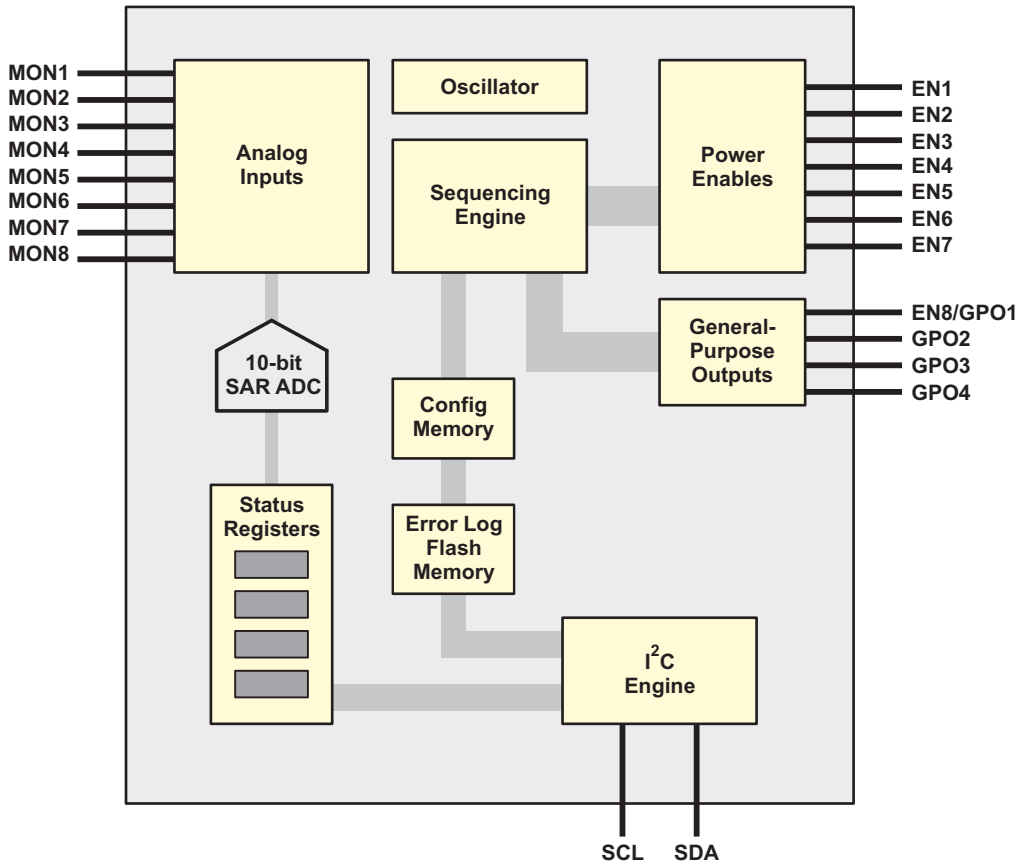
These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

FUNCTIONAL BLOCK DIAGRAM



ORDERING INFORMATION

For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI Web site at www.ti.com.

RHB PACKAGE
(TOP VIEW)

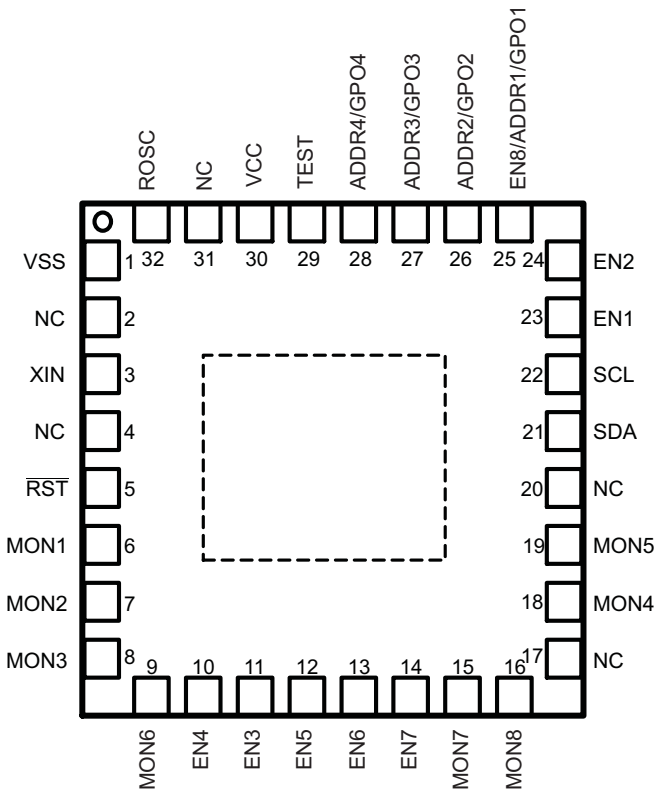


Table 1. PIN FUNCTIONS

PIN		I/O	DESCRIPTION
NAME	NO.		
ADDR2/GPO2	26	I/O	I^2C address select 2, general-purpose digital output 2.
ADDR3/GPO3	27	I/O	I^2C address select 3, general-purpose digital output 3.
ADDR4/GPO4	28	I/O	I^2C address select 4, general-purpose digital output 4.
EN1	23	I/O	Voltage rail 1 enable (digital output).
EN2	24	I/O	Voltage rail 2 enable (digital output).
EN3	11	I/O	Voltage rail 3 enable (digital output).
EN4	10	I/O	Voltage rail 4 enable (digital output).
EN5	12	I/O	Voltage rail 5 enable (digital output).
EN6	13	I/O	Voltage rail 6 enable (digital output).
EN7	14	I/O	Voltage rail 7 enable (digital output).
EN8/ADDR1/ GPO1	25	I/O	Voltage rail 8 enable (digital output), I^2C address select 1, general-purpose digital output 1
MON1	6	I	Analog input for voltage rail 1.
MON2	7	I	Analog input for voltage rail 2.
MON3	8	I	Analog input for voltage rail 3.
MON4	18	I	Analog input for voltage rail 4.
MON5	19	I	Analog input for voltage rail 5.
MON6	9	I	Analog input for voltage rail 6.
MON7	15	I	Analog input for voltage rail 7.
MON8	16	I	Analog input for voltage rail 8.
NC	2		Do not connect.
NC	4,17, 20, 31		Recommended to connect to V_{SS}, pin is not connected internally.
ROSC	32		Internal oscillator frequency adjust. Must use 100-kΩ pullup to V_{CC} for minimum drift and maximum frequency when sampling voltage rails.
$\overline{RST}$	5	I	Reset input.
SCL	22	I/O	I^2C clock. Must pull up to 3.3 V.
SDA	21	I/O	I^2C data. Must pull up to 3.3 V.
TEST	29	I	Connect to V_{SS}
V_{CC}	30		Supply voltage
V_{SS}	1		Ground reference
XIN	3		Connect to V_{CC}
PowerPAD™	Package Pad		Package Pad. Recommended to connect to V_{SS}.

ABSOLUTE MAXIMUM RATINGS(1)

		VALUE	UNIT
	Voltage applied from V_{CC} to V_{SS}	–0.3 to 4.1	V
	Voltage applied to any pin(2)	–0.3 to V_{CC} + 0.3	V
	ESD Diode current at any device terminal	±2	mA
T_{stg}	Storage temperature	–40 to 85	°C

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltages referenced to V_{SS}.

RECOMMENDED OPERATING CONDITIONS

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage during operation	3	3.3	3.6	V
	Supply during configuration changes	3	3.3	3.6	
T_A	Operating free-air temperature range	–40		85	°C

ELECTRICAL CHARACTERISTICS

These specifications are over recommended ranges of supply voltage and operating free-air temperature, unless otherwise noted

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
SUPPLY CURRENT							
I_S	Supply current into V_{CC}, excluding external current	T_A = 25°C			3	4	mA
I_C	Supply current during configuration	V_{CC} = 3.6 V			3	7	mA
STANDARD INPUTS (RST, TEST)							
V_{IL}	Low-level input voltage	V_{CC} = 3 V		V_{SS}		V_{SS} + 0.6	V
V_{IH}	High-level input voltage	V_{CC} = 3 V		0.8 V_{CC}		V_{CC}	V
SCHMITT TRIGGER INPUTS (SDA, SCL, EN1, EN2, EN3, EN4, EN5, EN6, EN7, EN8/ADDR1, ADDR2, ADDR3, ADDR4)							
V_{IT+}	Positive-going input threshold voltage	V_{CC} = 3 V		1.5		1.9	V
V_{IT-}	Negative-going input threshold voltage	V_{CC} = 3 V		0.9		1.3	V
V_{hys}	Input voltage hysteresis, (V_{IT+} – V_{IT-})	V_{CC} = 3 V		0.5		1	V
I_{lkg}	High impedance leakage current					±50	nA
ANALOG INPUTS (MON1, MON2, MON3, MON4, MON5, MON6, MON7, MON8, ROSC)							
V_{CC}	Analog supply voltage	V_{SS} = 0 V		3		3.6	V
$V_{MON<1..8>}$	Analog input voltage	Internal voltage reference selected		0		2.5	V
		External voltage reference selected (V_{CC} used as reference)		0		V_{CC}	
C_I(1)	Input capacitance	Only one terminal can be selected at a time (MON1–MON8)				27	pF
R_I(1)	Input MUX ON resistance	0 V ≤ V_{MONx} ≤ V_{CC}, V_{CC} = 3V				2000	Ω
I_{lkg}	High-impedance leakage current	MON1–MON8				±50	nA
V_{REF+}	Positive internal reference voltage	Internal voltage reference selected, V_{CC} = 3V		2.35	2.5	2.65	V
V_{TUE}	ADC Total unadjusted error	V_{R+}= 2.5V (Internal reference)	V_{CC} = 3V			±12.2	mV
		V_{R+}= V_{CC} (External reference)				±14.7	
T_{REF+}(1)	Temperature coefficient of internal voltage reference	$I_{(VREF+)}$ is a constant in the range of 0 mA ≤ $I_{(VREF+)}$ ≤ 1 mA, V_{CC} = 3V				±100	ppm/°C

(1) Not production tested. Limits verified by design.

ELECTRICAL CHARACTERISTICS (continued)

These specifications are over recommended ranges of supply voltage and operating free-air temperature, unless otherwise noted

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
MISCELLANEOUS						
$T_{retention}$	Retention of configuration parameters	T_J = 25°C	100			Years
POR, BROWNOUT, RESET (see (2) (3))						
$t_{d(BOR)}$	Brownout				2000	µs
$V_{CC(start)}$		$dV_{CC}/dt \le 3V/s$		0.7×V(B_IT-)		V
$V_{(B\_IT-)}$					1.71	V
$V_{hys(B\_IT-)}$			70	130	180	mV
$t_{(reset)}$		Pulse length needed at RST pin to accept reset internally, V_{CC} = 3V	2			µs
DIGITAL OUTPUTS (EN8/GPO1, GPO2, GPO3, GPO4, EN1, EN2, EN3, EN4, EN5, EN6, EN7, SDA, SCL)						
V_{OH}	High-level output voltage	I_{OH}(max) = –1.5 mA, (4) V_{CC} = 3V	V_{CC} – 0.25		V_{CC}	V
		I_{OH}(max) = –6 mA, (5) V_{CC} = 3V	V_{CC} – 0.6		V_{CC}	
V_{OL}	Low-level output voltage	I_{OL}(max) = 1.5 mA, (4) V_{CC} = 3V	V_{SS}		V_{SS} + 0.25	V
		I_{OL}(max) = 6 mA, (5) V_{CC} = 3V	V_{SS}		V_{SS} + 0.6	
I_{lkg}	High-impedance leakage current	V_{CC} = 3V			±50	nA

(2) The current consumption of the brown-out module is already included in the I_{CC} current consumption data.
(3) During power up, device initialization starts following a period of $t_{d(BOR)}$ after $V_{CC} = V_{(B\_IT-)} + V_{hys(B\_IT-)}$.
(4) The maximum total current, I_{OH}max and I_{OL}max, for all outputs combined, should not exceed ±12 mA to hold the maximum voltage drop specified.
(5) The maximum total current, I_{OH}max and I_{OL}max, for all outputs combined, should not exceed ±48 mA to hold the maximum voltage drop specified.

DIGITAL OUTPUTS (only one output is loaded at a time)

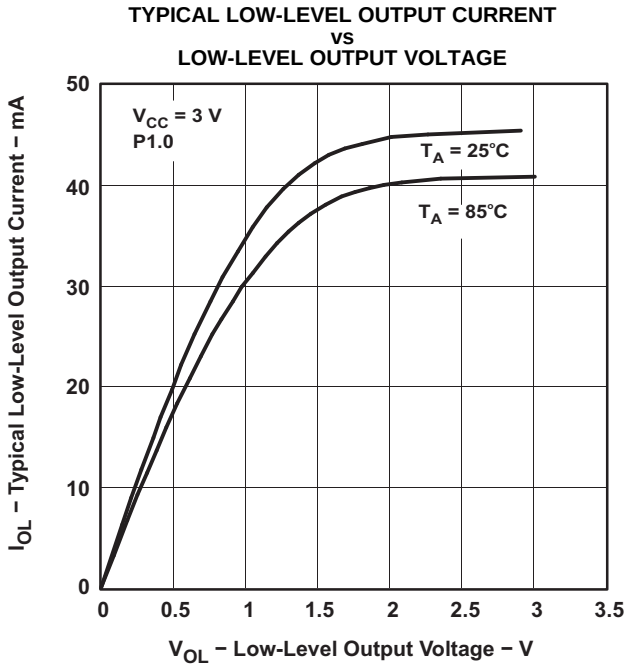


Figure 2.

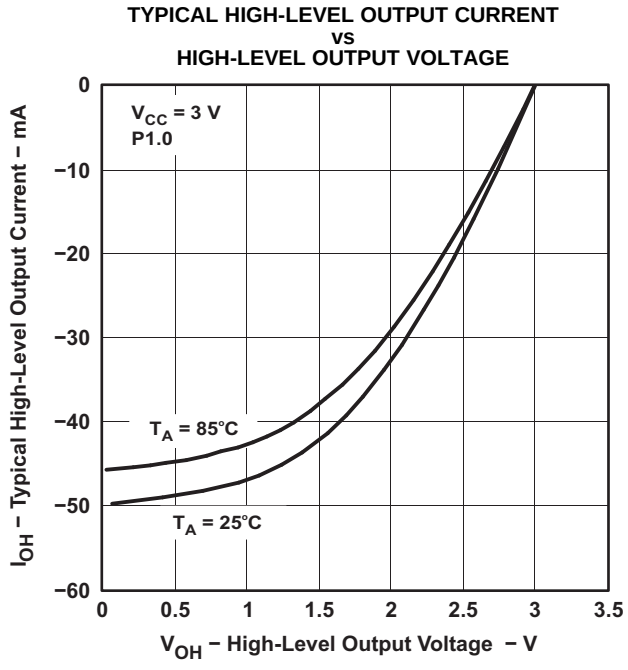


Figure 3.

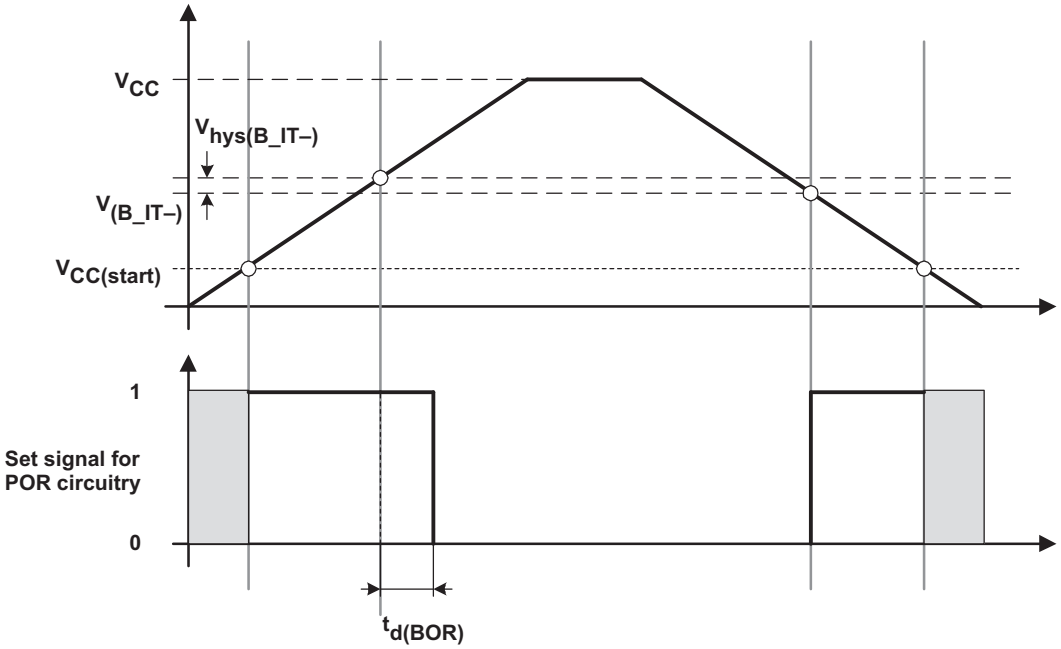


Figure 4. POR/Brownout Reset (BOR) vs Supply Voltage

DIGITAL OUTPUTS (only one output is loaded at a time) (continued)

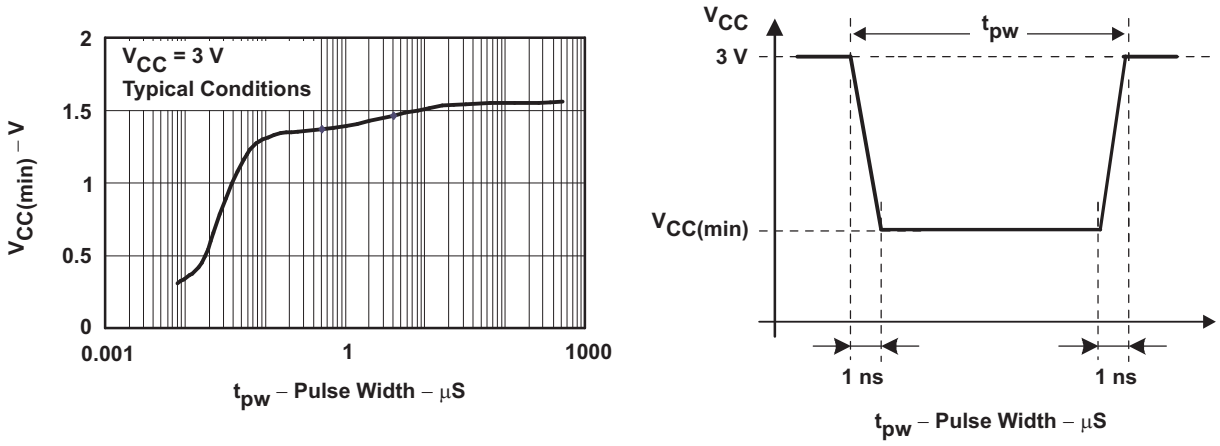


Figure 5. $V_{CC(min)}$ Level with a Square Voltage Drop to Generate a POR/Brownout Signal

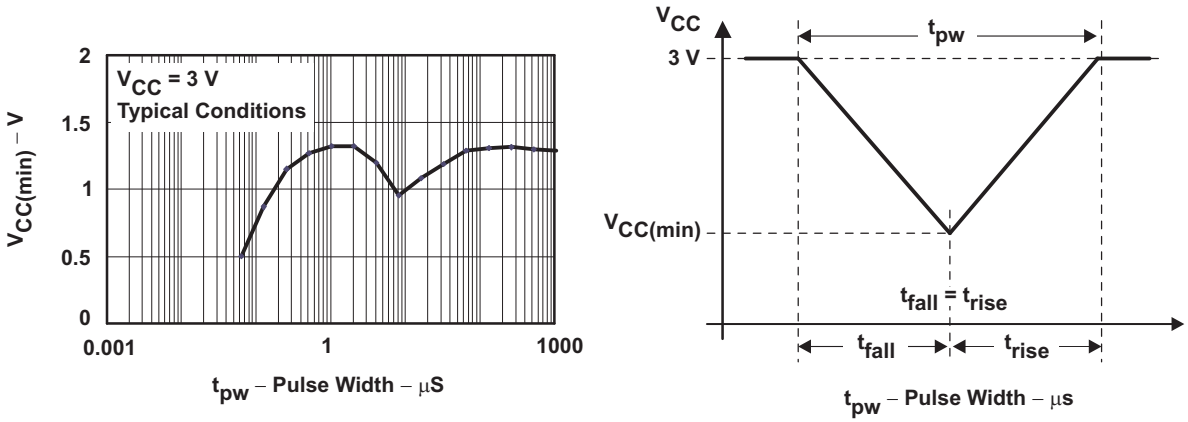


Figure 6. $V_{CC(min)}$ Level with a Triangle Voltage Drop to Generate a POR/Brownout Signal

FUNCTIONAL DESCRIPTION

POWER SUPPLY SEQUENCING

The UCD9081 can be configured to sequence power supply rails using the enable signals (ENx) or the general-purpose outputs (GPOx) in one of four ways:

1. A rail can be configured to not be sequenced
2. Using a delay time after UCD9081 RESET. The enable/GPO is asserted after UCD9081 RESET plus the user specified delay
3. Using a delay time after another (parent) rail has achieved regulation (V_{RAIL} is within specified under- and overvoltage settings). The enable/GPO is asserted after the (parent) rail is in regulation plus the user specified delay.
4. Using a (parent) rail voltage. The enable/GPO is asserted after the (parent) rail voltage is greater than or equal to the user specified voltage.

POWER-SUPPLY ENABLES

The UCD9081 can sequence and enable/disable up to eight power supplies through the ENx (EN1 to EN8) signals. These signals can be configured active-high or active-low, supporting power supplies with either polarity.

EN8 can also be configured as a GPO (GPO1). EN8/ADDR1/GPO1 is also used for I^2C address selection (ADDR1).

Note that while the UCD9081 is in RESET, the enable signals are in a high-impedance state. The enable signals should be pulled up or down on the board according to the desired default power-supply state (enabled or disabled).

GENERAL PURPOSE OUTPUTS

The UCD9081 can control up to four general-purpose digital outputs through the same sequencing mechanisms as the power supply enables. These general-purpose outputs (GPO1–GPO4) can be used for digital signals such as resets or status inputs to other devices. Note that these signals are multiplexed with other functions (primarily I^2C address selection). See the *Terminal Functions* table to ensure that these signals are used properly by the application. Also note that the GPO1 signal is multiplexed with EN8.

I^2C INTERFACE

The UCD9081 power-supply sequencer has a 100 kHz, slave mode I^2C interface for communication with an I^2C master. The I^2C master uses this interface to configure and monitor the UCD9081. Note that the master must support clock stretching in order to properly communicate with the UCD9081.

DEVICE RESET

UCD9081 RESET occurs due to one of the following conditions:

- External $\overline{\text{RST}}$ pin is asserted
- Power is applied to the device (power-on-reset) or power is cycled
- A sequence event occurs as a result of a configured rail alarm event
- RESTART command is issued over the I^2C bus

During RESET, the following takes place:

- All ENx and GPOx pins are placed in a high-impedance state
- All internal timers are reset to zero
- The I^2C address pins (ADDR1-ADDR4) are sampled and the device address is assigned accordingly
- All ENx and GPOx pins are driven to their inactive levels
- The UCD9081 runs a checksum function to validate its memory contents
- If there are no errors, the device starts sequencing according to the current sequencer configuration

During this time, the UCD9081 will not respond to host requests made over the I^2C bus.

In order to ensure the integrity of data within the device, the device runs a checksum function during RESET. If the configuration parameters of the device are valid, the UCD9081 will begin operating according to the current sequencer configuration. If the configuration parameters are invalid, the UCD9081 will overwrite the current configuration parameters with the last known good configuration and the device will begin operating with these parameters. This can cause a delay in the RESET time. Note that in order to establish a copy of the valid configuration, UCD9081 RESET time will be delayed the first time a new configuration is loaded.

VOLTAGE REFERENCE

The analog to digital converter in the UCD9081 has a selectable voltage reference, V_{R+}. The voltage reference can either be an internally generated 2.5V reference or an external reference derived from V_{CC}. The external reference is recommended for those systems requiring more accurate voltage readings. See the *Estimating UCD9081 Reporting Accuracy Over Variations In ADC Voltage Reference* section for information on calculating the accuracy of each reference.

VOLTAGE MONITORING

The UCD9081 can monitor eight voltage rails through the MONx terminals of the device (MON1–MON8). The UCD9081 samples these eight input channels and uses the selected reference to convert the voltages to digital values. These values are accessible via the I^2C interface. When monitoring a voltage rail that has a nominal voltage larger than the selected reference, a resistor divider network is typically used. The design must ensure that the source impedance of the resistor network is chosen properly in order to maintain the accuracy of the analog to digital conversion. For more details, see the *Application Information* section.

The UCD9081 allows the user to independently specify the following for each monitored rail:

- overvoltage threshold (OV)
- undervoltage threshold (UV)
- out of regulation time or glitch width (OORW)
- maximum time for regulation (MTFR)

The MTFR is used to determine whether or not a rail starts successfully after being enabled.

The UCD9081 also has the ability to ignore glitches. Glitches are fault conditions that last less than the specified OORW for that rail. Ignoring glitches may be useful in the case where the power supply is known to be noisy but still operates well. Ignoring glitches does not affect the monitoring capability of the UCD9081 with respect to detecting sustained UV or OV faults. It simply prevents the UCD9081 from logging glitch faults to the error log.

RAIL SHUTDOWN

Rail (or GPO) shutdown is the act of setting the ENx (or GPOx) pin to a state which disables the associated power supply output. A rail can shutdown for one of the following reasons:

- A fault condition on the rail itself
- A fault condition on a parent rail resulting in a shutdown
- An I^2C shutdown command

Each rail and GPO can be independently configured to shutdown according to a user-specified time delay between 0 - 4095 ms. This is referred to as the system shutdown configuration.

ALARM PROCESSING

Each rail can be independently configured to respond to an alarm or fault in a variety of ways. A fault can be an UV condition, OV condition, or a rail that did not start (MTFR exceeded before UV threshold achieved). The options for alarm processing are as follows:

- Ignore
- Log only
- Retry n times (n = 0,1,2,3,4)
- Retry continuously
- Sequence (immediately)
- Sequence After Shutdown

In addition to these options, a rail can be independently configured to log errors to FLASH to aid in failure analysis. For more details, see the section on *Error Logging*.

IGNORE

The UCD9081 can be configured to ignore all alarms on the rail. This is the recommended option for all unused power supply rails on the UCD9081.

LOG ONLY

The UCD9081 can be configured to log a fault and take no additional action. For more information, see the section on *Error Logging*.

RETRY n TIMES

The UCD9081 can be configured to attempt to restart a rail up to n times (n = 0,1,2,3, or 4) in response to a sustained fault condition. With this option, the user can also specify which rails and GPOs are dependent upon the configured rail. When a sustained fault is detected, the faulty rail will be disabled and re-enabled the desired number of times. The rail remains enabled for the specified MTFR before attempting another retry. If the rail does not achieve regulation after the desired number of retries, all user-specified dependent rails and GPOs will be shutdown according to the times specified in the system shutdown configuration. Note that if any of the dependent rails have other rails or GPOs marked as dependents, those dependent rails or GPOs will also be forced to shutdown regardless of their alarm processing configurations.

RETRY CONTINUOUSLY

The UCD9081 can be configured to continuously attempt to restart a faulty rail. When the UCD9081 detects a sustained fault condition on the configured rail, the rail is disabled and then re-enabled. The rail remains enabled for the specified MTFR. The retry process repeats for this rail until it properly achieves regulation.

SEQUENCE

The UCD9081 can be configured to sequence the entire system in response to a sustained fault condition. When the UCD9081 detects a fault on the configured rail, all rails and GPOs are shutdown immediately and UCD9081 RESET occurs (see section on *Device Reset*). Note that for this configuration, a shutdown according to the delay times specified by the system shutdown configuration does not occur prior to UCD9081 RESET.

SEQUENCE AFTER SHUTDOWN

Sequence after shutdown is an option that can be used in conjunction with *Retry n Times*. When a fault occurs on the configured rail, this option forces a UCD9081 RESET to occur after the procedure outlined in *Retry n Times* takes place. Note that if a rail is configured for sequence after shutdown and is forced to shutdown due to a fault on a parent rail, a sequence after shutdown will take place.

ERROR LOGGING

The UCD9081 is capable of logging errors in two ways. The first method uses an eight-deep FIFO located in volatile memory (SRAM) of the UCD9081. Error conditions are posted to the ERROR registers according to the configuration for that rail. The UCD9081 logs the type of error, the time (from Reset) when the error occurred, the rail number, and the rail voltage. If the user has specified *ignore glitches* as an option for the faulty rail, glitches will not be posted to the error log. If the user has specified *Ignore* as the alarm response for the faulty rail, no errors will be posted to the error log for that rail. All other alarm responses will result in the error condition being logged. Due to the unknown latency of the host extracting data from the FIFO, the UCD9081 only posts to the FIFO is if it has room to write. There is no impact to the monitoring operation of the UCD9081 if this FIFO is full and cannot be written.

The second method of error logging uses the non-volatile memory (FLASH) of the UCD9081. Similar to the error log in SRAM, faults will be posted for all rails that have the appropriate alarm processing options selected. In this case, errors will be posted to both the SRAM log and the FLASH log. The UCD9081 is capable of recording up to eight entries in the flash error log. Again, the UCD9081 will only post to the log if there is room to write. There is no impact to the monitoring operation of the UCD9081 if the error log is full and cannot be written.

In order to provide flexibility for a variety of systems, the UCD9081 has two modes for non-volatile error logging. The first mode configures the UCD9081 to hold in RESET when entries are present in the FLASH error log. This is advantageous in systems where a master I^2C device is available to read the error log following a critical system failure. When configured for this mode, the UCD9081 will check for a non-empty FLASH error log during RESET. If there are entries in the FLASH error log, the device will wait for a host to clear the error log before sequencing the device. For information on clearing the FLASH error log, see the section on *Resetting the Flash Error Log*.

The second mode allows the UCD9081 to sequence (following a RESET of the device) regardless of whether or not there are entries present in the FLASH error log. This is useful in systems with no master I^2C device, or where power cycles are common and not due to system failure.

For information on reading the error logs in each mode, see the section on *Monitoring the UCD9081.*

BROWNOUT

The brownout circuit is implemented to provide the proper internal reset signal to the device during power on and power off.

CONFIGURING AND MONITORING THE UCD9081

The UCD9081 supports both configuration and monitoring using its I^2C slave interface. A Microsoft™ Windows™ GUI is available for configuring and monitoring the UCD9081. This GUI can be downloaded from the TI website at www.ti.com.

For monitoring the sequencer, an I^2C memory map allows an I^2C host to perform memory-mapped reads (and in some cases writes) to obtain status information from the UCD9081. For instance, all rails can report their voltage through the I^2C memory map. For information on which parameters are available via the I^2C memory map, see the *Monitoring the UCD9081* section.

To change configuration parameters of the sequencer, a different mechanism is used. The entire set of configuration parameters must be written at one time to the device as one large transaction over the I^2C interface. This ensures that the configuration of the device is consistent at any given time. The process for configuring the UCD9081 is described in the *Configuring the UCD9081* section.

MONITORING THE UCD9081

Register Map

The UCD9081 allows all monitoring of the system through the I^2C interface on the device. The following is the memory map of the supported registers in the system. The detail of each of these registers is given in the next section as well.

Note that the UCD9081 supports functionality to increment the I^2C register address value automatically when a register is being accessed in order to more efficiently access blocks of like registers. The following table also shows the amount that the register address is incremented for each register access.

REGISTER NAME	ADDRESS	ACCESS	ADJUSTMENT AFTER ACCESS
RAIL1H	0x00	r	+1 (0x01)
RAIL1L	0x01	r	+1 (0x02)
RAIL2H	0x02	r	+1 (0x03)
RAIL2L	0x03	r	+1 (0x04)
RAIL3H	0x04	r	+1 (0x05)
RAIL3L	0x05	r	+1 (0x06)
RAIL4H	0x06	r	+1 (0x07)
RAIL4L	0x07	r	+1 (0x08)
RAIL5H	0x08	r	+1 (0x09)
RAIL5L	0x09	r	+1 (0x0A)
RAIL6H	0x0A	r	+1 (0x0B)
RAIL6L	0x0B	r	+1 (0x0C)
RAIL7H	0x0C	r	+1 (0x0D)
RAIL7L	0x0D	r	+1 (0x0E)
RAIL8H	0x0E	r	+1 (0x0F)
RAIL8L	0x0F	r	–15 (0x00)
ERROR1	0x20	r	+1 (0x21)
ERROR2	0x21	r	+1 (0x22)
ERROR3	0x22	r	+1 (0x23)
ERROR4	0x23	r	+1 (0x24)
ERROR5	0x24	r	+1 (0x25)
ERROR6	0x25	r	–5 (0x20)
STATUS	0x26	r	0 (0x26)
VERSION	0x27	r	0 (0x27)
RAILSTATUS1	0x28	r	+1 (0x29)
RAILSTATUS2	0x29	r	–1 (0x28)
FLASHLOCK	0x2E	rw	0 (0x2E)
RESTART	0x2F	w	0 (0x2F)
WADDR1	0x30	rw	+1 (0x31)
WADDR2	0x31	rw	–1 (0x30)
WDATA1	0x32	rw	+1 (0x33)
WDATA2	0x33	rw	–1 (0x32)

Register Descriptions

The following are the detailed descriptions of each of the UCD9081 I^2C registers.

The following register bit conventions are used. Each register is shown with a key indicating the accessibility of each bit, and the initial condition after device initialization.

KEY	ACCESS
rw	Read/write
r	Read-only
r0	Read as 0
r1	Read as 1
w	Write-only
w0	Write as 0
w1	Write as 1
rc	Read clears bit after read
rs	Read sets bit after read
-0, -1	Condition after initialization

RAIL

For each of eight voltage rails, the UCD9081 has two registers that contain the rolling average voltage for the associated rail as measured by the device. This average voltage is maintained in real-time by the UCD9081 and is calculated as the output of a 4-TAP FIR filter. There are two registers for each voltage rail. One holds the least-significant 8 bits of the voltage and the other the most-significant 2 bits of the voltage. This is shown in the following table.

REGISTER NAME	ADDRESS	REGISTER CONTENTS
RAIL1H	0x00	RAIL1 voltage, bits 9:8
RAIL1L	0x01	RAIL1 voltage, bits 7:0
RAIL2H	0x02	RAIL2 voltage, bits 9:8
RAIL2L	0x03	RAIL2 voltage, bits 7:0
RAIL3H	0x04	RAIL3 voltage, bits 9:8
RAIL3L	0x05	RAIL3 voltage, bits 7:0
RAIL4H	0x06	RAIL4 voltage, bits 9:8
RAIL4L	0x07	RAIL4 voltage, bits 7:0
RAIL5H	0x08	RAIL5 voltage, bits 9:8
RAIL5L	0x09	RAIL5 voltage, bits 7:0
RAIL6H	0x0A	RAIL6 voltage, bits 9:8
RAIL6L	0x0B	RAIL6 voltage, bits 7:0
RAIL7H	0x0C	RAIL7 voltage, bits 9:8
RAIL7L	0x0D	RAIL7 voltage, bits 7:0
RAIL8H	0x0E	RAIL8 voltage, bits 9:8
RAIL8L	0x0F	RAIL8 voltage, bits 7:0

A rail voltage is read with a 16b access. The auto-increment feature of the UCD9081 allows multiple rail voltages to be read with a single access.

A rail voltage is provided as a 10-bit binary value in an unsigned format, as shown following.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
						RAILVn									
r0	r0	r0	r0	r0	r0	r	r	r	r	r	r	r	r	r	r

The following formulas can be used to calculate the actual measured rail voltage:

Without external voltage divider:

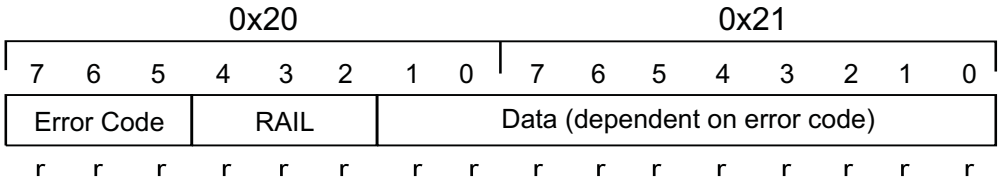
$$V_{RAILn} = \frac{RAILVn}{1024} \times V_{R+} \quad (1)$$

With external voltage divider:

$$V_{RAILn} = \frac{RAILVn}{1024} \times V_{R+} \times \frac{R_{PULLDOWN} + R_{PULLUP}}{R_{PULLDOWN}} \quad (2)$$

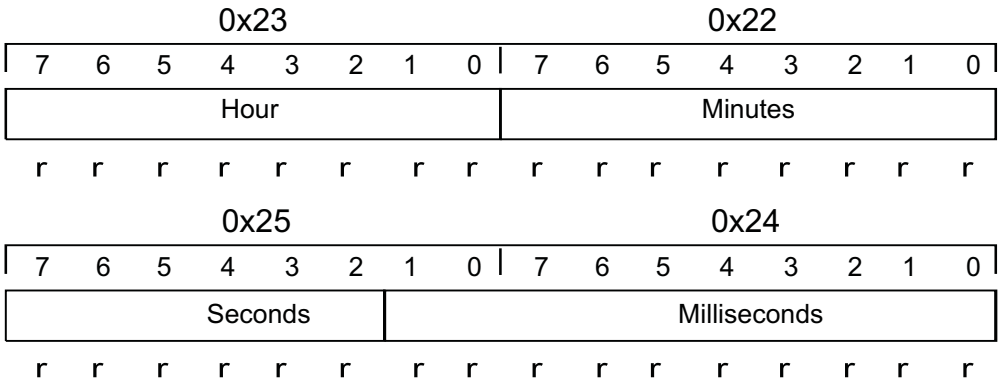
ERROR

Error conditions are logged by the UCD9081 and are accessible to the user via reading the ERROR register. This is a 6-byte register and it has the following format:



RAIL	Meaning	Rail #(n) – 1, RAIL = 0 through 7
Error Codes	**Meaning**	**Data**
0 0 0	Null alarm	0x0000
0 0 1	Supply did not start	Average voltage on rail
0 1 0	Sustained overvoltage detected	Average voltage on rail
0 1 1	Sustained undervoltage detected	Average voltage on rail
1 0 0	Overvoltage glitch detected	Glitch voltage level on rail
1 0 1	Undervoltage glitch detected	Glitch voltage level on rail
1 1 0	Reserved	Reserved
1 1 1	Reserved	Reserved

NOTE: When error code = *Null Alarm*, then the Hours, Minutes, Seconds, and Milliseconds fields are zero.



Faults encountered during operation post error logs as described in the section on *Error Logging* . This register set is used for reading the SRAM error log. They can also be used to read the FLASH error log when the UCD9081 is held in RESET. If the error log is empty, the ERROR register set will return all 0's (NULL ALARM) when read.

The values in registers 0x22 through 0x25 are reset to a value of 0 during UCD9081 RESET.

STATUS

STATUS is an 8-bit read-only register. This register provides real-time status information about the state of the UCD9081. The following bits are defined.

7	6	5	4	3	2	1	0
IIC Error	RAIL Error	NVERRLOG	FW Error	PARAM Error		Register Status	
rc-0	rc-0	r	r	r	r-0	rc-0	

IIC Error	Meaning
0	No I^2C PHY layer error
1	I^2C PHY layer error

Register Status	Meaning
00	No error
01	Invalid address
10	Read access error
11	Write access error

RAIL Error	Meaning
0	No RAIL error pending
1	RAIL error pending

NVERRLOG	Meaning
0	ERROR points to run-time error log
1	ERROR points to non-volatile log (if held in RESET) and entries present in non-volatile log

FW Error	Meaning
0	No Error (normal operation)
1	Device firmware error detected, device is idle

PARAM Error	Meaning
0	No Error (normal operation)
1	Parameters invalid, last config loaded

Reading of the STATUS register clears the register except for the NVERRLOG bit, which is maintained until the device is reset. Descriptions of the different errors are below.

The IICERROR bit is set when an I^2C access fails. This is most often a case where the user has accessed an invalid address or performed an illegal number of operations for a given register (for example, reading 3 bytes from a 2-byte register). In the event of an I^2C error when the IICERROR is set, bits 1:0 of the STATUS register further define the nature of the error as shown in the preceding figure.

The RAIL error bit is set to alert the user to an issue with one of the voltage rails. When this bit is set, the user is advised to query the RAILSTATUS register to further ascertain which RAIL input(s) have an issue. The user may then query the ERROR registers to get further information about the nature of the error condition.

The NVERRLOG bit is set to 1 upon device RESET if the UCD9081 contains entries in the FLASH error log. Note that this bit is the only bit that is not automatically cleared by a read of the STATUS register; this bit is only cleared during UCD9081 RESET (if the nonvolatile error log is empty).

The FW Error bit is set to 1 if the device firmware memory contents are corrupted.

The PARAM Error bit is set to 1 if the contents of the UCD9081 configuration memory are invalid. If this occurs, the UCD9081 will load the last known good configuration to ensure device reliability.

VERSION

The VERSION register provides the user with access to the device revision of the UCD9081. The format of this register is a nibble-based major.minor format as shown below.

7	6	5	4	3	2	1	0
Major				Minor			
r	r	r	r	r	r	r	r

RAILSTATUS

The RAILSTATUS1 and RAILSTATUS2 registers are two 8-bit read-only registers that provide a bit mask to represent the error status of the rails as indicated in the following diagram.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
								RAIL8	RAIL7	RAIL6	RAIL5	RAIL4	RAIL3	RAIL2	RAIL1
rc-0	rc-0	rc-0	rc-0	rc-0	rc-0	rc-0	rc-0	rc-0	rc-0	rc-0	rc-0	rc-0	rc-0	rc-0	rc-0

RAILn	Meaning
0	No alarm pending for RAILn
1	Alarm pending for RAILn

Bits 15:8 are RAILSTATUS1 and bits 7:0 are RAILSTATUS2. These are read as two 8-bit registers or as a single 16-bit register.

If a bit is set in these registers, then the ERROR register is read to further ascertain the specific error. Bits in the RAILSTATUS1 and RAILSTATUS2 registers are cleared when read.

FLASHLOCK

The FLASHLOCK register is used to lock and unlock the configuration memory on the UCD9081 when updating the configuration. The *Configuring the UDC9081* section details this process.

The format for the FLASHLOCK register is as follows:

7	6	5	4	3	2	1	0
FLASHLOCK							
rw-0	rw-0	rw-0	rw-0	rw-0	rw-0	rw-0	rw-0

FLASHLOCK

0x00	**Lock flash (default)**
0x01	**Flash is being updated**
0x02	**Unlock flash (before configuration)**

RESTART

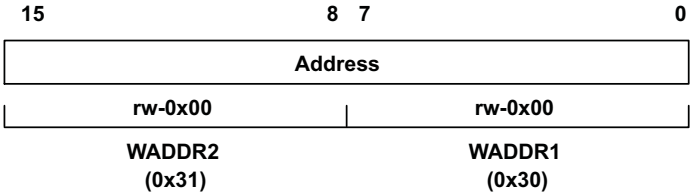
The RESTART register provides the capability for the I^2C host to force a RESET or Shutdown of the UCD9081. This is an 8-bit register, and when a value of 0x00 is written to the register, the UCD9081 RESET occurs and the rails are re-sequenced. Note that in order to respond to this I^2C request properly, there is a 50-µs delay before the system is restarted, so that the I^2C ACK can take place.

When a value of 0xC0 is written to the register, all rails and GPOs are shutdown according to the time delays specified in the system shutdown configuration. Once this procedure is complete, the UCD9081 will continue monitoring.

WADDR and WDATA

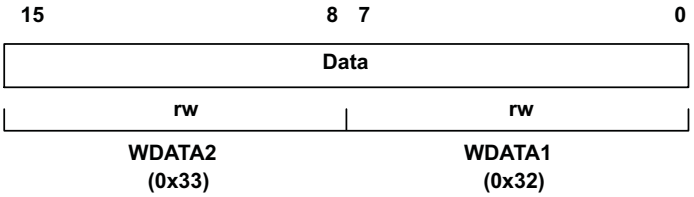
In order to update the configuration on the UCD9081, four registers are provided. WADDR2 (address 15:8) and WADDR1 (address bits 7:0) specify the memory address. WDATA2 (data bits 15:8) and WDATA1 (data bits 7:0) specify the data written to or read from that memory address.

The format for the WADDR register is as follows:



To set the memory address that will be accessed, write the LSB of the address to the WADDR1 register and the MSB of the address to the WADDR2 register. For example, to write the address 0x1234 to the device, set WADDR1 = 0x34 and WADDR2 = 0x12. Note that because these addresses support the auto-increment feature, the user can perform a single 16-bit write to WADDR1 to write the entire address.

The format for the WDATA register is as follows:



To set the value of the data that will be written to the UCD9081, write the LSB of the data to the WDATA1 register and the MSB of the data to the WDATA2 register. For example, to write the data 0xBEEF to the device, set WDATA1 = 0xEF and WDATA2 = 0xBE. Note that because these addresses support the auto-increment feature, the user can perform a single 16-bit write to WDATA1 to write the entire data. To read the value of the data at the specified address, read the LSB from WDATA1 and the MSB from WDATA2.

These registers are used for updating the UCD9081 configuration as explained in the *Configuring the UDC9081* section.

READING THE FLASH ERROR LOG

There are two ways to read the FLASH error log in the UCD9081. While the device is in RESET and the NVERRLOG bit in the *STATUS* register is set to a 1 (FLASH error logs present), the user may use the *ERROR* registers to read the log. During run-time, the FLASH error log can be accessed by performing an I^2C read transaction starting at address 0x1000 with a length of 48 bytes.

RESETTING THE FLASH ERROR LOG

The UCD9081 can be configured to log errors on a critical voltage rail to internal FLASH memory. This mechanism permits the error log to be read after the device has been reset, or if a loss of power causes non-volatile memory to be cleared. As outlined in the section on *Error Logging* , there are two modes for using this feature.

The first mode holds the UCD9081 in RESET (following a RESET of the device) if entries are present in the FLASH error log. This allows the user to successfully read and clear the FLASH error log before sequencing the system. When using this mode, the UCD9081 will not sequence until the FLASH error log is cleared. To clear the FLASH error log and sequence the device, perform the following steps:

- Write FLASHLOCK register to a value of 0x02
- Write WADDR register to a value of 0x1000
- Write WDATA register to a value of 0xBADC
- Write WADDR register to a value of 0x107E
- Write WDATA register to a value of 0xBADC
- Write FLASHLOCK register to a value of 0x00
- Write RESTART register to a value of 0x00

The second mode allows the UCD9081 to sequence (following a RESET of the device) regardless of whether or not there are entries present in the FLASH error log. When using this mode, the user still may wish to clear the FLASH error logs some time after RESET. To do this, perform the following steps:

- Write FLASHLOCK register to a value of 0x02
- Write WADDR register to a value of 0x1000
- Write WDATA register to a value of 0xBADC
- Write WADDR register to a value of 0x107E
- Write WDATA register to a value of 0xBADC
- Write FLASHLOCK register to a value of 0x00

Note that clearing the FLASH error log during run-time will cause a delay in monitoring.

CONFIGURING THE UCD9081

The UCD9081 has many different configurable parameters such as sequencing options, alarm processing options, and rail dependencies. A Microsoft™ Windows™ GUI is available for selecting and generating the necessary configuration parameters. To download and install the UCD9081 GUI, see the UCD9081 product folder at http://focus.ti.com/docs/prod/folders/print/ucd9081.html. See the *UCD9081 EVM User's Guide* (TI literature number SLVU249) for details on installing and using the GUI. Once the user-specific configuration parameters are selected, the GUI generates a hex file that can be loaded into the flash memory of the UCD9081 via the I^2C interface.

NOTE:

Since loading a new configuration requires writing to FLASH memory, the UCD9081 will not monitor the MONx inputs while the configuration parameters are being updated.

To download the configuration parameters generated by the GUI into the UCD9081, a contiguous block of configuration information is sent to the device via the I^2C interface. This block is 512 bytes long and starts at address 0xE000.

This 512-byte block of configuration information is sent to the device in multiple segments. The segment size can range from 2 to 32 bytes at one time, and must be a multiple of 2 bytes. That is, a master can send 256 2-byte segments or 32 16-byte segments, and so on. All the segments must be sent back-to-back in the proper sequence, and this operation must be completed by sending the last segment so that the last byte of the 512-byte block is written. If this is not done, the UCD9081 is in an unknown state and does not function as designed.

The process for sending the configuration information to the UCD9081 is as shown in Figure 7:

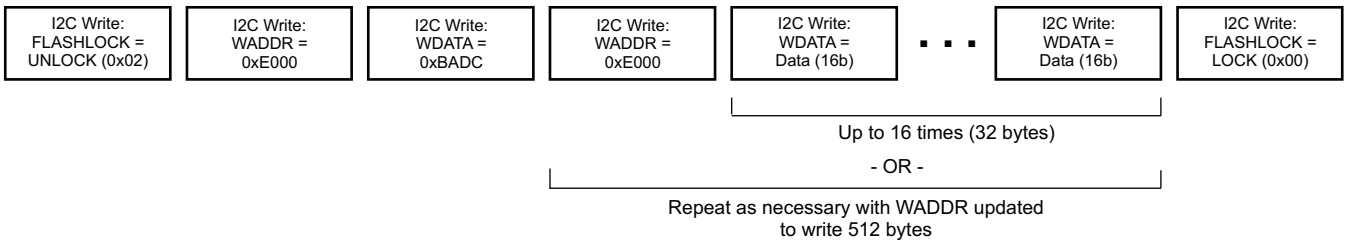


Figure 7. Configuration Information

As shown in Figure 7, the process for updating the configuration of the UCD9081 is as follows:

1. Unlock flash memory by writing the value 0x02 to the FLASHLOCK register
2. Write the address of the configuration section of memory (WADDR = 0xE000)
3. Write the constant 0xBADC to update memory (WDATA = 0xBADC)
4. Write the address of the configuration section of memory again (WADDR = 0xE000)
5. Write the data (WDATA = <varies>). Repeat steps 4 and 5 as necessary, depending on the data segment size used, to write 512 bytes. Increment the address as necessary.
6. Lock flash memory after the last byte of the last segment is written by writing the value 0x00 to the FLASHLOCK register

At the conclusion of this process, the configuration of the UCD9081 is updated with the configuration changes, as represented by the values from the data segments.

USER DATA

User data (128 bytes) can be stored in the UCD9081 FLASH memory at location 0x1080 to 0x10FF. Writes to the User Data section of memory are performed as follows:

1. Unlock flash memory by writing the value 0x02 to the FLASHLOCK register
2. Write the address of the USER DATA section of memory (WADDR = 0x1080)
3. Write the constant 0xBADC to update memory (WDATA = 0xBADC)
4. Write the address of the USER DATA section of memory again (WADDR = 0x1080)
5. Write the data (WDATA = <varies>). Repeat steps 4 and 5 as necessary depending on the data segment size used. Increment the address as necessary.
6. Lock flash memory after the last byte of the last segment is written by writing the value 0x00 to the FLASHLOCK register

To read the User Data section of memory, follow the procedure for reading memory outlined in the section on *WADDR and WDATA*.

I²C ADDRESS SELECTION

The UCD9081 supports 7-bit I²C addressing. The UCD9081 selects an I²C address by sampling the logic level of the four digital inputs to the device (ADDR1–ADDR4) during the RESET interval. When the UCD9081 is released from RESET, the ADDRx logic levels are latched and the I²C address is assigned as shown in *Figure 8*.

A7 = 1	A6 = 1	A5 = 0	A4 = ADDR4/GPO4	A3 = ADDR3/GPO3	A2 = ADDR2/GPO2	A1 = EN8/ADDR1/GPO1

Figure 8. I²C ADDRESS = 0x60–0x6F

External pullup/pulldown resistors are required to configure the I²C address; the UCD9081 does not have internal bias resistors. Note that the 7-bit I²C address refers to the address bits only, not the read/write bit in the first byte of the I²C protocol. The base I²C address is 0x60 and the I²C general call address (0x00) is not supported.

After the initialization process of the UCD9081 is complete, these four pins can be used for general-purpose outputs.

I²C TRANSACTIONS

The UCD9081 can be configured and monitored via I²C memory-mapped registers. Registers that are configurable (can be written) via an I²C write operation are implemented using an I²C unidirectional data transfer, from the master to slave, with a stop bit between transactions.

I²C UNIDIRECTIONAL TRANSFER

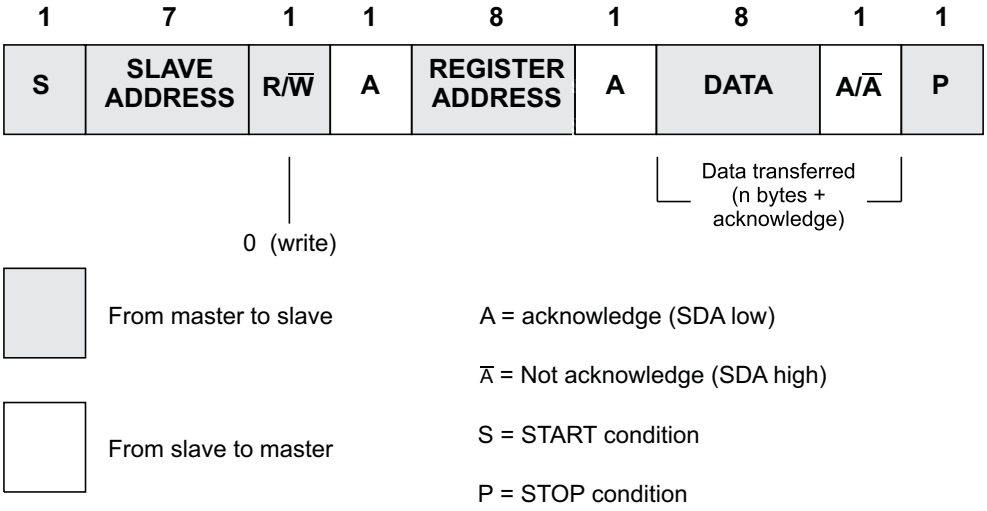


Figure 9. I²C Register Access with START/STOP

Registers that can be read are implemented using an I²C read operation, which can use the I²C combined format that changes data direction during the transaction. This transaction uses an I²C repeated START during the direction change.

I²C COMBINED FORMAT

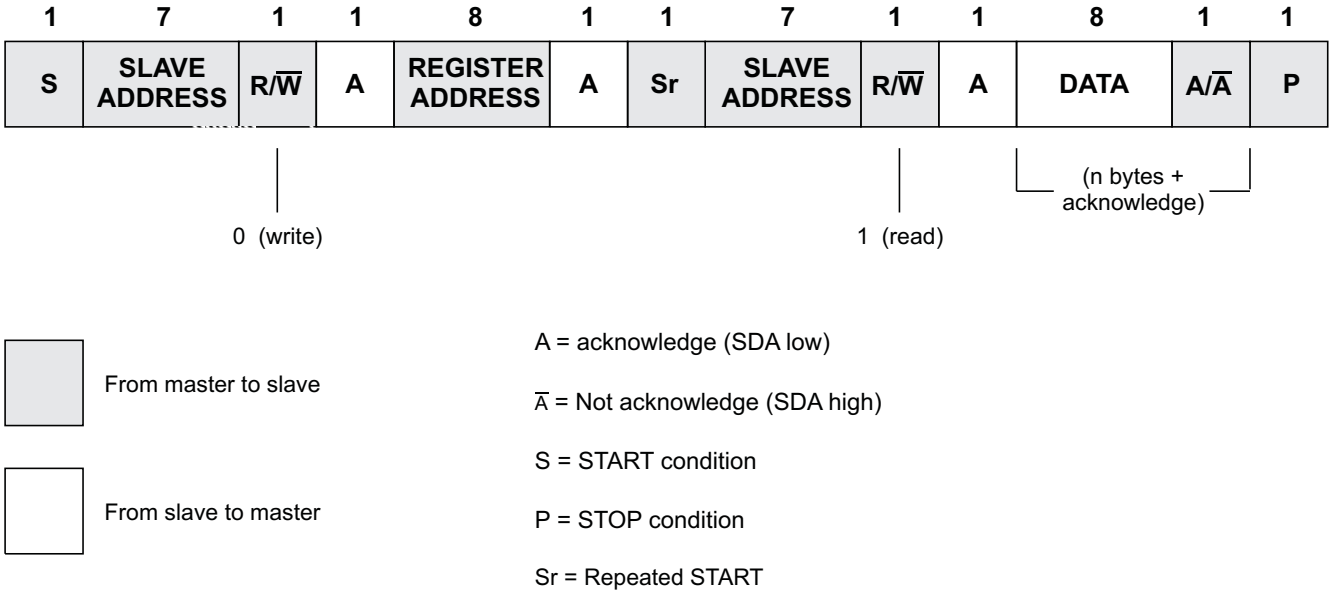


Figure 10. I²C Register Access with Repeated START

The UCD9081 also supports a feature that auto-increments the register address pointer for increased efficiency when accessing sequential blocks of data. It is not necessary to issue separate I²C transactions.

I²C TIMING

The UCD9081 supports the same timing parameters as standard-mode I²C. See the following timing diagram and timing parameters for more information.

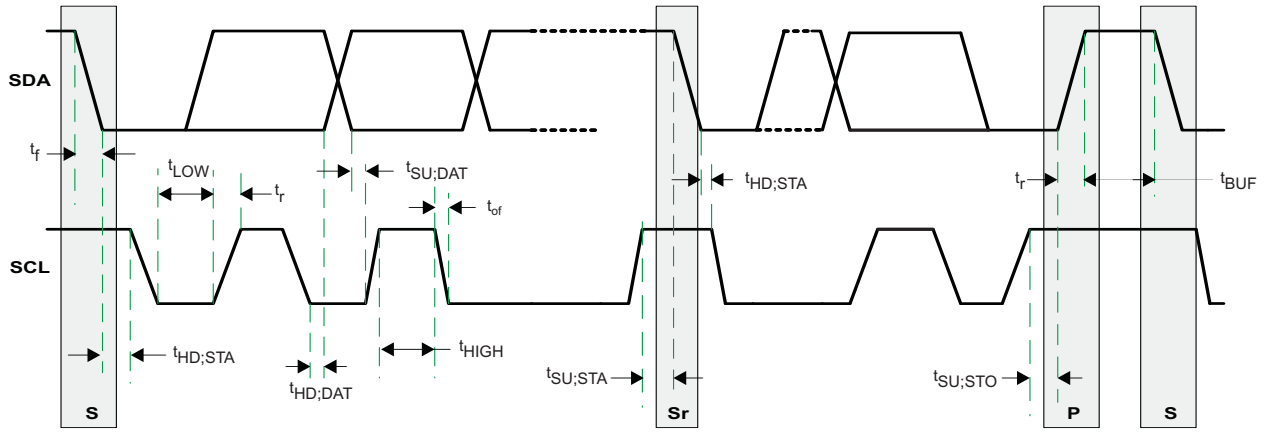


Figure 11. Timing Diagram for I²C Interface

TIMING PARAMETERS FOR I²C INTERFACE

	PARAMETER	MIN	MAX	UNIT
t_{of}	Output fall time from V_{OH} to V_{OL} (1) with a bus capacitance from 10 pF to 400 pF.		250 (2)	ns
C_I	Capacitance for each pin.		10	pF
f_{SCL}	SCL clock frequency	10	100	kHz
$t_{HD;STA}$	Hold time (repeated) START condition. After this period, the first clock pulse is generated.	4		µs
$t_{HD;DAT}$	Data hold time	0 (3)	3.45 (4)	µs
t_{LOW}	LOW period of the SCL clock	4.7		µs
t_{HIGH}	HIGH period of the SCL clock	4		µs
$t_{SU;STA}$	Set-up time for repeated start condition	4.7		µs
$t_{SU;DAT}$	Data set-up time	250		ns
t_r	Rise time of both SDA and SCL signals		1000	ns
t_f	Fall time of both SDA and SCL signals		300	ns
$t_{SU;STO}$	Set-up time for STOP condition	4		µs
t_{BUF}	Bus free time between a STOP and START condition	4.7		µs
$C_{(b)}$	Capacitive load for each bus line		400	pF
V_{nL}	Noise margin at the LOW level for each connected device (including hysteresis)	0.1 VDD		V
V_{nH}	Noise margin at the HIGH level for each connected device (including hysteresis)	0.2 VDD		V

(1) See the *Electrical Characteristics* section of this data sheet.
(2) The maximum t_f for the SDA and SCL bus lines (300 ns) is longer than the specified maximum t_{of} for the output stages (250 ns). This allows series protection resistors, R_s , to be connected between the SDA/SCL pins and the SDA/SCL bus lines without exceeding the maximum specified t_f.
(3) A device must internally provide a hold time of at least 300 ns for the SDA signal to bridge the undefined region of the falling edge of SCL.
(4) The maximum $t_{HD;DAT}$ must only be met if the device does not stretch the LOW period (t_{LOW}) of the SCL signal.

The UCD9081 is compatible with 3.3-V IO ports of microcontrollers, TMS320™ DSP family as well as ASICs. The UCD9081 is available in a plastic 32-pin QFN package (RHB).

APPLICATION INFORMATION

TYPICAL APPLICATION DIAGRAM

Figure 12 illustrates a typical power supply sequencing configuration. Power Supply 1 and Power Supply X require active low enables while Power Supply 2 and Power Supply 3 require active high enables. V_{OUT1} and V_{OUT3} exceed the selected A/D reference voltage so their outputs are divided before being sampled by the MON1 and MON3 inputs. V_{OUT2} and V_{OUTX} are within the selected A/D reference voltage so their outputs can be sampled directly by the MON2 and MON7 inputs. Figure 12 illustrates the use of the GPO digital output pins to provide status and power on reset to other system devices.

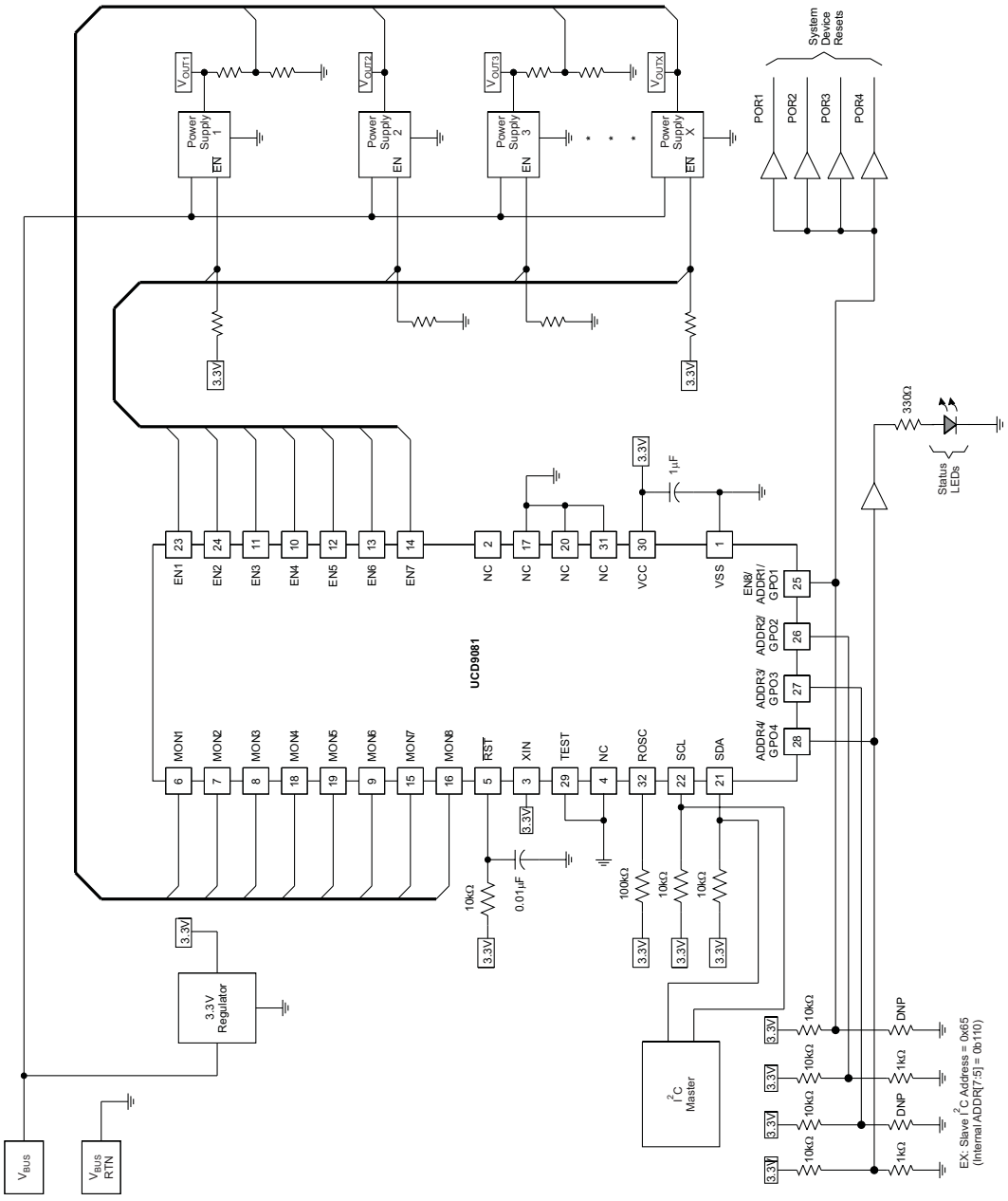


Figure 12. Typical Power Supply Sequencing Application

CONSIDERATIONS FOR MONX INPUT SERIES RESISTANCE, R_S

R_S is the series impedance between the sampled voltage source (low impedance power supply output) and the UCD9081 MONx input pin. This resistance can affect UCD9081 sampling accuracy if it is too large. In most cases (when the power supply being monitored has a lower VOUT than the UCD9081 voltage reference being used) this resistance is low and can be ignored. In cases where a voltage divider is used to scale the monitored voltage below the voltage reference, the impedance of this network must be chosen so that it does not adversely affect the analog to digital converter (ADC) conversion accuracy. The equivalent series impedance (R_S) of the divider network is just the parallel combination of the pullup and pulldown resistors.

The UCD9081 has an internal clock (DCO) whose frequency is set by ROSC on pin 32. The DCO frequency can be affected by several factors including supply voltage and temperature. This clock is used by the ADC to set up an ADC sample or gate time (T_{GATE}) at each MONx pin. The voltage sampled must be allowed to settle sufficiently during T_{GATE}. The settling time is affected by the UCD9081 internal capacitance and R_S. To allow for sufficient settling time over DCO frequency, supply voltage, and temperature variation, choose $R_S < 6k\Omega$.

ESTIMATING UCD9081 REPORTING ACCURACY OVER VARIATIONS IN ADC VOLTAGE REFERENCE

The UCD9081 uses a 10 bit ADC. The ADC in the UCD9081 derives its reference voltage (V_{R+}) from either the external (V_{CC} pin) or internal (V_{REF+}) reference voltage to scale the digitally reported voltage. The least significant bit (LSB) voltage value is $V_{LSB} = V_{R+}/2^n$ where n = 10 and V_{R+} is the reference voltage used (either external V_{CC} = 3.3V nominal, or internal V_{REF+} = 2.5V nominal). For external $V_{R+} = V_{CC}$ = 3.3V, V_{LSB} = 3.3/1024 = 3.22mV and for internal $V_{R+} = V_{REF+}$ = 2.5V, V_{LSB} = 2.5/1024 = 2.44mV.

The error in the reported voltage is a function of the ADC linearity error(s) as well as variations in the ADC reference voltage. The total unadjusted error (E_{TUE}) for the ADC in the UCD9081 is ±5 LSB and the variation of the internal 2.5V reference is ±6% maximum. V_{TUE} is calculated as $V_{LSB} \times E_{TUE}$ for the particular reference voltage used. The reported voltage error will be the sum of the reference voltage error and the ADC total unadjusted error. At lower monitored voltages, E_{TUE} may dominate reported error while at higher monitored voltages V_{R+} will dominate the reported error. Reported error (percent) can be calculated using the equation below where REFTOL is V_{R+} tolerance, V_{ACT} is actual voltage monitored (at the UCD9081 MONx pin), and V_{R+} is the nominal voltage of the ADC reference.

$$RPT_{ERR} = [(1 + REFTOL]/V_{ACT}] \times [V_{R+} \times E_{TUE}/1024 + V_{ACT}] - 1$$

Shown below are four examples using the equation above to estimate reported error:

V_{R+} = 2.5V, REFTOL = 6%, V_{ACT} = 0.25V, RPT_{ERR} = 11.2%
V_{R+} = 2.5V, REFTOL = 6%, V_{ACT} = 2.25V, RPT_{ERR} = 6.6%
V_{R+} = 3.3V, REFTOL = 1%, V_{ACT} = 0.25V, RPT_{ERR} = 7.5%
V_{R+} = 3.3V, REFTOL = 1%, V_{ACT} = 2.25V, RPT_{ERR} = 1.7%

In addition to the reporting errors due to ADC and voltage reference, there can be additional errors due to divider resistor tolerance when monitoring voltages higher than V_{R+}. These errors can be added to the reporting error described above.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)
UCD9081RHBR	ACTIVE	QFN	RHB	32	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
UCD9081RHBRG4	ACTIVE	QFN	RHB	32	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
UCD9081RHBT	ACTIVE	QFN	RHB	32	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
UCD9081RHBTG4	ACTIVE	QFN	RHB	32	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR

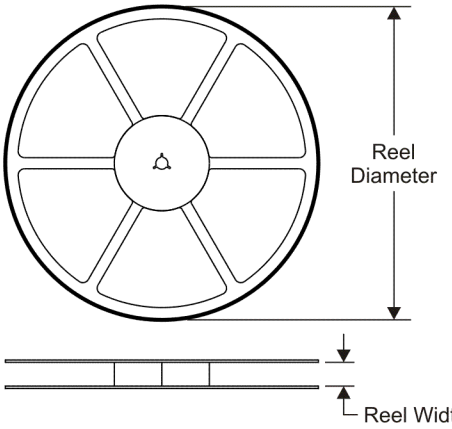
(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

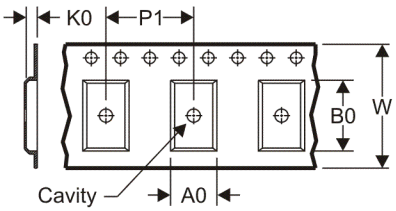
(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

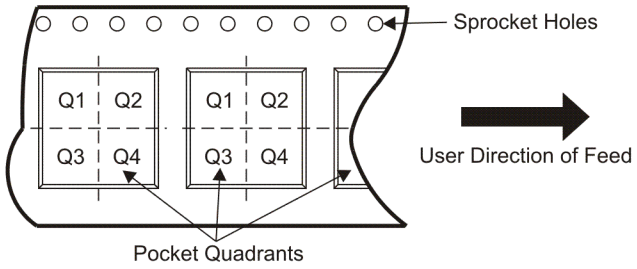


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

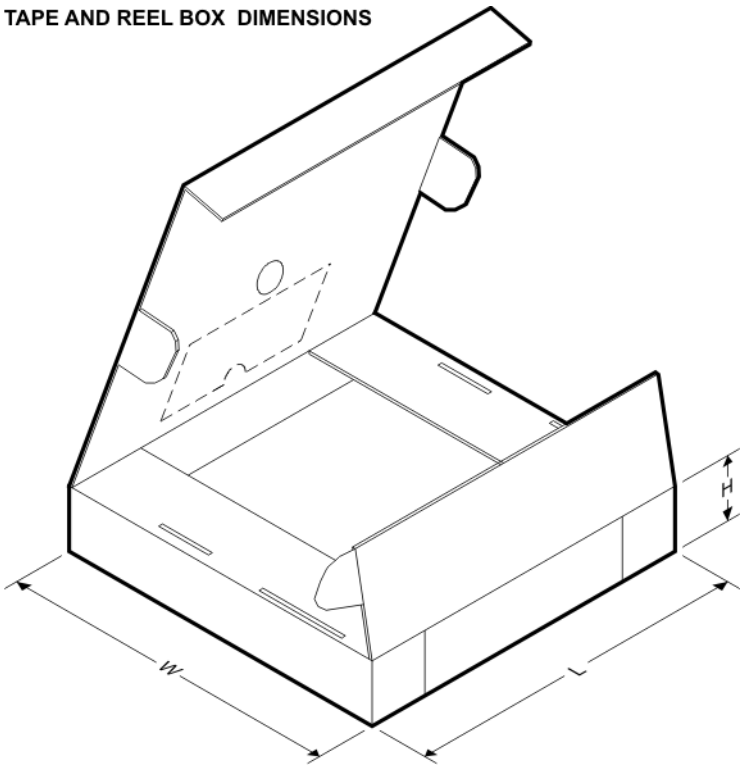
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
UCD9081RHBR	QFN	RHB	32	3000	330.0	12.4	5.3	5.3	1.5	8.0	12.0	Q2
UCD9081RHBT	QFN	RHB	32	250	180.0	12.4	5.3	5.3	1.5	8.0	12.0	Q2

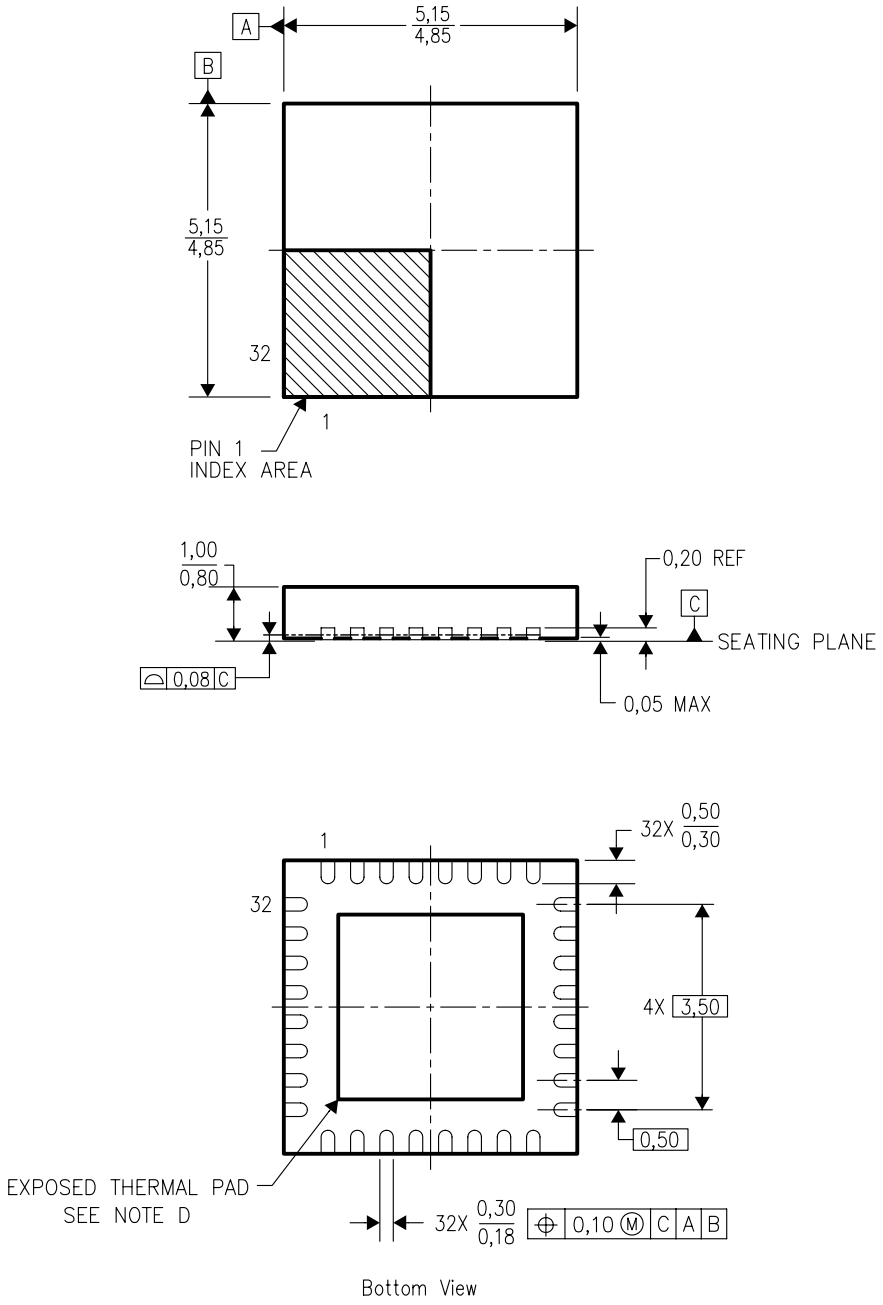
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
UCD9081RHBR	QFN	RHB	32	3000	346.0	346.0	29.0
UCD9081RHBT	QFN	RHB	32	250	190.5	212.7	31.8

RHB (S–PQFP–N32) PLASTIC QUAD FLATPACK



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. QFN (Quad Flatpack No–Lead) Package configuration.
D The Package thermal pad must be soldered to the board for thermal and mechanical performance. See product data sheet for details regarding the exposed thermal pad dimensions.
E. Falls within JEDEC MO–220.

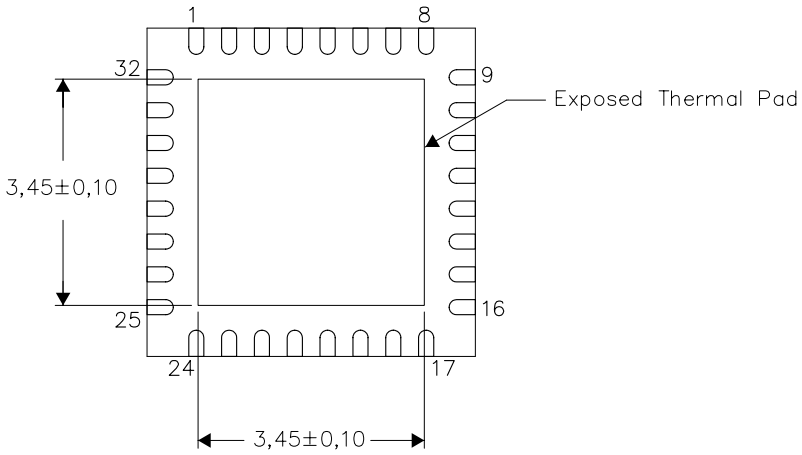
RHB (S–PVQFN–N32) PLASTIC QUAD FLATPACK NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



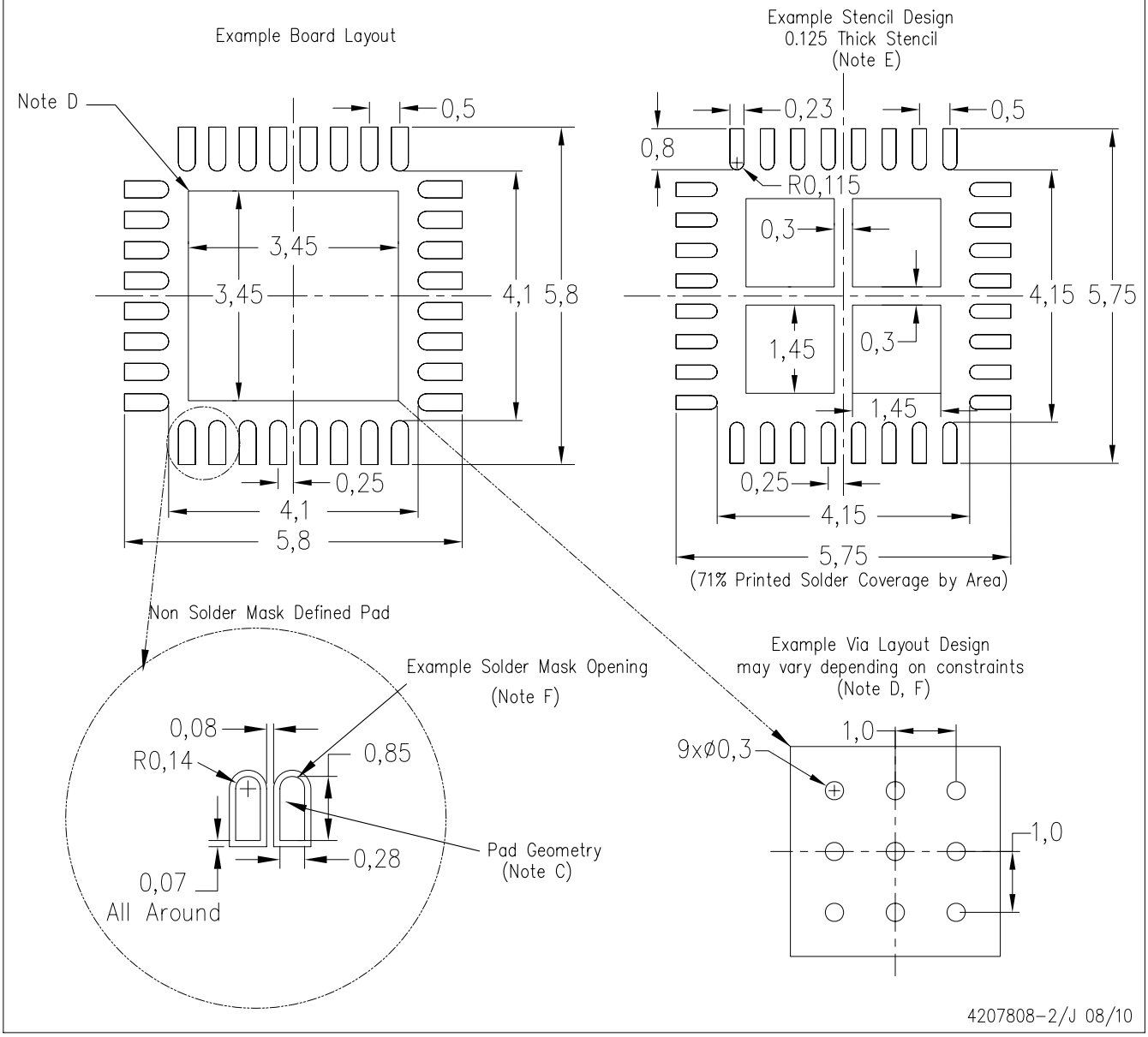
Bottom View

Exposed Thermal Pad Dimensions

4206356–2/P 08/10

NOTE: A. All linear dimensions are in millimeters

RHB (S–PVQFN–N32) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat–Pack Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
F. Customers should contact their board fabrication site for recommended solder mask tolerances and via tenting recommendations for vias placed in the thermal pad.

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